SCOPE: DUAL AND QUAD SPST NORMALLY OPEN RF/VIDEO SWITCHES

Device Type	Generic Number	Circuit Function
01	IH5048M(x)/883B	Dual SPST
02	IH5049M(x)/883B	Dual DPST
03	IH5050M(x)/883B	SPDT
04	IH5051M(x)/883B	Dual SPDT

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JE	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
LP	CQCC1-N20	20 LEADLESS CHIP CARRIER	L20

Absolute Maximum Ratings:

V^+ to V^- 36V
V^+ to V_D 30V
V_D to V^- 30V
V_D to V_S ..... ±28V
V_L to V^- 33V
V_L to V_{IN} 30V
V_L to GND 20V
V_{IN} to GND 20V

Digital Input Overvoltage Range ..... (V^+ +0.3V) to (V^+ -38V)
V_S or V_D 1/ ..... (V^-)-0.3V to (V^+) +0.3V
Continuous Current, Any terminal 30mA
Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max 100mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
20 leadless chip carrrier (derate 9.1mW/°C above +70°C) 727mW
16 lead CERDIP (derate 10.0mW/°C above +70°C) 800mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 20 leadless chip carrrier..... 20°C/W
Case Outline 16 lead CERDIP..... 50°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 20 leadless chip carrier ..... 110°C/W
Case Outline 16 lead CERDIP..... 100°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V^+) ..... +15V
Negative Supply Voltage (V^-) ..... -15V
V_{AL} (max) 0.8V
V_{AH} (min) 2.4V

NOTE 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current To maximum ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{AH}=2.4V, V_{AL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
INPUT							
Input Logic Current High	I_{INH}	V_{IN}=2.4V	1,3 2	All		±1 ±10	µA
Input Logic Current Low	I_{INL}	V_{IN}=0.0V	1,3 2	All		±1 ±10	µA
SWITCH							
Drain-Source On Resistance	$r_{DS(ON)}$	I_S =±10mA, V_D=±10V	1,3 2	All		60 40	Ω
On Resistance Match between Channels	$r_{DS(ON)}$	I_S =±10mA, V_D=±10V NOTE 2	1	All		8	Ω
Analog Signal Handling Capability	V_{ANALOG}		1	All	±14		V
Switch-OFF Resistance	$I_{S(OFF)}$	V_{ANALOG}=±10V	1 2	All		±1 ±100	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V_{ANALOG}=±10V	1 2	All		±1 ±100	nA
Switch- ON Leakage Current	$I_{S(OFF)}$ + $I_{D(OFF)}$	V_S=V_D=±10V	1 2	All		±2 ±200	nA
SUPPLY							
Positive Supply Quiescent Current	I+	V_A=0V, 5V	1,3 2	All		1 10	µA
Negative Supply Quiescent Current	I-	V_A=0V, 5V	1,3 2	All		1 10	µA
Logic Supply Quiescent Current	I_L	V_A=0V, 5V	1,3 2	All		1 10	µA
Ground Current	I_{GND}	V_A=0V, 5V	1,3 2	All		1 10	µA
DYNAMIC							
Turn-On Time NOTE 3	t_{ON}	Figure 1	9 10,11	All		500 750	ns
Turn-Off Time NOTE 3	t_{OFF}	Figure 1	9 10,11	All		250 500	ns

NOTE 2: Guaranteed but not production tested.

NOTE 3: Some channels are turned off by high (1) logic inputs and other channels by low (0) inputs; however 0.8V and 2.4V describe the minimum range for proper switching. Refer to logic diagrams for logical input value for on or off states.

Figure 1 Switching Time: See Commercial Data Sheet.

TERMINAL CONNECTIONS

TERMINAL NUMBER	01 IH5048	02 IH5049	03 IH5050	04 IH5051
0	J16	J16	J16	J16
1	D1	D1	D1	D1
2				
3		D3	D2	D3
4		S3	S2	S3
5		S4		S4
6		D4		D4
7				
8	D2	D2		D2
9	S2	S2		S2
10	IN2	IN2		IN2
11	V+	V+	V+	V+
12	VL	VL	VL	VL
13	GND	VR	VR	VR
14	V-	V-	V-	V-
15	IN1	IN1	IN	IN1
16	S1	S1	S1	S1

ORDERING INFORMATION:			
IH5048MJE/883B	16 CDIP	IH5048MLP/883B	20 pin LCC
IH5049MJE/883B	16 CDIP	IH5049MLP/883B	20 pin LCC
IH5050MJE/883B	16 CDIP	IH5050MLP/883B	20 pin LCC
IH5051MJE/883B	16 CDIP	IH5051MLP/883B	20 pin LCC

				TRUTH TABLES			
IH5048	& IH5049	IH5050	IH5050	IH5050	IH5051	IH5051	IH5051
LOGIC	SWITCH	LOGIC	SWITCH 1	SWITCH 2	LOGIC	SWITCH 1,2	SWITCH 3,4
0	OFF	0	OFF	ON	0	OFF	ON
1	ON	1	ON	OFF	1	ON	OFF

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.