

DATA SHEET

74F543

Octal registered transceiver,
non-inverting (3-State)

Product data sheet
Replaces data sheet 74F543/74F544 of 1994 Dec 05

2004 Jul 22

Octal registered transceiver, non-inverting (3-State)

74F543

FEATURES

- Combines 74F245 and 74F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 20 mA and source 3 mA
- B outputs sink 64 mA and source 15 mA
- 3-State outputs for bus-oriented applications
- Available in SSOP Type II package

DESCRIPTION

The 74F543 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{\text{LEAB}}$, $\overline{\text{LEBA}}$) and Output Enable ($\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The A outputs are guaranteed to sink 24 mA, while the B outputs are rated for 64 mA.

FUNCTIONAL DESCRIPTION

The 74F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{\text{EAB}}$) input must be LOW in order to enter data from A0 - A7 or take data from B0 - B7, as indicated in the Function Table. With $\overline{\text{EAB}}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition for the $\overline{\text{LEAB}}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{\text{EAB}}$ and $\overline{\text{OEAB}}$ both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{\text{EBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0 ns	80 mA

ORDERING INFORMATION

Commerical range: $V_{CC} = 5\text{ V} \pm 10\%$; $T_{amb} = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Type number	Package		
	Name	Description	Version
N74F543D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F543DB	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
N74F543N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

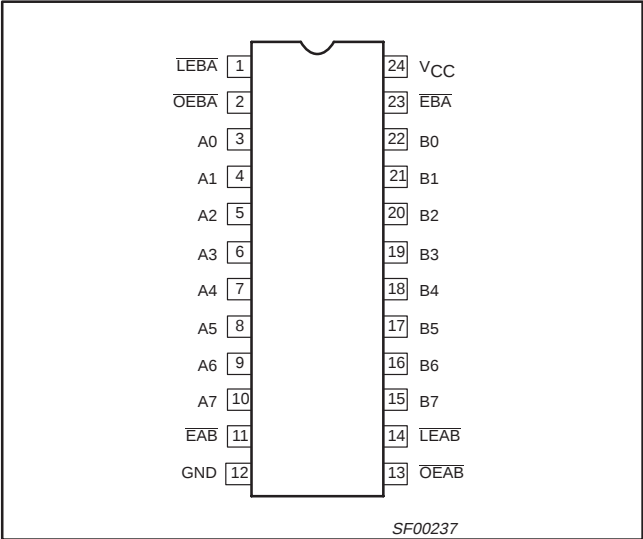
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7	Port A, 3-State inputs	3.5/1.0	70 μA /0.6 mA
B0 - B7	Port B, 3-State inputs	3.5/1.0	70 μA /0.6 mA
$\overline{\text{OEAB}}$	A-to-B Output Enable input (Active LOW)	1.0/1.0	20 μA /0.6 mA
$\overline{\text{OEBA}}$	B-to-A Output Enable input (Active LOW)	1.0/1.0	20 μA /0.6 mA
$\overline{\text{EAB}}$	A-to-B Enable input (Active LOW)	1.0/2.0	20 μA /1.2 mA
$\overline{\text{EBA}}$	B-to-A Enable input (Active LOW)	1.0/2.0	20 μA /1.2 mA
$\overline{\text{LEAB}}$	A-to-B Latch Enable input (Active LOW)	1.0/1.0	20 μA /0.6 mA
$\overline{\text{LEBA}}$	B-to-A Latch Enable input (Active LOW)	1.0/1.0	20 μA /0.6 mA
A0 - A7	Port A, 3-State outputs	150/40	3.0 mA/24 mA
B0 - B7	Port B, 3-State outputs	750/106.7	15 mA/64 mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μA in the HIGH State and 0.6mA in the LOW state.

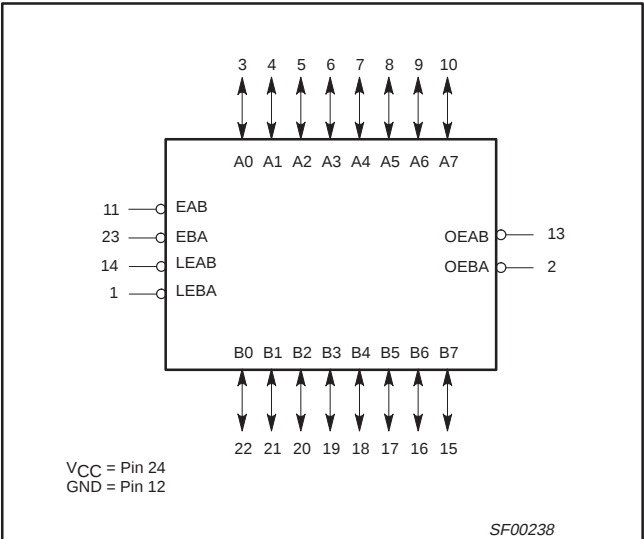
Octal registered transceiver, non-inverting (3-State)

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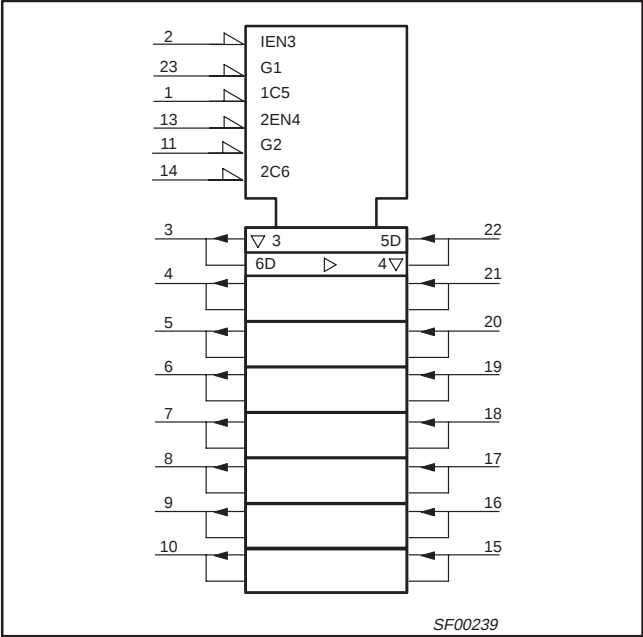
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for 74F543

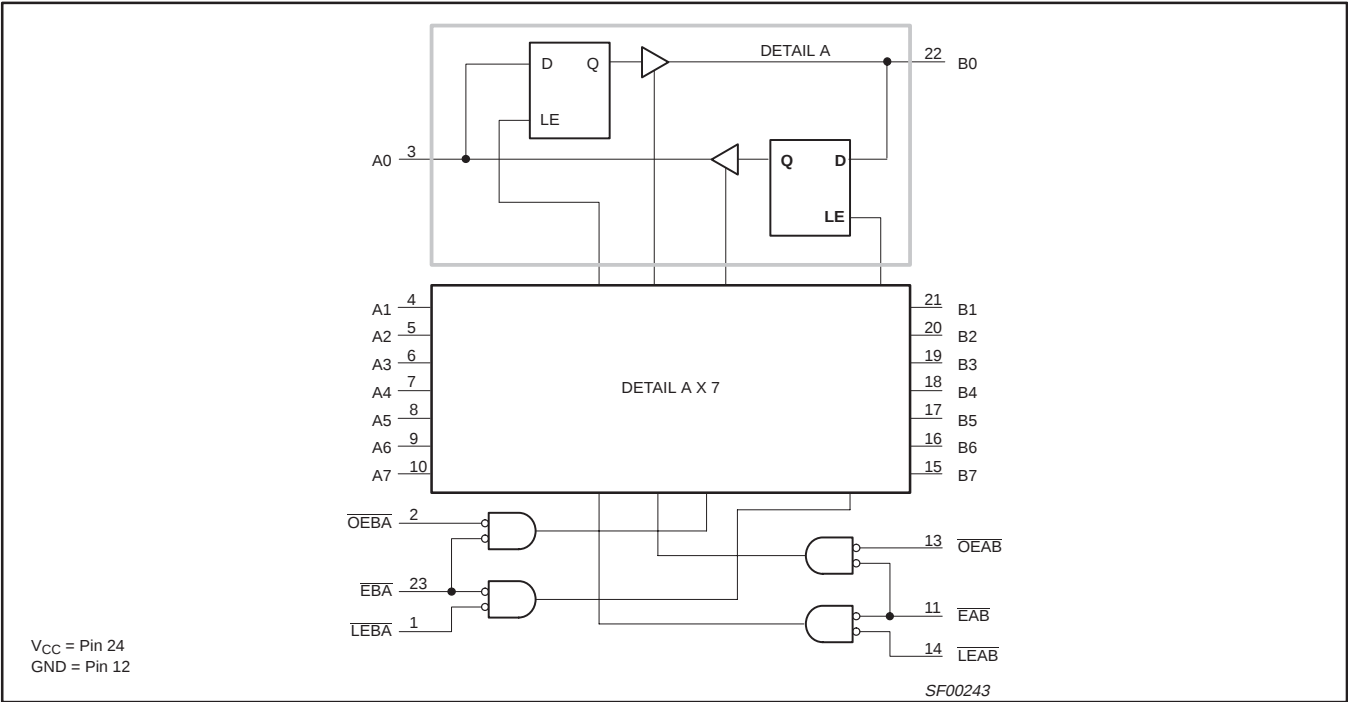
INPUTS				OUTPUTS	STATUS
OE $\overline{\text{XX}}$	$\overline{\text{EXX}}$	$\overline{\text{LEXX}}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	$\uparrow$	L	h	Z	Disable + Latch
L	$\uparrow$	L	l	Z	Disable + Latch
L	L	$\uparrow$	h	H	Latch + Display
L	L	$\uparrow$	l	L	Latch + Display
L	L	L	H	H	Transparent
L	L	L	L	L	Transparent
L	L	H	X	NC	Hold

- H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX=AB or BA)
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX=AB or BA)
 $\uparrow$ = LOW-to-HIGH transition of $\overline{\text{LEXX}}$ or $\overline{\text{EXX}}$ (XX=AB or BA)
X = Don't care
NC = No change
Z = High-impedance "off" state

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LOGIC DIAGRAM



Octal registered transceiver, non-inverting (3-State)

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in LOW output state	A0 - A7	48	mA
		B0 - B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	—	—	V
V_{IL}	LOW-level input voltage		—	—	0.8	V
I_{IK}	Input clamp current		—	—	−18	mA
I_{OH}	HIGH-level output current	A0 - A7	—	—	−3	mA
		B0 - B7	—	—	−15	mA
I_{OL}	LOW-level output current	A0 - A7	—	—	24	mA
		B0 - B7	—	—	64	mA
T_{amb}	Operating free-air temperature range		−0	—	+70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						MIN	TYP ²	MAX	
V _{OH}	HIGH-level output voltage	A0 - A7	V _{CC} = MIN V _{IL} = MAX	I _{OH} = −3 mA	± 10 % V _{CC}	2.4	—	—	V
					± 5 % V _{CC}	2.7	3.4	—	V
		B0 - B7	V _{IH} = MIN	I _{OH} = −15 mA	± 10 % V _{CC}	2.0	—	—	V
					± 5 % V _{CC}	2.0	—	—	V
V _{OL}	LOW-level output voltage	A0 - A7	V _{CC} = MIN V _{IL} = MAX	I _{OL} = 24 mA	± 10 % V _{CC}	—	0.35	0.50	V
					± 5 % V _{CC}	—	0.35	0.50	V
		B0 - B7	V _{IH} = MIN	I _{OL} = 64 mA	± 10 % V _{CC}	—	—	0.55	V
					± 5 % V _{CC}	—	0.42	0.55	V
V _{IK}	Input clamp voltage		V _{CC} = MIN; I _I = I _{IK}			—	−0.73	−1.2	V
I _I	Input current at maximum input voltage	OEAB, OEBA, EAB	V _{CC} = MAX; V _I = 7.0 V			—	—	100	μA
		Others	V _{CC} = 5.5 V; V _I = 5.5 V			—	—	1	mA
I _{IH}	HIGH-level input current		V _{CC} = MAX; V _I = 2.7 V			—	—	20	μA
I _{IL}	LOW-level input current	Others	V _{CC} = MAX; V _I = 0.5 V			—	—	−0.6	mA
		EAB, EBA				—	—	−1.2	mA
I _{OZH} + I _{IH}	Off-state output current, HIGH-level voltage applied		V _{CC} = MAX; V _O = 2.7 V			—	—	70	μA
I _{OZH} + I _{IL}	Off-state output current, LOW-level voltage applied		V _{CC} = MAX; V _O = 0. 5 V			—	—	−600	μA
I _{OS}	Short-circuit output current ³	A0 - A7	V _{CC} = MAX			−60	—	−150	mA
		B0 - B7				−100	—	−225	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX			—	70	105	mA
		I _{CCL}				—	95	135	mA
		I _{CCZ}				—	95	135	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5 \text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _{amb} = +25 °C V _{CC} = 5.0 V C _L = 50 pF; R _L = 500 Ω			T _{amb} = 0 °C to +70 °C V _{CC} = 5.0 V ± 10 % C _L = 50pF; R _L = 500 Ω			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay A _n to B _n	Waveform 1	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns	
t _{PLH} t _{PHL}	Propagation delay B _n to A _n	Waveform 1	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns	
t _{PLH} t _{PHL}	Propagation delay LEBA to A _n	Waveform 1	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns	
t _{PLH} t _{PHL}	Propagation delay LEAB to B _n	Waveform 1	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns	
t _{PZH} t _{PZL}	Output Enable time OEBA to A _n or OEAB to B _n	Waveform 3 Waveform 4	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns	
t _{PHZ} t _{PLZ}	Output Disable time OEBA to A _n or OEAB to B _n	Waveform 3 Waveform 4	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns	
t _{PZH} t _{PZL}	Output Enable time EBA to A _n or EAB to B _n	Waveform 3 Waveform 4	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns	
t _{PHZ} t _{PLZ}	Output Disable time EBA to A _n or EAB to B _n	Waveform 3 Waveform 4	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns	

AC SETUP REQUIREMENTS

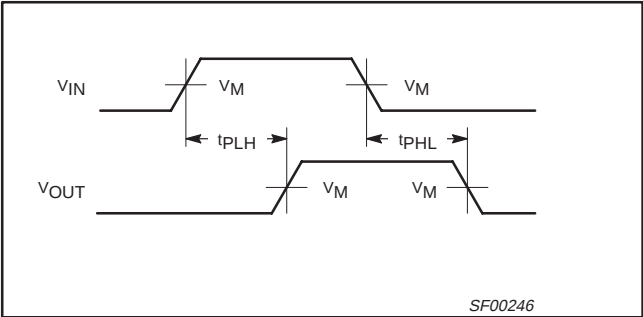
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			T _{amb} = +25 °C V _{CC} = 5.0 V C _L = 50 pF; R _L = 500 Ω		T _{amb} = 0 °C to +70 °C V _{CC} = 5.0 V ± 10 % C _L = 50 pF; R _L = 500 Ω		
			MIN	TYP	MIN	MAX	
t _S (H) t _S (L)	Setup time, HIGH or LOW A _n to $\overline{\text{LEAB}}$ or B _n to $\overline{\text{LEBA}}$	Waveform 2	0.0 2.5	— —	0.0 3.0	— —	ns
t _H (H) t _H (L)	Hold time, HIGH or LOW A _n to $\overline{\text{LEAB}}$ or B _n to $\overline{\text{LEBA}}$	Waveform 2	0.0 1.5	— —	0.0 2.0	— —	ns
t _S (H) t _S (L)	Setup time, HIGH or LOW A _n to $\overline{\text{EAB}}$ or B _n to $\overline{\text{EBA}}$	Waveform 2	1.0 2.5	— —	1.5 3.0	— —	ns
t _H (H) t _H (L)	Hold time, HIGH or LOW A _n to $\overline{\text{EAB}}$ or B _n to $\overline{\text{EBA}}$	Waveform 2	0.0 1.5	— —	0.0 2.0	— —	ns
t _W (L)	Latch enable pulse width, LOW	Waveform 2	4.0	—	4.5	—	ns

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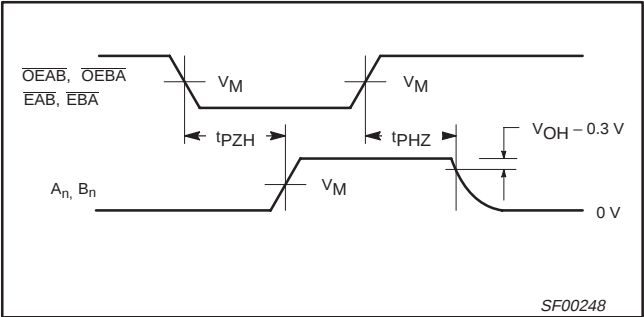
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AC WAVEFORMS

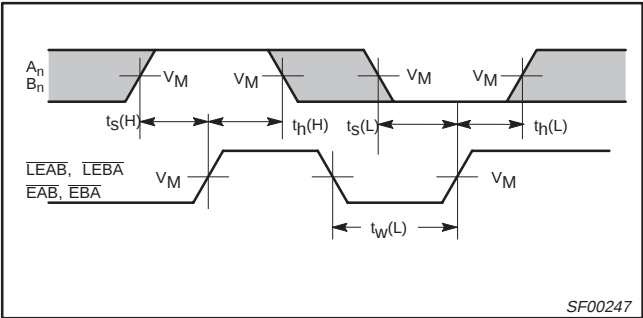
$V_M = 1.5\text{ V}$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



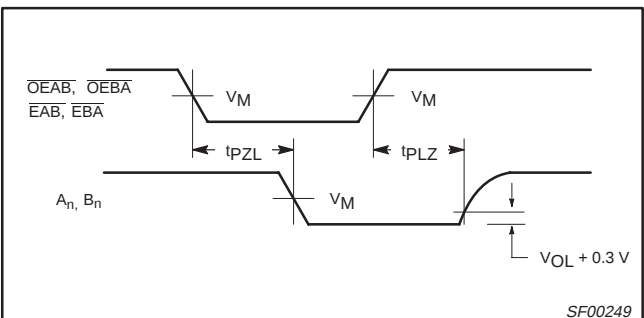
Waveform 1. Propagation delay for non-inverting outputs



Waveform 3. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level



Waveform 2. Data Setup Time and Hold Times, and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
tPLZ	closed
tPZL	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

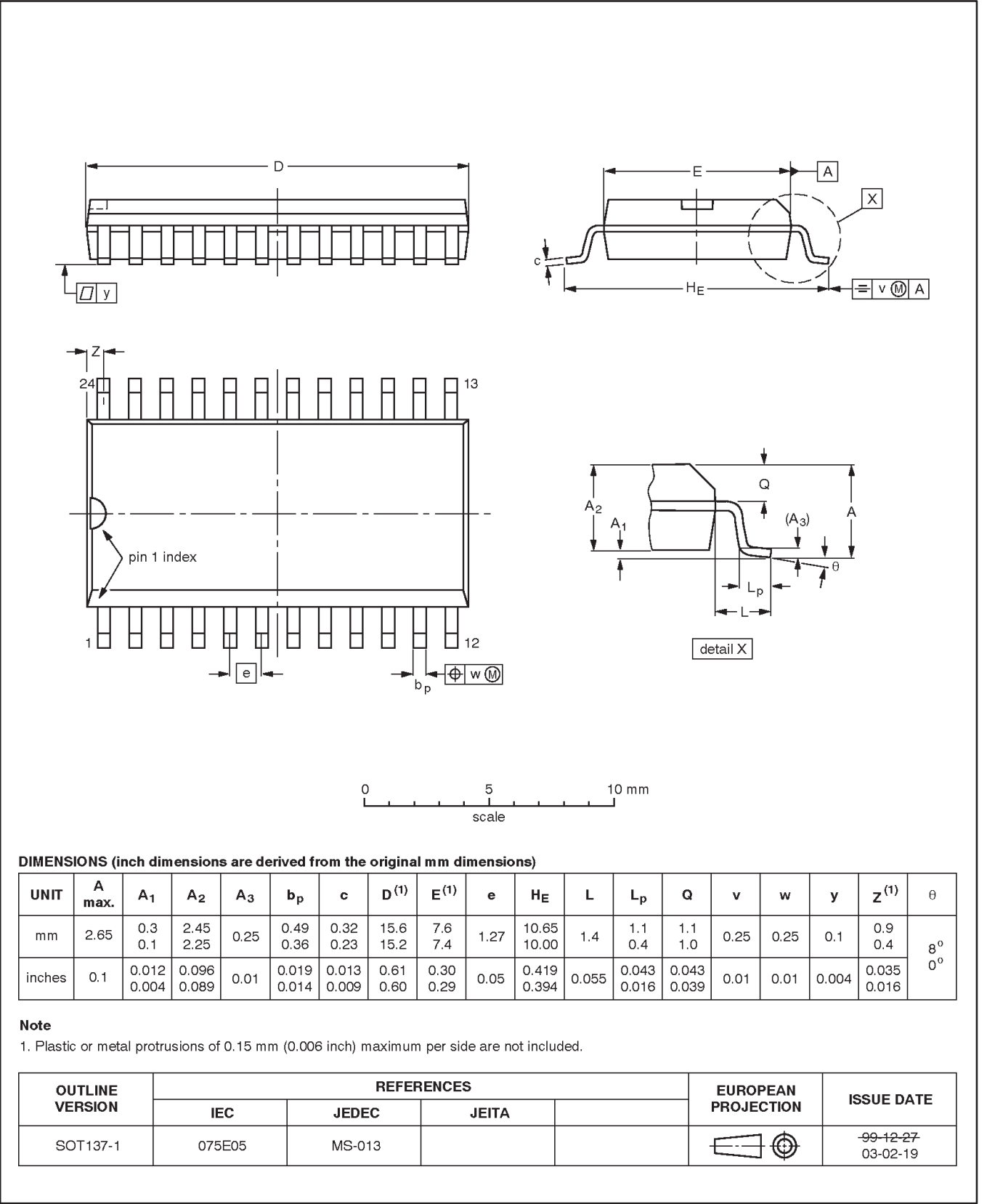
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{THL}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

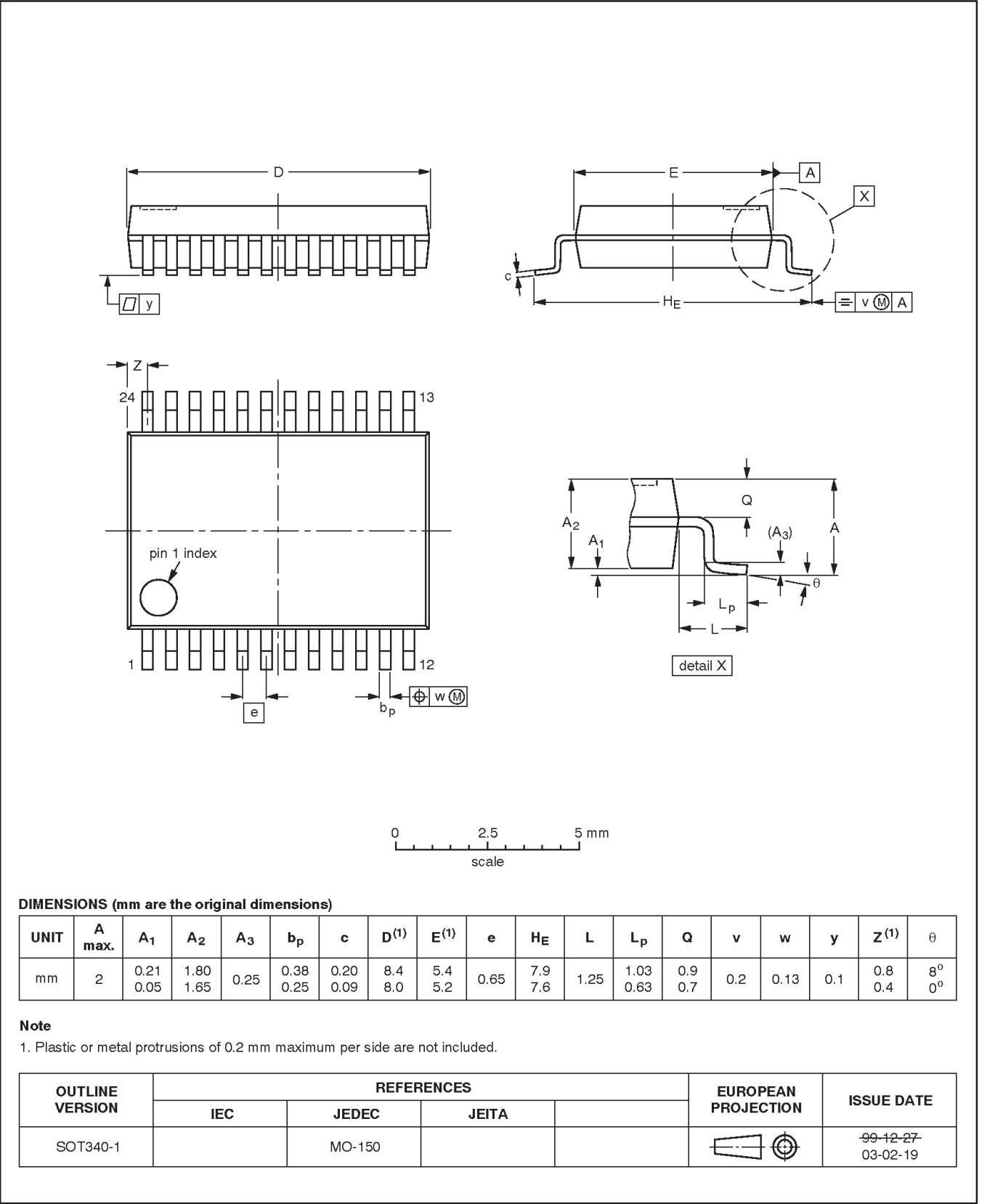


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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



Octal registered transceiver, non-inverting (3-State)

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

0 5 10 mm
scale

DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				99-12-27 03-03-12

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REVISION HISTORY

Rev	Date	Description
_3	20040722	Product data sheet (9397 750 13803). Replaces Product specification 74F543_544_1 of 1994 Dec 05 (9397 750 05135). Modifications: - Remove part-type 74F544 and all its references. - Change Type number for SSOP24 package from "74F543DB" to "N74F543DB".
_2	19941205	Product specification (9397 750 05135). ECN 853-0874 14379 of 05 December 1994.

Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Document order number: 9397 750 13803

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