

# 0.45-Ω CMOS, 1.65-V to 3.6-V, Dual DPDT Analog Switch

## FEATURES

- Low Voltage Operation (1.65 V to 3.6 V)
- Low On-Resistance -  $r_{ON}$ : 0.45 Ω @ 2.7 V
- Fast Switching:  $t_{ON}$  = 28 ns  
 $t_{OFF}$  = 17 ns
- QFN-16 (3x3) Package

## BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.8-V Logic Compatible
- High Bandwidth

## APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

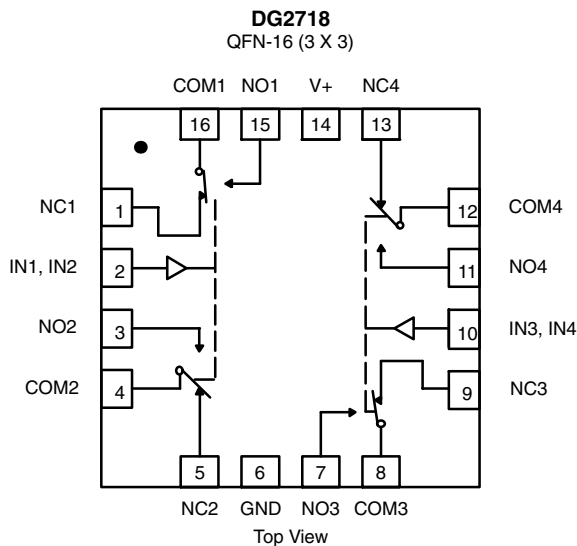
## DESCRIPTION

The DG2718 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2718 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2718 is built on Vishay Siliconix's low voltage process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



**NOTE:**

Underside exposed pad has no device electrical connection. It is recommended that no electrical connection is made to it.

TRUTH TABLE		
Logic	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION*		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin QFN (3 x 3 mm) Variation 2	DG2718DN-T1-E4

\* Lead-Free Version Available

**ABSOLUTE MAXIMUM RATINGS**

Reference to GND

V+	-0.3 to +4.0 V
IN, COM, NC, NO <sup>a</sup>	-0.3 to (V+ + 0.3 V)
Current (Any terminal except NO, NC or COM)	30 mA
Continuous Current (NO, NC, or COM)	± 300 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	± 500 mA
Storage Temperature (D Suffix)	-65 to 150°C
Package Solder Reflow Conditions <sup>d</sup>	
16-Pin QFN (3 x 3 mm)	250°C
Power Dissipation (Packages) <sup>b</sup>	

QFN-16<sup>c</sup> ..... 1385 mW

- Notes:
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 17.3 mW/°C above 70°C
  - Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 1.8 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 1.8 V, V <sub>IN</sub> = 0.4 or 1.1 V <sup>e</sup>	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub>		Full	0		V+	V
On-Resistance <sup>d</sup>	r <sub>ON</sub>	V+ = 1.8 V, V <sub>COM</sub> = 0.2 V/0.9 V, I <sub>NO</sub> , I <sub>NC</sub> = 100 mA	Room Full		0.7	2.0 2.8	Ω
<b>Digital Control</b>							
Input High Voltage	V <sub>INH</sub>		Full	1.1			V
Input Low Voltage	V <sub>INL</sub>		Full			0.4	
Input Capacitance	C <sub>in</sub>		Full		6		pF
Input Current	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> = 0 or V+	Full	-1		1	μA
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	Room Full		62	94 92	ns
Turn-Off Time	t <sub>OFF</sub>		Room Full		24	52 55	
Break-Before-Make Time	t <sub>d</sub>		Full	16			
Charge Injection <sup>d</sup>	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω	Room		65		pC
Off-Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz	Room		-74		dB
Crosstalk <sup>d</sup>	X <sub>TALK</sub>		Room		-74		
N <sub>O</sub> , N <sub>C</sub> Off Capacitance <sup>d</sup>	C <sub>NO(off)</sub>	V <sub>IN</sub> = 0 or V+, f = 1 MHz	Room		108		pF
	C <sub>NC(off)</sub>		Room		108		
Channel-On Capacitance <sup>d</sup>	C <sub>NO(on)</sub>		Room		225		
	C <sub>NC(on)</sub>		Room		225		
			Room		225		
<b>Power Supply</b>							
Power Supply Current	I+	V <sub>IN</sub> = 0 or V+	Full			1.0	μA

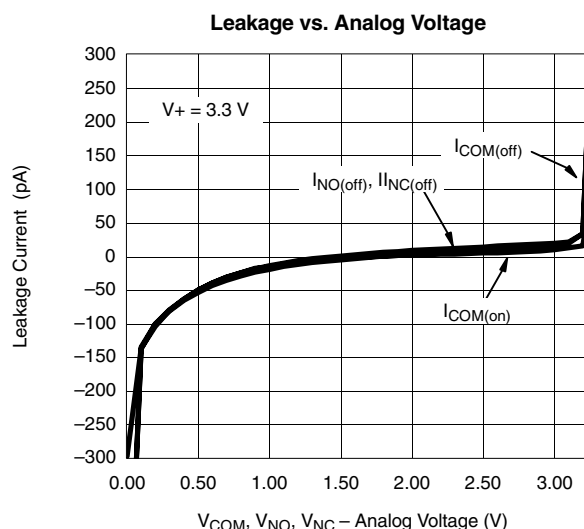
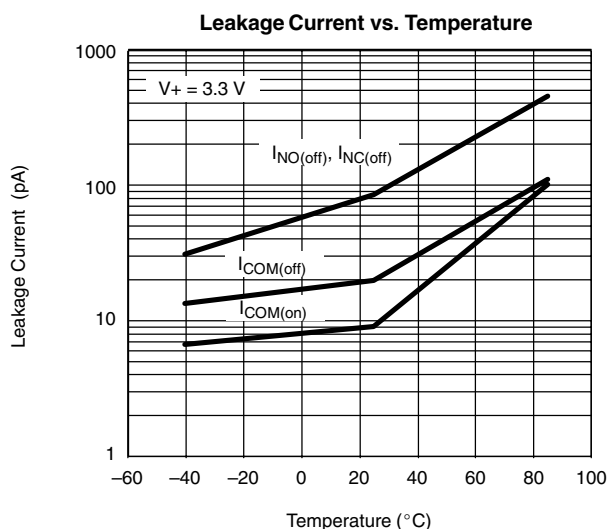
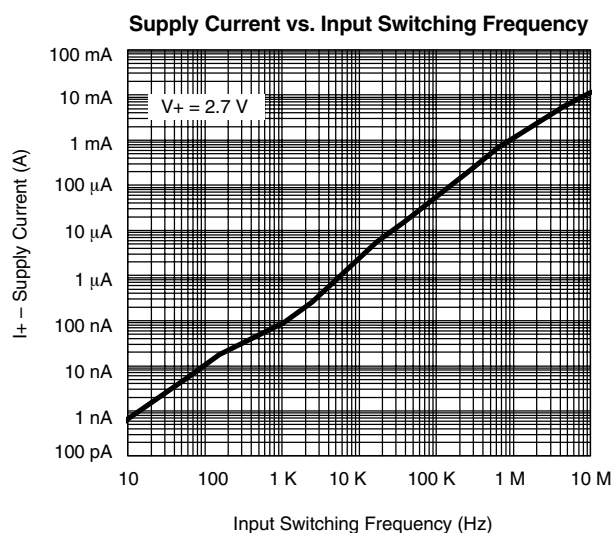
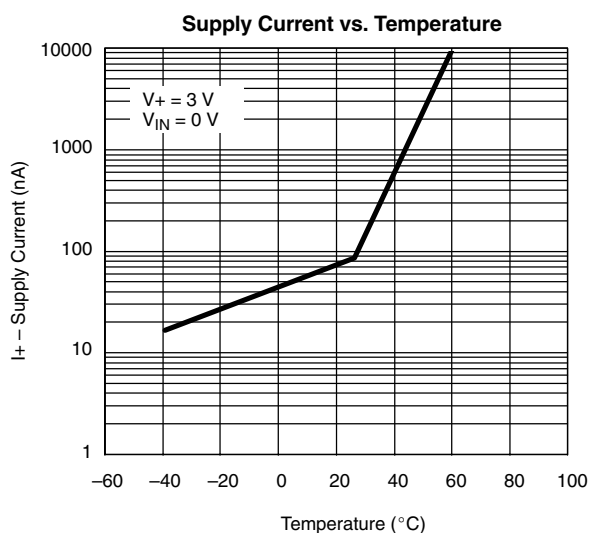
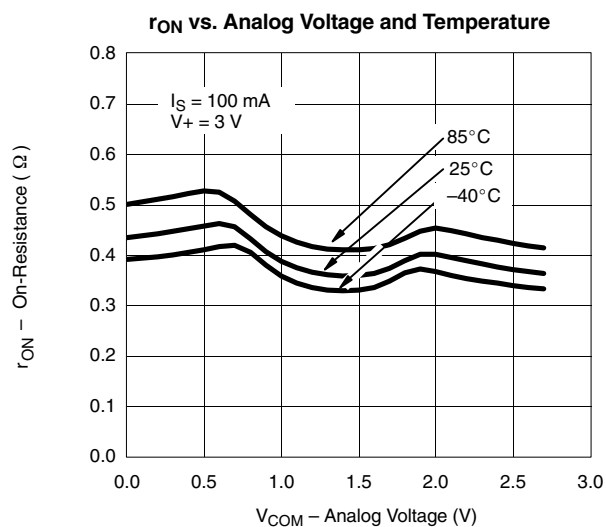
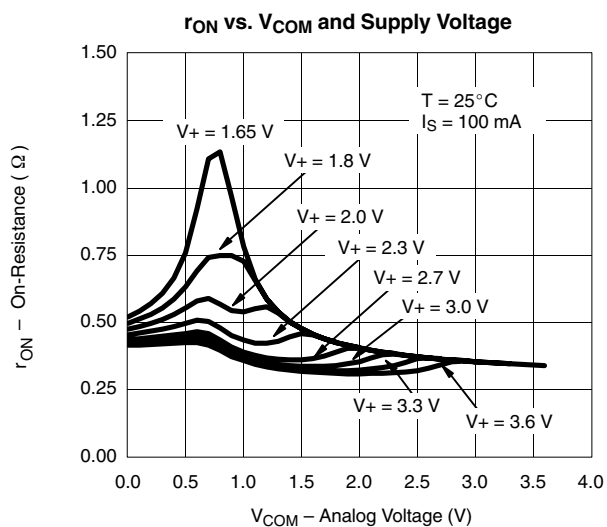


SPECIFICATIONS (V+ = 3 V)									
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.5 or 1.4 V <sup>e</sup>	Temp <sup>a</sup>	Limits –40 to 85°C			Unit		
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>			
<b>Analog Switch</b>									
Analog Signal Range <sup>d</sup>	V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub>		Full	0		V+	V		
On-Resistance <sup>d</sup>	r <sub>ON</sub>	V+ = 2.7 V, V <sub>COM</sub> = 0.2 V/1.5 V, I <sub>NO</sub> , I <sub>NC</sub> = 100 mA	Room Full		0.45	0.6 0.7	Ω		
r <sub>ON</sub> Flatness <sup>d</sup>	r <sub>ON</sub> Flatness	V+ = 2.7 V V <sub>COM</sub> = 0 to V+, I <sub>NO</sub> , I <sub>NC</sub> = 100 mA	Room		0.1	0.15			
r <sub>ON</sub> Match <sup>d</sup>	Δr <sub>ON</sub>		Room		0.05				
Switch Off Leakage Current	I <sub>NO(off)</sub> , I <sub>NC(off)</sub>	V+ = 3.3 V, V <sub>NO</sub> , V <sub>NC</sub> = 0.3 V/3 V V <sub>COM</sub> = 3 V/0.3 V	Room Full	–1 –10		1 10	nA		
	I <sub>COM(off)</sub>		Room Full	–1 –10		1 10			
Channel-On Leakage Current	I <sub>COM(on)</sub>	V+ = 3.3 V, V <sub>NO</sub> , V <sub>NC</sub> = V <sub>COM</sub> = 0.3 V/3 V	Room Full	–1 –10		1 10			
<b>Digital Control</b>									
Input High Voltage	V <sub>INH</sub>		Full	1.4			V		
Input Low Voltage	V <sub>INL</sub>		Full			0.5			
Input Capacitance	C <sub>in</sub>		Full		6		pF		
Input Current	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> = 0 or V+	Full	–1		1	μA		
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF	Room Full		28	57 60	ns		
Turn-Off Time	t <sub>OFF</sub>		Room Full		17	45 47			
Break-Before-Make Time	t <sub>d</sub>		Full	1					
Charge Injection <sup>d</sup>	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω	Room		232		pC		
Off-Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 100 kHz	Room		–75		dB		
Crosstalk <sup>d</sup>	X <sub>TALK</sub>		Room		–75				
N <sub>O</sub> , N <sub>C</sub> Off Capacitance <sup>d</sup>	C <sub>NO(off)</sub>	V <sub>IN</sub> = 0 or V+, f = 1 MHz	Room		102		pF		
	C <sub>NC(off)</sub>		Room		102				
Channel-On Capacitance <sup>d</sup>	C <sub>NO(on)</sub>		Room		234				
	C <sub>NC(on)</sub>		Room		234				
<b>Power Supply</b>									
Power Supply Range	V+				2.7			3.3	V
Power Supply Current	I+	V <sub>IN</sub> = 0 or V+	Full			1.0	μA		

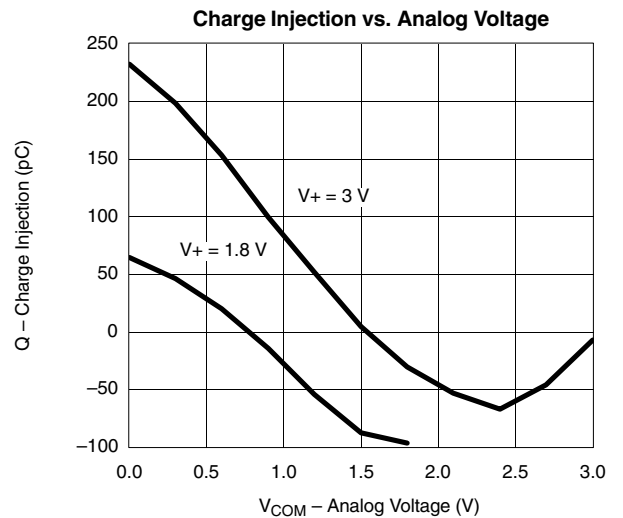
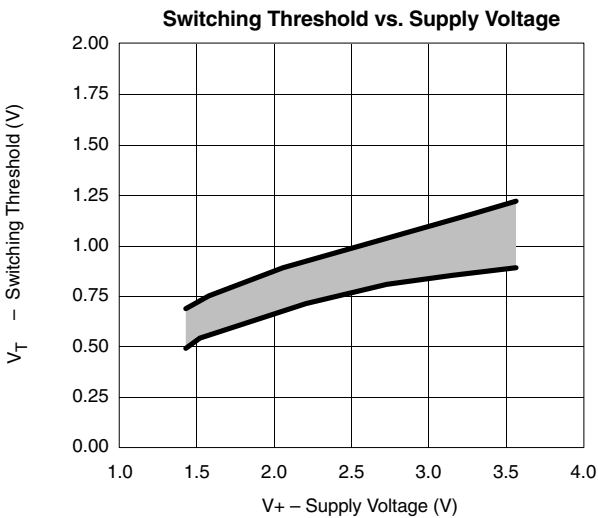
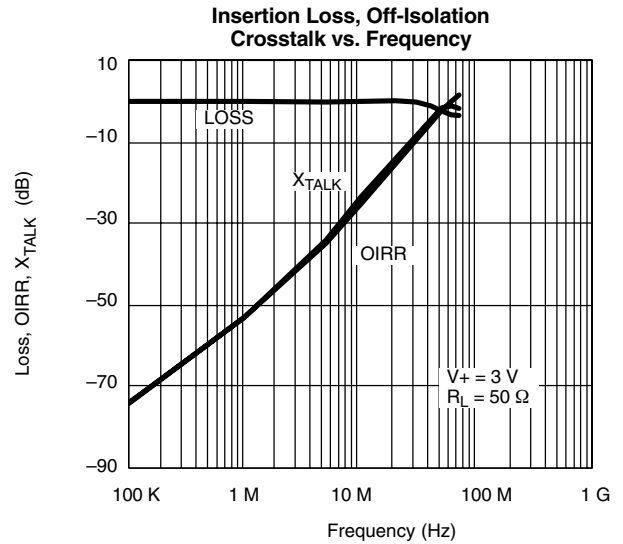
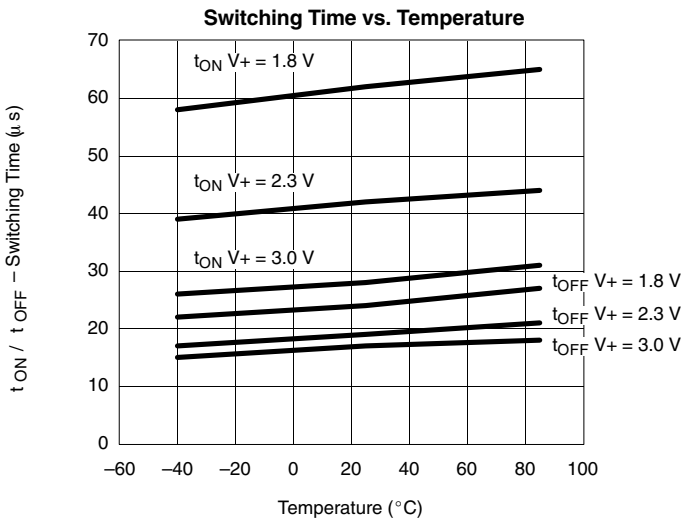
Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V<sub>IN</sub> = input voltage to perform proper function.
- Guaranteed by 5-V leakage testing, not production tested.

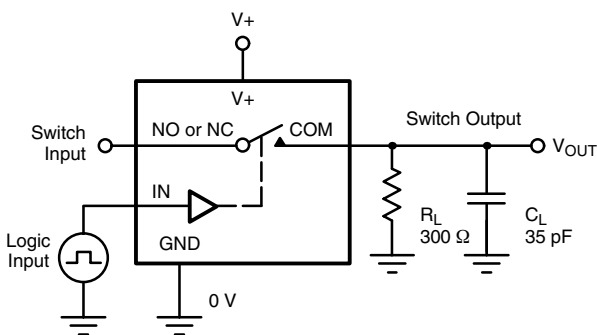
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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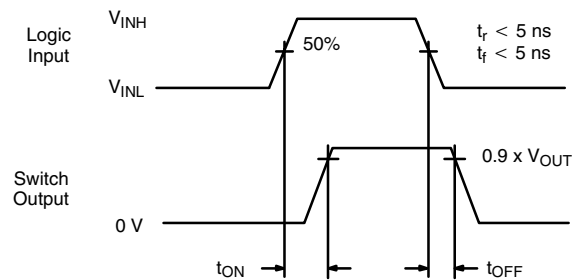


**TEST CIRCUITS**



$C_L$  (includes fixture and stray capacitance)

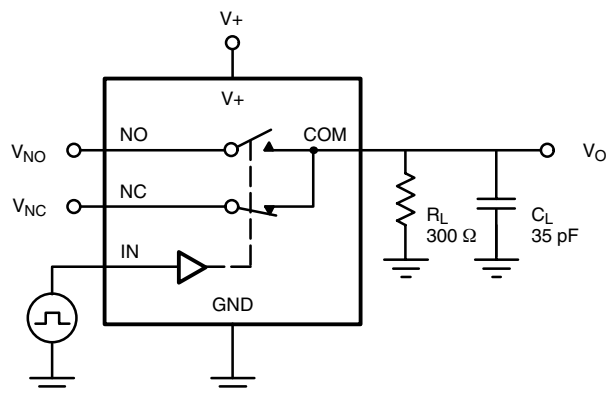
$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)

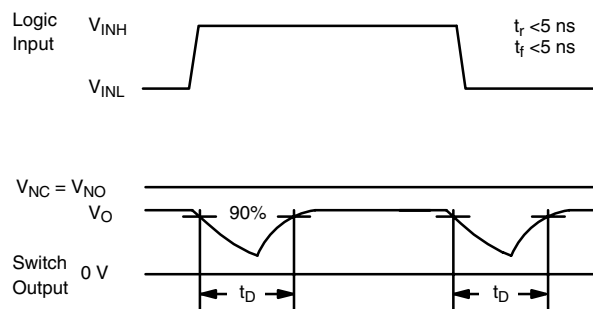
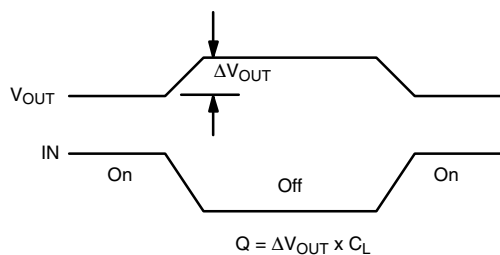
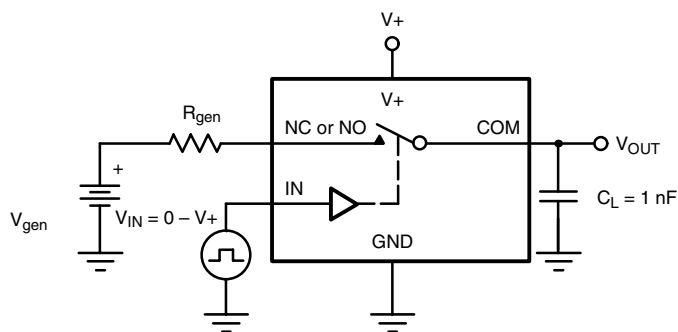


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

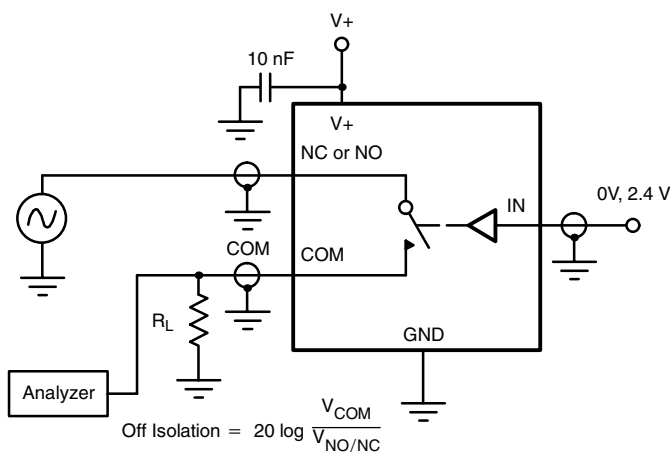


Figure 4. Off-Isolation

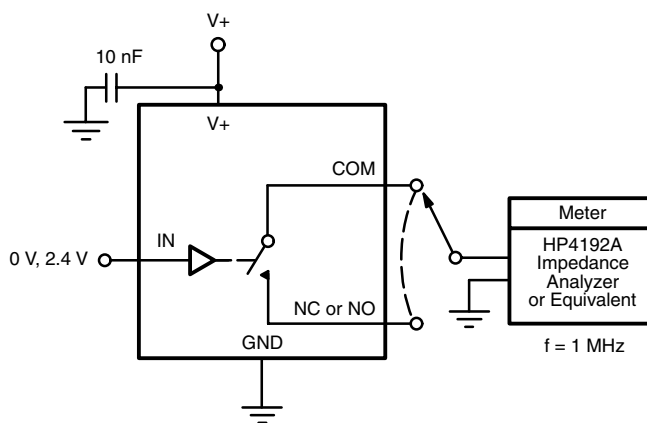


Figure 5. Channel Off/On Capacitance



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