



# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

**MAX9969**

## General Description

The MAX9969 dual, low-power, high-speed, pin electronics driver/comparator with 35mA load IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. An additional differential comparator allows comparisons between the two channels. The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, and differential outputs. The clamps provide damping of high-speed device-under-test (DUT) waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric testing of IOH and IOL, and pullup of high-output-impedance devices. The MAX9969A features tighter matching of offset for the drivers and the comparators.

The MAX9969 provides high-speed, differential control inputs with optional internal termination resistors that are compatible with LVPECL, LVDS, and GTL. Flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, slew-rate limit, and tri-state/terminate operational configurations of the MAX9969.

The MAX9969's operating range is -1.5V to +6.5V with power dissipation of only 1.4W per channel. The device is available in a 100-pin, 14mm x 14mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +60°C to +100°C, and features a die temperature monitor output.

## Applications

High-Performance Mixed-Signal/  
System-on-Chip ATE  
High-Performance Memory ATE

## Features

- ◆ **Low-Power Dissipation: 1.4W/Channel (typ)**
- ◆ **Greatly Reduced Power Penalty when Load Commutated**
- ◆ **High Speed: 1200Mbps at 3Vp-p and 1800Mbps at 1Vp-p**
- ◆ **Programmable 35mA Active-Load Current**
- ◆ **Low Timing Dispersion**
- ◆ **Wide -1.5V to +6.5V Operating Range**
- ◆ **Active Termination (3rd-Level Drive)**
- ◆ **Low-Leakage Mode: 15nA**
- ◆ **Integrated Clamps**
- ◆ **Integrated Differential Comparator**
- ◆ **Interfaces Easily with Most Logic Families**
- ◆ **Digitally Programmable Slew Rate**
- ◆ **Internal Termination Resistors**
- ◆ **Low Offset Error**
- ◆ **Pin Compatible with the MAX9967**

## Ordering Information

| PART          | TEMP RANGE   | PIN-PACKAGE    |
|---------------|--------------|----------------|
| MAX9969ADCCQ  | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969AGCCQ* | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969ALCCQ  | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969ARCCQ* | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969BDCCQ  | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969BGCCQ* | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969BLCCQ  | 0°C to +70°C | 100 TQFP-EPR** |
| MAX9969BRCCQ  | 0°C to +70°C | 100 TQFP-EPR** |

\*Future product—contact factory for availability.

\*\*EPR = Exposed pad reversed (TOP).

Pin Configuration and Selector Guide appear at end of data sheet.



Maxim Integrated Products 1

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## ABSOLUTE MAXIMUM RATINGS

|                                                                                                                                  |                       |
|----------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| V <sub>CC</sub> to GND                                                                                                           | .....-0.3V to +11V    |
| V <sub>EE</sub> to GND                                                                                                           | .....-5.75V to +0.3V  |
| V <sub>CC</sub> - V <sub>EE</sub>                                                                                                | .....-0.3V to +16.75V |
| GS to GND                                                                                                                        | .....±1V              |
| DUT <sub>-</sub> to GND                                                                                                          | .....-2.75V to +7.5V  |
| LDH <sub>-</sub> , LDL <sub>-</sub> to GND                                                                                       | .....-0.3V to +6V     |
| DATA <sub>-</sub> , NDATA <sub>-</sub> , RCV <sub>-</sub> , NRCV <sub>-</sub> , LDEN <sub>-</sub> ,<br>NLDEN <sub>-</sub> to GND | .....-2.5V to +5V     |
| DATA <sub>-</sub> to NDATA <sub>-</sub> , RCV <sub>-</sub> to NRCV <sub>-</sub> ,<br>LDEN <sub>-</sub> to NLDEN <sub>-</sub>     | .....±1.5V            |
| TDATA <sub>-</sub> , TRCV <sub>-</sub> , TLDEN <sub>-</sub> to GND                                                               | .....-2.5V to +5V     |
| DATA <sub>-</sub> , NDATA <sub>-</sub> to TDATA <sub>-</sub>                                                                     | .....±2V              |
| RCV <sub>-</sub> , NRCV <sub>-</sub> to TRCV <sub>-</sub>                                                                        | .....±2V              |
| LDEN <sub>-</sub> , NLDEN <sub>-</sub> to TLDEN <sub>-</sub>                                                                     | .....±2V              |
| V <sub>CCO</sub> <sub>-</sub> to GND                                                                                             | .....-0.3V to +5V     |
| SCLK, DIN, $\overline{\text{CS}}$ , $\overline{\text{RST}}$ to GND                                                               | .....-1V to +5V       |

|                                                                                                                           |                                                           |
|---------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|
| DHV <sub>-</sub> , DLV <sub>-</sub> , DTV <sub>-</sub> , CHV <sub>-</sub> , CLV <sub>-</sub> ,<br>COM <sub>-</sub> to GND | .....-2.5V to +7.5V                                       |
| CPHV <sub>-</sub> to GND                                                                                                  | .....-1V to +8.5V                                         |
| CPLV <sub>-</sub> to GND                                                                                                  | .....-3.5V to +6V                                         |
| DHV <sub>-</sub> to DLV <sub>-</sub>                                                                                      | .....±10V                                                 |
| DHV <sub>-</sub> to DTV <sub>-</sub>                                                                                      | .....±10V                                                 |
| DLV <sub>-</sub> to DTV <sub>-</sub>                                                                                      | .....±10V                                                 |
| CHV <sub>-</sub> or CLV <sub>-</sub> to DUT <sub>-</sub>                                                                  | .....±10V                                                 |
| CH <sub>-</sub> , NCH <sub>-</sub> , CL <sub>-</sub> , NCL <sub>-</sub> to GND                                            | .....-1V to +5V                                           |
| All Other Pins to GND                                                                                                     | .....(V <sub>EE</sub> - 0.3V) to (V <sub>CC</sub> + 0.3V) |
| TEMP Current                                                                                                              | .....-0.5mA to +20mA                                      |
| DUT <sub>-</sub> Short Circuit to -1.5V to +6.5V                                                                          | .....Continuous                                           |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)                                                                     | .....                                                     |
| MAX9969 <sub>-</sub> CCQ (derate 167mW/°C above +70°C) ...13.3W*                                                          | .....                                                     |
| Storage Temperature Range                                                                                                 | .....-65°C to +150°C                                      |
| Junction Temperature                                                                                                      | .....+125°C                                               |

\*Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +9.75V, V<sub>EE</sub> = -4.75V, V<sub>CCO</sub> = +2.5V, SC1 = SC0 = 0, V<sub>CPHV</sub> = +7.2V, V<sub>CPLV</sub> = -2.2V, V<sub>LDH</sub> = V<sub>LDL</sub> = 0, V<sub>GS</sub> = 0, T<sub>J</sub> = +85°C, unless otherwise noted. All temperature coefficients are measured at T<sub>J</sub> = +60°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER                              | SYMBOL           | CONDITIONS                                                                                                                     | MIN   | TYP   | MAX   | UNITS |
|----------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------|
| POWER SUPPLIES                         |                  |                                                                                                                                |       |       |       |       |
| Positive Supply                        | V <sub>CC</sub>  |                                                                                                                                | 9.5   | 9.75  | 10.5  | V     |
| Negative Supply                        | V <sub>EE</sub>  |                                                                                                                                | -5.25 | -4.75 | -4.50 | V     |
| Positive Supply Current (Note 2)       | I <sub>CC</sub>  | V <sub>LDH</sub> = V <sub>LDL</sub> = 0, R <sub>L</sub> ≥ 10MΩ                                                                 |       | 165   | 185   | mA    |
|                                        |                  | V <sub>LDH</sub> = V <sub>LDL</sub> = 3.5V, R <sub>L</sub> = 0, V <sub>COM</sub> = 1.5V, load enabled, driver = high impedance |       | 245   | 275   |       |
| Negative Supply Current (Note 2)       | I <sub>EE</sub>  | V <sub>LDH</sub> = V <sub>LDL</sub> = 0, R <sub>L</sub> ≥ 10MΩ                                                                 |       | -235  | -260  | mA    |
|                                        |                  | V <sub>LDH</sub> = V <sub>LDL</sub> = 3.5V, R <sub>L</sub> = 0, V <sub>COM</sub> = -1V, load enabled, driver = high impedance  |       | -315  | -350  |       |
| Power Dissipation (Notes 2, 3)         | P <sub>D</sub>   | V <sub>LDH</sub> = V <sub>LDL</sub> = 0                                                                                        |       | 2.8   | 3.2   | W     |
|                                        |                  | V <sub>LDH</sub> = V <sub>LDL</sub> = 3.5V, R <sub>L</sub> = 0, V <sub>COM</sub> = 1.5V, load enabled, driver = high impedance |       | 3.3   | 3.7   |       |
| DUT_ CHARACTERISTICS                   |                  |                                                                                                                                |       |       |       |       |
| Operating Voltage Range                | V <sub>DUT</sub> | (Note 4)                                                                                                                       | -1.5  |       | +6.5  | V     |
| Leakage Current in High-Impedance Mode | I <sub>DUT</sub> | LLEAK = 0; V <sub>DUT</sub> = -1.5V, 0, +3V, +6.5V                                                                             |       |       | ±3    | μA    |
| Leakage Current in Low-Leakage Mode    |                  | LLEAK = 1; V <sub>DUT</sub> = -1.5V, 0, +3V, +6.5V                                                                             |       |       | ±15   | nA    |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

MAX9969

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +9.75V, V<sub>EE</sub> = -4.75V, V<sub>CCO</sub> = +2.5V, SC1 = SC0 = 0, V<sub>CPHV</sub> = +7.2V, V<sub>CPLV</sub> = -2.2V, V<sub>LDH</sub> = V<sub>LDL</sub> = 0, V<sub>GS</sub> = 0, T<sub>J</sub> = +85°C, unless otherwise noted. All temperature coefficients are measured at T<sub>J</sub> = +60°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER                                                                                      | SYMBOL                                                        | CONDITIONS                                                                                              | MIN                    | TYP  | MAX                    | UNITS |
|------------------------------------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------------------------|------|------------------------|-------|
| Combined Capacitance                                                                           | C <sub>DUT</sub>                                              | Driver in term mode (DUT_ = DTV_)                                                                       |                        | 3    | 5                      | pF    |
|                                                                                                |                                                               | Driver in high-impedance mode                                                                           |                        | 5    | 6                      |       |
| Low-Leakage Enable Time                                                                        |                                                               | (Notes 5, 6)                                                                                            |                        | 20   |                        | μs    |
| Low-Leakage Disable Time                                                                       |                                                               | (Notes 6, 7)                                                                                            |                        | 0.1  |                        | μs    |
| Low-Leakage Recovery                                                                           |                                                               | Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Note 7)                 |                        | 4    |                        | μs    |
| <b>LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)</b> |                                                               |                                                                                                         |                        |      |                        |       |
| Input Bias Current                                                                             | I <sub>BIAS</sub>                                             | MAX9969_RCCQ                                                                                            |                        |      | ±25                    | μA    |
| Settling Time                                                                                  |                                                               | To 0.1% of full scale change (Note 7)                                                                   |                        | 1    |                        | μs    |
| <b>DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)</b>                 |                                                               |                                                                                                         |                        |      |                        |       |
| Input High Voltage                                                                             | V <sub>IH</sub>                                               |                                                                                                         | 0                      |      | 3.5                    | V     |
| Input Low Voltage                                                                              | V <sub>IL</sub>                                               |                                                                                                         | -0.2                   |      | +3.1                   | V     |
| Differential Input Voltage                                                                     | V <sub>DIFF</sub>                                             | Between differential inputs                                                                             | ±0.15                  |      | ±1.00                  | V     |
|                                                                                                |                                                               | Between a differential input and its termination voltage (Note 7)                                       |                        |      | ±1.9                   |       |
| Input Bias Current                                                                             |                                                               | MAX9969_DCCQ, MAX9969_RCCQ                                                                              |                        |      | ±25                    | μA    |
| Input Termination Voltage                                                                      | V <sub>TDATA</sub><br>V <sub>TRCV</sub><br>V <sub>TLDEN</sub> | MAX9969_GCCQ, MAX9969_LCCQ and MAX9969_RCCQ                                                             | 0                      |      | +3.5                   | V     |
| Input Termination Resistor                                                                     |                                                               | MAX9969_GCCQ, MAX9969_LCCQ, and MAX9969_RCCQ between signal and corresponding termination voltage input | 47.5                   |      | 52.5                   | Ω     |
| <b>SINGLE-ENDED CONTROL INPUTS (CS_, SCLK, DIN, RST)</b>                                       |                                                               |                                                                                                         |                        |      |                        |       |
| Internal Threshold Reference                                                                   | V <sub>THRINT</sub>                                           |                                                                                                         | 1.05                   | 1.25 | 1.45                   | V     |
| Internal Reference Output Resistance                                                           | R <sub>O</sub>                                                |                                                                                                         |                        | 20   |                        | kΩ    |
| External Threshold Reference                                                                   | V <sub>THR</sub>                                              |                                                                                                         | 0.43                   |      | 1.73                   | V     |
| Input High Voltage                                                                             | V <sub>IH</sub>                                               |                                                                                                         | V <sub>THR</sub> + 0.2 |      | 3.5                    | V     |
| Input Low Voltage                                                                              | V <sub>IL</sub>                                               |                                                                                                         | -0.1                   |      | V <sub>THR</sub> - 0.2 | V     |
| Input Bias Current                                                                             | I <sub>B</sub>                                                |                                                                                                         |                        |      | ±25                    | μA    |
| <b>SERIAL INTERFACE TIMING (Figure 5)</b>                                                      |                                                               |                                                                                                         |                        |      |                        |       |
| SCLK Frequency                                                                                 | f <sub>SCLK</sub>                                             |                                                                                                         |                        | 50   |                        | MHz   |
| SCLK Pulse-Width High                                                                          | t <sub>CH</sub>                                               |                                                                                                         | 8                      |      |                        | ns    |
| SCLK Pulse-Width Low                                                                           | t <sub>CL</sub>                                               |                                                                                                         | 8                      |      |                        | ns    |
| CS Low to SCLK High Setup                                                                      | t <sub>CSS0</sub>                                             |                                                                                                         | 3.5                    |      |                        | ns    |
| CS High to SCLK High Setup                                                                     | t <sub>CSS1</sub>                                             |                                                                                                         | 3.5                    |      |                        | ns    |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV} = +7.2V$ ,  $V_{CPLV} = -2.2V$ ,  $V_{LDH} = V_{LDL} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^\circ C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                                                                         | SYMBOL                        | CONDITIONS                                                                                                                                                 |          | MIN   | TYP   | MAX    | UNITS |
|---------------------------------------------------------------------------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------|-------|--------|-------|
| SCLK High to $\overline{CS}$ High Hold                                                            | t <sub>CSH1</sub>             |                                                                                                                                                            |          | 3.5   |       |        | ns    |
| DIN to SCLK High Setup                                                                            | t <sub>DS</sub>               |                                                                                                                                                            |          | 3.5   |       |        | ns    |
| DIN to SCLK High Hold                                                                             | t <sub>DH</sub>               |                                                                                                                                                            |          | 3.5   |       |        | ns    |
| $\overline{CS}$ Pulse Width High                                                                  | t <sub>CSWH</sub>             |                                                                                                                                                            |          | 20    |       |        | ns    |
| TEMPERATURE MONITOR (TEMP)                                                                        |                               |                                                                                                                                                            |          |       |       |        |       |
| Nominal Voltage                                                                                   |                               | T <sub>J</sub> = +70°C, R <sub>L</sub> ≥ 10MΩ                                                                                                              |          | 3.33  |       |        | V     |
| Temperature Coefficient                                                                           |                               |                                                                                                                                                            |          | +10   |       |        | mV/°C |
| Output Resistance                                                                                 |                               |                                                                                                                                                            |          | 20    |       |        | kΩ    |
| DRIVERS (Note 8)                                                                                  |                               |                                                                                                                                                            |          |       |       |        |       |
| DC OUTPUT CHARACTERISTICS (R <sub>L</sub> ≥ 10MΩ)                                                 |                               |                                                                                                                                                            |          |       |       |        |       |
| DHV <sub>-</sub> , DLV <sub>-</sub> , DTV <sub>-</sub> ,<br>Output Offset Voltage                 | V <sub>OS</sub>               | At DUT <sub>-</sub> with V <sub>DHV<sub>-</sub></sub> ,<br>V <sub>DTV<sub>-</sub></sub> , V <sub>DLV<sub>-</sub></sub><br>independently tested<br>at +1.5V | MAX9969A | ±15   |       | mV     |       |
|                                                                                                   |                               |                                                                                                                                                            | MAX9969B | ±100  |       |        |       |
| DHV <sub>-</sub> , DLV <sub>-</sub> , DTV <sub>-</sub> , Output Offset<br>Temperature Coefficient |                               |                                                                                                                                                            |          | +200  |       | μV/°C  |       |
| DHV <sub>-</sub> , DLV <sub>-</sub> , DTV <sub>-</sub> , Gain                                     | A <sub>V</sub>                | Measured with V <sub>DHV<sub>-</sub></sub> , V <sub>DLV<sub>-</sub></sub> ,<br>and V <sub>DTV<sub>-</sub></sub> at 0 and 4.5V                              |          | 0.960 | 1.001 | V/V    |       |
| DHV <sub>-</sub> , DLV <sub>-</sub> , DTV <sub>-</sub> , Gain<br>Temperature Coefficient          |                               |                                                                                                                                                            |          | -50   |       | ppm/°C |       |
| Linearity Error                                                                                   |                               | V <sub>DUT<sub>-</sub></sub> = 1.5V, 3V (Note 9)                                                                                                           |          | ±5    |       | mV     |       |
|                                                                                                   |                               | Full range (Notes 9, 10)                                                                                                                                   |          | ±15   |       |        |       |
| DHV <sub>-</sub> to DLV <sub>-</sub> Crosstalk                                                    |                               | V <sub>DLV<sub>-</sub></sub> = 0; V <sub>DHV<sub>-</sub></sub> = 200mV, 6.5V                                                                               |          | ±2    |       | mV     |       |
| DLV <sub>-</sub> to DHV <sub>-</sub> Crosstalk                                                    |                               | V <sub>DHV<sub>-</sub></sub> = 5V; V <sub>DLV<sub>-</sub></sub> = -1.5V, +4.8V                                                                             |          | ±2    |       | mV     |       |
| DTV <sub>-</sub> to DLV <sub>-</sub> and DHV <sub>-</sub><br>Crosstalk                            |                               | V <sub>DHV<sub>-</sub></sub> = 3V; V <sub>DLV<sub>-</sub></sub> = 0;<br>V <sub>DTV<sub>-</sub></sub> = -1.5V, +6.5V                                        |          | ±2    |       | mV     |       |
| DHV <sub>-</sub> to DTV <sub>-</sub> Crosstalk                                                    |                               | V <sub>DTV<sub>-</sub></sub> = 1.5V; V <sub>DLV<sub>-</sub></sub> = 0; V <sub>DHV<sub>-</sub></sub> = 1.6V, 3V                                             |          | ±2    |       | mV     |       |
| DLV <sub>-</sub> to DTV <sub>-</sub> Crosstalk                                                    |                               | V <sub>DTV<sub>-</sub></sub> = 1.5V; V <sub>DHV<sub>-</sub></sub> = 3V; V <sub>DLV<sub>-</sub></sub> = 0, 1.4V                                             |          | ±2    |       | mV     |       |
| DHV <sub>-</sub> , DTV <sub>-</sub> , DLV <sub>-</sub> DC<br>Power-Supply Rejection Ratio         | PSRR                          | (Note 11)                                                                                                                                                  |          | ±18   |       | mV/V   |       |
| Maximum DC Drive Current                                                                          | I <sub>DUT<sub>-</sub></sub>  |                                                                                                                                                            |          | ±40   | ±80   | mA     |       |
| DC Output Resistance                                                                              | R <sub>DUT<sub>-</sub></sub>  | I <sub>DUT<sub>-</sub></sub> = ±30mA (Note 12)                                                                                                             |          | 49    | 50    | 51     | Ω     |
| DC Output Resistance Variation                                                                    | _R <sub>DUT<sub>-</sub></sub> | I <sub>DUT<sub>-</sub></sub> = ±1mA, ±8mA                                                                                                                  |          | 0.5   | 1     | Ω      |       |
|                                                                                                   |                               | I <sub>DUT<sub>-</sub></sub> = ±1mA, ±8mA, ±15mA, ±40mA                                                                                                    |          | 0.75  | 1.5   |        |       |
| DYNAMIC OUTPUT CHARACTERISTICS (Z <sub>L</sub> = 50Ω)                                             |                               |                                                                                                                                                            |          |       |       |        |       |
| AC Drive Current                                                                                  |                               |                                                                                                                                                            |          | ±80   |       |        | mA    |
| Drive-Mode Overshoot                                                                              |                               | V <sub>DLV<sub>-</sub></sub> = 0, V <sub>DHV<sub>-</sub></sub> = 0.1V                                                                                      |          | 15    | 22    | mV     |       |
|                                                                                                   |                               | V <sub>DLV<sub>-</sub></sub> = 0, V <sub>DHV<sub>-</sub></sub> = 1V                                                                                        |          | 110   | 130   |        |       |
|                                                                                                   |                               | V <sub>DLV<sub>-</sub></sub> = 0, V <sub>DHV<sub>-</sub></sub> = 3V                                                                                        |          | 210   | 370   |        |       |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

MAX9969

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>CC</sub> = +9.75V, V<sub>EE</sub> = -4.75V, V<sub>CCO</sub> = +2.5V, SC1 = SC0 = 0, V<sub>CPHV</sub> = +7.2V, V<sub>CPV</sub> = -2.2V, V<sub>LDH</sub> = V<sub>LDL</sub> = 0, V<sub>GS</sub> = 0, T<sub>J</sub> = +85°C, unless otherwise noted. All temperature coefficients are measured at T<sub>J</sub> = +60°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER                                               | SYMBOL | CONDITIONS                                                                                                    |                                                                                                     | MIN                                          | TYP  | MAX  | UNITS |     |
|---------------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|----------------------------------------------|------|------|-------|-----|
| Drive-Mode Undershoot                                   |        | VDLV_ = 0, VDHV_ = 0.1V                                                                                       |                                                                                                     |                                              | 4    | 11   | mV    |     |
|                                                         |        | VDLV_ = 0, VDHV_ = 1V                                                                                         |                                                                                                     |                                              | 20   | 65   |       |     |
|                                                         |        | VDLV_ = 0, VDHV_ = 3V                                                                                         |                                                                                                     |                                              | 30   | 185  |       |     |
| Term-Mode Overshoot                                     |        | (Note 13)                                                                                                     | V <sub>DUT</sub> _ = 1.0V <sub>P-P</sub> ,<br>t <sub>R</sub> = t <sub>F</sub> = 250ps<br>10% to 90% |                                              | 60   | 150  | mV    |     |
|                                                         |        |                                                                                                               | V <sub>DUT</sub> _ = 3.0V <sub>P-P</sub> ,<br>t <sub>R</sub> = t <sub>F</sub> = 500ps<br>10% to 90% |                                              | 0    |      |       |     |
| Term-Mode Spike                                         |        | VDHV_ = V <sub>DTV</sub> _ = 1V, V <sub>DLV</sub> _ = 0                                                       |                                                                                                     |                                              | 180  | 250  | mV    |     |
|                                                         |        | VDLV_ = V <sub>DTV</sub> _ = 0, VDHV_ = 1V                                                                    |                                                                                                     |                                              | 180  | 250  |       |     |
| High-Impedance Mode Spike                               |        | VDLV_ = -1.0V, VDHV_ = 0                                                                                      |                                                                                                     |                                              | 100  |      | mV    |     |
|                                                         |        | VDLV_ = 0, VDHV_ = 1V                                                                                         |                                                                                                     |                                              | 100  |      |       |     |
| Settling Time to within 25mV                            |        | 3V step (Note 14)                                                                                             |                                                                                                     |                                              | 4    |      | ns    |     |
| Settling Time to within 5mV                             |        | 3V step (Note 14)                                                                                             |                                                                                                     |                                              | 40   |      | ns    |     |
| TIMING CHARACTERISTICS (Z <sub>L</sub> = 50Ω) (Note 15) |        |                                                                                                               |                                                                                                     |                                              |      |      |       |     |
| Prop Delay, Data to Output                              | tpDD   |                                                                                                               |                                                                                                     | 1.5                                          | 1.7  | 2.0  | ns    |     |
| Prop Delay Match, t <sub>LH</sub> vs. t <sub>HL</sub>   |        | 3V <sub>P-P</sub>                                                                                             |                                                                                                     |                                              | ±40  | ±80  | ps    |     |
| Prop Delay Match, Drivers within Package                |        | (Note 16)                                                                                                     |                                                                                                     |                                              | 40   |      | ps    |     |
| Prop Delay Temperature Coefficient                      |        |                                                                                                               |                                                                                                     |                                              | +1.6 |      | ps/°C |     |
| Prop Delay Change vs. Pulse Width                       |        | 0.2V <sub>P-P</sub> , 40MHz,<br>0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width                   | MAX9969_DCCQ                                                                                        |                                              | ±70  |      | ps    |     |
|                                                         |        |                                                                                                               | MAX9969_GCCQ<br>MAX9969_LCCQ<br>MAX9969_RCCQ                                                        |                                              | ±25  | ±50  |       |     |
|                                                         |        |                                                                                                               | MAX9969_DCCQ                                                                                        |                                              | ±70  |      |       |     |
|                                                         |        | 1V <sub>P-P</sub> , 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width                        | MAX9969_GCCQ<br>MAX9969_LCCQ<br>MAX9969_RCCQ                                                        |                                              | ±25  | ±50  |       |     |
|                                                         |        |                                                                                                               | 3V <sub>P-P</sub> , 40MHz, 0.9ns to 24.1ns pulse width, relative to 12.5ns pulse width              | MAX9969_DCCQ                                 |      | ±80  |       |     |
|                                                         |        |                                                                                                               |                                                                                                     | MAX9969_GCCQ<br>MAX9969_LCCQ<br>MAX9969_RCCQ |      | ±35  |       | ±60 |
|                                                         |        | 5V <sub>P-P</sub> , Z <sub>L</sub> = 500Ω, 40MHz, 1.4ns to 23.6ns pulse width, relative to 12.5ns pulse width |                                                                                                     | MAX9969_DCCQ                                 |      | ±100 |       |     |
|                                                         |        |                                                                                                               | MAX9969_GCCQ<br>MAX9969_LCCQ<br>MAX9969_RCCQ                                                        |                                              | ±100 |      |       |     |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO-} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV-} = +7.2V$ ,  $V_{CPLV-} = -2.2V$ ,  $V_{LDH-} = V_{LDL-} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                                | SYMBOL             | CONDITIONS                                                                             | MIN                                   | TYP  | MAX  | UNITS             |
|----------------------------------------------------------|--------------------|----------------------------------------------------------------------------------------|---------------------------------------|------|------|-------------------|
| Prop Delay Change vs. Common-Mode Voltage                |                    | $V_{DHV-} - V_{DLV-} = 1V$ , $V_{DHV-} = 0$ to $6V$                                    |                                       | 50   | 75   | ps                |
| Prop Delay, Drive to High Impedance                      | $t_{PDDZ}$         | $V_{DHV-} = 1.0V$ , $V_{DLV-} = -1.0V$ , $V_{DTV-} = 0$                                | 2.0                                   | 2.3  | 2.6  | ns                |
| Prop Delay, High Impedance to Drive                      | $t_{PDZD}$         | $V_{DHV-} = 1.0V$ , $V_{DLV-} = -1.0V$ , $V_{DTV-} = 0$                                | 3.0                                   | 3.4  | 3.9  | ns                |
| Prop Delay Match, $t_{PDDZ}$ vs. $t_{PDZD}$              |                    |                                                                                        | -1.3                                  | -1.1 | -0.9 | ns                |
| Prop Delay Match, $t_{PDDZ}$ vs. $t_{LH}$                |                    |                                                                                        | 0.4                                   | 0.6  | 0.8  | ns                |
| Prop Delay, Drive to Term                                | $t_{PDDT}$         | $V_{DHV-} = 3V$ , $V_{DLV-} = 0$ , $V_{DTV-} = 1.5V$                                   | 1.7                                   | 2.0  | 2.3  | ns                |
| Prop Delay, Term to Drive                                | $t_{PDTD}$         | $V_{DHV-} = 3V$ , $V_{DLV-} = 0$ , $V_{DTV-} = 1.5V$                                   | 2.0                                   | 2.3  | 2.7  | ns                |
| Prop Delay Match, $t_{PDDT}$ vs. $t_{PDTD}$              |                    |                                                                                        | 0.5                                   | 0.3  | 0.1  | ns                |
| Prop Delay Match, $t_{PDDT}$ vs. $t_{LH}$                |                    |                                                                                        | 0.1                                   | 0.3  | 0.5  | ns                |
| <b>DYNAMIC PERFORMANCE (<math>Z_L = 50\Omega</math>)</b> |                    |                                                                                        |                                       |      |      |                   |
| Rise and Fall Time                                       | $t_R, t_F$         | 0.2V <sub>P-P</sub> , 10% to 90%                                                       | 300                                   | 350  | 400  | ps                |
|                                                          |                    | 1V <sub>P-P</sub> , 10% to 90%                                                         | 330                                   | 390  | 450  |                   |
|                                                          |                    | 3V <sub>P-P</sub> , 10% to 90%                                                         | 500                                   | 650  | 750  |                   |
|                                                          |                    | 5V <sub>P-P</sub> , $Z_L = 500\Omega$ , 10% to 90%                                     | 800                                   | 1000 | 1200 |                   |
| Rise and Fall Time Match                                 | $t_R$ vs. $t_F$    | 3V <sub>P-P</sub> , 10% to 90%                                                         | $\pm 50$                              |      |      | ps                |
| SC1 = 0, SC0 = 1 Slew Rate                               |                    | Percent of full speed (SC0 = SC1 = 0), 3V <sub>P-P</sub> , 20% to 80%                  | 63                                    | 70   | 77   | %                 |
| SC1 = 1, SC0 = 0 Slew Rate                               |                    | Percent of full speed (SC0 = SC1 = 0), 3V <sub>P-P</sub> , 20% to 80%                  | 40                                    | 47   | 55   | %                 |
| SC1 = 1, SC0 = 1 Slew Rate                               |                    | Percent of full speed (SC0 = SC1 = 0), 3V <sub>P-P</sub> , 20% to 80%                  | 18                                    | 25   | 32   | %                 |
| Minimum Pulse Width                                      |                    | (Note 17)                                                                              | 0.2V <sub>P-P</sub>                   | 550  | 630  | ps                |
|                                                          |                    |                                                                                        | 1V <sub>P-P</sub>                     | 550  | 630  |                   |
|                                                          |                    |                                                                                        | 3V <sub>P-P</sub>                     | 850  | 1000 |                   |
|                                                          |                    |                                                                                        | 5V <sub>P-P</sub> , $Z_L = 500\Omega$ | 1300 |      |                   |
| Data Rate                                                |                    | (Note 18)                                                                              | 0.2V <sub>P-P</sub>                   | 1800 |      | Mbps              |
|                                                          |                    |                                                                                        | 1V <sub>P-P</sub>                     | 1800 |      |                   |
|                                                          |                    |                                                                                        | 3V <sub>P-P</sub>                     | 1200 |      |                   |
|                                                          |                    |                                                                                        | 5V <sub>P-P</sub> , $Z_L = 500\Omega$ | 800  |      |                   |
| Dynamic Crosstalk                                        |                    | (Note 19)                                                                              | 12                                    |      |      | mV <sub>P-P</sub> |
| Rise and Fall Time, Drive to Term                        | $t_{DTR}, t_{DTF}$ | $V_{DHV-} = 3V$ , $V_{DLV-} = 0$ , $V_{DTV-} = 1.5V$ , 10% to 90%, Figure 1a (Note 20) | 0.6                                   | 1.0  | 1.3  | ns                |
| Rise and Fall Time, Term to Drive                        | $t_{TDR}, t_{TDF}$ | $V_{DHV-} = 3V$ , $V_{DLV-} = 0$ , $V_{DTV-} = 1.5V$ , 10% to 90%, Figure 1b (Note 20) | 0.6                                   | 1.0  | 1.3  | ns                |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

MAX9969

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO\_} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV\_} = +7.2V$ ,  $V_{CPLV\_} = -2.2V$ ,  $V_{LDH\_} = V_{LDL\_} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                    | SYMBOL               | CONDITIONS                                                                                                                                                                           |                                  | MIN    | TYP  | MAX  | UNITS |
|----------------------------------------------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|--------|------|------|-------|
| COMPARATORS (Note 8)                         |                      |                                                                                                                                                                                      |                                  |        |      |      |       |
| DC CHARACTERISTICS                           |                      |                                                                                                                                                                                      |                                  |        |      |      |       |
| Input Voltage Range                          | V <sub>IN</sub>      | (Note 4)                                                                                                                                                                             |                                  | -1.5   |      | +6.5 | V     |
| Differential Input Voltage                   | V <sub>DIFF</sub>    |                                                                                                                                                                                      |                                  | ±8     |      |      | V     |
| Hysteresis                                   | V <sub>HYST</sub>    |                                                                                                                                                                                      |                                  |        | 0    |      | mV    |
| Input Offset Voltage                         | V <sub>OS</sub>      | V <sub>DUT_</sub> = 1.5V                                                                                                                                                             | MAX9969A                         |        |      | ±20  | mV    |
|                                              |                      |                                                                                                                                                                                      | MAX9969B                         |        |      | ±100 |       |
| Input Offset Voltage Temperature Coefficient |                      |                                                                                                                                                                                      |                                  |        | ±10  |      | µV/°C |
| Common-Mode Rejection Ratio                  | CMRR                 | V <sub>DUT_</sub> = -1.5V, +6.5V (Note 21)                                                                                                                                           |                                  | ±0.25  |      | ±2   | mV/V  |
| Linearity Error                              |                      | (Note 10)                                                                                                                                                                            | V <sub>DUT_</sub> = 1.5V, 3V     |        |      | ±3   | mV    |
|                                              |                      |                                                                                                                                                                                      | V <sub>DUT_</sub> = -1.5V, +6.5V |        |      | ±10  |       |
| Power-Supply Rejection Ratio                 | PSRR                 | V <sub>DUT_</sub> = 1.5V (Note 11)                                                                                                                                                   |                                  | ±0.035 |      | ±2   | mV/V  |
| AC CHARACTERISTICS (Note 22)                 |                      |                                                                                                                                                                                      |                                  |        |      |      |       |
| Bandwidth                                    |                      | Term mode, t <sub>R</sub> = t <sub>F</sub> = 150ps                                                                                                                                   |                                  | 2      | 3    |      | GHz   |
|                                              |                      | High-impedance mode                                                                                                                                                                  |                                  | 0.65   | 0.75 |      |       |
| Minimum Pulse Width                          | t <sub>PW(MIN)</sub> | (Note 23)                                                                                                                                                                            | MAX9969_LCCQ and MAX9969_RCCQ    |        | 500  | 650  | ps    |
|                                              |                      |                                                                                                                                                                                      | MAX9969_DCCQ and MAX9969_GCCQ    |        | 600  |      |       |
| Prop Delay                                   | t <sub>PDL</sub>     |                                                                                                                                                                                      |                                  | 1.0    | 1.3  | 1.6  | ns    |
| Prop Delay Temperature Coefficient           |                      |                                                                                                                                                                                      |                                  |        | +1.7 |      | ps/°C |
| Prop Delay Match, High/Low vs. Low/High      |                      |                                                                                                                                                                                      |                                  |        | ±10  | ±50  | ps    |
| Prop Delay Match High vs. Low Comparator     |                      |                                                                                                                                                                                      |                                  |        | ±50  |      | ps    |
| Prop Delay Match, Comparators within Package |                      | (Note 16)                                                                                                                                                                            |                                  |        | ±80  |      | ps    |
| Prop Delay Dispersion vs. Common-Mode Input  |                      | V <sub>CHV_</sub> = V <sub>CLV_</sub> = -1.4V to +6.4V (Note 24)                                                                                                                     |                                  |        | 40   | 60   | ps    |
| Prop Delay Dispersion vs. Overdrive          |                      | V <sub>CHV_</sub> = V <sub>CLV_</sub> = 0.1V to 0.9V, V <sub>DUT_</sub> = 1V <sub>P-P</sub> , t <sub>R</sub> = t <sub>F</sub> = 250ps, 10% to 90% relative to timing at 50% point    |                                  |        | ±40  | ±60  | ps    |
|                                              |                      | V <sub>CHV_</sub> = V <sub>CLV_</sub> = 40mV to 160mV, V <sub>DUT_</sub> = 0.2V <sub>P-P</sub> , t <sub>R</sub> = t <sub>F</sub> = 150ps, 10% to 90% relative to timing at 50% point |                                  |        | ±40  | ±60  |       |
| Prop Delay Dispersion vs. Pulse Width        |                      | 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width                                                                                                                          |                                  |        | ±30  | ±50  | ps    |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO\_} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV\_} = +7.2V$ ,  $V_{CPLV\_} = -2.2V$ ,  $V_{LDH\_} = V_{LDL\_} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                            | SYMBOL | CONDITIONS                                                                                        |                                                        | MIN          | TYP           | MAX          | UNITS |
|--------------------------------------|--------|---------------------------------------------------------------------------------------------------|--------------------------------------------------------|--------------|---------------|--------------|-------|
| Prop Delay Dispersion vs. Slew Rate  |        | 0.5V/ns to 6V/ns slew rate, relative to 4V/ns slew rate                                           |                                                        |              | ±30           | ±60          | ps    |
| Waveform Tracking 10% to 90%         |        | VDUT_ = 1.0VP-P, tR = tF = 250ps, 10% to 90% relative to timing at 50% point, term mode           |                                                        |              | ±40           | ±60          | ps    |
|                                      |        | VDUT_ = 1.0VP-P, tR = tF = 250ps, 10% to 90% relative to timing at 50% point, high-impedance mode |                                                        |              | ±190          | ±250         |       |
|                                      |        | VDUT_ = 3VP-P, tR = tF = 500ps, 10% to 90% relative to timing at 50% point, high-impedance mode   |                                                        |              | ±150          | ±200         |       |
| DUT_ Slew-Rate Tracking              |        | Term mode                                                                                         |                                                        |              | 6             |              | V/ns  |
|                                      |        | High-impedance mode                                                                               |                                                        |              | 5             |              |       |
| LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_) |        |                                                                                                   |                                                        |              |               |              |       |
| VCCO_ Voltage Range                  | VVCCO_ |                                                                                                   |                                                        | 0            |               | 3.5          | V     |
| VCCO_ Current                        | IVCCO_ |                                                                                                   |                                                        |              | 32            |              | mA    |
| Output Low Voltage Compliance        |        | Set by IOL, RTERM, and VCCO_                                                                      |                                                        |              | -0.5          |              | V     |
| Output High Current                  | IOH    | MAX9969_DCCQ, MAX9969_GCCQ                                                                        |                                                        | -0.1         |               | +0.3         | mA    |
| Output Low Current                   | IOL    | MAX9969_DCCQ, MAX9969_GCCQ                                                                        |                                                        |              | 8             |              | mA    |
| Output Current Swing                 |        | MAX9969_DCCQ, MAX9969_GCCQ                                                                        |                                                        | 7.6          |               | 8.4          | mA    |
| Output High Voltage                  | VOH    | ICH_ = INCH_ = ICL_ = INCL_ = 0, MAX9969_LCCQ, MAX9969_RCCQ                                       |                                                        | VCCO_ - 0.05 | VCCO_ - 0.005 | VCCO_ + 0.01 | V     |
| Output Low Voltage                   | VOL    | ICH_ = INCH_ = ICL_ = INCL_ = 0, MAX9969_LCCQ, MAX9969_RCCQ                                       |                                                        |              | VCCO_ - 0.4   |              | V     |
| Output Voltage Swing                 |        | ICH_ = INCH_ = ICL_ = INCL_ = 0, MAX9969_LCCQ, MAX9969_RCCQ                                       |                                                        | 380          | 400           | 420          | mV    |
| Output Termination Resistor          | RTERM  | Single-ended measurement from VCCO_ to CH_, NCH_, CL_, NCL_, MAX9969_LCCQ, MAX9969_RCCQ           |                                                        | 48           |               | 52           | Ω     |
| Differential Rise and Fall Times     | tR, tF | 20% to 80%                                                                                        | MAX9969_DCCQ, MAX9969_GCCQ, RTERM = 50Ω at end of line |              | 240           |              | ps    |
|                                      |        |                                                                                                   | MAX9969_LCCQ, MAX9969_RCCQ                             |              | 190           | 230          |       |
| CLAMPS                               |        |                                                                                                   |                                                        |              |               |              |       |
| High Clamp Input Voltage Range       | VCPH_  |                                                                                                   |                                                        | 0            |               | +7.5         | V     |
| Low Clamp Input Voltage Range        | VCPL_  |                                                                                                   |                                                        | -2.5         |               | +5.0         | V     |
| Clamp Offset Voltage                 | VOS    | At DUT_ with IDUT_ = 1mA, VCPHV_ = 0                                                              |                                                        |              |               | ±100         | mV    |
|                                      |        | At DUT_ with IDUT_ = -1mA, VCPLV_ = 0                                                             |                                                        |              |               | ±100         |       |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

MAX9969

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO\_} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV\_} = +7.2V$ ,  $V_{CPLV\_} = -2.2V$ ,  $V_{LDH\_} = V_{LDL\_} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                                                                  | SYMBOL  | CONDITIONS                                                   |                             | MIN   | TYP   | MAX | UNITS  |
|--------------------------------------------------------------------------------------------|---------|--------------------------------------------------------------|-----------------------------|-------|-------|-----|--------|
| Offset-Voltage Temperature Coefficient                                                     |         |                                                              |                             | ±250  |       |     | μV/°C  |
| Clamp Power-Supply Rejection Ratio                                                         | PSRR    | (Note 11)                                                    | IDUT_ = 1mA,<br>VCPHV_ = 0  | ±10   |       |     | mV/V   |
|                                                                                            |         |                                                              | IDUT_ = -1mA,<br>VCPLV_ = 0 | ±10   |       |     |        |
| Voltage Gain                                                                               | AV      |                                                              |                             | 0.960 | 1.005 |     | V/V    |
| Voltage-Gain Temperature Coefficient                                                       |         |                                                              |                             | -30   |       |     | ppm/°C |
| Clamp Linearity                                                                            |         | IDUT_ = 1mA, VCPLV_ = -1.5V,<br>VCPHV_ = 0 to 6.5V           |                             | ±10   |       |     | mV     |
|                                                                                            |         | IDUT_ = -1mA, VCPHV_ = 6.5V,<br>VCPLV_ = -1.5V to +5V        |                             | ±10   |       |     |        |
| Short-Circuit Output Current                                                               | ISCDUT_ | VCPHV_ = 0, VCPLV_ = -1.5V,<br>VDUT_ = 6.5V                  |                             | 40    | 80    |     | mA     |
|                                                                                            |         | VCPHV_ = 6.5V, VCPLV_ = 5V,<br>VDUT_ = -1.5V                 |                             | -80   | -40   |     |        |
| Clamp DC Impedance                                                                         | ROUT    | VCPHV_ = 3V, VCPLV_ = 0,<br>IDUT_ = ±5mA and ±15mA           |                             | 50    | 55    |     | Ω      |
| Clamp DC Impedance Variation                                                               |         | VCPHV_ = 2.5V; VCPLV_ = -1.5V;<br>IDUT_ = 10mA, 20mA, 30mA   |                             | 1.5   |       |     | Ω      |
|                                                                                            |         | VCPHV_ = 6.5V; VCPLV_ = 2.5V;<br>IDUT_ = -10mA, -20mA, -30mA |                             | 1.5   |       |     |        |
| ACTIVE LOAD (VCOM_ = 1.5V, RL > 1MΩ, driver in high-impedance mode unless otherwise noted) |         |                                                              |                             |       |       |     |        |
| COM_ Voltage Range                                                                         | VCOM_   |                                                              |                             | -1    | +6    |     | V      |
| Differential Voltage Range                                                                 |         | VDUT_ - VCOM_                                                |                             | -7.5  | +7.5  |     | V      |
| COM_ Offset Voltage                                                                        | Vos     | ISOURCE = ISINK = 20mA                                       |                             | ±100  |       |     | mV     |
| Offset-Voltage Temperature Coefficient                                                     |         |                                                              |                             | +100  |       |     | μV/°C  |
| COM_ Voltage Gain                                                                          | AV      | VCOM_ = 0, 4.5V; ISOURCE = ISINK = 20mA                      |                             | 0.98  | 1.00  |     | V/V    |
| Voltage-Gain Temperature Coefficient                                                       |         |                                                              |                             | -10   |       |     | ppm/°C |
| COM_ Linearity Error                                                                       |         | VCOM_ = -1V, +6V;<br>ISOURCE = ISINK = 20mA                  |                             | ±3    | ±15   |     | mV     |
| COM_ Output Voltage Power-Supply Rejection Ratio                                           | PSRR    | VCOM_ = 2.5V,<br>ISOURCE = ISINK = 20mA                      |                             | ±10   |       |     | mV/V   |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO\_} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV\_} = +7.2V$ ,  $V_{CPLV\_} = -2.2V$ ,  $V_{LDH\_} = V_{LDL\_} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                              | SYMBOL | CONDITIONS                                                                       |                          | MIN    | TYP | MAX   | UNITS |
|--------------------------------------------------------|--------|----------------------------------------------------------------------------------|--------------------------|--------|-----|-------|-------|
| Output Resistance, Sink or Source                      | Ro     | VDUT_ = 3V, 6.5V with VCOM_ = -1V and VDUT_ = -1.5V, +2V with VCOM_ = 6V         | ISOURCE = ISINK = 35mA   | 30     |     | kΩ    |       |
|                                                        |        |                                                                                  | ISOURCE = ISINK = 1mA    | 500    |     |       |       |
| Output Resistance, Linear Region                       | Ro     | IDUT_ = ±33.25mA, ISOURCE = ISINK = 35mA, VCOM_ = 2.5V verified by deadband test |                          | 1115   |     | Ω     |       |
| Deadband                                               |        | VCOM_ = 2.5V, 95% ISOURCE to 95% ISINK                                           |                          | 700800 |     | mV    |       |
| SOURCE CURRENT (VDUT_ = 4.5V)                          |        |                                                                                  |                          |        |     |       |       |
| Maximum Source Current                                 |        | VLDL_ = 3.8V                                                                     |                          | 3640   |     | mA    |       |
| Source Programming Gain                                | ATC    | VLDL_ = 0.2V, 3V; VLDH_ = 0.1V                                                   |                          | 9.75   | 10  | 10.25 | mA/V  |
| Source Current Offset (Combined Offset of LDL_ and GS) | IOS    | VLDL_ = 200mV                                                                    |                          | -10000 |     | μA    |       |
| Source-Current Temperature Coefficient                 |        | ISOURCE = 35mA                                                                   |                          | -15    |     | μA/°C |       |
| Source-Current Power-Supply Rejection Ratio            | PSRR   | ISOURCE = 25mA                                                                   |                          | ±60    |     | μA/V  |       |
|                                                        |        | ISOURCE = 35mA                                                                   |                          | ±84    |     |       |       |
| Source Current Linearity                               |        | (Note 25)                                                                        | VLDL_ = 100mV, 1V, 2.25V | ±60    |     | μA    |       |
|                                                        |        |                                                                                  | VLDL_ = 3V               | ±130   |     |       |       |
| SINK CURRENT (VDUT_ = -1.5V)                           |        |                                                                                  |                          |        |     |       |       |
| Maximum Sink Current                                   |        | VLDH_ = 3.8V                                                                     |                          | -40-36 |     | mA    |       |
| Sink Programming Gain                                  | ATC    | VLDH_ = 0.2V, 3V; VLDL_ = 0.1V                                                   |                          | -10.25 | -10 | -9.75 | mA/V  |
| Sink-Current Offset (Combined Offset of LDH_ and GS)   | IOS    | VLDH_ = 200mV                                                                    |                          | 01000  |     | μA    |       |
| Sink-Current Temperature Coefficient                   |        | ISINK = 35mA                                                                     |                          | +8     |     | μA/°C |       |
| Sink-Current Power-Supply Rejection Ratio              | PSRR   | ISINK = 25mA                                                                     |                          | ±60    |     | μA/V  |       |
|                                                        |        | ISINK = 35mA                                                                     |                          | ±84    |     |       |       |
| Sink-Current Linearity                                 |        | (Note 25)                                                                        | VLDH_ = 100mV, 1V, 2.25V | ±60    |     | μA    |       |
|                                                        |        |                                                                                  | VLDH_ = 3V               | ±130   |     |       |       |
| GROUND SENSE                                           |        |                                                                                  |                          |        |     |       |       |
| GS Voltage Range                                       | VGS    | Verified by GS common-mode error test                                            |                          | ±250   |     | mV    |       |
| GS Common-Mode Error                                   |        | VDUT_ = -1.5V, VGS = ±250mV, VLDH_ - VGS = 0.2V                                  |                          | ±20    |     | μA    |       |
|                                                        |        | VDUT_ = +4.5V, VGS = ±250mV, VLDL_ - VGS = 0.2V                                  |                          | ±20    |     |       |       |
| GS Input Bias Current                                  |        | VGS = 0                                                                          |                          | ±25    |     | μA    |       |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

MAX9969

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO\_} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV\_} = +7.2V$ ,  $V_{CPLV\_} = -2.2V$ ,  $V_{LDH\_} = V_{LDL\_} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

| PARAMETER                                        | SYMBOL           | CONDITIONS                                                                       |                                                                   | MIN | TYP | MAX | UNITS |   |
|--------------------------------------------------|------------------|----------------------------------------------------------------------------------|-------------------------------------------------------------------|-----|-----|-----|-------|---|
| AC CHARACTERISTICS (Z <sub>L</sub> = 50Ω to GND) |                  |                                                                                  |                                                                   |     |     |     |       |   |
| Enable Time                                      | t <sub>EN</sub>  | (Note 26)                                                                        | I <sub>SOURCE</sub> = 10mA,<br>V <sub>COM<sub>L</sub></sub> = -1V | 3   | 3.5 | 4   | ns    |   |
|                                                  |                  |                                                                                  | I <sub>SINK</sub> = 10mA,<br>V <sub>COM<sub>L</sub></sub> = 1V    | 3   | 3.5 | 4   |       |   |
| Disable Time                                     | t <sub>DIS</sub> | (Note 26)                                                                        | I <sub>SOURCE</sub> = 10mA,<br>V <sub>COM<sub>L</sub></sub> = 1V  | 1.7 | 2   | 2.3 | ns    |   |
|                                                  |                  |                                                                                  | I <sub>SINK</sub> = 10mA,<br>V <sub>COM<sub>L</sub></sub> = -1V   | 1.7 | 2   | 2.3 |       |   |
| Current Settling Time on<br>Commutation          |                  | I <sub>SOURCE</sub> = I <sub>SINK</sub> =<br>1mA (Note 27)                       | To 10%                                                            | 15  |     |     | ns    |   |
|                                                  |                  |                                                                                  | To 1.5%                                                           | 50  |     |     |       |   |
|                                                  |                  | I <sub>SOURCE</sub> = I <sub>SINK</sub> =<br>20mA (Note 27)                      | To 10%                                                            | 3   |     |     |       | 5 |
|                                                  |                  |                                                                                  | To 1.5%                                                           | 15  |     |     |       |   |
| Spike During Enable/Disable<br>Transition        |                  | I <sub>SOURCE</sub> = I <sub>SINK</sub> = 35mA, V <sub>COM<sub>L</sub></sub> = 0 |                                                                   |     | 200 | 300 | mV    |   |

**Note 1:** All minimum and maximum DC and driver 3V rise- and fall-time test limits are 100% production tested. All other test limits are guaranteed by design. Tests are performed at nominal supply voltages, unless otherwise noted.

**Note 2:** Total for dual device at worst-case setting.

**Note 3:** Does not include above ground internal dissipation of the comparator outputs. Additional power dissipation is typically  $(32mA \times V_{VCCO\_})$

**Note 4:** Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

**Note 5:** Transition time from LLEAK being asserted to leakage current dropping below specified limits.

**Note 6:** Based on simulation results only.

**Note 7:** Transition time from LLEAK being deasserted to output returning to normal operating mode.

**Note 8:** With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

**Note 9:** Specifications measured at the endpoints of the full range. Full range is  $-1.3V \leq V_{DHF\_} \leq +6.5V$ ,  $-1.5V \leq V_{DLV\_} \leq +6.3V$ ,  $-1.5V \leq V_{DTV\_} \leq +6.5V$ .

**Note 10:** Relative to straight line between 0 and 4.5V.

**Note 11:** Change in offset voltage with power supplies independently set to their minimum and maximum values.

**Note 12:** Nominal target value is  $50\Omega$ . Contact factory for alternate trim selections within the  $45\Omega$  to  $51\Omega$  range.

**Note 13:**  $V_{DTV\_}$  = midpoint of voltage swing,  $R_S = 50\Omega$ . Measurement is made using the comparator.

**Note 14:** Measured from the crossing point of  $DATA\_$  inputs to the settling of the driver output.

**Note 15:** Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs  $DATA\_$  and  $RCV\_$  are 250ps (10% to 90%).

**Note 16:** Rising edge to rising edge or falling edge to falling edge.

**Note 17:** Specified amplitude is programmed. At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at  $DATA\_$ .

**Note 18:** Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 90% of its programmed amplitude may be generated at one-half of this frequency.

**Note 19:** Crosstalk from either driver to the other. Aggressor channel is driving  $3V_{P\_}$  into a  $50\Omega$  load. Victim channel is in term mode with  $V_{DTV\_} = +1.5V$ .

**Note 20:** Indicative of switching speed from  $DHF\_$  or  $DLV\_$  to  $DTV\_$  and  $DTV\_$  to  $DHF\_$  or  $DLV\_$  when  $V_{DLV\_} < V_{DTV\_} < V_{DHF\_}$ . If  $V_{DTV\_} < V_{DLV\_}$  or  $V_{DTV\_} > V_{DHF\_}$ , switching speed is degraded by a factor of approximately 3.

**Note 21:** Change in offset voltage over the input range.

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +9.75V$ ,  $V_{EE} = -4.75V$ ,  $V_{CCO\_} = +2.5V$ ,  $SC1 = SC0 = 0$ ,  $V_{CPHV\_} = +7.2V$ ,  $V_{CPLV\_} = -2.2V$ ,  $V_{LDH\_} = V_{LDL\_} = 0$ ,  $V_{GS} = 0$ ,  $T_J = +85^{\circ}C$ , unless otherwise noted. All temperature coefficients are measured at  $T_J = +60^{\circ}C$  to  $+100^{\circ}C$ , unless otherwise noted.) (Note 1)

**Note 22:** Unless otherwise noted, all propagation delays are measured at 40MHz,  $V_{DUT\_} = 0$  to  $+1V$ ,  $V_{CHV\_} = V_{CLV\_} = +0.5V$ ,  $t_R = t_F = 250ps$ ,  $Z_S = 50\Omega$ , driver in term mode with  $V_{DTV\_} = +0.5V$ . Comparator outputs are terminated with  $50\Omega$  to 1.25V and  $V_{CCO\_} = 2.5V$ . Measured from  $V_{DUT\_}$  crossing calibrated  $CHV\_/CLV\_$  threshold to crossing point of differential outputs.

**Note 23:** At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

**Note 24:**  $V_{DUT\_} = 200mV_{p-p}$ . Overdrive = 100mV.

**Note 25:** Relative to segmented interpolations between 200mV, 2V, 2.5V, and 3.5V.

**Note 26:** Measured from crossing of  $LDEN\_$  inputs to the 50% point of the output current change.

**Note 27:**  $V_{COM} = 1V$ ,  $R_S = 50\Omega$ , driving voltage = 1.55V to 0.45V transition and 0.45V to 1.55V transition (at 1mA) or +2.5V to -0.5V transition and -0.5V to +2.5V transition (at 20mA). Settling time is measured from  $V_{DUT\_} = 1V$  to  $I_{SINK}/I_{SOURCE}$  settling within specified tolerance.

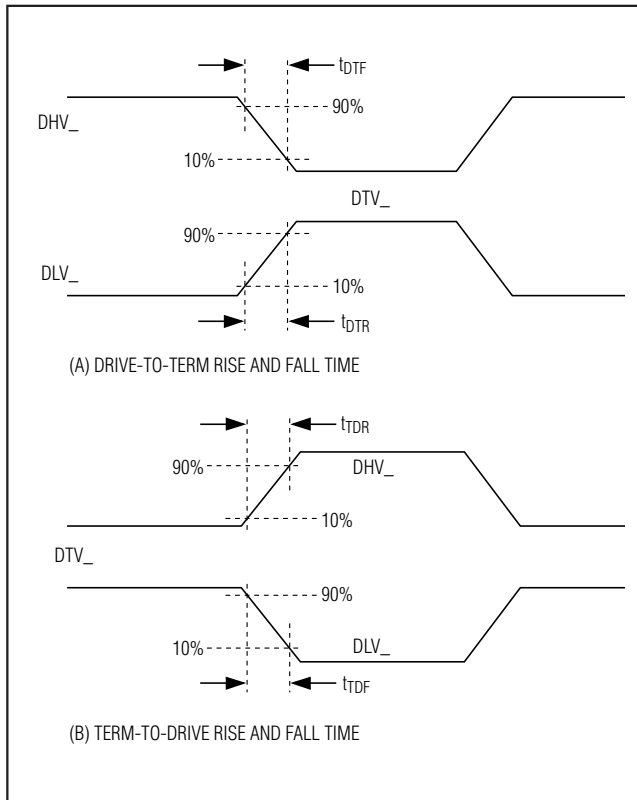


Figure 1. Drive-to-Term and Term-to-Drive Rise and Fall Times

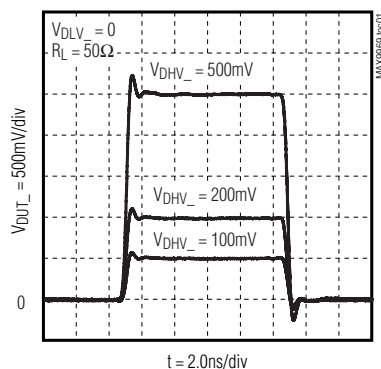
# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Typical Operating Characteristics

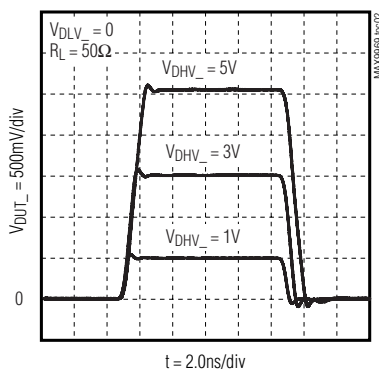
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

MAX9969

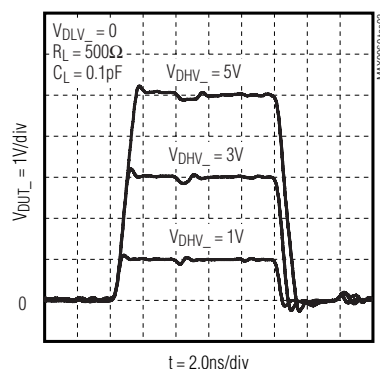
**DRIVER SMALL-SIGNAL RESPONSE**



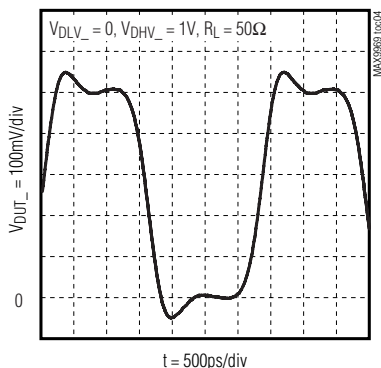
**DRIVER LARGE-SIGNAL RESPONSE**



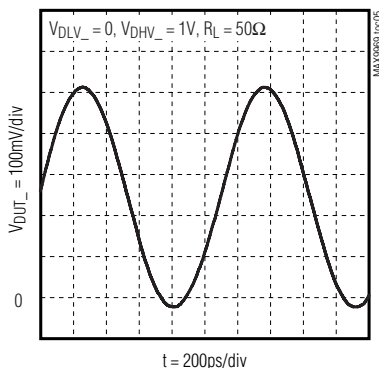
**DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω**



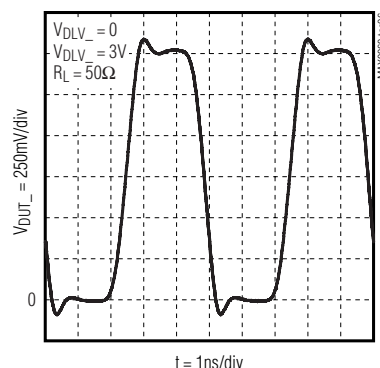
**DRIVER 1V 600Mbps SIGNAL RESPONSE**



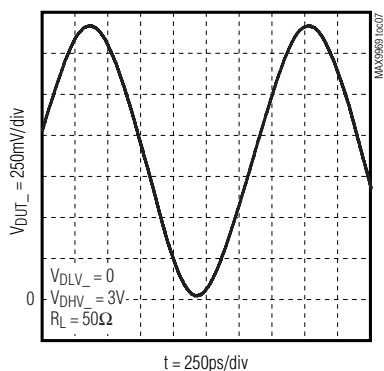
**DRIVER 1V 1800Mbps SIGNAL RESPONSE**



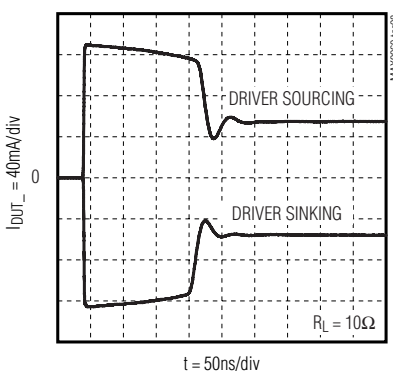
**DRIVER 3V 400Mbps SIGNAL RESPONSE**



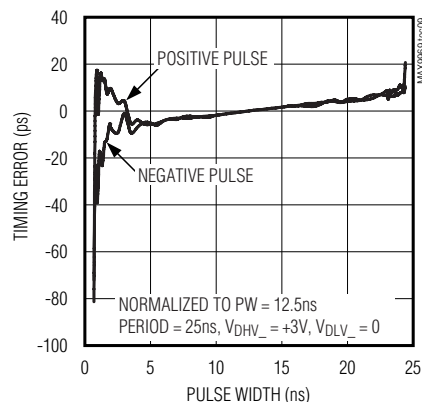
**DRIVER 3V 1200Mbps SIGNAL RESPONSE**



**DRIVER DYNAMIC CURRENT-LIMIT RESPONSE**



**DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH**

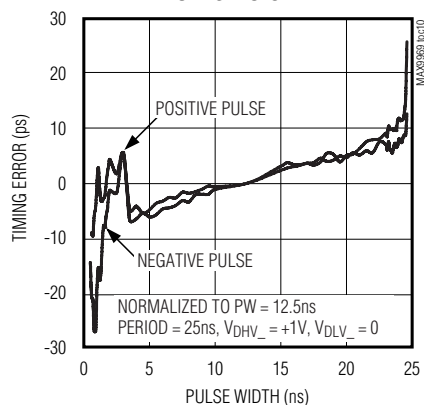


# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

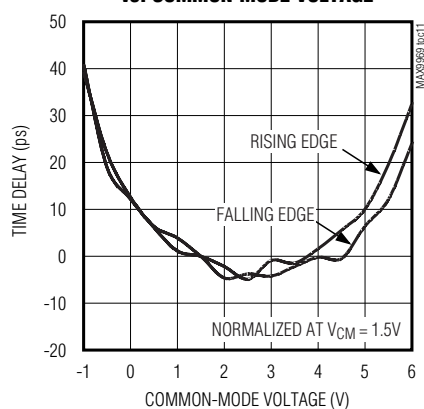
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

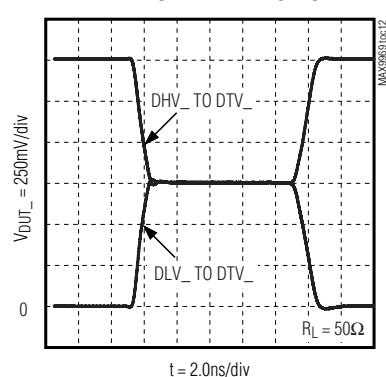
**DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH**



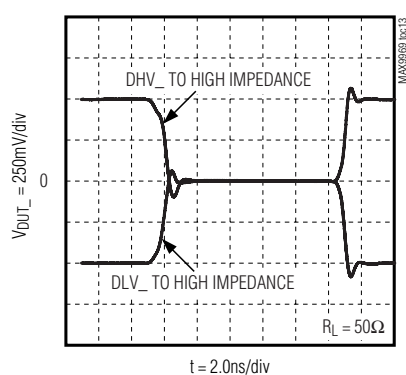
**DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE**



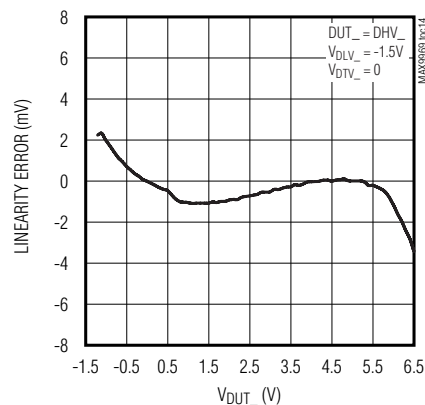
**DRIVE-TO-TERM TRANSITION**



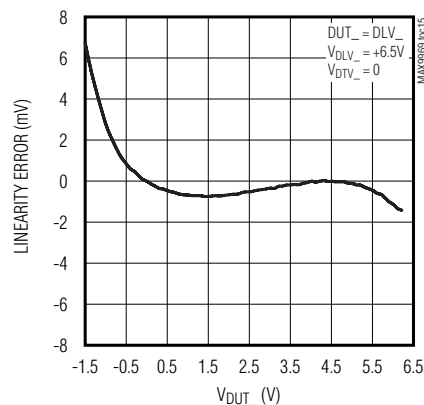
**DRIVE TO HIGH-IMPEDANCE TRANSITION**



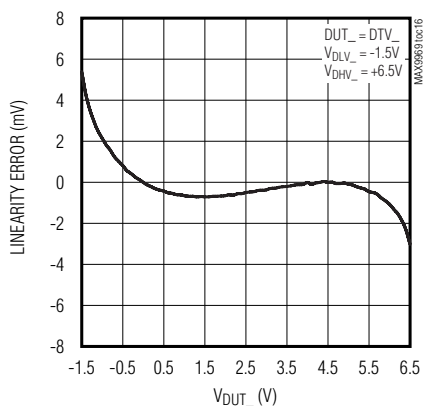
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



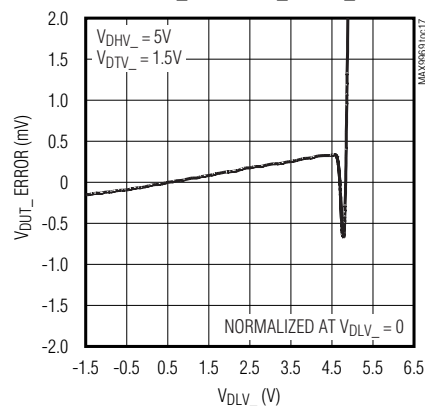
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



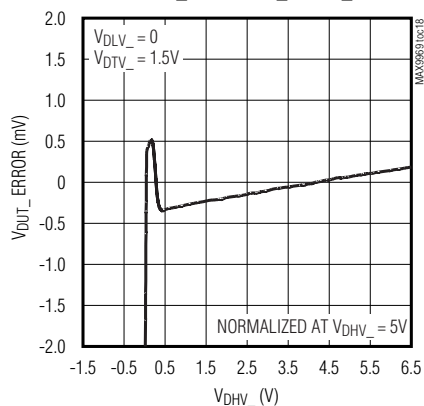
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



**CROSSTALK TO DUT\_ FROM DLV\_ WITH DUT\_ = DHV\_**



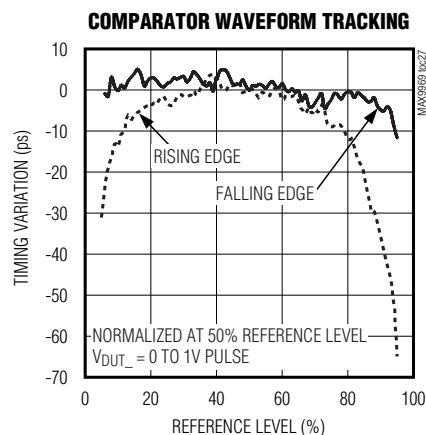
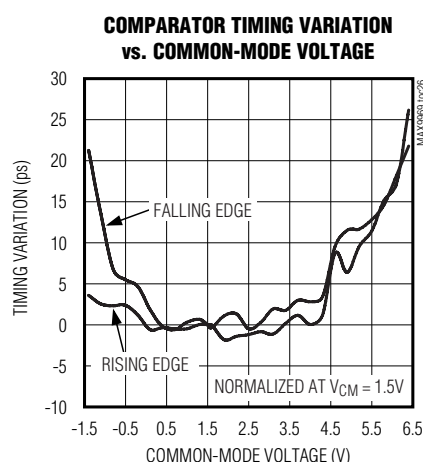
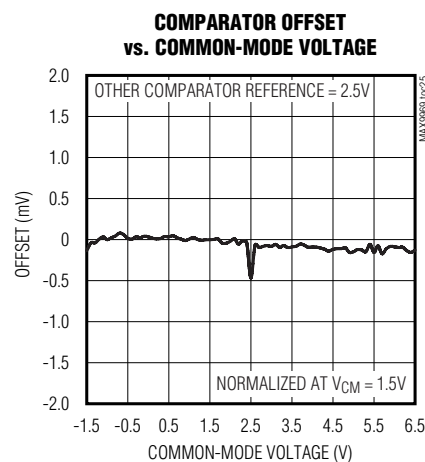
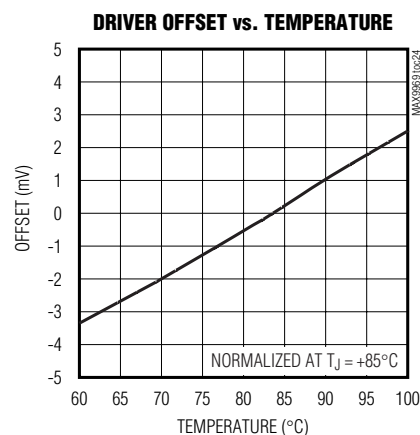
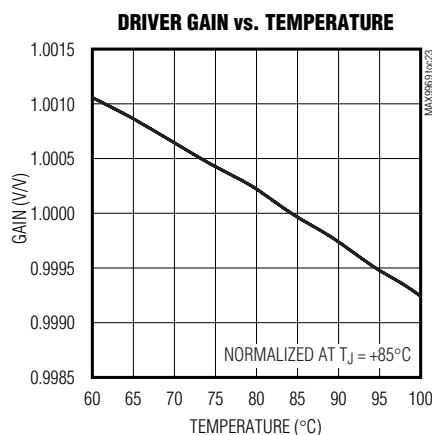
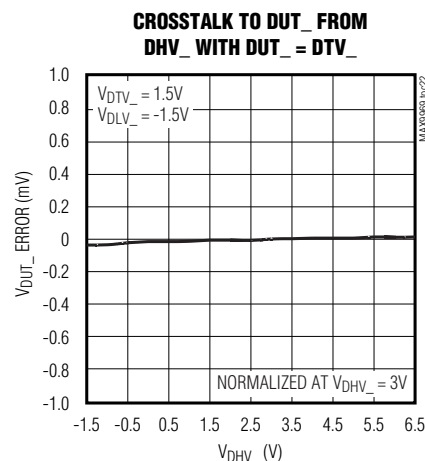
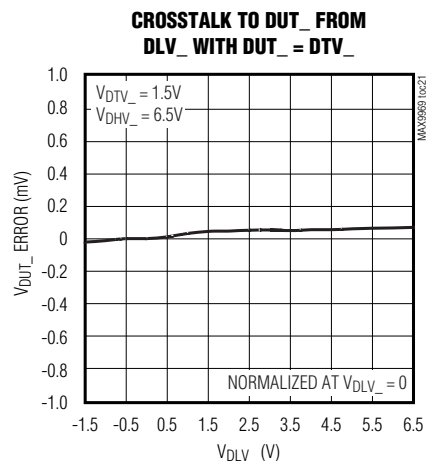
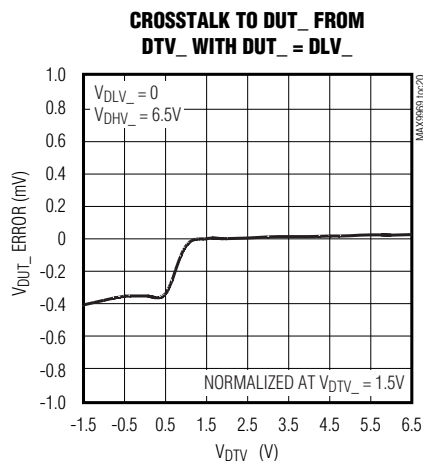
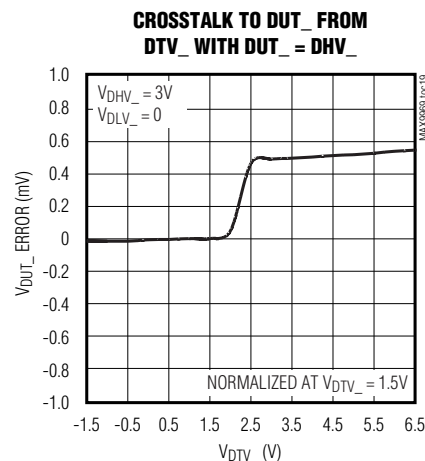
**CROSSTALK TO DUT\_ FROM DHV\_ WITH DUT\_ = DLV\_**



# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

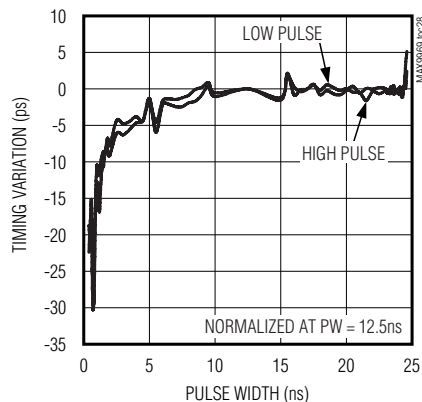


# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

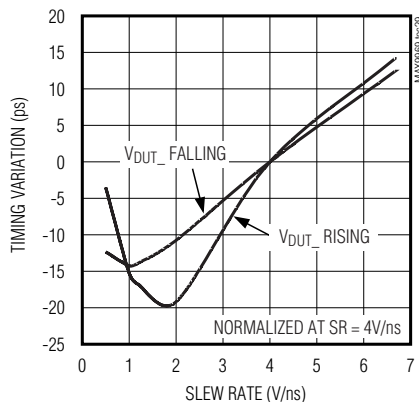
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

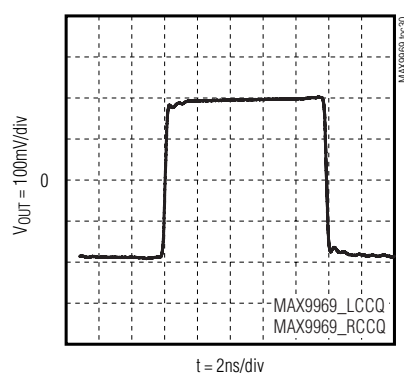
**COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH**



**COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE**

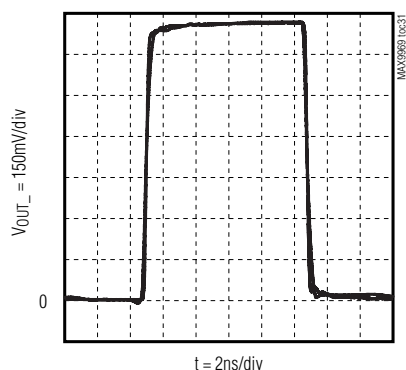


**COMPARATOR DIFFERENTIAL OUTPUT RESPONSE**



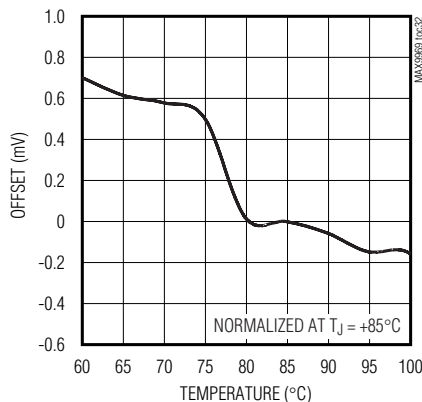
$V_{DUT\_} = 0 \text{ TO } 3\text{V PULSE}$   
 $V_{CHV\_} = V_{CLV\_} = 1.5\text{V}$   
 EXTERNAL LOAD =  $50\Omega$

**COMPARATOR RESPONSE TO HIGH SLEW RATE OVERDRIVE**

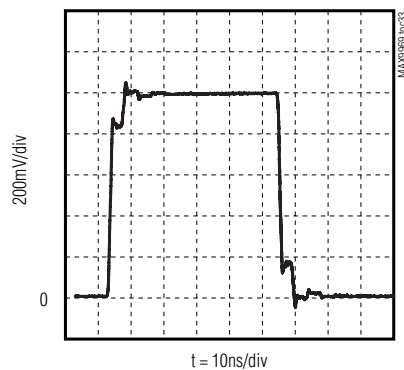


INPUT SLEW RATE = 4V/ns  
HIGH IMPEDANCE

**COMPARATOR OFFSET vs. TEMPERATURE**

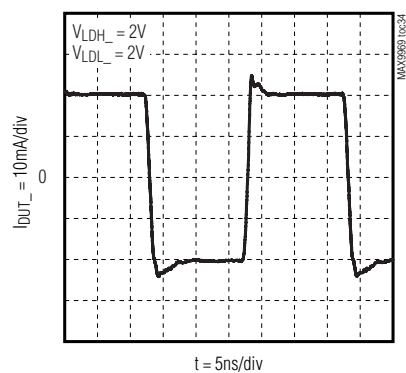


**CLAMP RESPONSE AT SOURCE**



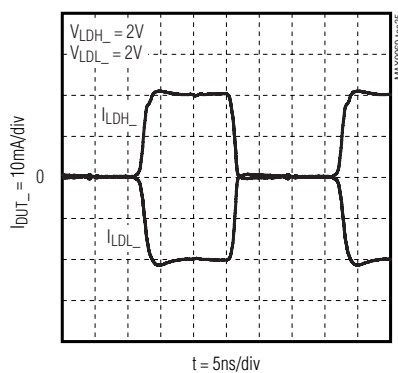
$V_{DUT\_} = 0 \text{ TO } 1\text{V SQUARE WAVE}$   
 $R_S = 10\Omega$   
 $V_{CPLV\_} = -0.1\text{V}$ ,  $V_{CPHV\_} = +1.1\text{V}$

**ACTIVE-LOAD COMMUTATION SIGNAL RESPONSE**



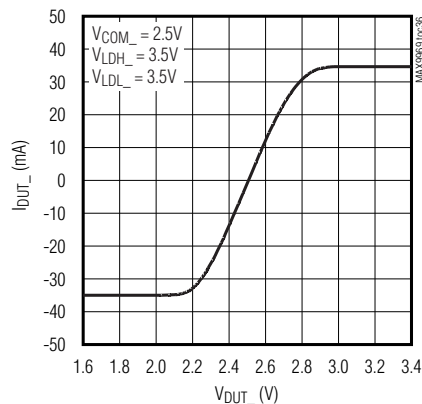
$V_{LDH\_} = 2\text{V}$   
 $V_{LDL\_} = 2\text{V}$

**ACTIVE-LOAD ENABLE SIGNAL RESPONSE**



$V_{LDH\_} = 2\text{V}$   
 $V_{LDL\_} = 2\text{V}$

**ACTIVE-LOAD CURRENT vs. LOAD VOLTAGE**

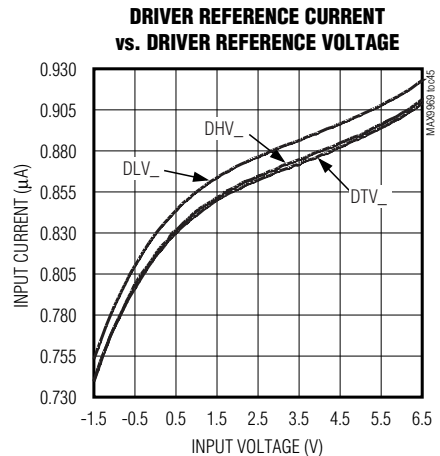
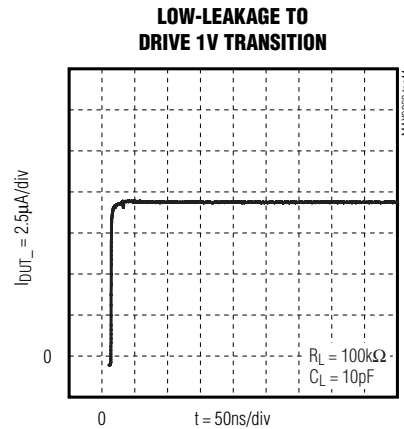
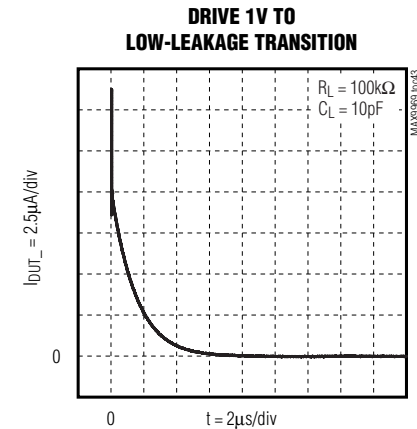
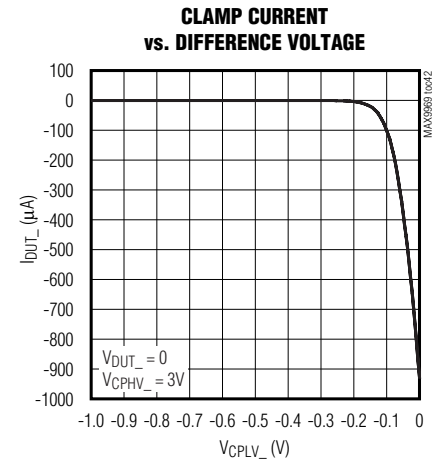
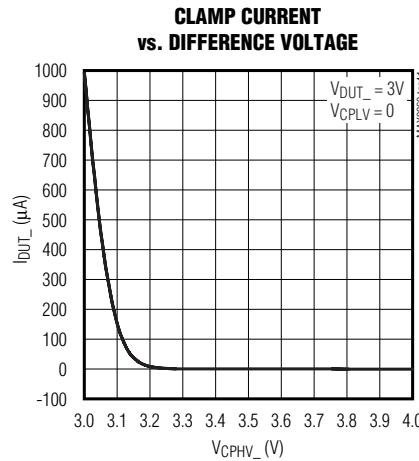
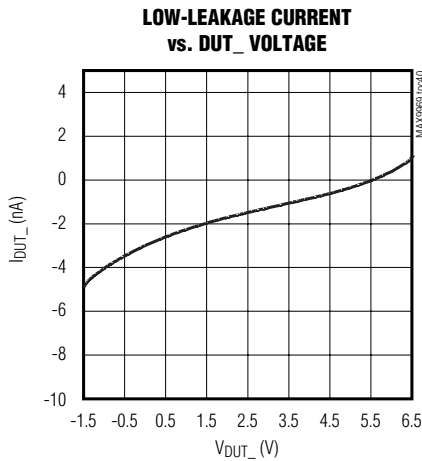
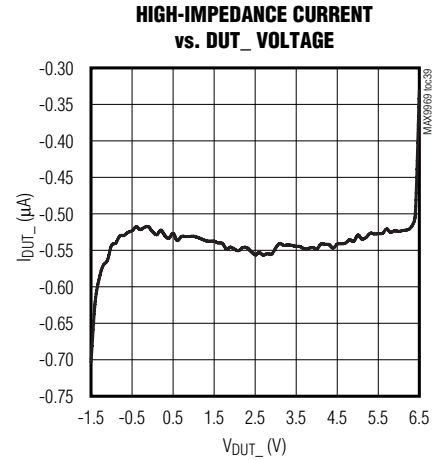
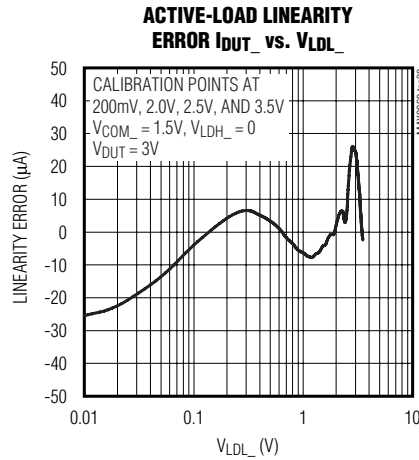
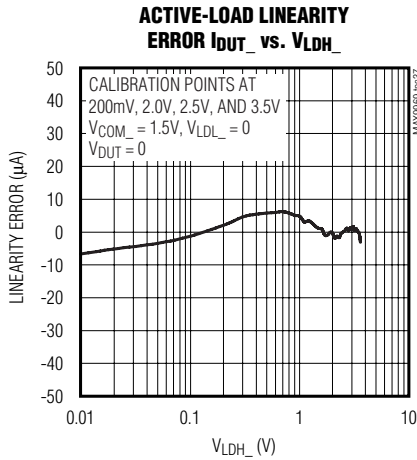


$V_{COM\_} = 2.5\text{V}$   
 $V_{LDH\_} = 3.5\text{V}$   
 $V_{LDL\_} = 3.5\text{V}$

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Typical Operating Characteristics (continued)

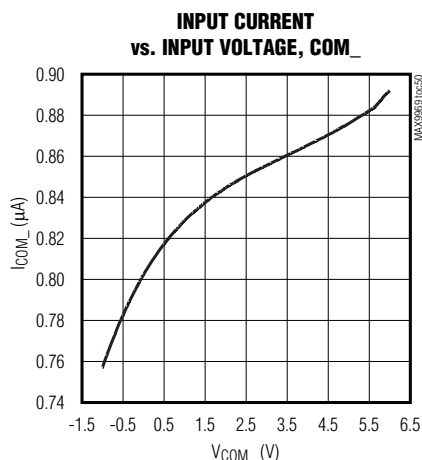
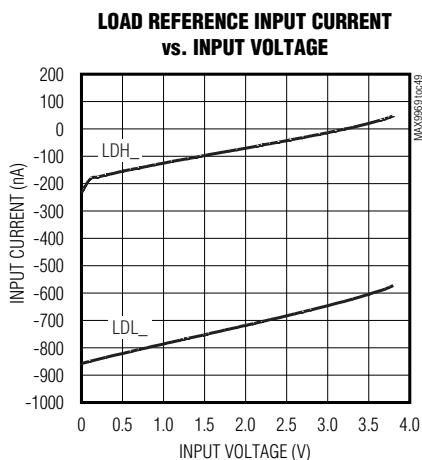
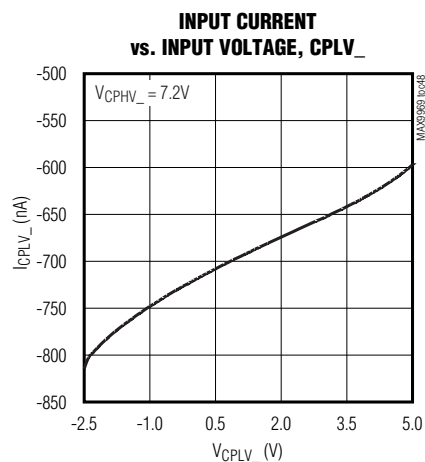
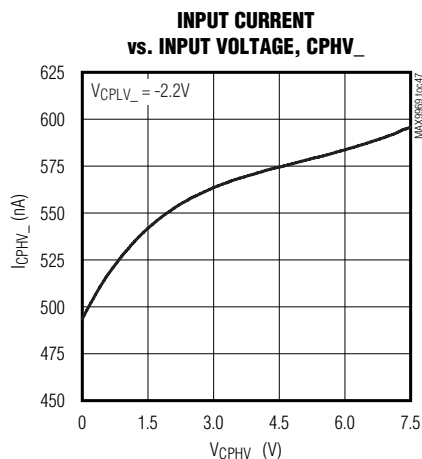
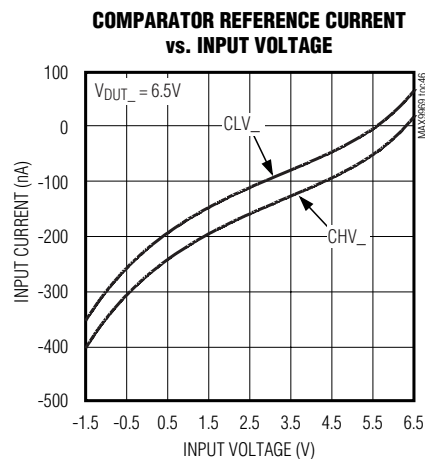
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

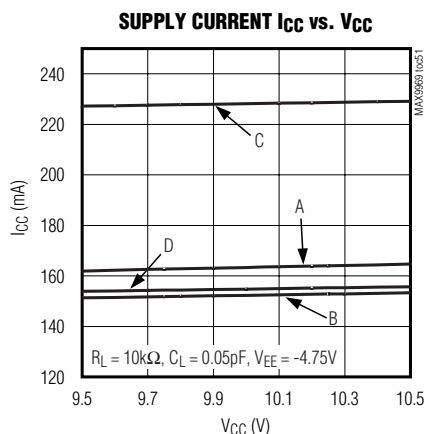


# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

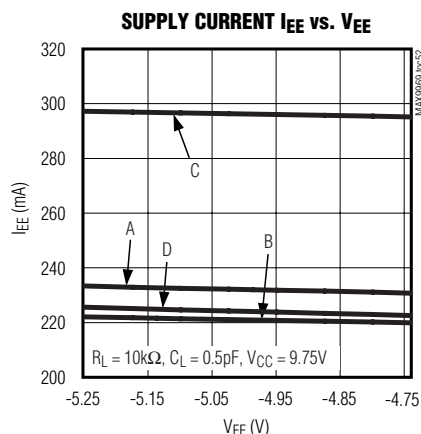
## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

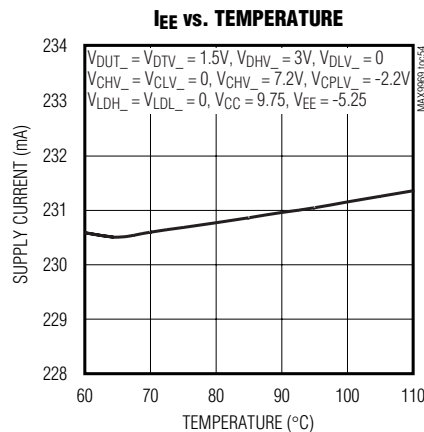
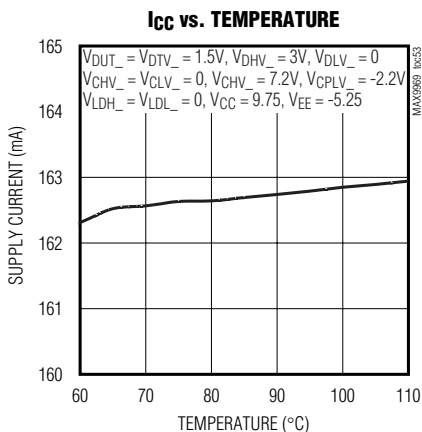
MAX9969



A:  $V_{OUT\_} = V_{DTV\_} = 1.5V$ ,  $V_{DHV\_} = 3V$ ,  $V_{DLV\_} = 0$   
 $V_{CHV\_} = V_{CLV\_} = 0$ ,  $V_{CPHV\_} = 7.2V$ ,  $V_{CPLV\_} = -2.2V$   
 $V_{LDH\_} = V_{LDL\_} = 0$ ,  $I_{SOURCE} = I_{SINK} = 0$   
 B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED  
 C: SAME AS B EXCEPT  $I_{SOURCE} = I_{SINK} = 35mA$ ,  $V_{COM\_} = 1.5V$ ,  $R_L = 0$   
 D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED



A:  $V_{OUT\_} = V_{DTV\_} = 1.5V$ ,  $V_{DHV\_} = 3V$ ,  $V_{DLV\_} = 0$   
 $V_{CHV\_} = V_{CLV\_} = 0$ ,  $V_{CPHV\_} = 7.2V$ ,  $V_{CPLV\_} = -2.2V$   
 $V_{LDH\_} = V_{LDL\_} = 0$ ,  $I_{SOURCE} = I_{SINK} = 0$   
 B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED  
 C: SAME AS B EXCEPT  $I_{SOURCE} = I_{SINK} = 35mA$ ,  $V_{COM\_} = -1V$ ,  $R_L = 0$   
 D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED



# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Pin Description

| PIN                                              | NAME  | FUNCTION                                                                                                                                                                                                                                                        |
|--------------------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                                | TEMP  | Temperature Monitor Output                                                                                                                                                                                                                                      |
| 2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91 | VEE   | Negative Power-Supply Input                                                                                                                                                                                                                                     |
| 3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92 | GND   | Ground Connection                                                                                                                                                                                                                                               |
| 4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93        | VCC   | Positive Power-Supply Input                                                                                                                                                                                                                                     |
| 6, 8, 18, 20, 50, 76                             | N.C.  | No Connection. Do not connect.                                                                                                                                                                                                                                  |
| 7                                                | DUT1  | Channel 1 DUT Input/Output. Combined I/O for driver, comparator, clamp, and load.                                                                                                                                                                               |
| 13                                               | GS    | Ground Sense. GS is the ground reference for LDH_ and LDL_.                                                                                                                                                                                                     |
| 19                                               | DUT2  | Channel 2 DUT Input/Output. Combined I/O for driver, comparator, clamp, and load.                                                                                                                                                                               |
| 26                                               | CLV2  | Channel 2 Low-Comparator Reference Input                                                                                                                                                                                                                        |
| 27                                               | CHV2  | Channel 2 High-Comparator Reference Input                                                                                                                                                                                                                       |
| 28                                               | DLV2  | Channel 2 Driver-Low Reference Input                                                                                                                                                                                                                            |
| 29                                               | DTV2  | Channel 2 Driver-Termination Reference Input                                                                                                                                                                                                                    |
| 30                                               | DHV2  | Channel 2 Driver-High Reference Input                                                                                                                                                                                                                           |
| 31                                               | CPLV2 | Channel 2 Low-Clamp Reference Input                                                                                                                                                                                                                             |
| 32                                               | CPHV2 | Channel 2 High-Clamp Reference Input                                                                                                                                                                                                                            |
| 36                                               | NCH2  | Channel 2 High-Comparator Output. Differential output of channel 2 high comparator.                                                                                                                                                                             |
| 37                                               | CH2   |                                                                                                                                                                                                                                                                 |
| 38                                               | VCCO2 | Channel 2 Collector Voltage Input. Voltage input for channel 2 comparator output termination resistors. Provides pullup voltage and current for the output termination resistors. Not internally connected for versions without internal termination resistors. |
| 39                                               | NCL2  | Channel 2 Comparator Low Output. Differential output of channel 2 low comparator.                                                                                                                                                                               |
| 40                                               | CL2   |                                                                                                                                                                                                                                                                 |
| 47                                               | COM2  | Channel 2 Active-Load Commutation-Voltage Reference Input                                                                                                                                                                                                       |

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Pin Description (continued)

| PIN | NAME             | FUNCTION                                                                                                                                                                                                                                  |
|-----|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 48  | LDL2             | Channel 2 Active-Load Source-Current Reference Input                                                                                                                                                                                      |
| 49  | LDH2             | Channel 2 Active-Load Sink-Current Reference Input                                                                                                                                                                                        |
| 51  | TDATA2           | Channel 2 Data-Termination Voltage Input. Termination voltage input for the DATA2 and NDATA2 differential inputs. Not internally connected on versions without internal termination resistors.                                            |
| 52  | NDATA2           | Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2.                                 |
| 53  | DATA2            |                                                                                                                                                                                                                                           |
| 54  | TRCV2            | Channel 2 RCV Termination Voltage Input. Termination voltage input for the RCV2 and NRCV2 differential inputs. Not internally connected on versions without internal termination resistors.                                               |
| 55  | NRCV2            | Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 in receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode.       |
| 56  | RCV2             |                                                                                                                                                                                                                                           |
| 57  | TLDEN2           | Channel 2 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN2 and NLDEN2 differential inputs. Not internally connected on versions without internal termination resistors.                                     |
| 58  | NLDEN2           | Channel 2 Multiplexer Control Inputs. Differential controls LDEN2 and NLDEN2 enable/disable the active load. Drive LDEN2 above NLDEN2 to enable the channel 2 active load. Drive NLDEN2 above LDEN2 to disable the channel 2 active load. |
| 59  | LDEN2            |                                                                                                                                                                                                                                           |
| 61  | $\overline{RST}$ | Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low.                                                                                                                                            |
| 62  | $\overline{CS}$  | Chip-Select Input. Serial port activation input. $\overline{CS}$ is active low.                                                                                                                                                           |
| 63  | THR              | Single-Ended Logic Threshold. Leave THR unconnected to set the threshold to +1.25V or force THR to a desired threshold voltage.                                                                                                           |
| 64  | SCLK             | Serial Clock Input. Clock for serial port.                                                                                                                                                                                                |
| 65  | DIN              | Data Input. Serial port data input.                                                                                                                                                                                                       |
| 67  | LDEN1            | Channel 1 Multiplexer Control Inputs. Differential controls LDEN1 and NLDEN1 enable/disable the active load. Drive LDEN1 above NLDEN1 to enable the channel 1 active load. Drive NLDEN1 above LDEN1 to disable the channel 1 active load. |
| 68  | NLDEN1           |                                                                                                                                                                                                                                           |
| 69  | TLDEN1           | Channel 1 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN1 and NLDEN1 differential inputs. Not internally connected on versions without internal termination resistors.                                     |

MAX9969

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Pin Description (continued)

| PIN | NAME   | FUNCTION                                                                                                                                                                                                                                                        |
|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 70  | RCV1   | Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 in receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.                             |
| 71  | NRCV1  |                                                                                                                                                                                                                                                                 |
| 72  | TRCV1  | Channel 1 RCV Termination Voltage Input. Termination voltage input for the RCV1 and NRCV1 differential inputs. Not internally connected on versions without internal termination resistors.                                                                     |
| 73  | DATA1  | Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.                                                       |
| 74  | NDATA1 |                                                                                                                                                                                                                                                                 |
| 75  | TDATA1 | Channel 1 Data-Termination Voltage Input. Termination voltage input for the DATA1 and NDATA1 differential inputs. Not internally connected on versions without internal termination resistors.                                                                  |
| 77  | LDH1   | Channel 1 Active-Load Sink-Current Reference Input                                                                                                                                                                                                              |
| 78  | LDL1   | Channel 1 Active-Load Source-Current Reference Input                                                                                                                                                                                                            |
| 79  | COM1   | Channel 1 Active-Load Commutation-Voltage Reference Input                                                                                                                                                                                                       |
| 86  | CL1    | Channel 1 Low-Comparator Output. Differential output of channel 1 low comparator.                                                                                                                                                                               |
| 87  | NCL1   |                                                                                                                                                                                                                                                                 |
| 88  | VCCO1  | Channel 1 Collector Voltage Input. Voltage input for channel 1 comparator output-termination resistors. Provides pullup voltage and current for the output-termination resistors. Not internally connected for versions without internal termination resistors. |
| 89  | CH1    | Channel 1 High-Comparator Output. Differential output of channel 1 high comparator.                                                                                                                                                                             |
| 90  | NCH1   |                                                                                                                                                                                                                                                                 |
| 94  | CPHV1  | Channel 1 High-Clamp Reference Input                                                                                                                                                                                                                            |
| 95  | CPLV1  | Channel 1 Low-Clamp Reference Input                                                                                                                                                                                                                             |
| 96  | DHV1   | Channel 1 Driver-High Reference Input                                                                                                                                                                                                                           |
| 97  | DTV1   | Channel 1 Driver-Termination Reference Input                                                                                                                                                                                                                    |
| 98  | DLV1   | Channel 1 Driver-Low Reference Input                                                                                                                                                                                                                            |
| 99  | CHV1   | Channel 1 High-Comparator Reference Input                                                                                                                                                                                                                       |
| 100 | CLV1   | Channel 1 Low-Comparator Reference Input                                                                                                                                                                                                                        |

# MAX9969

# MAX9969



# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Detailed Description

The MAX9969 dual, low-power, high-speed, pin electronics DCL IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. An additional differential comparator allows comparisons between the two channels. The driver features a -1.5V to +6.5V operating range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low-voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, and differential outputs. The clamps provide damping of high-speed DUT waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric test of IOH and IOL, and pullup of high-output-impedance devices. The MAX9969A features tighter matching of offset for the drivers and the comparators.

Optional internal resistors at the high-speed inputs provide compatibility with LVPECL, LVDS, and GTL interfaces. Connect the termination voltage inputs (TDATA\_, TRCV\_, TLDEN\_) to the appropriate voltage for terminating LV\_PECL, GTL, or other logic. Leave the inputs

unconnected for 100Ω differential LVDS termination. In addition, flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage CMOS-compatible serial interface programs the low-leakage, load-disable, slew-rate, differential/window comparator and tri-state/terminate operational configurations of the MAX9969.

## Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV\_, DLV\_, or DTV\_. This switching is controlled by high-speed inputs DATA\_ and RCV\_ and mode-control bit TMSEL (Table 1). A slew-rate circuit controls the slew rate of the buffer input. Select to one of four possible slew rates according to Table 2. The speed of the internal multiplexer sets the 100% driver slew rate (see the Driver Large-Signal Response graph in the *Typical Operating Characteristics*).

DUT\_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). In high-impedance mode, the clamps are connected. High-speed input RCV\_ and mode-control bits TMSEL and

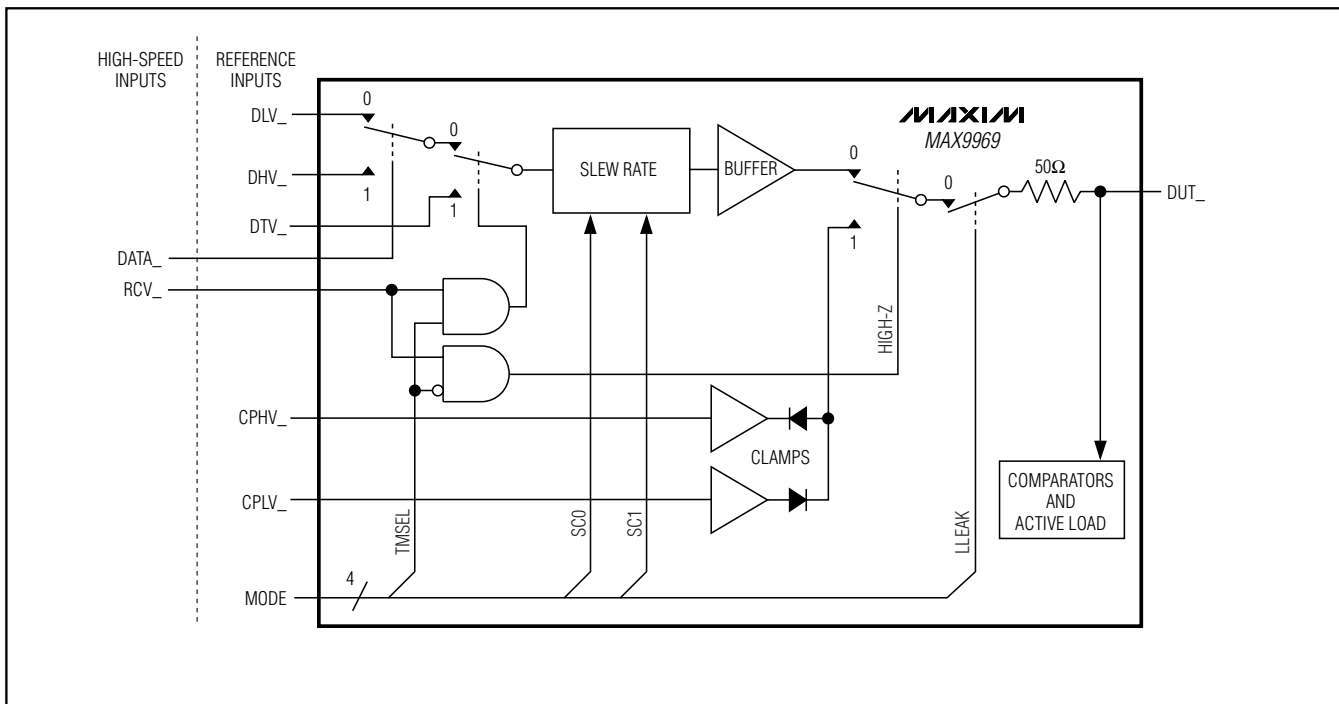


Figure 2. Simplified Driver Channel

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

MAX9969

**Table 1. Driver Logic**

| EXTERNAL CONNECTIONS |     | INTERNAL CONTROL REGISTER |       | DRIVER OUTPUT                |
|----------------------|-----|---------------------------|-------|------------------------------|
| DATA                 | RCV | TMSEL                     | LLEAK |                              |
| 1                    | 0   | X                         | 0     | Drive to DHV_                |
| 0                    | 0   | X                         | 0     | Drive to DLV_                |
| X                    | 1   | 1                         | 0     | Drive to DTV_ (term mode)    |
| X                    | 1   | 0                         | 0     | High-impedance mode (high-Z) |
| X                    | X   | X                         | 1     | Low-leakage mode             |

**Table 2. Slew-Rate Logic**

| SC1 | SC0 | DRIVER SLEW RATE (%) |
|-----|-----|----------------------|
| 0   | 0   | 100                  |
| 0   | 1   | 75                   |
| 1   | 0   | 50                   |
| 1   | 1   | 25                   |

LLEAK control the switching. In high-impedance mode, the bias current at DUT\_ is less than 3μA over the 0 to 3V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT\_ is further reduced to less than 15nA, and signal tracking slows. See the *Low-Leakage Mode, LLEAK* section for more details.

The nominal driver output resistance is 50Ω. Contact the factory for different resistance values within the 45Ω to 51Ω range.

## Clamps

Configure the voltage clamps (high and low) to limit the voltage at DUT\_ and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the external connections CPHV\_ and CPLV\_. The clamps are enabled only when the driver is in high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT\_ voltage range. The optimal clamp voltages are application specific and must be empirically determined. If clamping is

**Table 3a. Comparator Logic, CDIFF = 0**

| DUT_ > CHV_ | DUT_ > CLV_ | CL_, NCL_ | CH_, NCH_ |
|-------------|-------------|-----------|-----------|
| 0           | 0           | 0         | 0         |
| 0           | 1           | 1         | 0         |
| 1           | 0           | 0         | 1         |
| 1           | 1           | 1         | 1         |

**Table 3b. Comparator Logic, CDIFF = 1**

| DUT1 > DUT2 | DUT_ > CLV_ | CL_, NCL_ | CH_, NCH_ |
|-------------|-------------|-----------|-----------|
| 0           | 0           | 0         | 0         |
| 0           | 1           | 1         | 0         |
| 1           | 0           | 0         | 1         |
| 1           | 1           | 1         | 1         |

not desired, set the clamp voltages at least 0.7V outside the expected DUT\_ voltage range; overvoltage protection remains active without loading DUT\_.

## Comparators

The MAX9969 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT\_ and the other input connected to either CHV\_ or CLV\_ (see the *Functional Diagram*). Comparator outputs are a logical result of the input conditions, as indicated in Tables 3a and 3b.

The comparator differential outputs are open-collector outputs to ease interfacing with a wide variety of logic families. Versions with and without internal termination resistors switch an 8mA current source between the two outputs (Figure 3). The optional termination resistors connect the outputs to voltage input VCCO\_. For versions without internal termination, leave VCCO\_ unconnected and add the required external resistors. These resistors are typically 50Ω to the pullup voltage at the receiving end of the output trace. Alternate configurations can be used provided that the *Absolute Maximum Ratings* are not exceeded. For versions with internal termination, connect VCCO\_ to the desired VOH voltage. Each output provides a nominal 400mVp-p swing and 50Ω source termination.

The upper comparators are configurable as differential receivers for LVDS and other differential DUT\_ signals. When mode bit CDIFF is asserted, the upper comparator inputs are routed from the DUT\_ outputs for both channels.

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

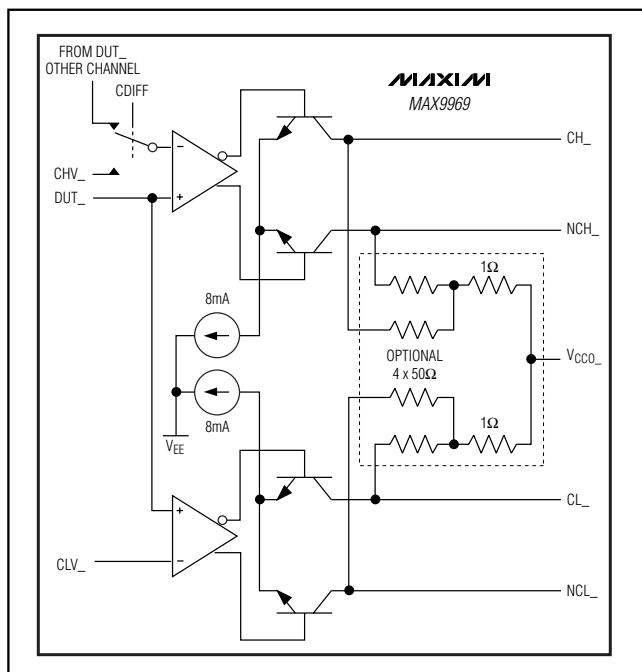


Figure 3. Open-Collector Comparator Outputs

## Active Load

The active load consists of linearly programmable, class AB source and sink current sources, a commutation buffer, and a diode bridge (see the *Functional Diagram*). Analog control inputs LDH\_ and LDL\_ program the sink and source currents, respectively, within the 0 to 35mA range. Analog reference input COM\_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the DUT. Current out of the MAX9969 constitutes sink current and current into the MAX9969 constitutes source current. The class AB loads of the MAX9969 offer substantial efficiency improvement over conventional active-load circuitry.

The programmed source (low) current loads the DUT when  $V_{DUT\_} > V_{COM\_}$ . The programmed sink (high) current loads the DUT when  $V_{DUT\_} < V_{COM\_}$ .

High-speed differential input LDEN\_ and 2 bits of the control word (LDDIS and LLEAK) control the load (Table 4). When the load is enabled, the internal source and sink current sources connect to the diode bridge. When the load is disabled, the internal current sources shunt to ground and the top and bottom of the bridge float (see the *Functional Diagram*). LLEAK places the load in low-leakage mode, and overrides LDEN\_. See the

Table 4. Active Load Programming

| EXTERNAL CONNECTIONS | INTERNAL CONTROL REGISTER |             | MODE                                 |
|----------------------|---------------------------|-------------|--------------------------------------|
|                      | LDEN_                     | LDDIS LLEAK |                                      |
| 0                    | 0                         | 0           | Normal operating mode, load disabled |
| 1                    | 0                         | 0           | Normal operating mode, load enabled  |
| X                    | 1                         | 0           | Load disabled                        |
| X                    | X                         | 1           | Low-leakage mode                     |

*Low-Leakage Mode*, LLEAK section for more detailed information.

## LDDIS

In some tester configurations, the load enable is driven with the complement of the driver high-impedance signal (RCV\_), so disabling the driver enables the load and vice versa. The LDDIS signal allows the load to be disabled independent of the state of LDEN\_ (Table 4).

## GS Input

The GS input allows a single level-setting DAC, such as the MAX5631 or MAX5734, to program the MAX9969's active load, driver, comparator, and clamps. Although all the DAC levels are typically offset by  $V_{GS}$ , the operation of the MAX9969's ground-sense input nullifies this offset with respect to the active-load current. Connect GS to the ground reference used by the DAC. ( $V_{LDL\_} - V_{GS}$ ) sets the source current by +10mA/V. ( $V_{LDH\_} - V_{GS}$ ) sets the sink current by -10mA/V.

To maintain an 8V range in the presence of GS variations, DHV\_, DLV\_, DTV\_, CPHV\_, CPLV\_, and COM\_ ranges are offset by GS. Adequate supply headroom must be maintained in the presence of GS variations. Ensure:

$$V_{CC} \geq 9.5V + \text{Max}(V_{GS})$$

$$V_{EE} \leq -4.5V + \text{Min}(V_{GS})$$

## Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with RST places the MAX9969 into a very low-leakage state (see the *Electrical Characteristics*). With LLEAK asserted, the comparators function at a reduced speed, and the driver, clamps, and active load are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel.

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

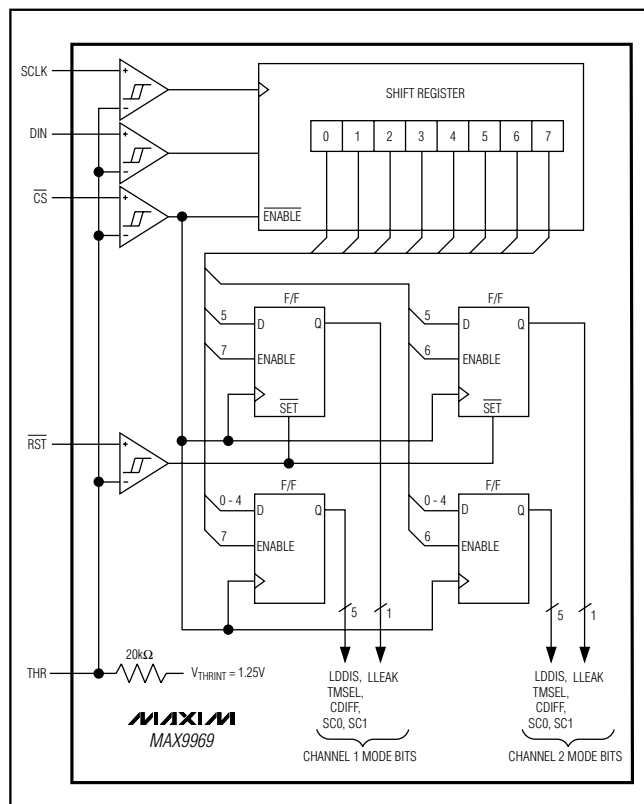


Figure 4. Serial Interface

When DUT<sub>+</sub> is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal opera-

tion. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

## Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9969 modes (Figure 4 and Table 5). Control data flow into an 8-bit shift register (MSB first) and are latched when  $\overline{CS}$  is taken high, as shown in Figure 5. Latches contain 6 control bits for each channel of the dual pin driver. Data from the shift register are loaded to either or both of the latches as determined by bits D6 and D7. When  $CDIFF = 1$ , its effect is independent of bits D6 and D7. The control bits, in conjunction with external inputs DATA<sub>+</sub> and RCV<sub>+</sub>, manage the features of each channel, as shown in Tables 1 and 2.  $\overline{RST}$  sets  $LLEAK = 1$  for both channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold  $\overline{RST}$  low until  $V_{CC}$  and  $V_{EE}$  have stabilized.

Analog control input THR sets the threshold for the input logic, allowing operation with CMOS logic as low as 0.9V. Leaving THR unconnected results in a nominal threshold of 1.25V from an internal reference, providing compatibility with 2.5V to 3.3V logic.

## MAX9967 Compatibility

The MAX9969 is pin compatible with the MAX9967 with minor changes.

- No PMU force/sense connection on the MAX9969
- Different common-mode ranges for control inputs
- MAX9967 comparator outputs additionally support open emitter
- Different serial interface bit structures

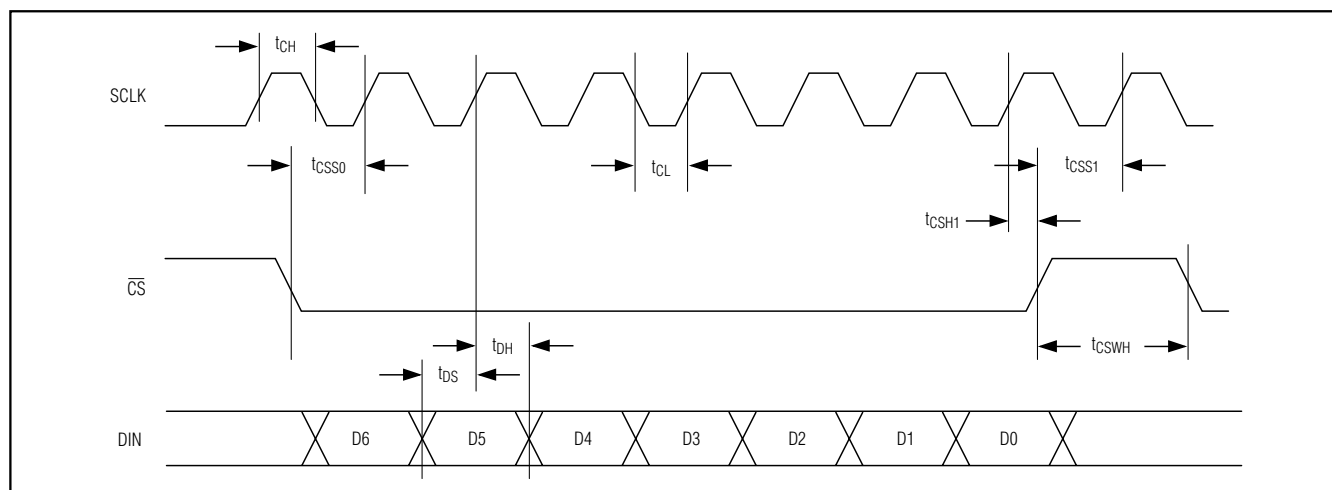


Figure 5. Serial-Interface Timing

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

**Table 5. Shift Register Functions**

| BIT | NAME  | DESCRIPTION                                                                                                                                                                                                                           |
|-----|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D7  | CH1   | Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.                                                                                                                  |
| D6  | CH2   | Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.                                                                                                                  |
| D5  | LLEAK | Low-Leakage Select. Set to 1 to put driver, load, and clamps in low-leakage mode. Comparators remain active in low-leakage mode, but at reduced speed. Set to 0 for normal operation.                                                 |
| D4  | TMSEL | Termination Select. Driver Termination Select Bit. Set to 1 to force the driver output to the DTV_ voltage when RCV_ = 1 (term mode). Set to 0 to place the driver into high-impedance mode when RCV_ = 1 (high-Z). See Table 1.      |
| D3  | SC1   | Driver Slew Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.                                                                                                                                                           |
| D2  | SC0   |                                                                                                                                                                                                                                       |
| D1  | CDIFF | Differential Comparator Enable. Set to 1 to enable the differential comparators and disable the CH_ window comparators. Set to 0 to enable the CH_ window comparators and disable the differential comparators. See Tables 3a and 3b. |
| D0  | LDDIS | Load Disable. Set LDDIS to 1 to disable the load. Set to 0 for normal operation. See Table 4.                                                                                                                                         |

## Temperature Monitor

The MAX9969 supplies a temperature output signal, TEMP, that asserts a 3.33V nominal output voltage at a +70°C (343K) die temperature. The output voltage changes proportionally with temperature at 10mV/°C.

## Heat Removal

Under normal circumstances, the MAX9969 requires heat removal through the exposed pad by use of an external heat sink. The exposed pad is electrically at VEE potential, and must be either connected to VEE or isolated.

Power dissipation is highly dependent upon the application. The *Electrical Characteristics* table indicates power dissipation under the condition that the source

and sink currents are programmed to 0mA. Maximum dissipation occurs when the source and sink currents are both at 35mA, the VDUT\_ is at an extreme of the voltage range (-1.5V or +6.5V), and the diode bridge is fully commutated. Under these conditions, the additional power dissipated (per channel) is:

If DUT\_ is sourcing current:

$$P_D = (V_{DUT\_} - V_{EE}) \times I_{SOURCE}$$

If DUT\_ is sinking current:

$$P_D = (V_{CC} - V_{DUT\_}) \times I_{SINK}$$

DUT\_ sources the programmed (low) current when  $V_{DUT\_} > V_{COM\_}$ . The path of the current is from DUT\_ through the outside of the diode bridge and the source (low) current source to VEE. The programmed sink current is greatly reduced by the class AB load architecture.

DUT\_ sinks the programmed (high) current when  $V_{DUT\_} < V_{COM\_}$ . The path of the current is from VCC through the sink (high) current source and the outside of the diode bridge to DUT\_. The programmed source current is greatly reduced by the class AB architecture.

$\theta_{JC}$  of the exposed-pad package is very low, approximately 1°C/W to 2°C/W. Die temperature is thus highly dependent upon the heat removal techniques used in the application. Maximum total power dissipation occurs under the following conditions:

- $V_{CC} = +10.5V$
- $V_{EE} = -5.25V$
- $I_{SOURCE} = I_{SINK} = 35mA$  for both channels
- Load enabled
- $V_{DUT\_} = -1.5V$
- $V_{COM\_} = +0.5V$

Under these extreme conditions, the total power dissipation is 3.9W typical and 4.4W maximum. If the die temperature cannot be maintained at an acceptable level under these conditions, use software clamping to limit the load output currents to lower values and/or reduce the supply voltages.

## Power-Supply Considerations

Bypass all VCC and VEE power input pins with 0.01μF capacitors, and use bulk bypassing of at least 10μF on each supply.

## Chip Information

TRANSISTOR COUNT: 5284

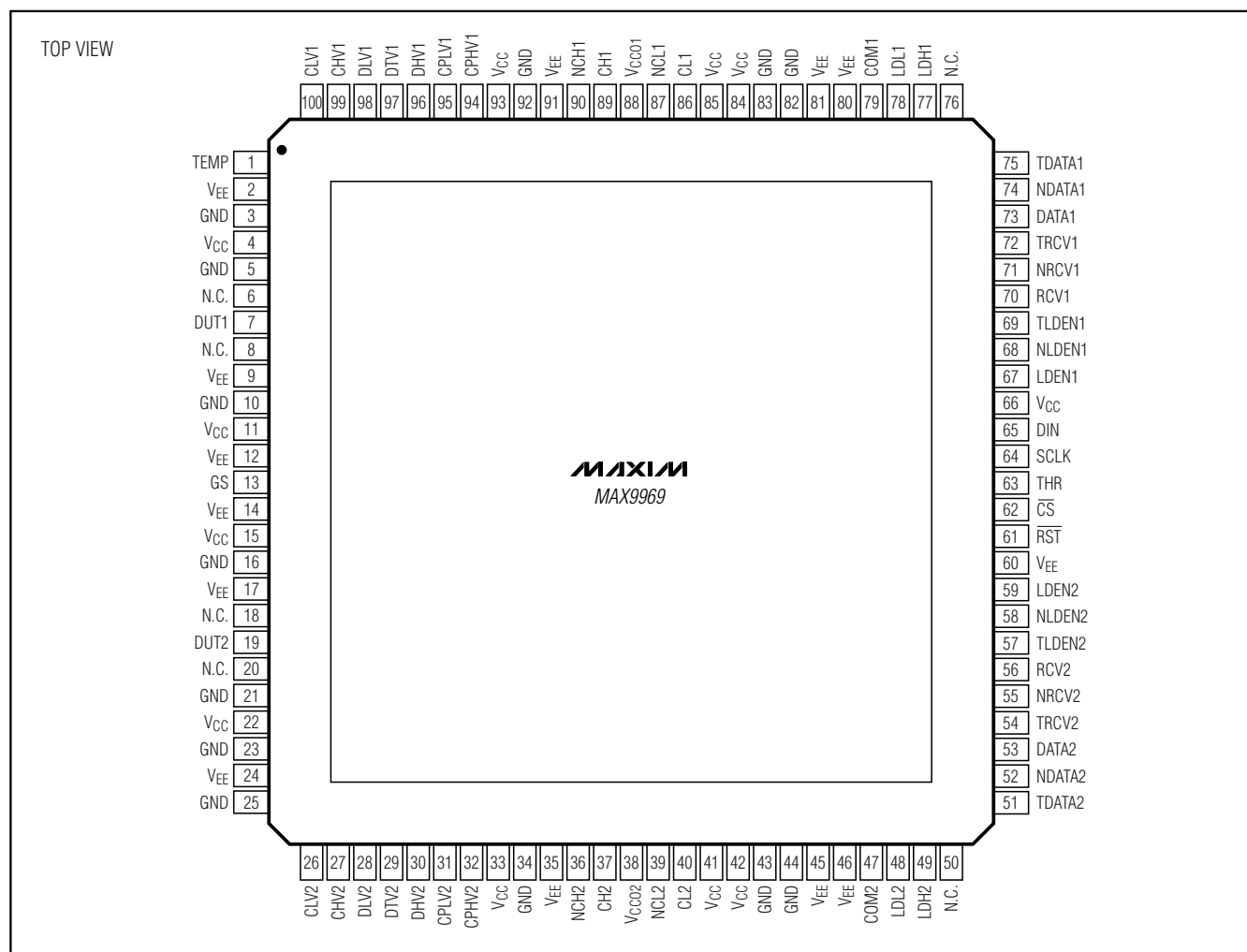
PROCESS: Bipolar

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Selector Guide

| PART         | ACCURACY GRADE | COMPARATOR OUTPUT TERMINATION | HIGH-SPEED DIGITAL INPUT TERMINATION ( $\Omega$ ) |       |       | HEAT EXTRACTION |
|--------------|----------------|-------------------------------|---------------------------------------------------|-------|-------|-----------------|
|              |                |                               | RCV_                                              | DATA_ | LDEN_ |                 |
| MAX9969ADCCQ | A              | None                          | None                                              | None  | None  | Top             |
| MAX9969AGCCQ | A              | None                          | 100                                               | 100   | 100   | Top             |
| MAX9969ALCCQ | A              | 50 $\Omega$ to VCCO_          | 100                                               | 100   | 100   | Top             |
| MAX9969ARCCQ | A              | 50 $\Omega$ to VCCO_          | None                                              | 100   | 100   | Top             |
| MAX9969BDCCQ | B              | None                          | None                                              | None  | None  | Top             |
| MAX9969BGCCQ | B              | None                          | 100                                               | 100   | 100   | Top             |
| MAX9969BLCCQ | B              | 50 $\Omega$ to VCCO_          | 100                                               | 100   | 100   | Top             |
| MAX9969BRCCQ | B              | 50 $\Omega$ to VCCO_          | None                                              | 100   | 100   | Top             |

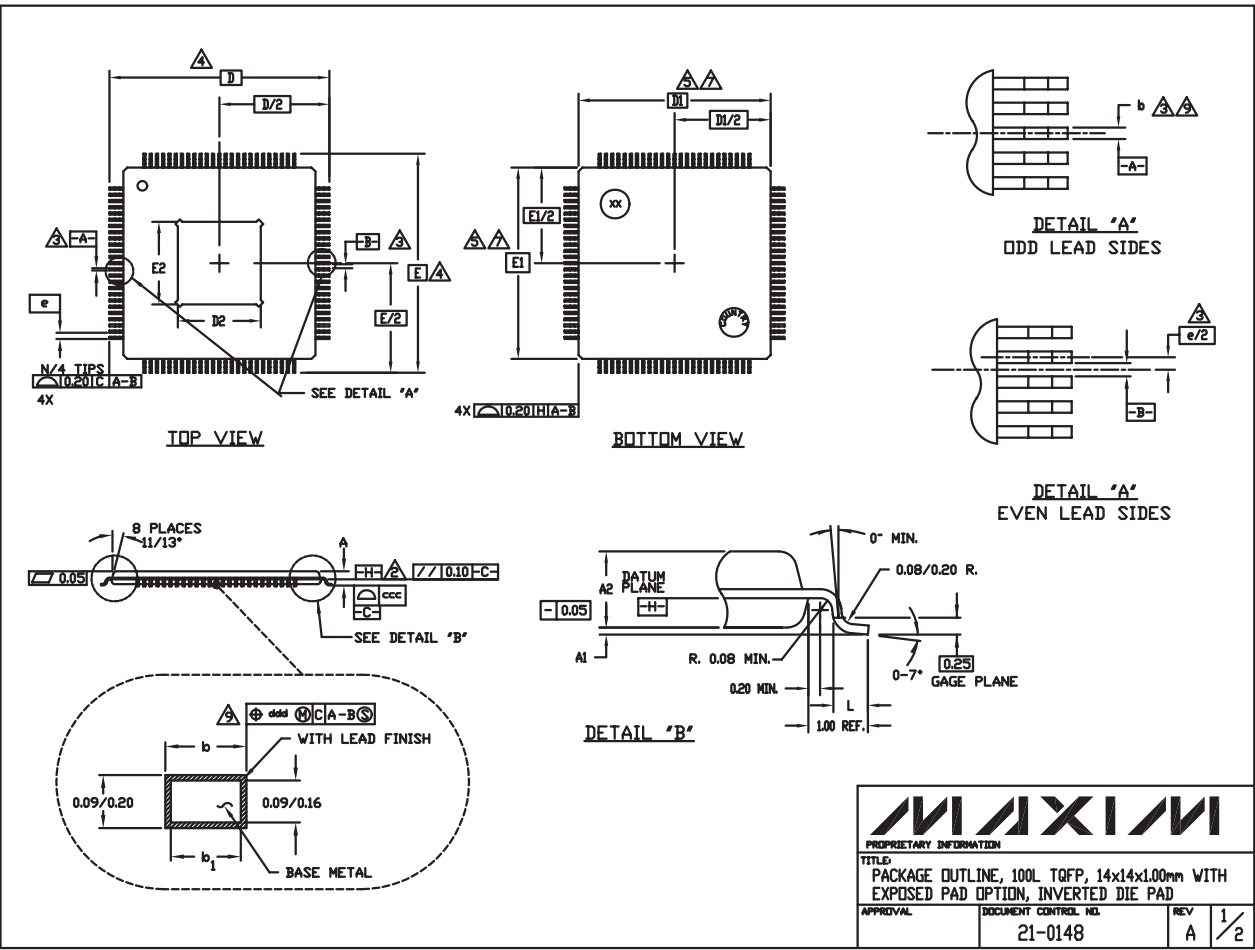
## Pin Configuration



# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



TQFP 14x14.EPS

# Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX9969

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. DATUM PLANE  $\square H$  LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUM  $\square A-B$  TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE  $\square H$ .
4. TO BE DETERMINED AT SEATING PLANE  $\square C$ .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254mm ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE  $\square H$ .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.50mm.
12. THIS OUTLINE IS NOT YET JEDEC REGISTERED.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
14. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05mm.
15. METAL AREA OF EXPOSED DIE PAD SHALL BE WITHIN 0.30mm OF THE NOMINAL DIE PAD SIZE.
16. COUNTRY OF ORIGIN MUST BE MARKED ON THE PACKAGE.

| SYMBOL | COMMON DIMENSIONS                 |        |      |      |
|--------|-----------------------------------|--------|------|------|
|        | ALL DIMENSIONS ARE IN MILLIMETERS |        |      | NOTE |
|        | MIN.                              | NOM.   | MAX. |      |
| A      | $\sim$                            | $\sim$ | 1.20 |      |
| A1     | 0.05                              | $\sim$ | 0.15 | 13   |
| A2     | 0.95                              | 1.00   | 1.05 |      |
| D      | 16.00 BSC.                        |        |      | 4    |
| D1     | 14.00 BSC.                        |        |      | 7,8  |
| E      | 16.00 BSC.                        |        |      | 4    |
| E1     | 14.00 BSC.                        |        |      | 7,8  |
| L      | 0.45                              | 0.60   | 0.75 |      |
| N      | 100                               |        |      |      |
| e      | 0.50 BSC.                         |        |      |      |
| b      | 0.17                              | 0.22   | 0.27 | 9    |
| b1     | 0.17                              | 0.20   | 0.23 |      |
| ccc    | $\sim$                            | $\sim$ | 0.08 |      |
| ddd    | $\sim$                            | $\sim$ | 0.08 |      |

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |
|------------------------|------|------|------|------|------|------|
| PKG. CODE              | D2   |      |      | E2   |      |      |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| C100E-8R               | 7.70 | 8.00 | 8.30 | 7.70 | 8.00 | 8.30 |

| MAXIM                                                                                       |                      |     |     |
|---------------------------------------------------------------------------------------------|----------------------|-----|-----|
| PROPRIETARY INFORMATION                                                                     |                      |     |     |
| TITLE<br>PACKAGE OUTLINE, 100L TQFP, 14x14x1.00mm WITH EXPOSED PAD OPTION, INVERTED DIE PAD |                      |     |     |
| APPROVAL                                                                                    | DOCUMENT CONTROL NO. | REV | 2/2 |
|                                                                                             | 21-0148              | A   |     |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 31