

TYPES SN54H103, SN74H103 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

REVISED DECEMBER 1983

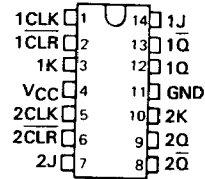
- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

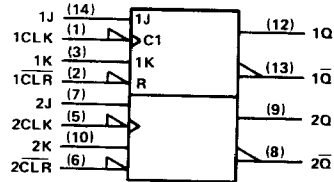
These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

The SN54H103 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74H103 is characterized for operation from 0° to 70°C .

SN54H103 ... J OR W PACKAGE
SN74H103 ... J OR N PACKAGE
(TOP VIEW)



logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	Q_0	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

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TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

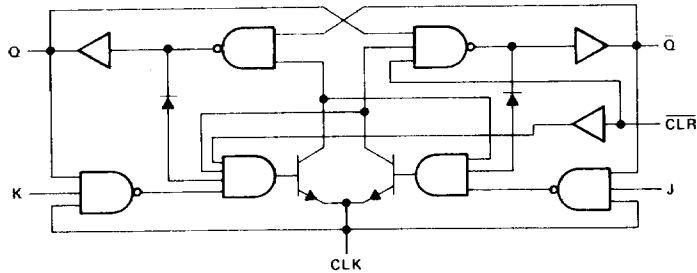
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TEXAS
INSTRUMENTS

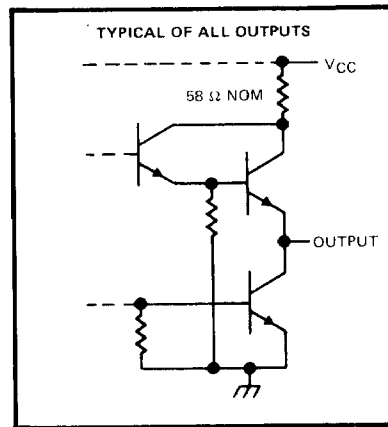
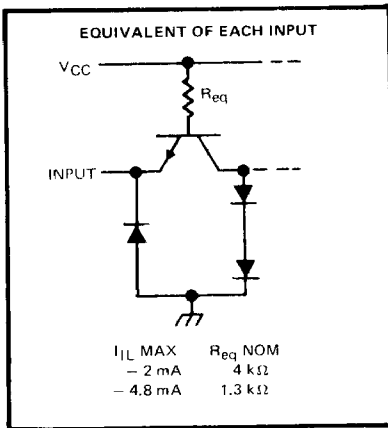
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TYPES SN54H103, SN74H103 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54H'	-55°C to 125°C
SN74H'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TTL DEVICES

TYPES SN54H103, SN74H103

DUAL J-K NEGATIVE-EDGE-TRIGGERED

FLIP-FLOPS WITH CLEAR

recommended operating conditions

		SN54H103			SN74H103			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	Low-level output current			− 0.5			− 0.5	μA
I _{OL}	Low-level output current			20			20	mA
t _w	Pulse duration	CLK high			10			ns
		CLK low			15			
		CLR low			16			
t _{su}	Setup time before CLK ↓	High-level data			10			ns
		Low-level data			13			
t _h	Hold time-data after CLK ↓	0			0			ns
T _A	Operating free-air temperature	− 55			125			70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54H103			SN74H103			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -8 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.5 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.2	0.4		0.2	0.4		V
I _I	V _{CC} = MAX, V _I = 5.5 V		1			1		mA
I _{IH}	Any J or K		50			50		μA
	CLR		100			100		
	CLK	0	-1		0	-1		
I _{IL}	Any J or K	-1	-2		-1	-2		mA
	CLR	-1	-2		-1	-2		
	CLK	-3	-4.8		-3	-4.8		
I _{OS} §	V _{CC} = MAX	-40	-100		-40	-100		mA
I _{CC}	V _{CC} = MAX, See Note 2		20	38		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f _{max}			R _L = 280 Ω, C _L = 25 pF		40	50		MHz
t _{PLH}	CL _R	Q or Q̄				8	12	ns
t _{PHL}	CL _R (CLK high)	Q̄ or Q				15	20	ns
	CL _R (CLK low)					23	35	
t _{PLH}	CLK	Q or Q̄				10	15	ns
t _{PHL}						16	20	

NOTE 3: See General Information Section for load circuits and voltage waveforms.