NCP451

3A Ultra-Small Low Ron and Controlled Load Switch with Auto-Discharge Path

The NCP451 is a very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with NMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail.

Proposed in a wide input voltage range from 0.75 V to 5.5 V, in a small 0.9 x 1.4 mm WLCSP6, pitch 0.5 mm.

Features

- 0.75 V – 5.5 V Operating Range
- 12 mΩ N MOSFET from 3.6 V to 5.5 V
- 13 mΩ N MOSFET from 1 V to 3.3 V
- DC Current Up to 3 A
- Output Auto−Discharge
- Active High EN Pin
- WLCSP6 0.9 x 1.4 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

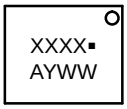
ON Semiconductor®

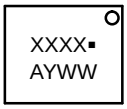
www.onsemi.com

WLCSP6
FC SUFFIX
CASE 499BR

WLCSP6
AFC SUFFIX
CASE 567KB

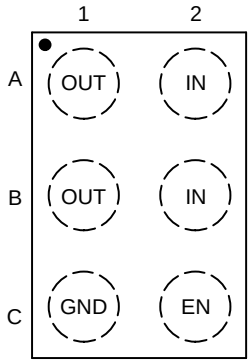
MARKING DIAGRAM





XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

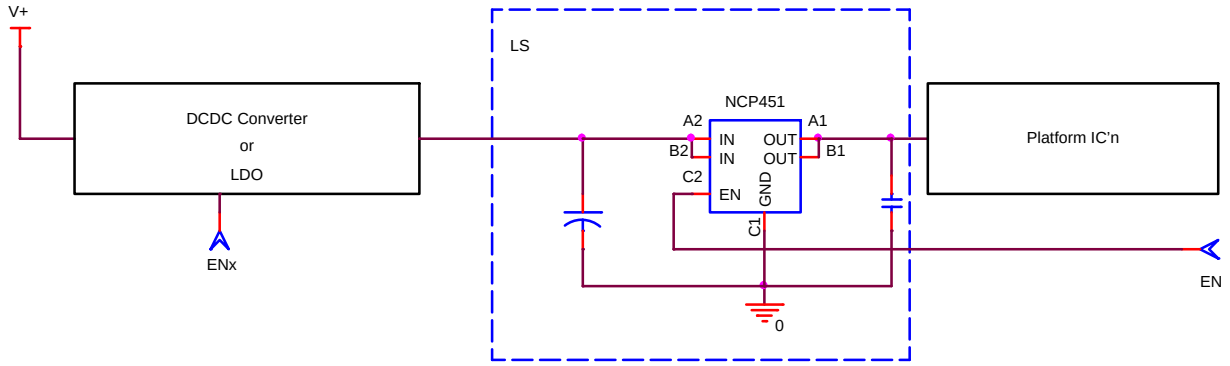


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2, B2	POWER	Load−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	C1	POWER	Ground connection.
EN	C2	INPUT	Enable input, logic high turns on power switch.
OUT	A1, B1	OUTPUT	Load−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

BLOCK DIAGRAM

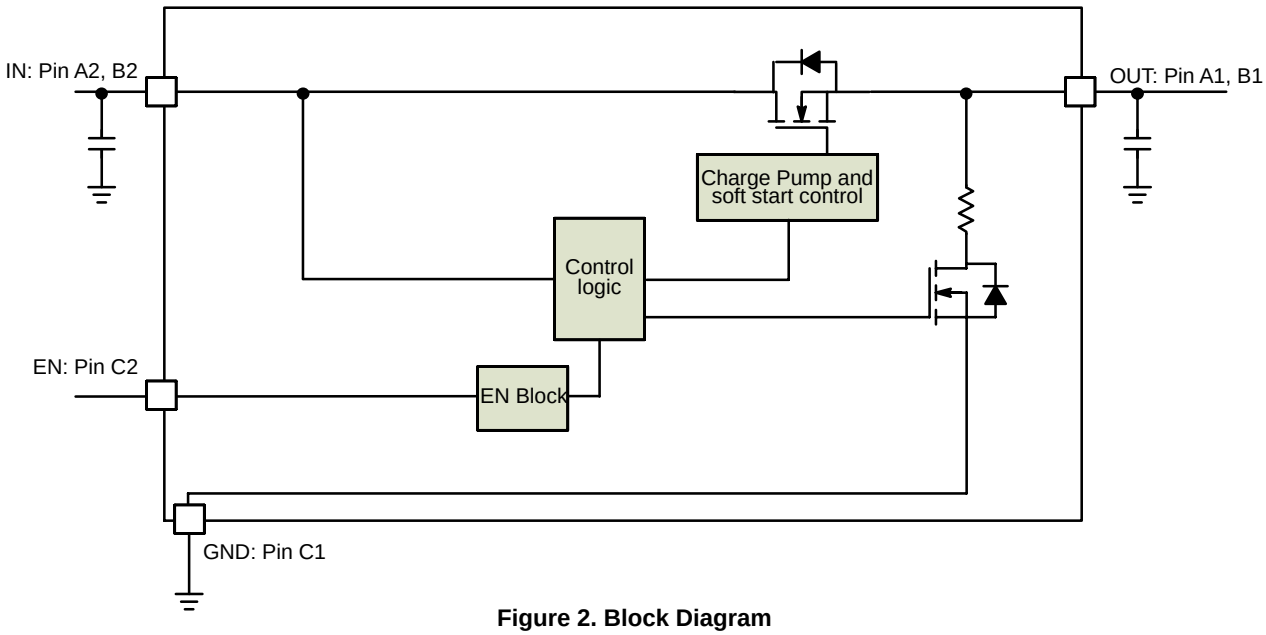


Figure 2. Block Diagram

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
IN, OUT, EN, Pins: (Note 1)	V_{EN}, V_{IN}, V_{OUT}	−0.3 to + 7.0	V
From IN to OUT Pins: Input/Output (Note 1)	V_{IN}, V_{OUT}	0 to + 7.0	V
Human Body Model (HBM) ESD Rating are (Notes 1 and 2)	ESD HBM	1.5	kV
Machine Model (MM) ESD Rating are (Notes 1 and 2)	ESD MM	250	V
Charge Device Model (CDM) ESD Rating are (Notes 1 and 2)	ESD CDM	2000	V
Latch−up protection (Note 3) −Pins IN, OUT, EN	LU	100	mA
Maximum Junction Temperature	T_J	−40 to + 125	°C
Storage Temperature Range	T_{STG}	−40 to + 150	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±1.5 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±250 V per JEDEC standard: JESD22−A115 for all pins.
   Charge Device Model (CDM) ±2.0 kV per JEDEC standard: JESD22−C101 for all pins.
3. Latchup Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Operational Power Supply		0.75		5.5	V
V_{EN}	Enable Voltage		0		5.5	V
T_A	Ambient Temperature Range		−40	25	+85	°C
T_J	Junction Temperature Range		−40	25	+125	°C
C_{IN}	Decoupling input capacitor		1			μF
C_{OUT}	Decoupling output capacitor		1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	(Note 5)		100		°C/W
I_{OUT}	Maximum DC current				3	A
P_D	Power Dissipation Rating (Note 6)	Over temperature		0.315		W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 0.75 V to 5.0 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{IN} = 3.6 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance	V_{IN} = 5 V	I_{OUT} = 200 mA, T_A = 25°C		12	20	mΩ
			T_J = 125°C			25	
		V_{IN} = 3.6 V	I_{OUT} = 200 mA, T_A = 25°C		12	20	
			T_J = 125°C			25	
		V_{IN} = 3.3 V	I_{OUT} = 200 mA, T_A = 25°C		13	24	
			T_J = 125°C			28	
		V_{IN} = 2.5 V	I_{OUT} = 200 mA, T_A = 25°C		13	24	
			T_J = 125°C			28	
		V_{IN} = 1.8 V	I_{OUT} = 200 mA, T_A = 25°C		13	24	
			T_J = 125°C			28	
		V_{IN} = 1.0 V	I_{OUT} = 200 mA, T_A = 25°C		13	24	
			T_J = 125°C			28	
		V_{IN} = 0.75 V	I_{OUT} = 200 mA, T_A = 25°C		15	28	
			T_J = 125°C			35	
Rdis	Output discharge path	EN = low	NCP451		1.2	1.7	MΩ
			NCP451A		1.0	1.7	kΩ
V_{IH}	High−level input voltage			0.8			V
V_{IL}	Low−level input voltage					0.4	
I_{EN}	EN pin leakage current	V_{IN} = 3.6 V				0.1	μA
QUIESCENT CURRENT							
Istd	Standby current	V_{IN} = 4.2 V	EN = low, No load		0.9	2	μA
Iq	Quiescent current	V_{IN} = 3.6 V V_{IN} = 2.5 V V_{IN} = 1.8 V V_{IN} = 1.2 V V_{IN} = 1.0 V V_{IN} = 0.75 V	EN = high, No load (Note 7)		8	15	μA
TIMINGS							
T_{EN}	Enable time	V_{IN} = 3.6 V (Note 8)	R_L = 25 Ω, C_{OUT} = 1 μF		600		μs
T_R	Output rise time		R_L = 25 Ω, C_{OUT} = 1 μF		800		
T_{ON}	ON time (T_{EN} + T_R)		R_L = 25 Ω, C_{OUT} = 1 μF		1400		
T_F	Output fall time		R_L = 25 Ω, C_{OUT} = 1 μF		55		
TIMINGS							
T_{EN}	Enable time	V_{IN} = 3.6 V (Note 8)	R_L = 10 Ω, C_{OUT} = 0.1 μF		540		μs
T_R	Output rise time		R_L = 10 Ω, C_{OUT} = 0.1 μF		670		
T_{ON}	ON time (T_{EN} + T_R)		R_L = 10 Ω, C_{OUT} = 0.1 μF		1210		
T_F	Output fall time		R_L = 10 Ω, C_{OUT} = 0.1 μF		2.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Production tested at V_{IN} = 3.6 V.
8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

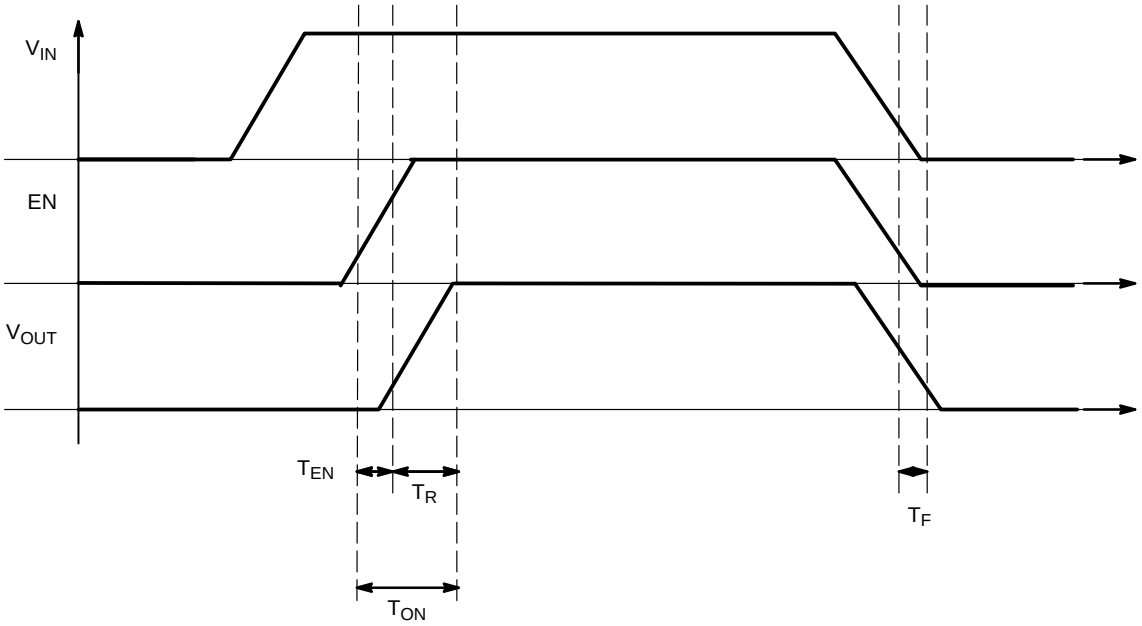


Figure 3. Enable, Rise and Fall Time

ELECTRICAL CURVES

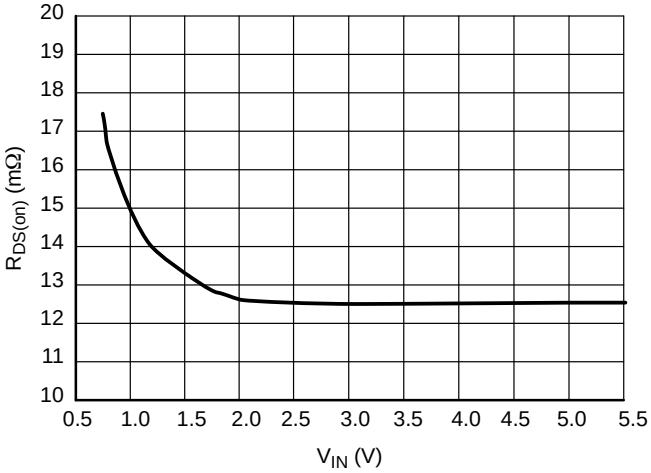


Figure 4. $R_{DS(on)}$ vs. V_{IN}, Low Load

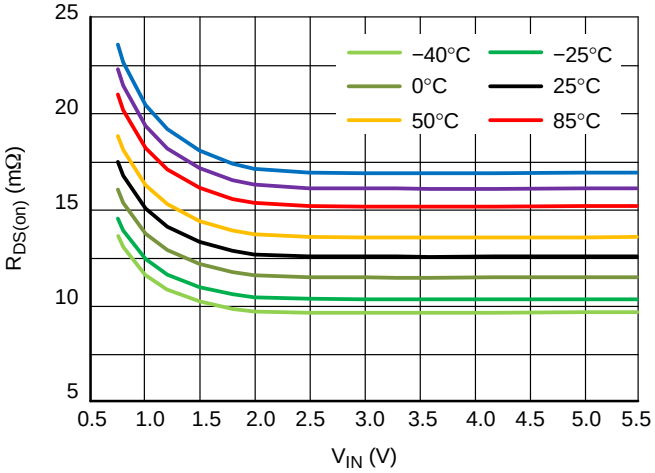


Figure 5. $R_{DS(on)}$ vs. V_{IN}, Low Load, Multi Temperature

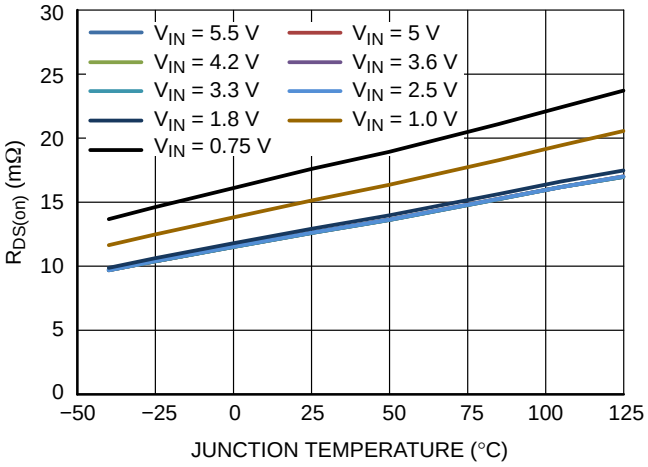


Figure 6. $R_{DS(on)}$ vs. Temperature, Multi V_{IN} Voltage

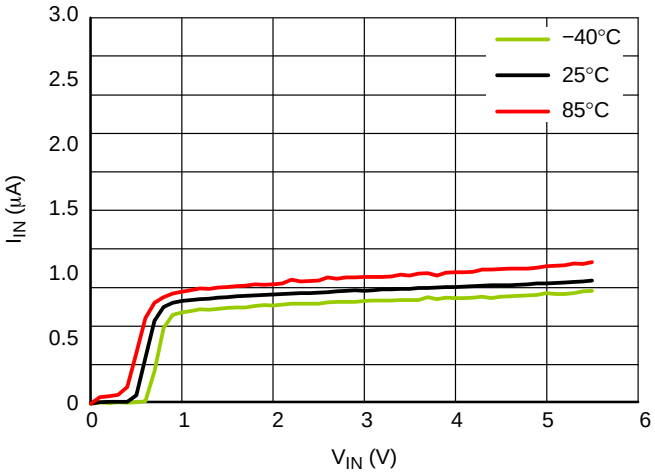


Figure 7. Standby Current (μA) vs. Temperature

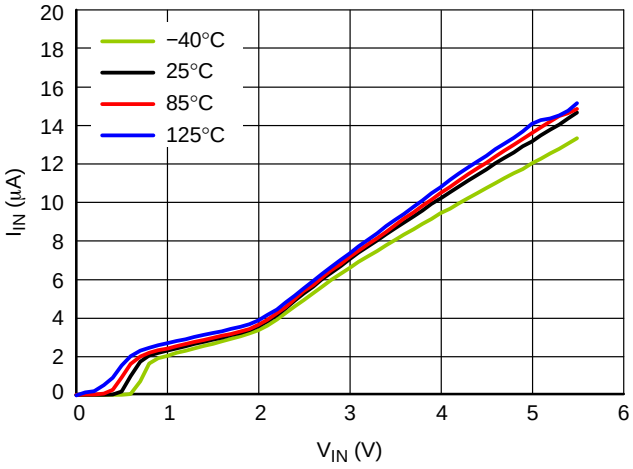


Figure 8. Quiescent Current (μA) vs. Temperature

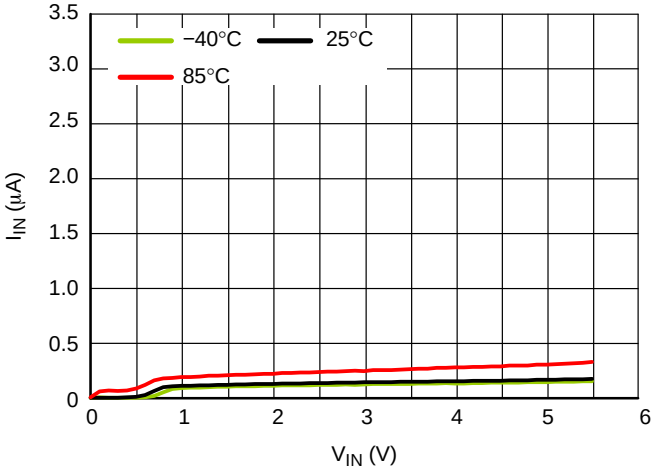


Figure 9. MOSFET Leakage Current (μA) vs. Temperature

ELECTRICAL CURVES

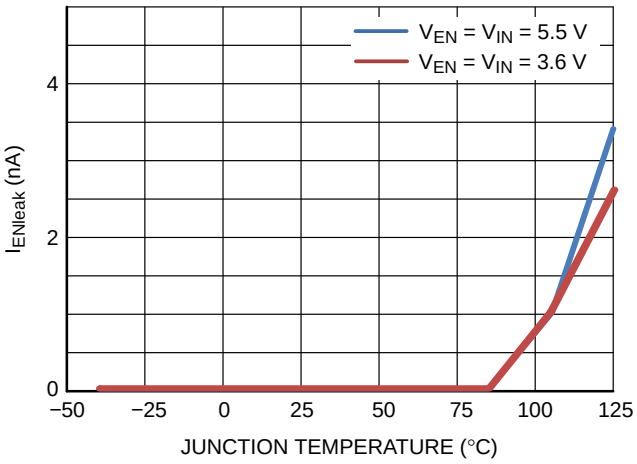


Figure 10. EN Pin Leakage vs. Temperature

FUNCTIONAL DESCRIPTION

Overview

The NCP451 is a high side N channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 0.75 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing N−MOSFET switch off.

The IN/OUT path is activated with a minimum of Vin of 0.75 V and EN forced to high level.

Auto Discharge

N−MOSFET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto−discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and V_{IN} > 0.75 V.

In order to limit the current across the internal discharge N−MOSFET, the typical value is set at R_{DIS}.

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μF, at least, capacitors must be placed as close as possible the part to for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times \left(I_{OUT}\right)^2$$

P_D = Power dissipation (W)

$R_{DS(on)}$ = Power MOSFET on resistance (Ω)

I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A$$

T_J = Junction temperature (°C)

$R_{\theta JA}$ = Package thermal resistance (°C/W)

T_A = Ambient temperature (°C)

PCB Recommendations

The NCP451 integrates an up to 3 A rated NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

Routing example: 2 oz, 4 layers with vias across 2 internal inners.

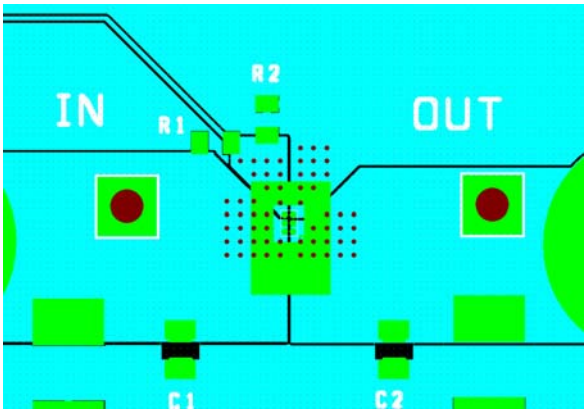


Figure 11.

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J: junction temperature.

T_A: ambient temperature.

Rtheta= Thermal resistance between IC and air, through PCB.

$R_{DS(on)}$: intrinsic resistance of the IC MOSFET.

I: load DC current.

Taking into account of Rtheta obtain with:

1 oz, 2 layers: 100°C/W.

At 3 A, 25°C ambient temperature, $R_{DS(on)}$ 20 mΩ @ V_{IN} 5 V, the junction temperature will be:

$$T_J - T_A = Rtheta \times P_D = 25 + \left(0.02 \times 3^3\right) \times 100 = 43^\circ C$$

Taking into account of Rtheta obtain with:

2 oz, 4 layers: 60°C/W.

At 3 A, 65°C ambient temperature, $R_{DS(on)}$ 24 mΩ @ V_{IN} 5 V, the junction temperature will be:

$$T_J = T_A + Rtheta \times P_D = 65 + \left(0.024 \times 3^2\right) \times 60 = 78^\circ C$$

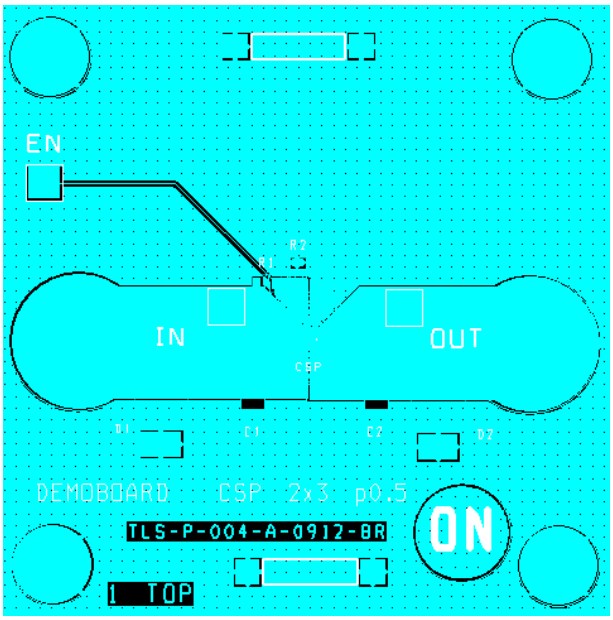


Figure 12. Demoboard PCB Top View

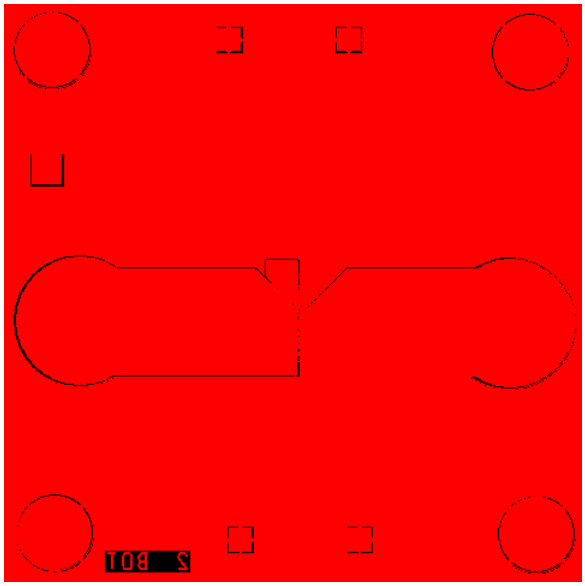


Figure 13. Demoboard PCB Top View

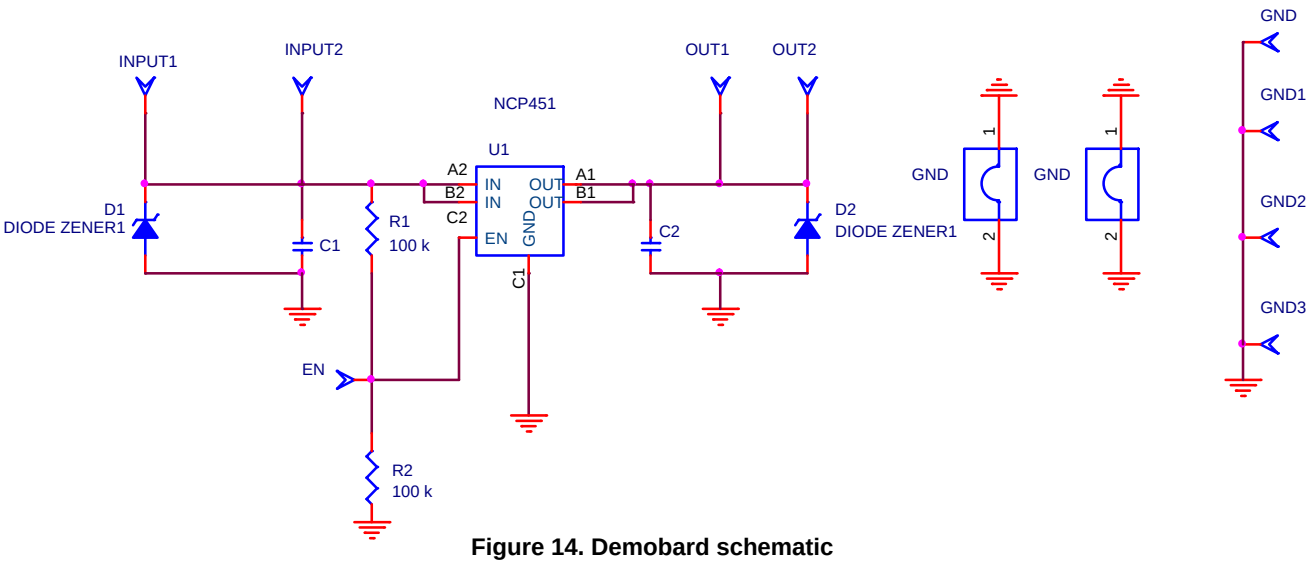


Figure 14. Demobard schematic

BILL OF MATERIAL

Quantity	Reference Scheme	Part Description	Part Number	Manufacturer
2	IN, OUT	Socket, 4mm, metal, PK5	B010	HIRSCHMANN
3	IN_2, OUT_2, , EN	HEADER200	2.54 mm, 77313−101−06LF	FC
3	C1, C2	1uF	GRM155R70J105KA12#	Murata
1	D1, D2	TVS (not mounted)	ESD9x	ON semiconductor
2	GND2,GND	GND JUMPER	D3082F05	Harvin
2	R2, R3	Resistor 100k 0603	MC 0.063 0603 1% 100K	MULTICOMP
1	U1	Load switch	NCP451	ON semiconductor

ORDERING INFORMATION

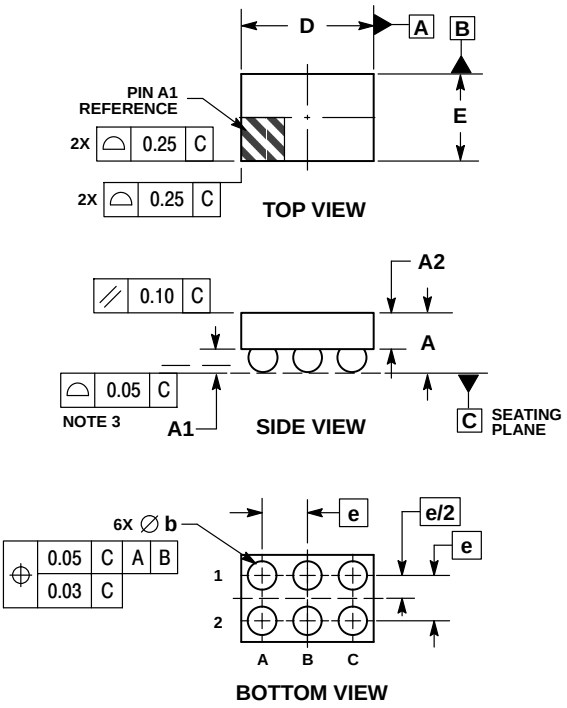
Device	Marking	Option	Package	Shipping†
NCP451FCT2G	451	Auto Discharge 1.2 MΩ	Case 499BR (Pb−Free)	3000 / Tape & Reel
NCP451AFCT2G	51A	Auto Discharge 1.0 kΩ	Case 567KB* (Pb−Free)	3000 / Tape & Reel
NCP451AFCCT2G	51AC	Auto Discharge 1.0 kΩ with ChipCoat	Case 567KB* (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*UBM = 205 μm (±8 μm)

PACKAGE DIMENSIONS

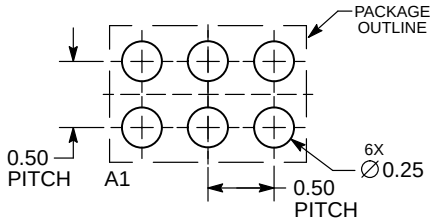
WLCSP6, 1.40x0.90
CASE 567KB
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	0.510
A1	0.142	---	0.172
A2	---	0.320	0.338
b	0.195	---	0.235
D	---	1.400	1.440
E	---	0.900	0.940
e	0.50 BSC		

RECOMMENDED SOLDERING FOOTPRINT*

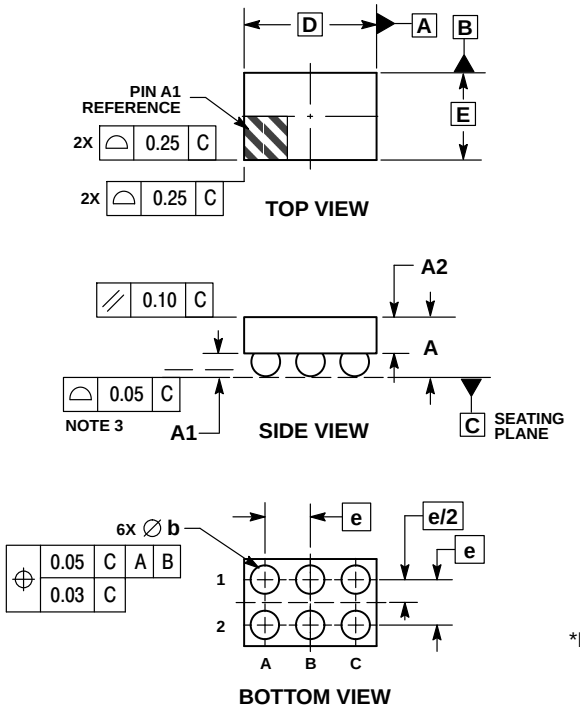


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WLCSP6, 1.40x0.90
CASE 499BR
ISSUE A



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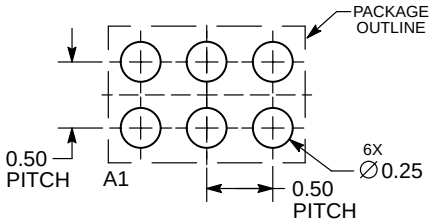
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	–––	0.50
A1	0.17	0.23
A2	0.25 REF	
b	0.21	0.25
D	1.40 BSC	
E	0.90 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Europe, Middle East and Africa Technical Support:
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