

July 2013

## **FDZ4010**

# **Integrated Load Switch**

### **Features**

- Input Voltage Range from 2 V to 5 V
- 10 mA output current
- Ultra Thin and Small Package WL-CSP 0.8 X 1.2 mm<sup>2</sup>, Height 0.5 mm
- RoHS Compliant



## **General Description**

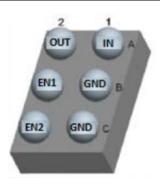
The FDZ4010 is a 10 mA high side Pch MOSFET switch that can be controlled by two enable signals. It is an AND function switch activated by asserting both enable signals high. Input voltage range operates from 2 V to 5 V to align with the requirement of portable devices power requirement. FDZ4010 is uniquely designed for optimized low power dissipation and precise driver requirement. FDZ4010 comes in a tiny 0.8 mm X 1.2 mm WLCSP, 6 bumps, with 0.4 mm pitch.

## **Application**

■ Smart Phone / Table Accessory







**BOTTOM View** 

6 Balls, 0.8 X 1.2 mm<sup>2</sup> WL-CSP

#### **Package Marking and Ordering Information**

Part Number	Device Marking	Ball Pitch	Package	Reel Size	Tape Width	Quantity
FDZ4010	Z5	0.4 mm	0.8 mm x 1.2 mm WL-CSP, 6 Bumps	7 "	8 mm	3000



for Fairchild's definition of Eco Status, please visit: <a href="http://www.fairchildsemi.com/company/green/rohs">http://www.fairchildsemi.com/company/green/rohs</a> green.html

## **Application Diagram**

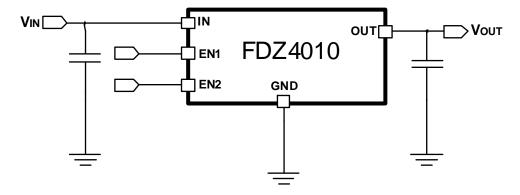


Figure 1. Typical Application

## **Block Diagram**

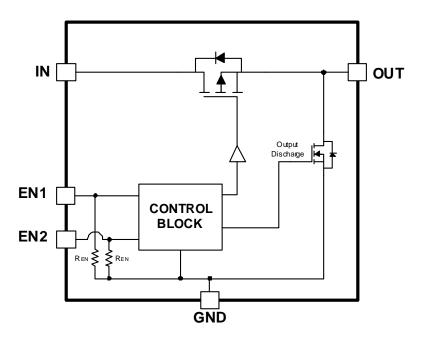


Figure 2. Functional Block Diagram

## **Truth Table**

V <sub>IN</sub> (2 V to 5 V)	EN1	EN2	PCH MOSFET Status	V <sub>OUT</sub> Status
YES	HIGH	HIGH	ON	V <sub>IN</sub>
YES	LOW	LOW	OFF	LOW
YES	HIGH	LOW	OFF	LOW
YES	LOW	HIGH	OFF	LOW

**Table 1. Truth Table for OUT Status** 

## Pin Configuration

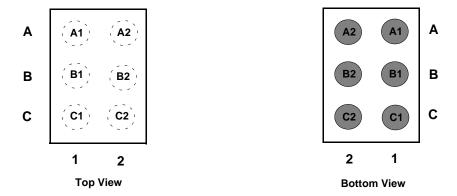


Figure 3. Pin Assignments

## **Pin Definitions**

Pin#	Name	Description	
A1	IN	Input of the Pch MOSFET Switch	
A2	OUT	Output of the Pch MOSFET Switch. Internally, this pin is pulled down through an output discharge FET to Ground when EN pins are low and V <sub>IN</sub> is present.	
B1, C1	GND	Ground	
B2	EN1	ON/OFF control input, Active High.	
C2	EN2	ON/OFF control input, Active High.	

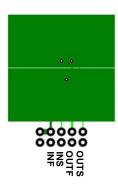
## **Absolute Maximum Ratings**

Characterist	Min.	Max.	Unit	
V <sub>IN</sub> , V <sub>OUT</sub> to GND		-0.3	6	V
V <sub>EN1</sub> ,V <sub>EN2</sub> to GND		-0.3	6	V
Continuous Output Current			20	mA
Junction Temperature (T <sub>J</sub> )		150	°C	
Storage Temperature Range (T <sub>STG</sub> )	-65	150	°C	
Thermal Resistance, Junction to Ambient $(\theta_{JA})$	(Note 1b)		312	°C/W
Flootypototic Discharge	Human Body Model, ANSI/ESDA/ JEDEC JS-001-2012	5		kV
Electrostatic Discharge	Charged Device Model, JESD22- C101	2		- KV

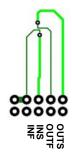
## **Recommended Operating Conditions**

Characteristics	Symbol	Min.	Max.	Unit
IN Voltage	V <sub>IN</sub>	2	5	V
OUT Current, $V_{IN} = 3.3 \text{ V}$ , $V_{EN1} = V_{EN2} = 3.3 \text{ V}$	Гоит		10	mA
EN1, EN2 Voltage	V <sub>EN1</sub> , V <sub>EN2</sub>		5	V
Operating Temperature Range		-40	85	°C

Notes: 1.  $R_{0JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting suface of the drain pins.  $R_{0JC}$  is guaranteed by design while  $R_{0CA}$  is determined by the user's board design.



a. 115 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

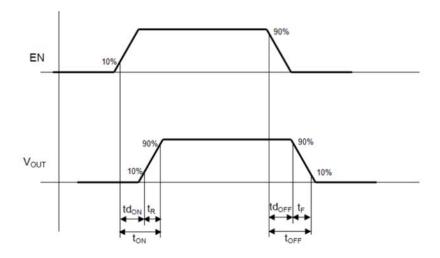


b. 312 °C/W when mounted on a minimum pad of 2 oz copper.

# **Electrical Characteristics** $V_{\text{IN}}$ = 2 V to 5 V, $T_{\text{J}}$ = 25 °C , unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
V <sub>IH</sub>	Input High Voltage, EN1, EN2	V <sub>IN</sub> = 2.5 V to 5 V and across temperature range	1.375			V
$V_{IH}$	Input High Voltage, EN1, EN2	V <sub>IN</sub> = 2 V and across temperature range	1.525			V
V <sub>IL</sub>	Input Low Voltage, EN1, EN2	V <sub>IN</sub> = 2 V to 5 V and across temperature range			0.95	V
R <sub>EN</sub>	Pull Down Resistance at EN1, EN2	V <sub>EN1</sub> = V <sub>EN2</sub> = 1 V and across temperature range	70	100	130	kΩ
C <sub>EN</sub>	Input Capacitance of EN1, EN2	f = 1 MHz and across temperature range (Note 2)			10	pF
R <sub>DS(ON)</sub>	On-Resistance of Pch MOSFET	I <sub>OUT</sub> = 10 mA, V <sub>IN</sub> = 2 V to 5 V			1.5	Ω
IQ	Quiescent Current	$V_{IN} = 5 \text{ V}, V_{EN1} = V_{EN2} = 5 \text{ V},$ $V_{OUT}$ floating ( $I_{OUT} = 0$ ), Across temperature range			500	μА
		$V_{\text{IN}} = 3.3 \text{ V}, V_{\text{EN1}} = V_{\text{EN2}} = 0 \text{ V}, \\ V_{\text{OUT}} \text{ floating } (I_{\text{OUT}} = 0), \\ \text{Across temperature range}$			1	μА
I <sub>SD</sub>	Shutdown Current	$ \begin{aligned} & \overline{V_{IN}} = 3.3 \; V, \\ & V_{EN1} = 825 \; mV \; \& \; V_{EN2} = 425 \; mV, \\ & V_{EN1} = 425 \; mV \; \& \; V_{EN2} = 825 \; mV, \\ & V_{OUT} \; floating \; (I_{OUT} = 0), \\ & Across \; temperature \; range \end{aligned} $			10	μΑ
R <sub>OUT</sub>	Pull Down Resistance at OUT Pin	$V_{EN1} = V_{EN2} = 0 V$		1	1.3	kΩ
t <sub>on</sub>	Turn-On Time	Load Impedance,			1	μS
t <sub>r</sub>	Turn-On Rise Time	$V_{IN} = 3.3 \text{ V},$			0.95	μS
t <sub>off</sub>	Turn-Off Time	$C_L = 50 \text{ pF}, R_L = 500 \Omega,$ $V_{EN1} = V_{EN2} = 0 \text{ V to } 2.3 \text{ V},$			2	μS
t <sub>f</sub>	Turn-Off Fall Time	$V_{\text{EN1}} = V_{\text{EN2}} = 0 \text{ V to 2.3 V},$ (500 ns rise time)			2	μS

**Notes:**2. Guaranteed by characterization and design



td<sub>ON</sub> = Delay On Time t<sub>R</sub> = V<sub>OUT</sub> Rise Time ton = Turn-On Time td<sub>OFF</sub>= Delay Off Time  $t_F = V_{OUT}$  Fall Time  $t_{OFF} = Turn-Off Time$ 

Figure 4. Timing Diagram

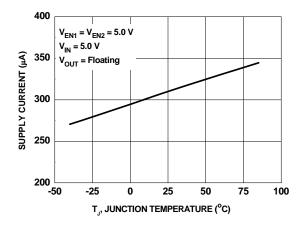


Figure 5. Quiescent Current vs Temperature

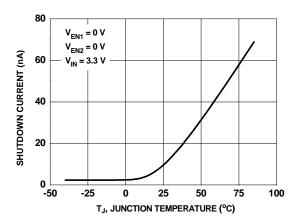


Figure 7. Shutdown Current vs Temperature

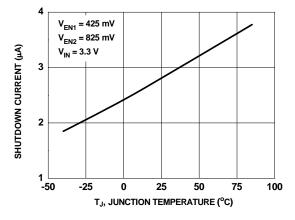


Figure 9. Shutdown Current vs Temperature

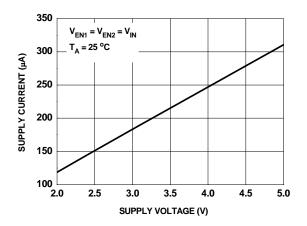


Figure 6. Quiescent Current vs Supply Voltage

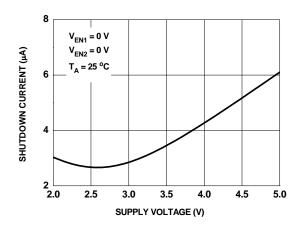


Figure 8. Shutdown Current vs Supply Voltage

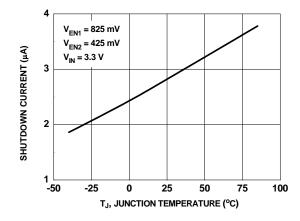
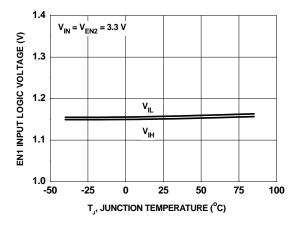


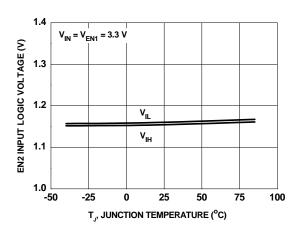
Figure 10. Shutdown Current vs Temperature



1.4 T<sub>A</sub> = 25 °C EN1 INPUT LOGIC VOLTAGE (V)  $V_{IN} = V_{EN2}$ 1.3  $V_{IL}$  $V_{IH}$ 1.1 2.5 3.0 3.5 4.0 4.5 5.0 SUPPLY VOLTAGE (V)

Figure 11. EN1 Logic Voltage vs Temperature

Figure 12. EN1 Logic Voltage vs Supply Voltage (VIN)



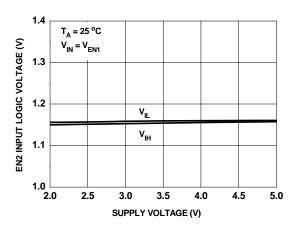
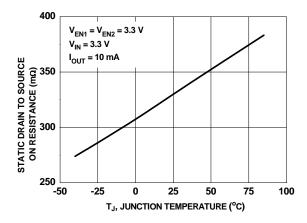


Figure 13. EN2 Logic Voltage vs Temperature

Figure 14. EN2 Logic Voltage vs Supply Voltage (VIN)



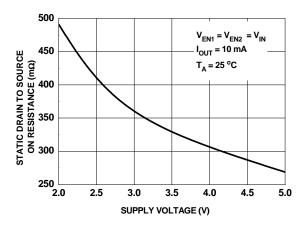


Figure 15. Static Drain to Source ON Resistance vs Temperature

Figure 16. Static Drain to Source ON Resistance vs Supply Voltage

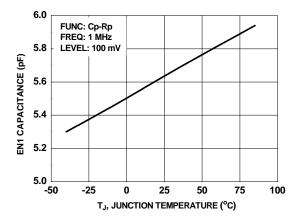


Figure 17. EN1 Capacitance vs Temperature

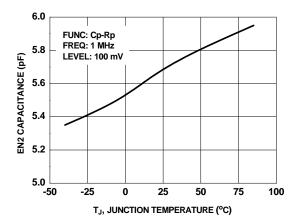


Figure 18. EN2 Capacitance vs Temperature

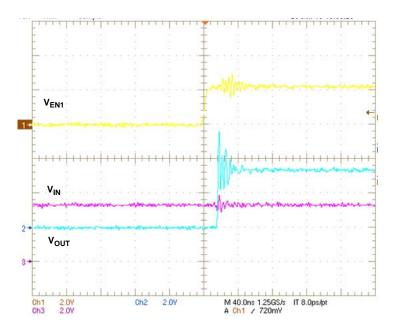


Figure 19. Turn-On Time (V<sub>IN</sub> = 3.3 V, V<sub>EN2</sub> = 2.3 V, V<sub>EN1</sub>= 0 to 2.3 V, C<sub>OUT</sub> = 50 pF, R<sub>L</sub>= 500  $\Omega$ , timescale = 40 us/div)

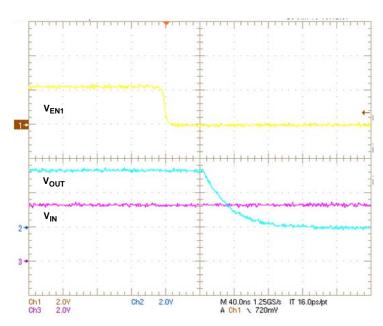


Figure 20. Turn-Off Time (V<sub>IN</sub> = 3.3 V, V<sub>EN2</sub> = 2.3 V, V<sub>EN1</sub> = 2.3 to 0 V, C<sub>OUT</sub> = 50 pF, R<sub>L</sub>= 500  $\Omega$ , timescale = 40 us/div)

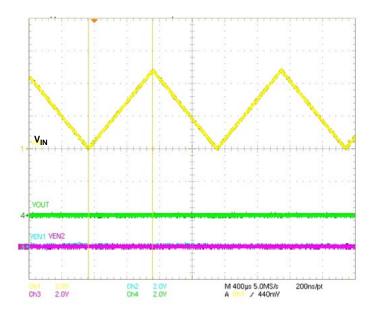


Figure 21. V<sub>IN</sub> Ramp Up and Down (V<sub>IN</sub> = 0 to 4.8 V (6100 V/sec), EN1 and EN2 are floating(Internally GND),  $C_{OUT}$  = 50 pF,  $R_L$ = 500  $\Omega$ , timescale = 400 us/div)

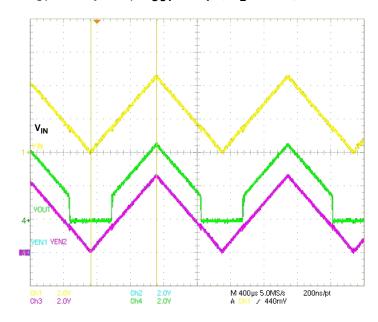


Figure 22. V<sub>IN</sub> Ramp Up and Down (EN1 = EN2 = V<sub>IN</sub> = 0 to 4.8 V (6100 V/sec),  $C_{OUT}$  = 50 pF,  $R_{L}$ = 500  $\Omega$ , timescale = 400 us/div)

#### **Application Information**

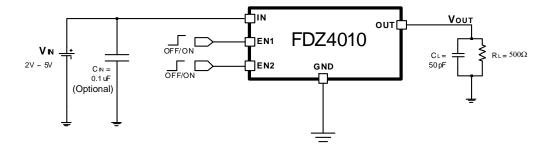


Figure 23. Typical Application Circuit

#### **Input Voltage**

Input Voltage (V<sub>IN</sub>) is set from 2 V to 5 V.

#### **Input Capacitor**

To prevent the input voltage being pulled below the minimum operating voltage, a reservoir capacitor can be connected from IN to GND.  $0.1~\mu F$  ceramic type is suitable.

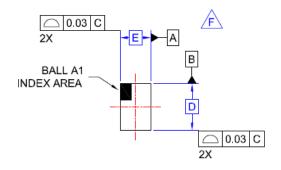
### **Enable/Shutdown Operation**

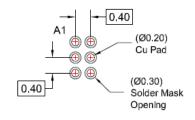
To turn on the switch, both the EN pins need to be asserted high. To ensure proper operation, Enable signals must be able to swing above and below the specified turn-on/off voltage threshold described in the Electrical Charateristics table under VIL and VIH for the selected input voltage.

#### **Power up Sequence**

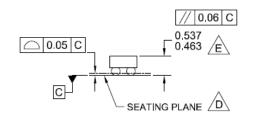
Turn on input voltage ( $V_{IN}$ ) within range from 2 V to 5 V then turn on EN1 or/and EN2 signal.  $V_{OUT}$  status changed by EN1 or/and EN2 signal input and defined the status in Table 1 Truth Table.

## **Dimensional Outline and Pad Layout**

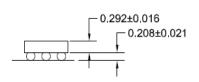




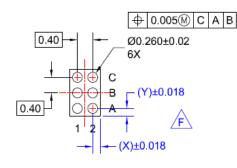
#### TOP VIEW



# RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



#### SIDE VIEWS



**BOTTOM VIEW** 

#### NOTES:

- A, NO JEDEC REGISTRATION APPLIES,
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASMEY14,5M, 1994.

DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E PACKAGE TYPICAL HEIGHT IS 463 MICRONS ±37 MICRONS (463-537 MICRONS).

FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

## **Product-Specific Dimensions**

Product	D	E	X	Y
FDZ4010	1.16 mm	0.76 mm	0.18 mm	0.18 mm





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