



Low *I*BIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

MAX4036-MAX4039

General Description

The single MAX4036/MAX4037 and dual MAX4038/MAX4039 operational amplifiers operate from a single +1.4V to +3.6V (without reference) or +1.8V to +3.6V (with reference) supply and consume only 800nA of supply current per amplifier, and 1.1μA for the optional reference. The MAX4036/MAX4038 feature a common-mode input voltage range from 0V to $V_{DD} - 0.4V$ at $V_{DD} = 1.4V$. The MAX4037/MAX4039 feature a 1.232V voltage reference capable of sourcing 100μA and sinking 20μA.

The MAX4036-MAX4039s' rail-to-rail outputs drive 5kΩ loads to within 25mV of the rails. Ultra-low supply current, low operating voltage, and rail-to-rail outputs make the MAX4036-MAX4039 ideal for use in single-cell lithium-ion (Li+), or two-cell NiCd/NiMH/alkaline battery-powered applications.

The MAX4036 is available in an SC70 package, the MAX4037 in a SOT23 package, and the MAX4038/MAX4039 in UCSP™, μMAX®, and TDFN packages.

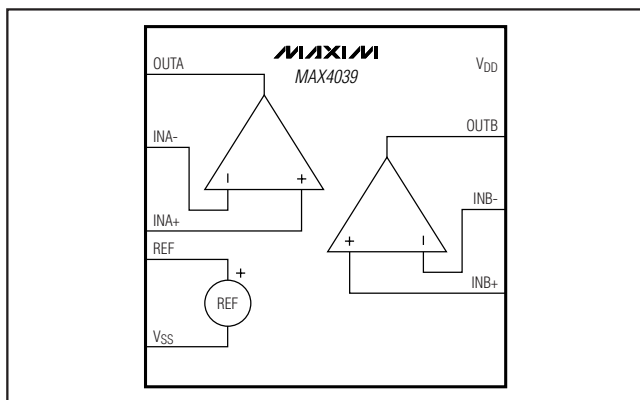
Applications

Battery-Powered/Solar-Powered Systems
 Portable Medical Instrumentation
 Pagers and Cell Phones
 Micropower Thermostats and Potentiostats
 Electrometer Amplifiers
 Remote Sensor Amplifiers
 Active Badges
 pH Meters

Pin Configurations and Selector Guide appear at end of data sheet.

μMAX is a registered trademark and UCSP is a trademark of Maxim Integrated Products, Inc.

Functional Diagram



Features

- ♦ Ultra-Low 800nA per Amplifier Supply Current
- ♦ Ultra-Low 1.4V Supply Voltage Operation (1.8V for MAX4037/MAX4039)
- ♦ Rail-to-Rail Outputs Drive 5kΩ and 5000pF Load
- ♦ 1.232V ±0.5%, 120ppm/°C (max) Reference (MAX4037/MAX4039)
- ♦ No External Reference Bypass Capacitor Required
- ♦ No Phase Reversal for Overdriven Inputs
- ♦ Low 1.0pA (typ) Input Bias Current
- ♦ Low 200μV Input Offset Voltage
- ♦ Unity-Gain Stable
- ♦ Available in Tiny UCSP, SC70, SOT23, TDFN, and μMAX Packages
- ♦ Available in -40°C to +125°C Temperature Range (MAX4036A/MAX4038A)

Ordering Information

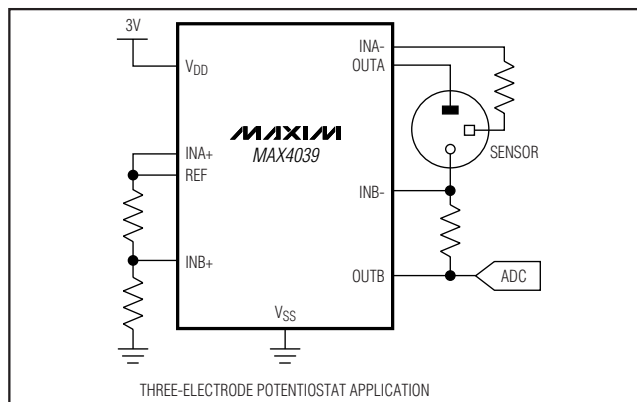
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4036EXK-T	-40°C to +85°C	5 SC70-5	AFR
MAX4036AAXK+T	-40°C to +125°C	5 SC70-5	ASN
MAX4037EUT-T	-40°C to +85°C	6 SOT23-6	ABRX
MAX4038ETA-T	-40°C to +85°C	8 TDFN-EP*	AGO
MAX4038EUA	-40°C to +85°C	8 μMAX	—
MAX4038EBL-T	-40°C to +85°C	9 UCSP-9	AEG
MAX4038AAUA	-40°C to +125°C	8 μMAX	—

+Denotes lead-free package.

*EP = Exposed paddle.

Ordering Information continued at end of data sheet.

Typical Operating Circuit



MAXIM

Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} -0.3V to +4.0V
 INA+, INB+, INA-, INB-, IN+, IN-, OUTA, OUTB, OUT, REF (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
 OUTA, OUTB, OUT, REF Shorted to V_{SS} or V_{DD} Continuous
 Maximum Continuous Power Dissipation (T_A = +70°C)
 5-Pin SC70 (derate 3.1mW/°C above +70°C) 247mW
 6-Pin SOT23 (derate 8.7mW/°C above +70°C) 696mW
 8-Pin μ MAX (derate 4.5mW/°C above +70°C) 362mW
 8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW

9-Bump UCSP (derate 5.2mW/°C above +70°C) 412mW
 10-Pin μ MAX (derate 5.6mW/°C above +70°C) 444mW
 10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
 Operating Temperature Range
 MAX403_E_ -40°C to +85°C
 MAX403_A_ -40°C to +125°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{SS} = V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L to V_{DD}/2, C_L = 15pF, T_A = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V _{DD}	MAX4036/MAX4038, guaranteed by PSRR tests		1.4		3.6	V
		MAX4037/MAX4039, guaranteed by PSRR and line regulation tests		1.8		3.6	
Supply Current	I _{DD}	MAX4036	V _{DD} = 1.4V		0.8	1.2	μA
			V _{DD} = 3.6V		0.9	1.3	
		MAX4037	V _{DD} = 1.8V		1.9	2.4	
			V _{DD} = 3.6V		2.0	2.5	
		MAX4038	V _{DD} = 1.4V		1.7	2.3	
			V _{DD} = 3.6V		1.9	2.5	
		MAX4039	V _{DD} = 1.8V		2.8	4.0	
			V _{DD} = 3.6V		3.0	4.1	
OPERATIONAL AMPLIFIERS							
Input Offset Voltage	V _{OS}				±0.2	±2.0	mV
Input Bias Current	I _B	(Note 1)			±1.0	±10	pA
Input Offset Current	I _{OS}	(Note 1)			±0.3	±20	pA
Input Common-Mode Voltage Range	V _{CM}	Guaranteed by CMRR test	V _{DD} = 1.4V (MAX4036/MAX4038 only)	V _{SS}		V _{DD} - 0.4	V
			V _{DD} = 1.8V	V _{SS}		V _{DD} - 0.3	
			V _{DD} = 3.3V	V _{SS}		V _{DD} - 0.2	
Common-Mode Rejection Ratio	CMRR	V _{DD} = 1.4V, V _{SS} ≤ V _{CM} ≤ (V _{DD} - 0.4V) (MAX4036/MAX4038 only)		50	70		dB
		V _{DD} = 1.8V, V _{SS} ≤ V _{CM} ≤ (V _{DD} - 0.3V)		50	70		
		V _{DD} = 3.3V, V _{SS} ≤ V _{CM} ≤ (V _{DD} - 0.2V)		56	76		
Power-Supply Rejection Ratio	PSRR	1.4V ≤ V _{DD} ≤ 3.6V (MAX4036/MAX4038 only)		62	82		dB
		1.8V ≤ V _{DD} ≤ 3.6V		62	84		

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

MAX4036-MAX4039

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +3V$, $V_{SS} = V_{CM} = 0V$, $V_{OUT_} = V_{DD}/2$, R_L to $V_{DD}/2$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_{VOL}	$R_L = 100k\Omega$, $50mV \leq V_{OUT} \leq (V_{DD} - 50mV)$	80	108		dB
		$R_L = 5k\Omega$, $150mV \leq V_{OUT} \leq (V_{DD} - 150mV)$	78	105		
Output Voltage Swing High	$V_{DD} - V_{OH}$	$R_L = 100k\Omega$		2	5	mV
		$R_L = 5k\Omega$		25	50	
Output Voltage Swing Low	$V_{OL} - V_{SS}$	$R_L = 100k\Omega$		2	5	mV
		$R_L = 5k\Omega$		25	50	
Output Short-Circuit Current	I_{SCO}	To V_{DD} or V_{SS}		± 13		mA
Gain-Bandwidth Product	GBW			4		kHz
Phase Margin	θ_M			90		Degrees
Slew Rate	SR			4		V/ms
Power-On Time	t_{ON}	(Note 3)		0.25		ms
Input Noise-Voltage Density	e_n	$f = 1kHz$		500		$nV/\sqrt{Hz}$
Capacitive-Load Stability	C_{LOAD}	$A_{VCL} = 1V/V$, no sustained oscillations		5000		pF
REFERENCE (MAX4037/MAX4039)						
Reference Voltage	V_{REF}		1.226	1.232	1.238	V
Line Regulation	$\Delta V_{REF}/\Delta V_{DD}$	$V_{DD} = +1.8V$ to $+3.6V$			0.3	%/V
Load Regulation	$\Delta V_{REF}/\Delta I_{LOAD}$	$0 \leq I_{LOAD} \leq 100\mu A$, sourcing			0.0015	%/μA
		$-20\mu A \leq I_{LOAD} \leq 0$, sinking			0.0075	
Reference Output Voltage Noise	e_n	0.1Hz to 10Hz		60		μV_{P-P}
Output Short-Circuit Current	I_{SCR}	Short to V_{DD}		0.25		mA
		Short to V_{SS}		1.9		
Capacitive-Load Stability Range	C_{LOAD}	(Note 1)	0		250	pF

ELECTRICAL CHARACTERISTICS

($V_{DD} = +3V$, $V_{SS} = V_{CM} = 0V$, $V_{OUT_} = V_{DD}/2$, R_L to $V_{DD}/2$, $C_L = 15pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	MAX4036/MAX4038, guaranteed by PSRR test	1.4		3.6	V
		MAX4037/MAX4039, guaranteed by PSRR and line regulation tests	1.8		3.6	
Supply Current	I_{DD}	MAX4036	$V_{DD} = 1.4V$		1.7	μA
			$V_{DD} = 3.6V$		1.8	
		MAX4036A	$V_{DD} = 1.4V$		2.0	
			$V_{DD} = 3.6V$		2.1	
		MAX4037	$V_{DD} = 1.8V$		3.1	
			$V_{DD} = 3.6V$		3.2	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{SS} = V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L to V_{DD}/2, C_L = 15pF, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I _{DD}	MAX4038	V _{DD} = 1.4V			2.9	μA
			V _{DD} = 3.6V			3.2	
		MAX4038A	V _{DD} = 1.4V			3.4	
			V _{DD} = 3.6V			3.7	
		MAX4039	V _{DD} = 1.8V			5.2	
			V _{DD} = 3.6V			5.3	
OPERATIONAL AMPLIFIERS							
Input Offset Voltage	V _{OS}					±8	mV
Input Offset Voltage Temperature Coefficient	TCV _{OS}					±1	μV/°C
Input Bias Current	I _B					±100	pA
Input Offset Current	I _{OS}					±200	pA
Input Common-Mode Voltage Range	V _{CM}	Guaranteed by CMRR test	V _{DD} = 1.4V (MAX4036/MAX4038 only)	V _{SS}		V _{DD} - 0.4	V
			V _{DD} = 1.8V	V _{SS}		V _{DD} - 0.4	
			V _{DD} = 3.3V	V _{SS}		V _{DD} - 0.2	
Common-Mode Rejection Ratio	CMRR	V _{DD} = 1.4V, V _{SS} ≤ V _{CM} ≤ (V _{DD} - 0.5V) (MAX4036/MAX4038 only)		44			dB
		V _{DD} = 1.8V, V _{SS} ≤ V _{CM} ≤ (V _{DD} - 0.4V)		50			
		V _{DD} = 3.3V, V _{SS} ≤ V _{CM} ≤ (V _{DD} - 0.3V)		52			
Power-Supply Rejection Ratio	PSRR	1.4V ≤ V _{DD} ≤ 3.6V (MAX4036/MAX4038 only)		60			dB
		1.8V ≤ V _{DD} ≤ 3.6V		60			
Large-Signal Voltage Gain	A _{VOL}	R _L = 100kΩ, 50mV ≤ V _{OUT} ≤ (V _{DD} - 50mV)		75			dB
		R _L = 5kΩ, 150mV ≤ V _{OUT} ≤ (V _{DD} - 150mV)		73			
Output Voltage Swing High	V _{DD} - V _{OH}	R _L = 100kΩ				10	mV
		R _L = 5kΩ				100	
Output Voltage Swing Low	V _{OL} - V _{SS}	R _L = 100kΩ				10	mV
		R _L = 5kΩ				100	
REFERENCE (MAX4037/MAX4039)							
Reference Voltage Temperature Coefficient	TCV _{REF}	(Note 1)	MAX4037EUT-T, MAX4039ETB, MAX4039EUB	25	120		ppm/°C
			MAX4039EBL-T	35	200		
Line Regulation	ΔV _{REF} / ΔV _{DD}	V _{DD} = 1.8V to 3.6V				0.6	%/V
Load Regulation	ΔV _{REF} / ΔI _{LOAD}	0 ≤ I _{LOAD} ≤ 100μA, sourcing				0.003	%/μA
		-20μA ≤ I _{LOAD} ≤ 0, sinking				0.015	
Capacitive-Load Stability Range	C _{LOAD}	(Note 1)		0		250	pF

Note 1: Guaranteed by design.

Note 2: All devices are production tested at T_A = +25°C. All temperature limits are guaranteed by design.

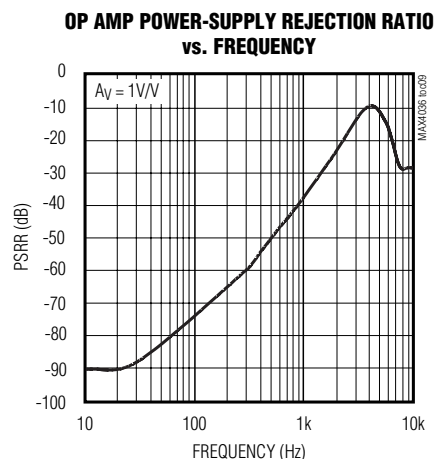
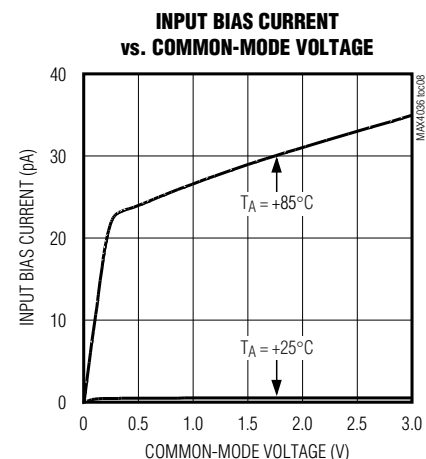
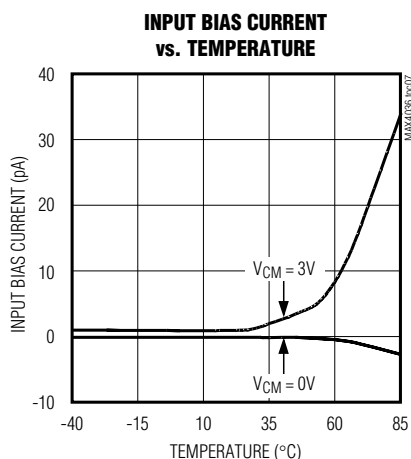
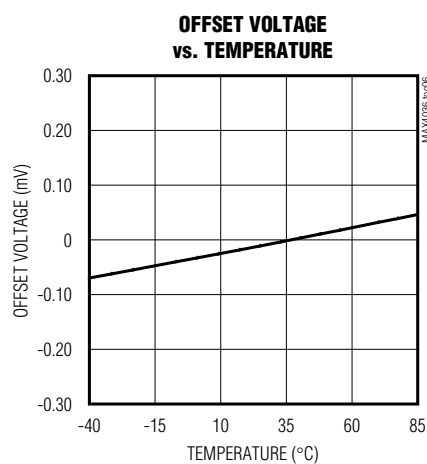
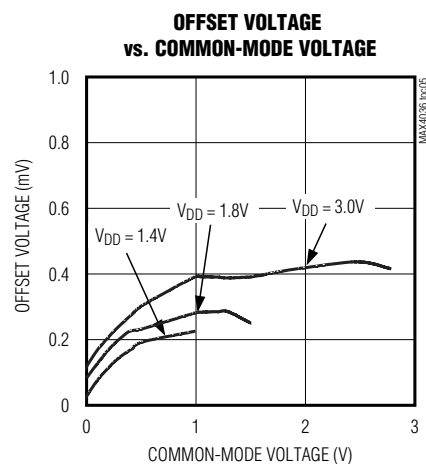
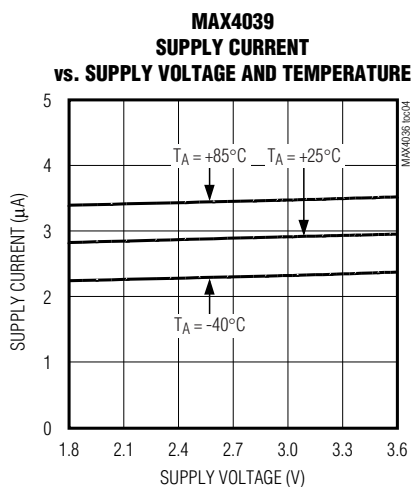
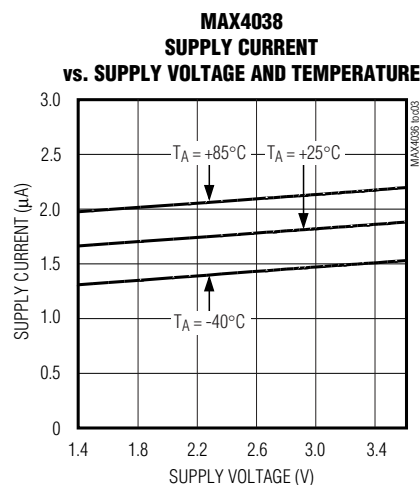
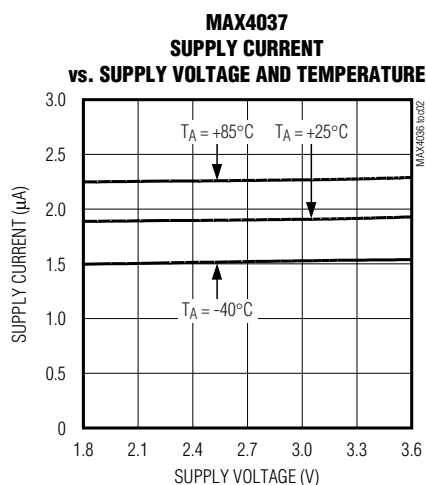
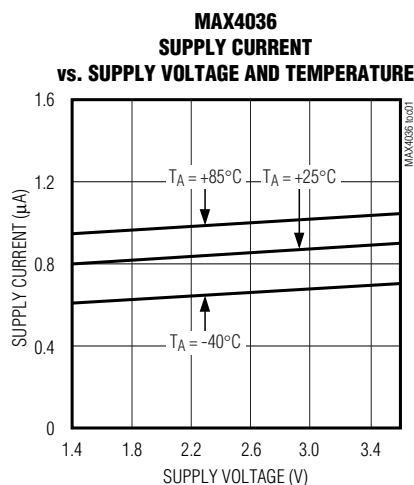
Note 3: Output settles within 1% of final value.

Low I_{BIAS} , +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Typical Operating Characteristics

($V_{DD} = 3V$, $V_{SS} = V_{CM} = 0V$, R_L to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

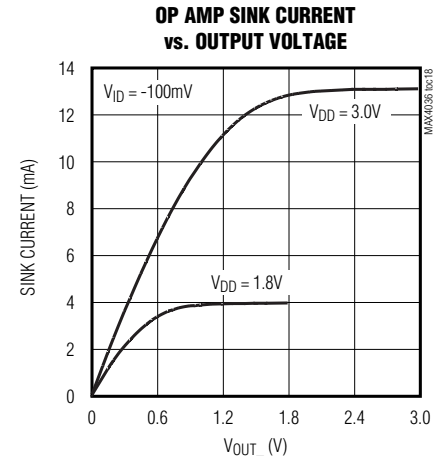
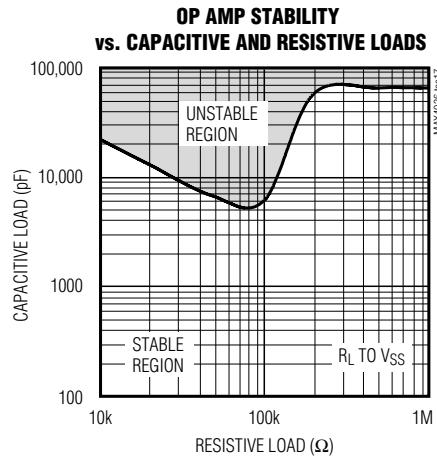
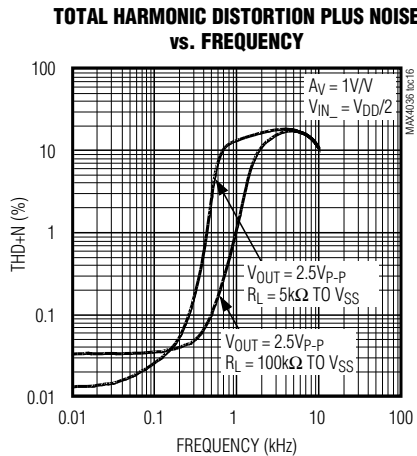
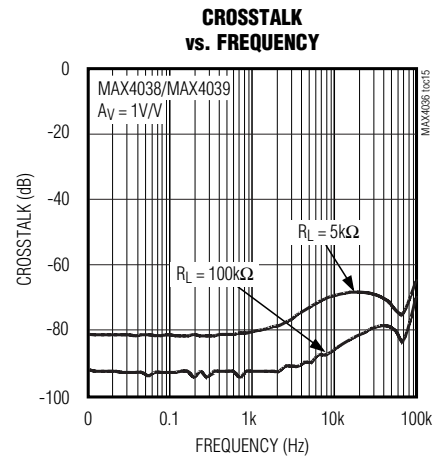
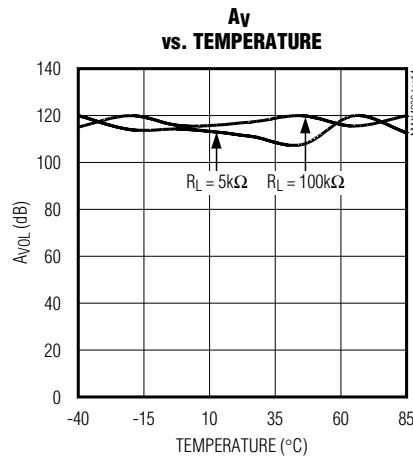
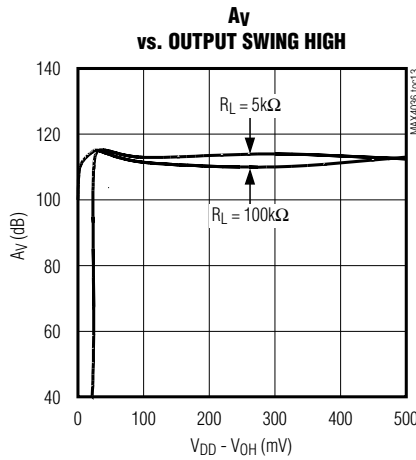
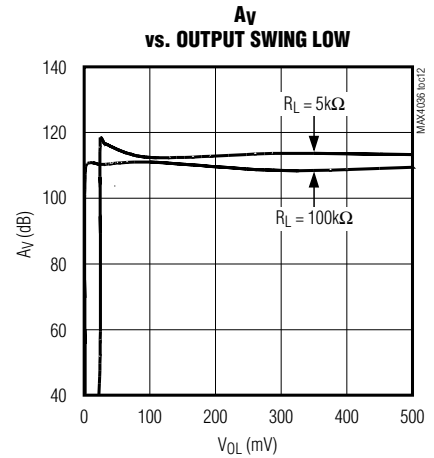
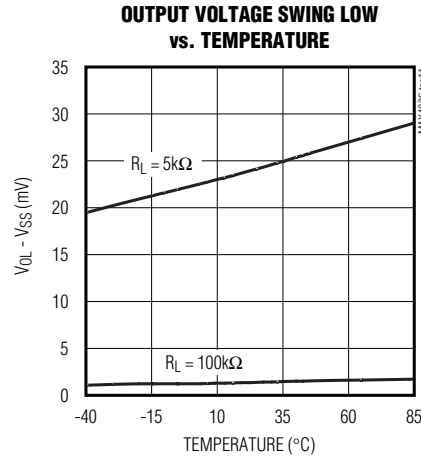
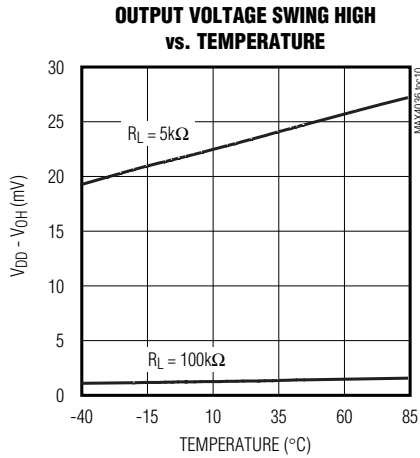
MAX4036-MAX4039



Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Typical Operating Characteristics (continued)

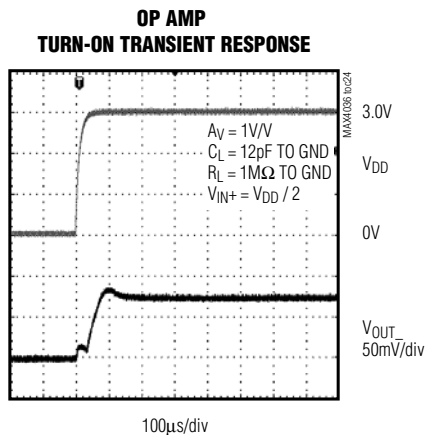
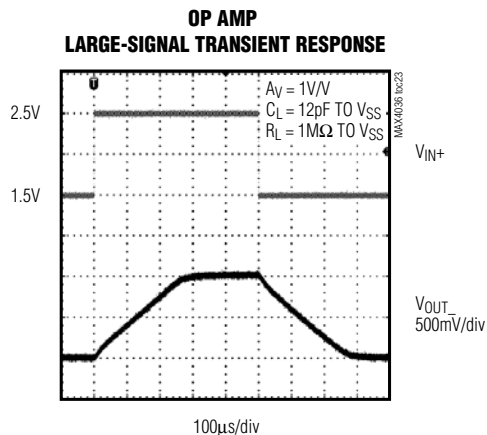
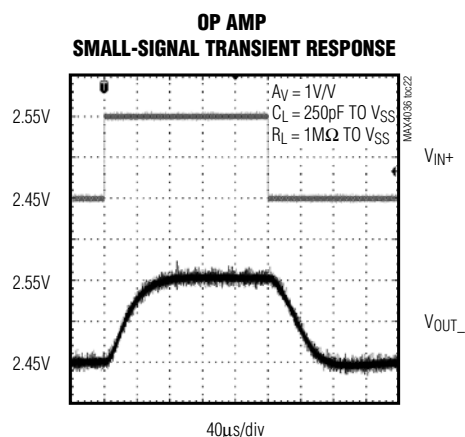
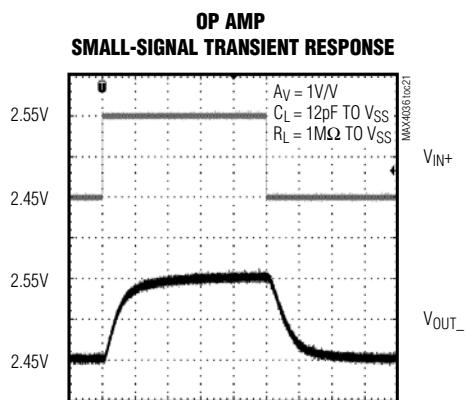
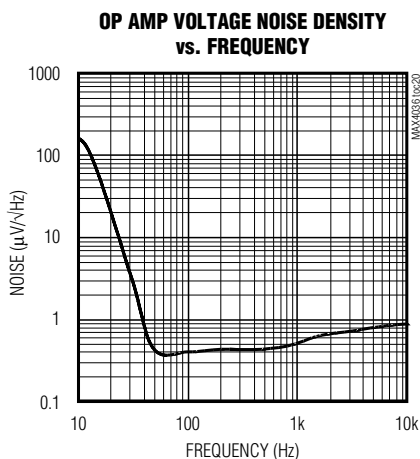
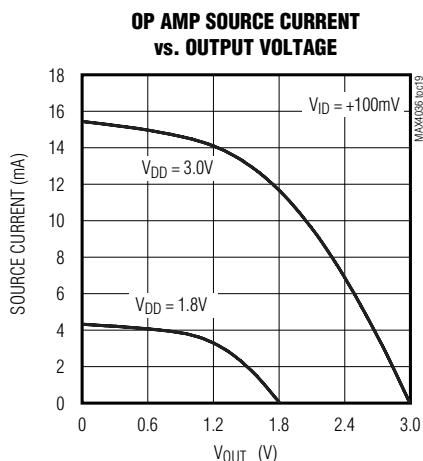
($V_{DD} = 3V$, $V_{SS} = V_{CM} = 0V$, R_L to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



Low I_{BIAS} , +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Typical Operating Characteristics (continued)

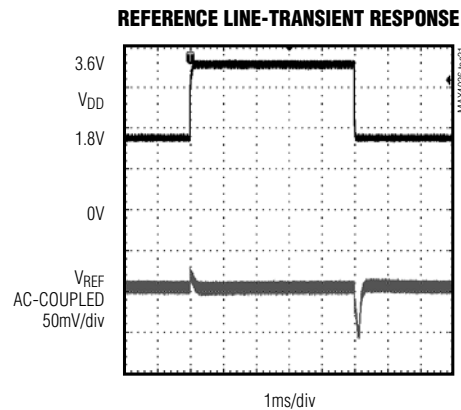
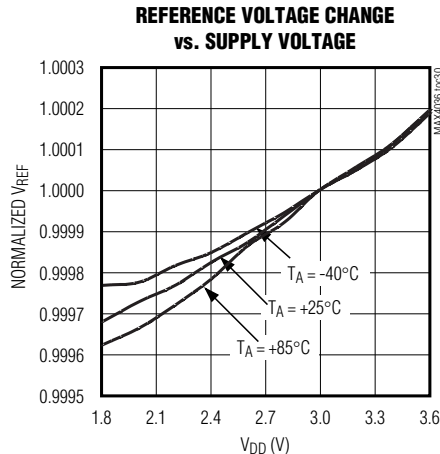
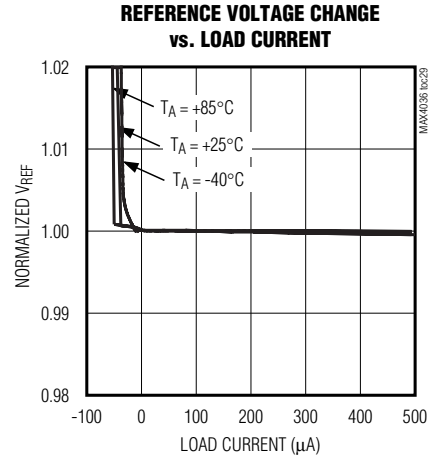
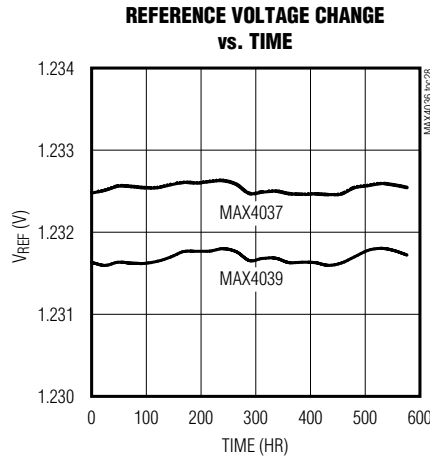
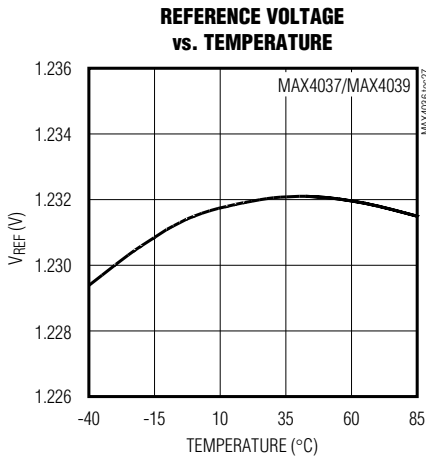
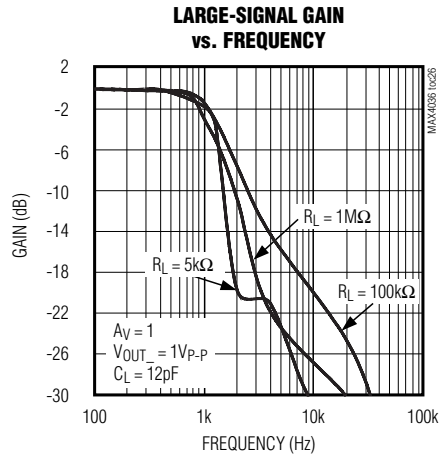
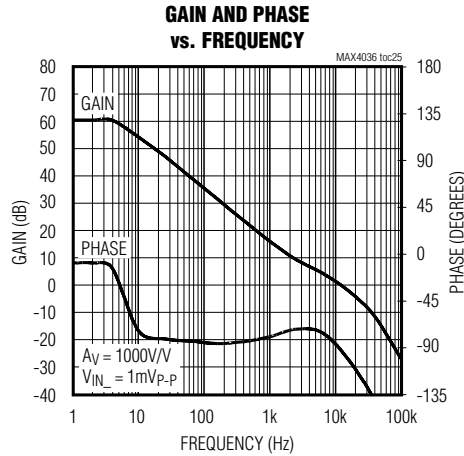
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Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Typical Operating Characteristics (continued)

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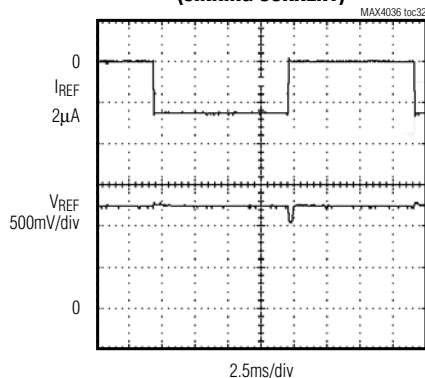


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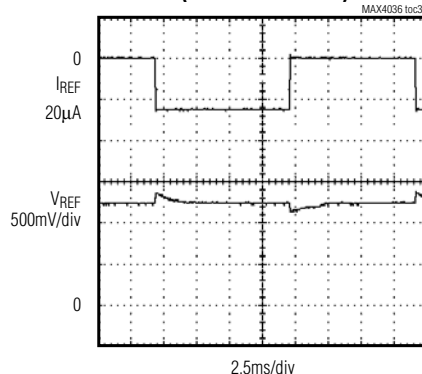
Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $V_{SS} = V_{CM} = 0V$, R_L to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

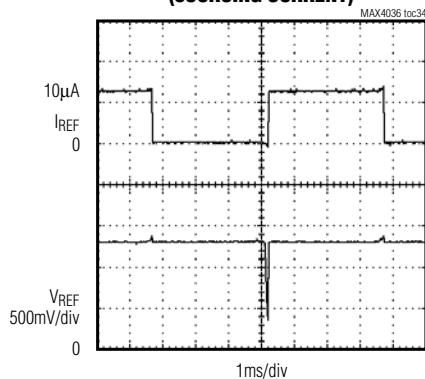
REFERENCE LOAD-TRANSIENT RESPONSE
(SINKING CURRENT)



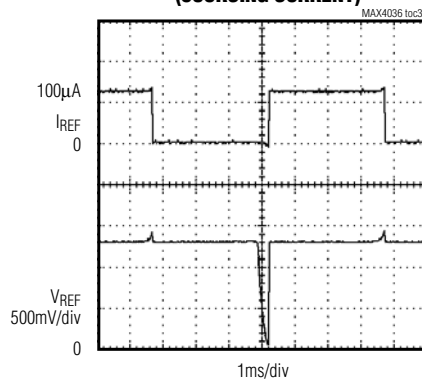
REFERENCE LOAD-TRANSIENT RESPONSE
(SINKING CURRENT)



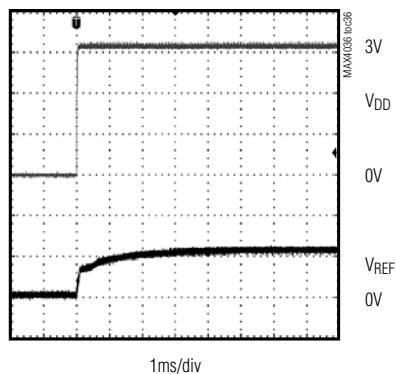
REFERENCE LOAD-TRANSIENT RESPONSE
(SOURCING CURRENT)



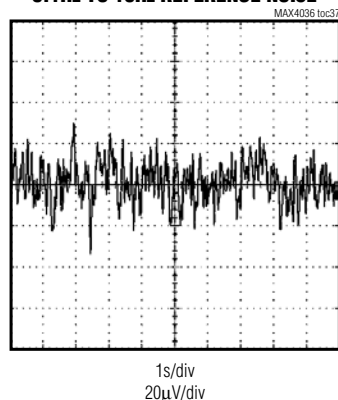
REFERENCE LOAD-TRANSIENT RESPONSE
(SOURCING CURRENT)



REFERENCE TURN-ON
TRANSIENT RESPONSE



0.1Hz TO 10Hz REFERENCE NOISE



Low *I*BIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

PIN						NAME	FUNCTION
MAX4036/ MAX4036A	MAX4037	MAX4038/ MAX4038A		MAX4039			
		μMAX*/TDFN	UCSP	μMAX/TDF	UCSP		
1	3	—	—	—	—	IN+	Noninverting Amplifier Input
2	2	4	A2	5	A2	V _{SS}	Negative Power-Supply Voltage
3	4	—	—	—	—	IN-	Inverting Amplifier Input
4	1	—	—	—	—	OUT	Amplifier Output
5	6	8	C2	10	C2	V _{DD}	Positive Power-Supply Voltage
—	5	—	—	6	B2	REF	Reference Voltage Output
—	—	1	C1	1	C1	OUTA	Amplifier Output (Channel A)
—	—	2	B1	2	B1	INA-	Inverting Amplifier Input (Channel A)
—	—	3	A1	3	A1	INA+	Noninverting Amplifier Input (Channel A)
—	—	5	A3	7	A3	INB+	Noninverting Amplifier Input (Channel B)
—	—	6	B3	8	B3	INB-	Inverting Amplifier Input (Channel B)
—	—	7	C3	9	C3	OUTB	Amplifier Output (Channel B)
—	—	—	B2	4	—	N.C.	No Connection. Not internally connected.
—	—	—	—	—	—	EP (TDFN only)	Exposed Paddle. Solder EP to V _{SS} or leave unconnected (TDFN packages only).

*Both MAX4038/MAX4038A available in μ MAX package only.

Detailed Description

The MAX4036–MAX4039 consume an ultra-low supply current and have rail-to-rail output stages specifically designed for low-voltage operation. The input common-mode voltage range extends from V_{DD} - 0.4V to V_{SS}, although full rail-to-rail input range is possible with degraded performance when operating from a supply voltage above 3.0V. The input offset voltage is typically 200 μ V. Low-operating supply voltage, low supply current, and rail-to-rail outputs make the MAX4036–MAX4039 an excellent choice for precision or general-purpose low-voltage, battery-powered systems.

Rail-to-Rail Outputs

The MAX4036–MAX4039 output stages can drive a 5k Ω load and still swing to within 40mV of the rails. Figure 1 shows the output voltage swing of the MAX4036–MAX4039 configured as a unity-gain buffer, powered from a single 2.4V supply. The output for this setup typically swings from 5mV to V_{DD} - 5mV with a 100k Ω load.

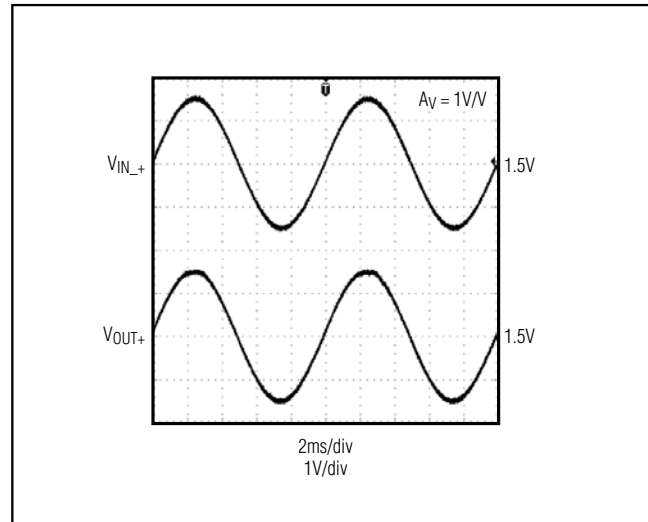


Figure 1. Rail-to-Rail Input/Output Voltage Range

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Applications Information

Power-Supply Considerations

The MAX4036–MAX4039 operate from a single 1.4V (MAX4036/MAX4038) or 1.8V (MAX4037/MAX4039) to 3.6V supply. A high amplifier power-supply rejection ratio of 82dB and the excellent reference line regulation allow the devices to be powered directly from a decaying battery voltage, simplifying design and extending battery life. The MAX4036–MAX4039 are ideally suited for low-voltage battery-powered systems. The *Typical Operating Characteristics* show the changes in supply current and reference output as a function of supply voltage.

Power-Up Settling Time

The MAX4036–MAX4039 typically require 0.25ms to power-up. During this startup time, the output is indeterminate. The application circuit should allow for this initial delay. See the *Typical Operating Characteristics* for amplifier and reference settling time curves.

Driving Capacitive Loads: Op Amps

The MAX4036–MAX4039 amplifier(s) require no output capacitor for stability, and are unity-gain stable for loads up to 5000pF. Applications that require greater capacitive-drive capability should use an isolation resistor between the output and the capacitive load (Figure 2). Note that this solution reduces the gain and output voltage swing because R_{ISO} forms a voltage-divider with the load resistor.

Crossover Distortion

The MAX4036–MAX4039 output stages are capable of sourcing and sinking currents with orders of magnitude greater than the stages' quiescent current, which is less than 1 μ A. This ability to drive heavy loads with such a small quiescent current introduces crossover

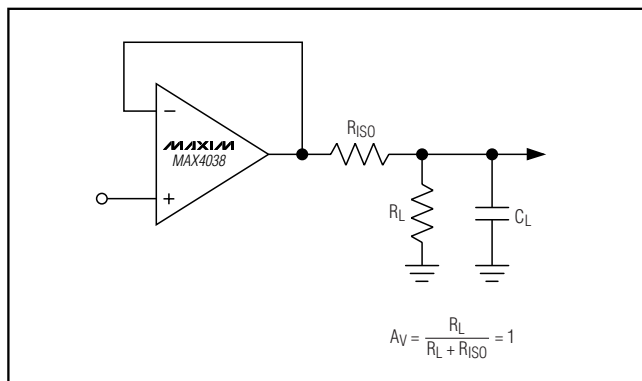


Figure 2. Using a Resistor to Isolate a Capacitive Load from the Op Amp

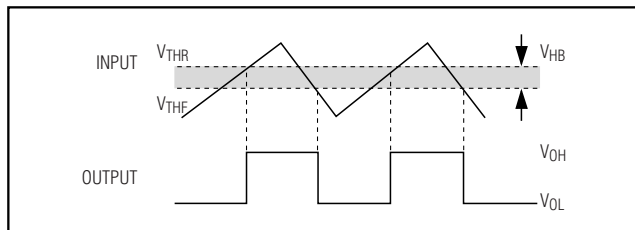


Figure 3. Hysteresis

distortion as the output stage passes between sinking and sourcing. In the crossover regions, the output impedance of the MAX4036–MAX4039 increases substantially, thereby changing the load-driving characteristics. The distortion can be greatly reduced by increasing the load resistance. For applications where low load resistance is required, bias the load such that the output current is always in one direction, to avoid crossover distortion.

Reference Bypassing

The MAX4037/MAX4039 reference requires no external capacitors.

Using the MAX4036–MAX4039 as a Comparator

Although optimized for use as an operational amplifier, the MAX4036–MAX4039 can be used as a rail-to-rail I/O comparator (Figures 3, 4). External hysteresis can be used to minimize the risk of output oscillation. The positive feedback circuit, shown in Figure 4, causes the input threshold to change when the output voltage changes state.

Battery Monitoring Using the MAX4037/MAX4039 and Hysteresis

The internal reference and low operating voltage of the MAX4037/MAX4039 make the devices ideal for battery-monitoring applications. Hysteresis can be set using resistors as shown in Figure 4, and the following design procedure:

- 1) Choose R_3 . The input bias current of IN_- is under 100pA over temperature, so a current through R_3 around 100nA maintains accuracy. The current through R_3 at the trip point is V_{REF} / R_3 , or 100nA for $R_3 = 12M\Omega$. $10M\Omega$ is a good practical value.
- 2) Choose the hysteresis voltage (V_{HB}), the voltage between the upper and lower thresholds. In this example, choose $V_{HB} = 50mV$ (see Figure 3).

Low *IBIAS*, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

- 3) Calculate R1:

$$\begin{aligned} R1 &= R3 \times \frac{V_{HB}}{V_{DD}} \\ &= 10\text{M}\Omega \times \frac{0.5\text{V}}{2.4\text{V}} \\ &= 210\text{k}\Omega \end{aligned}$$

- 4) Choose the threshold voltage for V_{IN} rising (V_{THR}). In this example, choose $V_{THR} = 2.0\text{V}$.

- 5) Calculate R2:

$$\begin{aligned} R2 &= \frac{1}{\left[\left(\frac{V_{THR}}{V_{REF} \times R1} \right) - \frac{1}{R1} - \frac{1}{R3} \right]} \\ &= \frac{1}{\left[\left(\frac{2.0\text{V}}{1.2\text{V} \times 210\text{k}\Omega} \right) - \frac{1}{210\text{k}\Omega} - \frac{1}{10\text{M}\Omega} \right]} \\ &= 325\text{k}\Omega \end{aligned}$$

- 6) Verify the threshold voltages with these formulas:
 V_{IN} rising:

$$V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3} \right)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - \left(\frac{R1 \times V_{DD}}{R3} \right)$$

In this application, the MAX4036–MAX4039 supply current will vary, depending on the output state of the comparator.

Power Supplies and Layout

The MAX4036–MAX4039 operate from a single 1.4V (MAX4036/MAX4038) or 1.8V (MAX4037/MAX4039) to 3.6V power supply. Bypass V_{DD} with a 0.1 μF capacitor to ground to minimize noise.

Good layout techniques optimize performance by decreasing the amount of stray capacitance to the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the device.

The exposed paddle (EP) on the TDFN packages of the MAX4038 and MAX4039 is internally connected to the device substrate, V_{SS} . Connect the exposed paddle to V_{SS} or leave EP unconnected. Running traces below the exposed paddle is not recommended.

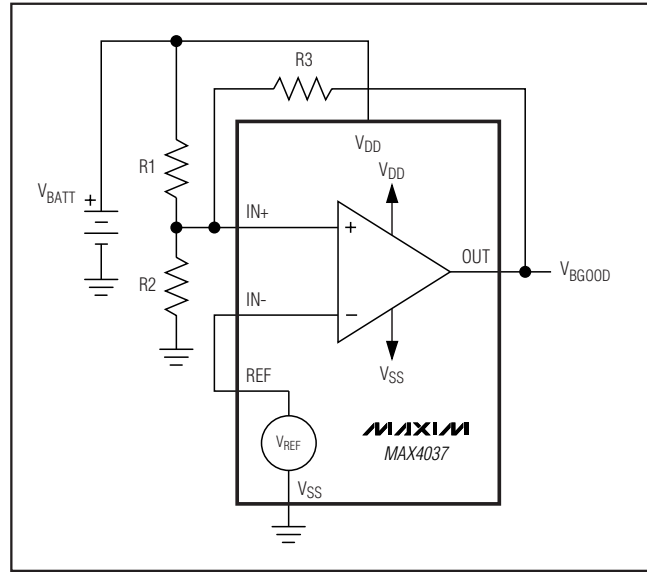


Figure 4. Battery Monitoring

Selector Guide

PART	NO. OF AMPLIFIERS	REFERENCE
MAX4036	1	—
MAX4037	1	✓
MAX4038	2	—
MAX4039	2	✓

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4039EBL-T	-40°C to +85°C	9 UCSP-9	AEH
MAX4039ETB-T	-40°C to +85°C	10 TDFN-EP*	AAN
MAX4039EUB	-40°C to +85°C	10 μMAX	—

*EP = Exposed paddle.

Chip Information

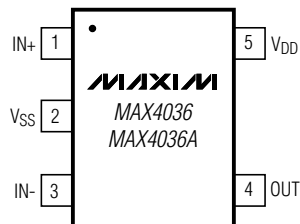
MAX4036 TRANSISTOR COUNT: 49
 MAX4037 TRANSISTOR COUNT: 119
 MAX4038 TRANSISTOR COUNT: 146
 MAX4039 TRANSISTOR COUNT: 146
 PROCESS: BiCMOS

Low *IBIAS*, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

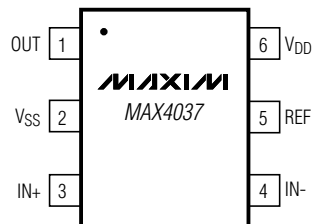
Pin Configurations

MAX4036-MAX4039

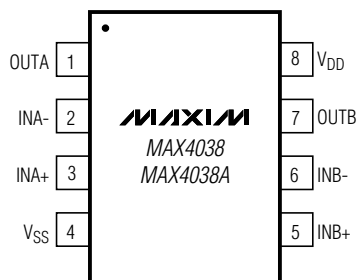
TOP VIEW



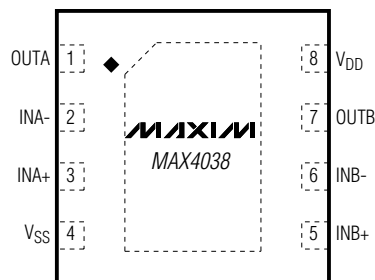
SC70



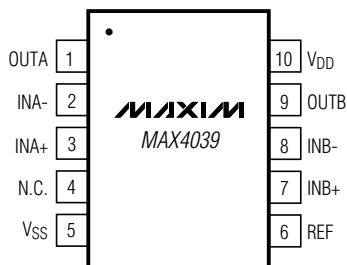
SOT23



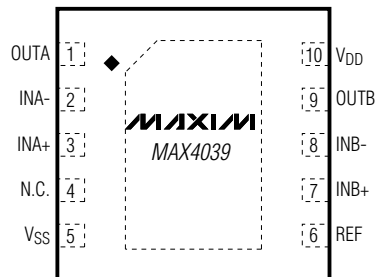
μMAX



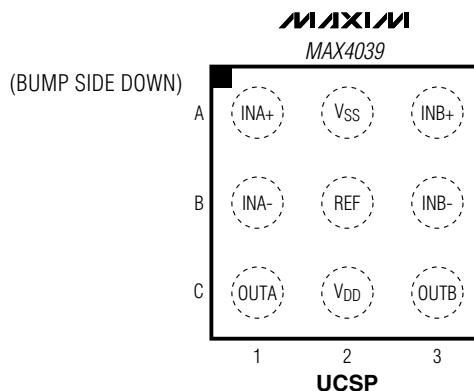
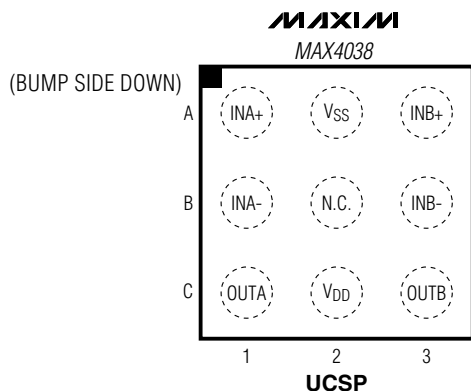
3mm x 3mm x 0.8mm TDFN
TDFN EXPOSED PAD CONNECTED TO VSS.



μMAX



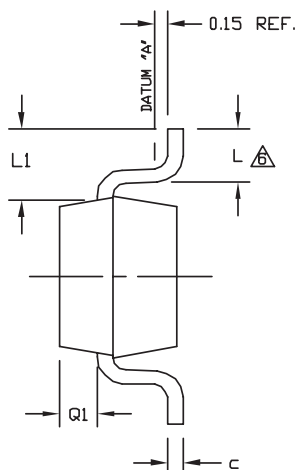
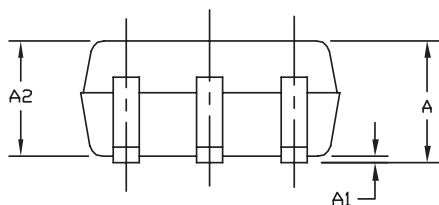
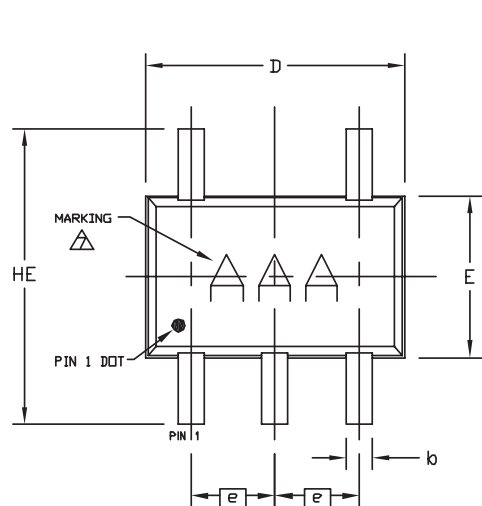
3mm x 3mm x 0.8mm TDFN
TDFN EXPOSED PAD CONNECTED TO VSS.



Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS		
SYMBOL	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.15	0.30
c	0.10	0.18
D	1.80	2.20
e	0.65 BSC.	
E	1.15	1.35
HE	1.80	2.40
L	0.10	0.40
L1	0.425 TYP.	
Q1	0.10	0.40

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO EIAJ SC70 EXCEPT FOR PIN COUNT AND DIMENSION "b".
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ± 0.05 .

-DRAWING NOT TO SCALE-

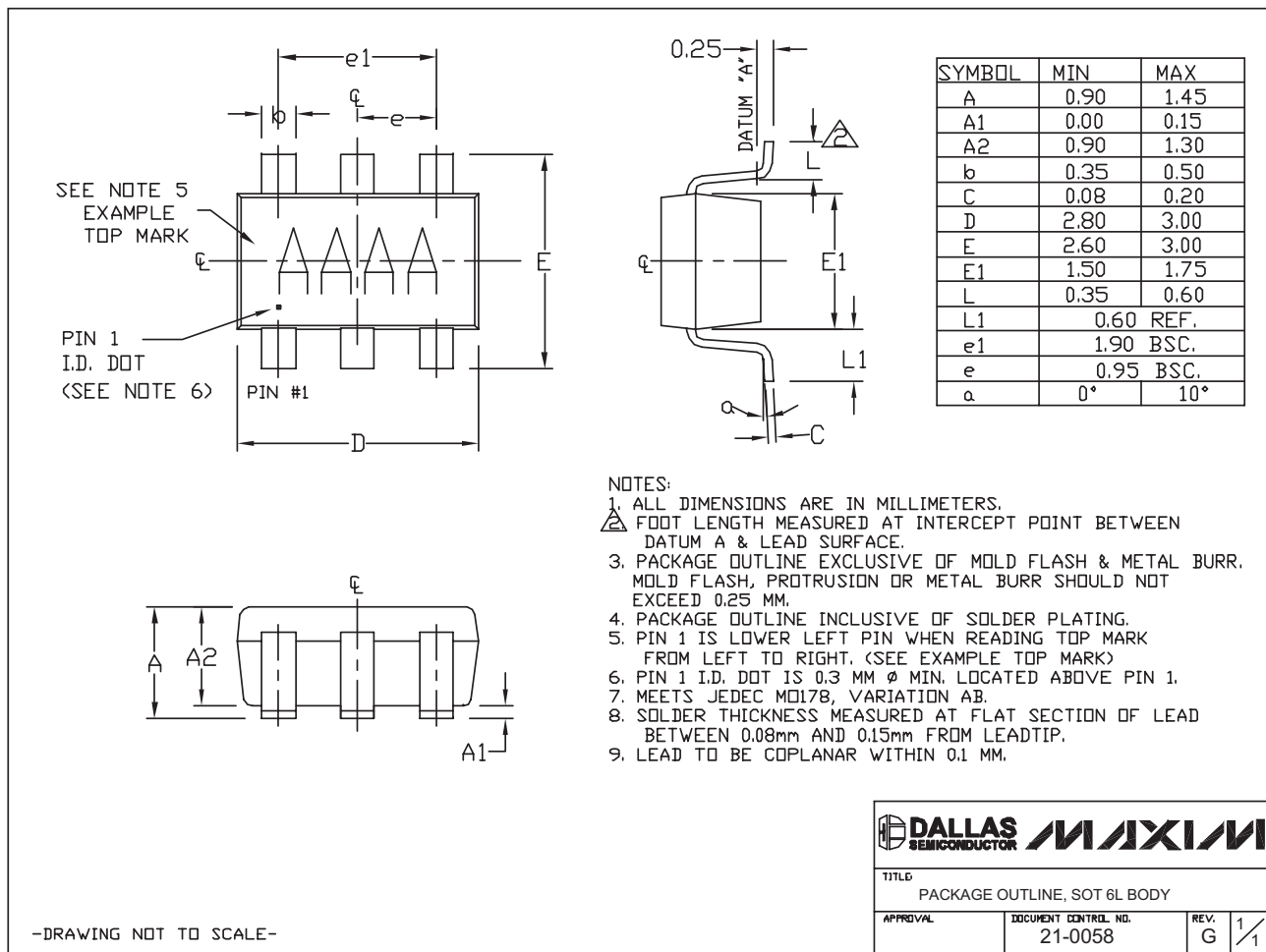
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APPROVAL	DOCUMENT CONTROL NO. 21-0076
REV. C	1/1

SC70, 5LEPS

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



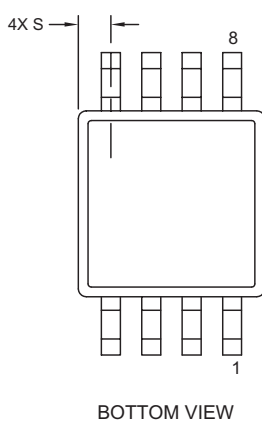
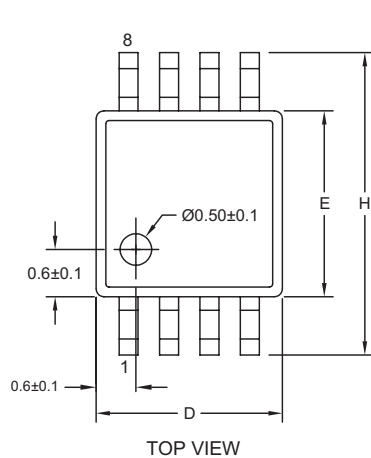
MAX4036-MAX4039

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

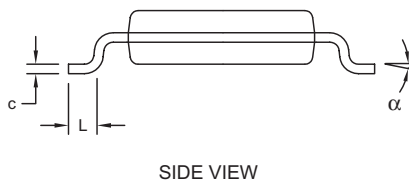
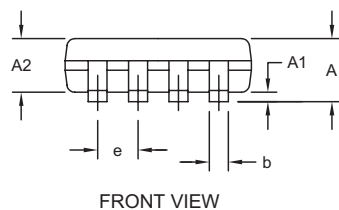
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

8LUMAXD EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	



NOTES:

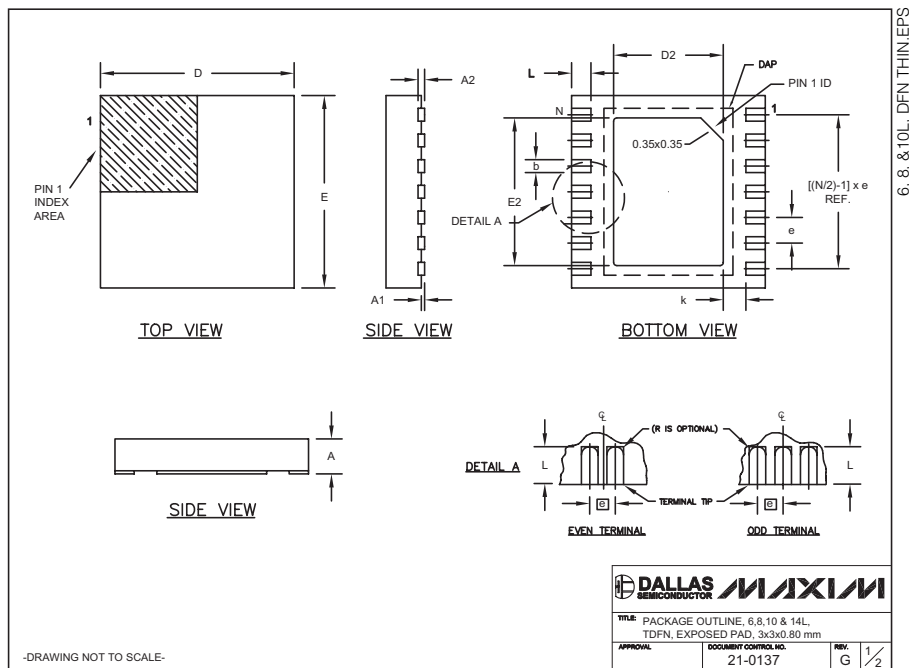
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE:			
PACKAGE OUTLINE, 8L uMAX/uSOP			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0036	J	

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	NO

- NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
 5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
 6. "N" IS THE TOTAL NUMBER OF LEADS.
 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

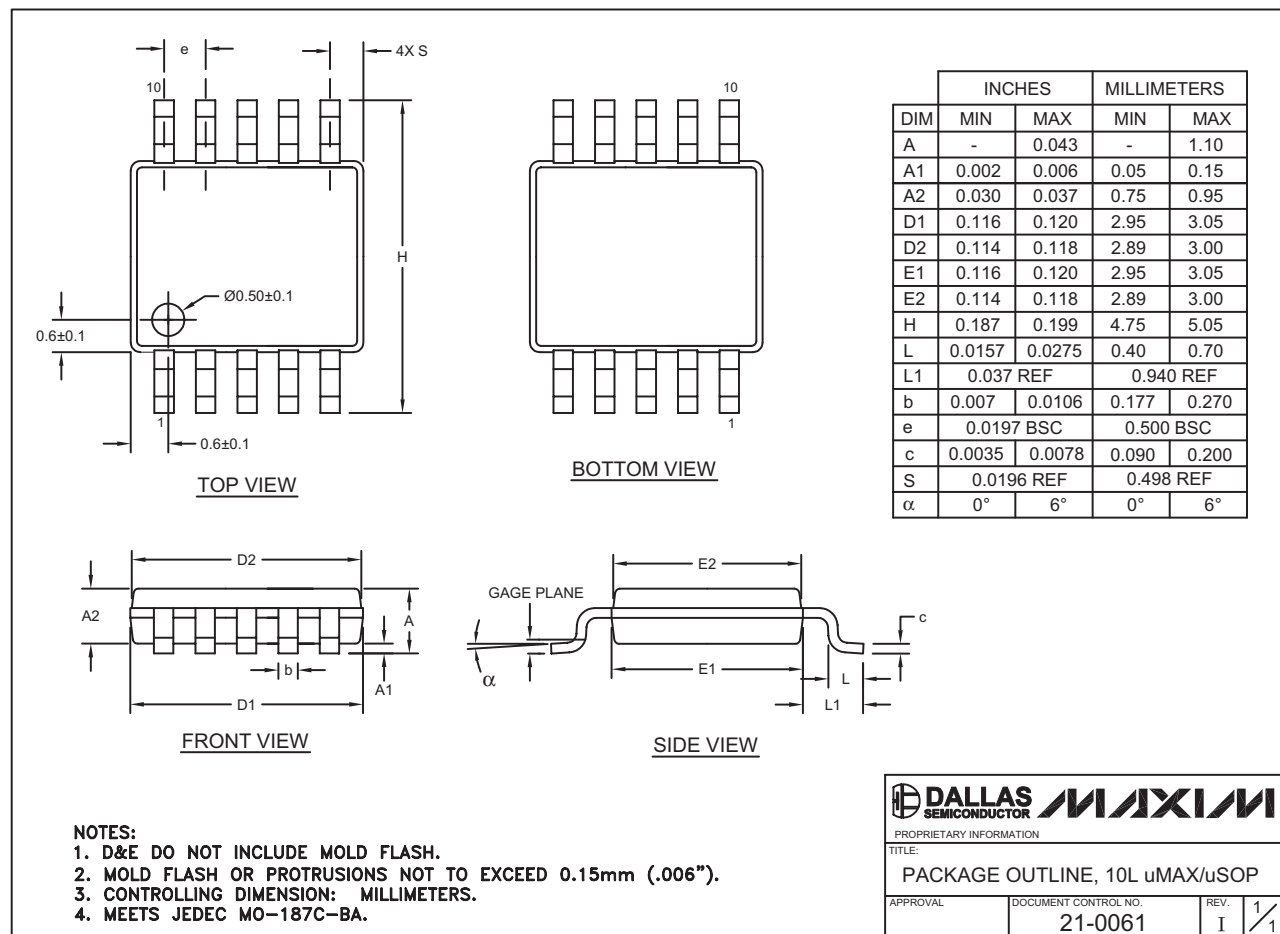
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DALLAS SEMICONDUCTOR MAXIM		
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm		
APPROVAL:	DOCUMENT CONTROL NO. 21-0137	REV: G 2/2

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



10LUMAX.EPS

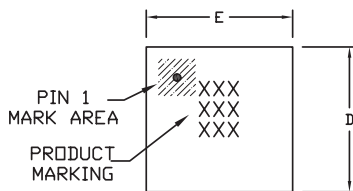
Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information (continued)

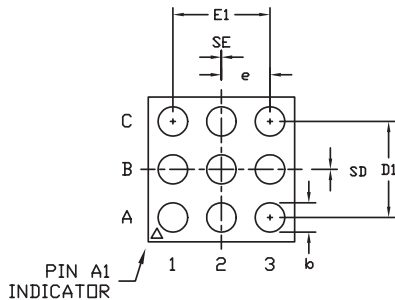
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4036-MAX4039

9LUCSP, 3x3.EPS



TOP VIEW



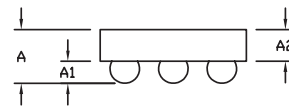
BOTTOM VIEW

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.60±0.05	1.60±0.05	A2, B1, B2, B3, C2

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

-DRAWING NOT TO SCALE-

 DALLAS SEMICONDUCTOR					
TITLE: PACKAGE OUTLINE, 3x3 UCSP					
APPROVAL		DOCUMENT CONTROL NO. 21-0093		REV. J 1/1	

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19