



TFA8200

Mono BTL class-D audio amplifier with digital inputs for IOT applications

Rev. 1 — 19 August 2019

Product data sheet

1 General description

The TFA8200 is a high-efficiency filter-free mono class-D audio amplifier with two separate digital inputs for Internet of things (IOT) applications.

The TFA8200 contains a processor that supports a range of sound processing features including a 5-band parametric equalizer, separate bass and treble control, a dynamic range compressor, soft clip control, and volume control. Excellent audio performance combined with high power supply rejection ratio (PSRR) is achieved by using a closed loop configuration.

Two independent digital audio inputs (I²S-bus/PCM/IOM2) are available for connecting a baseband and a multimedia processor.

The TFA8200 is available in an HVQFN24 package.

2 Features and benefits

2.1 General features

- Closed loop amplifier for:
 - High power supply rejection ratio
 - Excellent audio performance
- Digital input for high RF immunity
- High efficiency for maximizing battery life
- Wide supply voltage range (fully operational from 2.5 V to 5.5 V)
- Delivers high output power into 4 Ω and 8 Ω load impedances
- Phase-locked loop (PLL); no system clock required
- Protection including diagnostics via I²C-bus:
 - Overcurrent protection (OCP) to protect against short circuits across the speaker, to the supply line, or to ground
 - Overtemperature protection (OTP)
 - Digital inputs protected with underfrequency protection (UFP), overfrequency protection (OFP), and Invalid bit-clock protection (IBP)
- 'Pop noise' free at power-up/power down, during sample rate switching and when switching between digital inputs
- Four separate I²C-bus addresses for multi-channel applications
- 1.8 V/3.3 V tolerant digital inputs
- Only three external components required



2.2 Programmable digital sound processor (DSP)

- Digital volume control (–70 dB to +24 dB)
- Digital parametric 5-band equalizer
- Bass and treble control (–18 dB to +18 dB)
- Dynamic range compressor:
 - Programmable attack and release levels
 - Programmable attack and release rates
- Soft and hard mute control
- Programmable DC blocking via high-pass filter
- Power limiter (0 dB to –124 dB in 0.5 dB steps)
- Zero crossing volume control
- Stereo-to-mono down-mix function

2.3 Interface format support for digital audio inputs

- I²S formats ($f_s = 8$ kHz to 96 kHz):
 - Philips standard I²S-bus
 - Japanese I²S-bus MSB-justified
 - Sony I²S-bus LSB-justified
- PCM / IOM2 formats ($f_s = 8$ kHz or $f_s = 16$ kHz):
 - Long frame sync
 - Short frame sync

3 Applications

- Internet of things (IOT) devices
- Notebooks
- Portable gaming devices

4 Quick reference data

Table 1. Quick reference data

All parameters are guaranteed for $V_{DDD} = 1.8\text{ V}$; $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$; $L_L = 44\ \mu\text{H}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; clip control off; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_P	supply current	on pin V_{DDP} ; amplifier mode with load; soft mute on	-	5.7	-	mA
		on pin V_{DDP} ; power-down mode	-	-	20	μA
I_{DDD}	digital supply current	on pin V_{DDD} ; amplifier mode	-	1.2	-	mA
		on pin V_{DDD} ; power-down mode	[1] -	5	15	μA
$P_{o(RMS)}$	RMS output power	$R_L = 8\ \Omega$				
		THD+N = 1 %	0.65	0.7	-	W
		THD+N = 10 %	-	0.85	-	W
		$R_L = 4\ \Omega$				
		THD+N = 1 %	-	1.2	-	W
		THD+N = 10 %	-	1.5	-	W
		$R_L = 8\ \Omega$; $V_{DDP} = 4.2\text{ V}$				
		THD+N = 1 %	-	0.9	-	W
		THD+N = 10 %	-	1.1	-	W
		$R_L = 4\ \Omega$; $V_{DDP} = 4.2\text{ V}$				
		THD+N = 1 %	-	1.6	-	W
		THD+N = 10 %	-	1.95	-	W
		$R_L = 8\ \Omega$; $V_{DDP} = 5.0\text{ V}$				
		THD+N = 1 %	-	1.35	-	W
		THD+N = 10 %	-	1.6	-	W
		$R_L = 4\ \Omega$; $V_{DDP} = 5.0\text{ V}$				
		THD+N = 1 %	-	2.35	-	W
		THD + N = 10 %	-	2.75	-	W
η_{po}	output power efficiency	$P_{o(RMS)} = 850\text{ mW}$	-	92	-	%

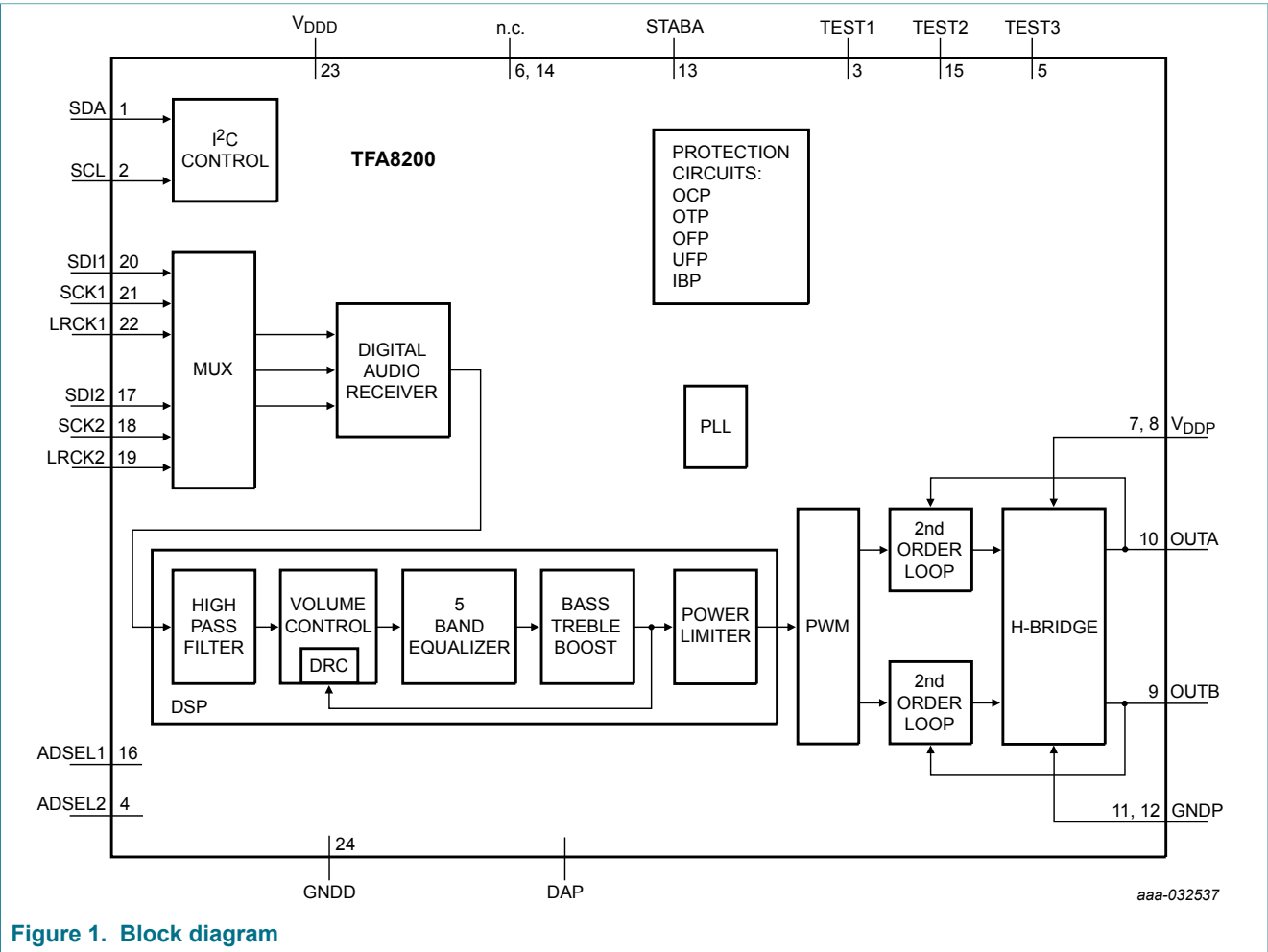
[1] After switching from off/amplifier mode to power-down mode.

5 Ordering information

Table 2. Ordering information

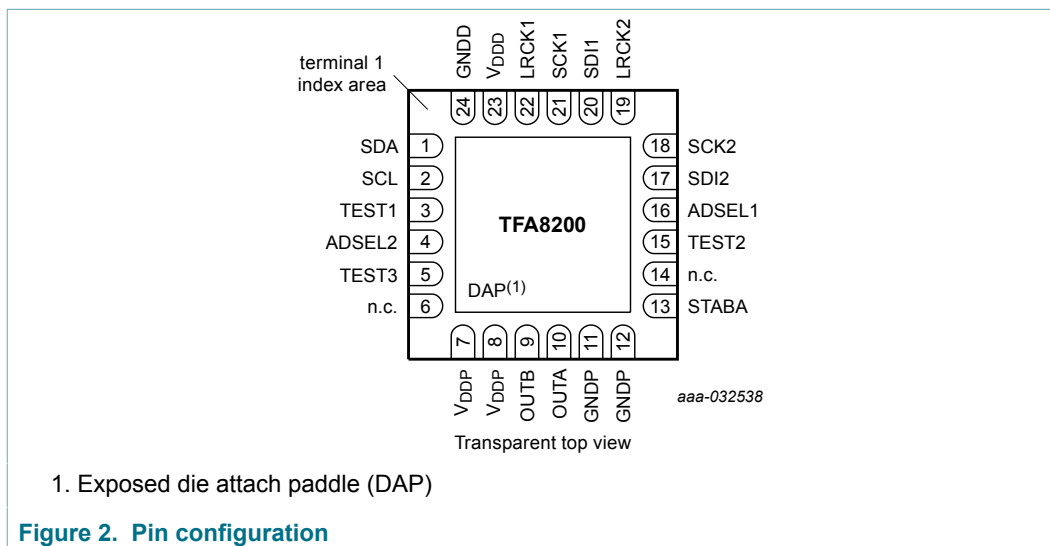
Type number	Package		Version
	Name	Description	
TFA8200HN	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616_3

6 Block diagram



7 Pinning information

7.1 Pinning



7.2 Pin description

Table 3. Pin description

Symbol	Pin	Pin Type	Description
SDA	1	IO	I ² C-bus data input/output
SCL	2	I	I ² C-bus bit clock input
TEST1	3	I	test signal input 1; for test purposes only; connect to PCB ground
ADSEL2	4	I	address selection input 2
TEST3	5	I	test signal input 3; for test purposes only; connect to PCB ground
n.c.	6	-	not connected; connect to PCB ground
V _{DDP}	7, 8	P	analog supply voltage (2.5 V to 5.5 V)
OUTB	9	O	output B (negative)
OUTA	10	O	output A (positive)
GNDP	11, 12	P	analog ground, PCB ground reference
STABA	13	O	1.8 V analog stabilizer output
n.c.	14	-	not connected; connect to PCB ground
TEST2	15	I	test signal input 2; for test purposes only; connect to PCB ground
ADSEL1	16	I	address selection input 1
SDI2	17	I	digital audio data input 2
SCK2	18	I	digital audio bit clock input 2
LRCK2	19	I	digital audio word select input 2
SDI1	20	I	digital audio data input 1

Symbol	Pin	Pin Type	Description
SCK1	21	I	digital audio bit clock input 1
LRCK1	22	I	digital audio word select input 1
V _{DDD}	23	P	digital supply voltage (1.8 V)
GNDD	24	P	digital ground, PCB ground reference
DAP	-	P	exposed Die Attached Paddle (DAP); connect to PCB ground

8 Functional description

The TFA8200 is a high-efficiency mono bridge tied load (BTL) class-D amplifier with digital audio inputs. It supports all commonly used formats.

The key functional blocks of the TFA8200 are shown in [Figure 1](#). In the digital domain, the audio signal is processed and converted into a pulse width modulated (PWM) signal using a 3-level modulation. In the analog domain, the PWM signal is amplified using a second order feedback loop.

The audio signal-processing path is described below:

1. The MUX selects the serial interface input to be used.
2. The digital audio receiver translates the serial input signal into a standard internal mono audio stream.
3. The programmable high-pass filter blocks DC signals and low frequency signals.
4. The volume control provides gain and attenuation functionality. The user can adjust it or it can be adjusted dynamically via the dynamic range compressor (DRC). The volume control can be used to adjust the signal level between -70 dB and +24 dB.
5. The 5-band parametric equalizer can be used to equalize the mono audio stream. It can be used for speaker transfer curve compensation to optimize the audio performance of the speakers.
6. The bass and treble boost function provides another way to adjust the sound.
7. The power limiter limits the maximum output signal of the TFA8200. The power limiter settings are 0 dB to -124 dB in steps of 0.5 dB. This function can be used to limit the maximum output power delivered to the speakers at a fixed supply voltage and speaker impedance.
8. The PWM controller block converts the audio signal into a 3-level modulated PWM signal. The 3-level modulation provides a high signal-to-noise performance and eliminates clock jitter noise.
9. The second-order feedback loop ensures excellent audio performance and high power supply rejection ratio.
10. The H-BRIDGE allows the TFA8200 to deliver the required output power between terminals OUTA and OUTB.

The internal clocks of the TFA8200 are derived from the digital audio interface (SCK1 and SCK2) using a PLL. The reference input for the PLL is selected via the digital input MUX.

The audio signal path can be selected via the I²C-bus interface.

The PLL block generates the system clock.

The following protection circuits are built into the TFA8200:

- Overtemperature protection (OTP)
- Overcurrent protection (OCP)
- Underfrequency protection (UFP)
- Overfrequency protection (OFP)
- Invalid bit-clock protection (IBP)
- DC-blocking

8.1 Operating modes

The TFA8200 supports the following operating modes, which are controlled via the I²C-bus interface:

- **Power-down mode**, used to switch off the device; current consumption is reduced to a minimum; the I²C-bus remains operational; the PWM outputs are disabled.
- **Off mode**, in which the class-D amplifier is switched off; the TFA8200 is completely biased and the PWM outputs are disabled.
- **Amplifier mode**, in which the digital inputs are used to generate a signal between OUTA and OUTB.

The TFA8200 device control settings are detailed in [Table 21](#).

8.1.1 Power-up/power-down

The power-up and power-down timing of the TFA8200 is illustrated in [Figure 3](#). Before the operating mode is selected, the external power supply levels, V_{DDP} and V_{DDD}, must be within the specified operating ranges. Before the operating mode can be selected via bits OPMODE, bit POWERUP in the device control register ([Table 21](#)) must be set to 1. After the turn-on delay ($t_{d(on)}$), the device automatically generates a soft unmute function. When OPMODE is set to 0, a soft mute function is generated. The TFA8200 must be set to power-down mode before the power supplies are disconnected or turned off.

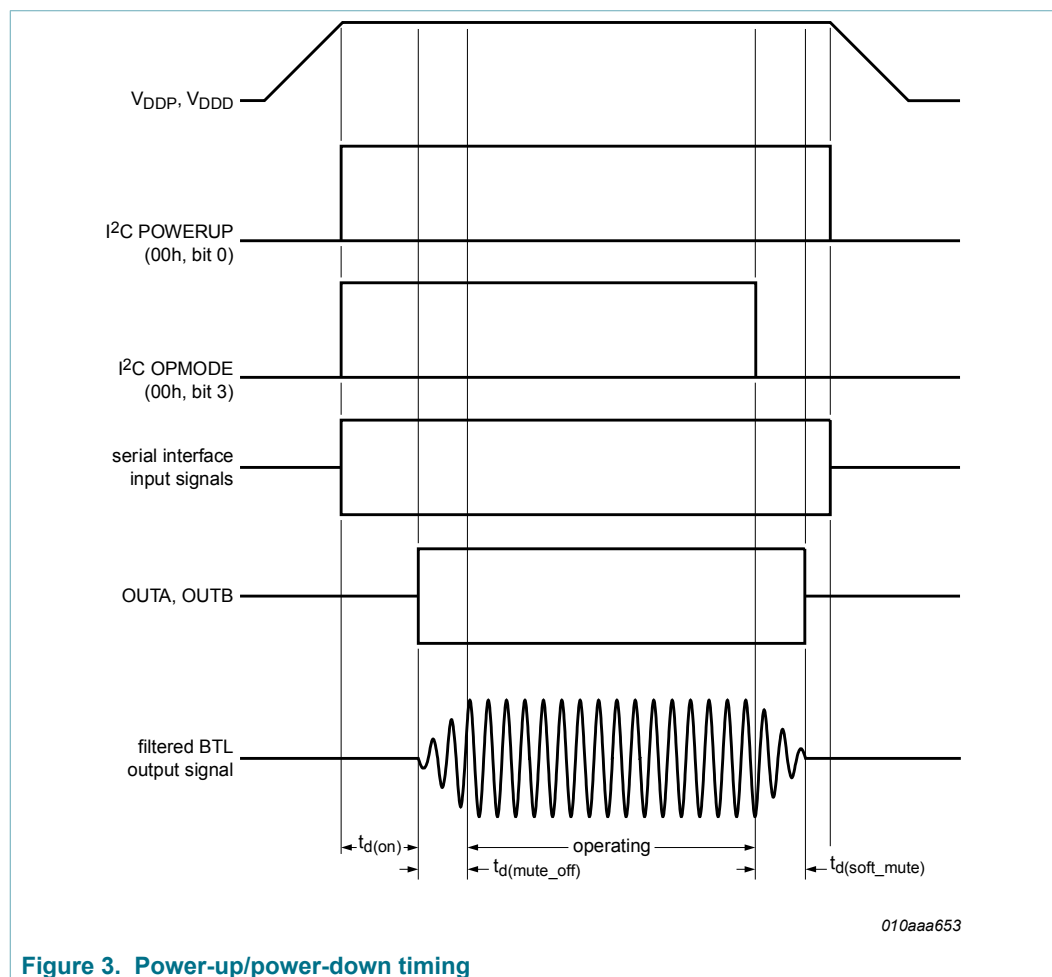


Figure 3. Power-up/power-down timing

8.1.2 Supported digital audio data formats

The TFA8200 supports a commonly used range of I²S, PCM, and IOM2 digital audio data formats. The I²S formats, selected via bits I2S_SET in the serial interface control register (Table 22), are listed in Table 4. The PCM/IOM2 formats are listed in Table 5. The TFA8200 automatically detects the number of slots by measuring the ratio between the sync frequency (8 kHz) and the data clock. Table 24 details the I²C settings for the PCM/IOM2 formats.

Table 4. I²S-supported digital audio data formats

SCK frequency	Interface format (MSB first)	Supported data format
32 f _s	I ² S (Philips) standard	up to 16-bit data
32 f _s	MSB-justified	up to 16-bit data
32 f _s	LSB-justified - 16 bits	16-bit data
64 f _s	I ² S (Philips) standard	up to 24-bit data
64 f _s	MSB-justified	up to 24-bit data
64 f _s	LSB-justified - 16 bits	16-bit data
64 f _s	LSB-justified - 18 bits	18-bit data
64 f _s	LSB-justified - 20 bits	20-bit data
64 f _s	LSB-justified - 24 bits	24-bit data

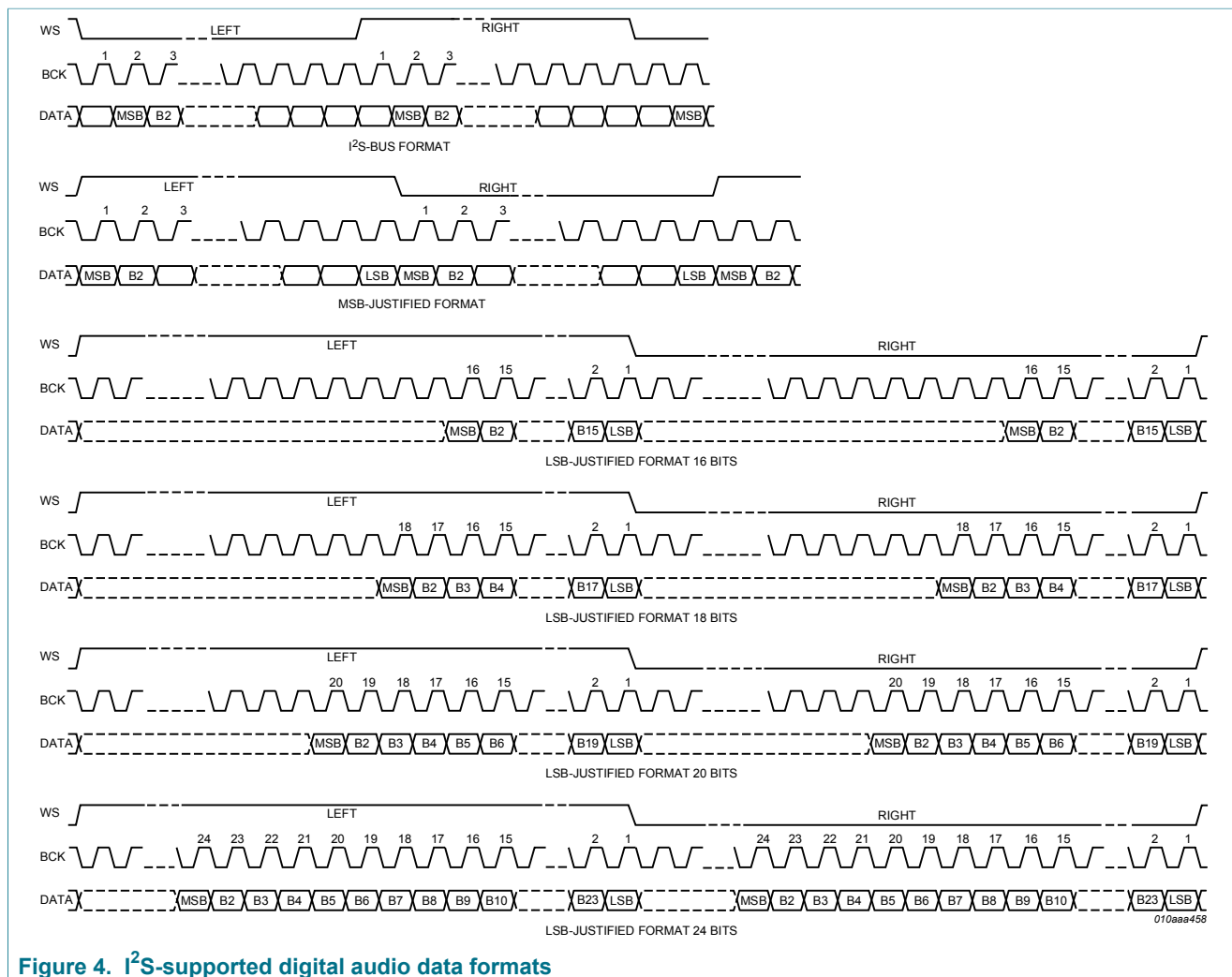
Figure 4. I²S-supported digital audio data formats

Table 5. PCM/IOM2-supported audio data formats

Number of slots	f _s (kHz)	Sync frequency (kHz) on LRCK pin	Supported data formats	Data clock (kHz) on SCK pin
2	8 or 16	8	8-bit data	128
2	8 or 16	8	8-bit data	128
4	8 or 16	8	8-bit data	256
4	8 or 16	8	8-bit data	256
6	8 or 16	8	8-bit data	384
8	8 or 16	8	8-bit data	512
12	8 or 16	8	8-bit data	768
16	8 or 16	8	8-bit data	1024
reserved				
2	8 or 16	8	16-bit data	256

Number of slots	f_s (kHz)	Sync frequency (kHz) on LRCK pin	Supported data formats	Data clock (kHz) on SCK pin
3	8 or 16	8	16-bit data	384
4	8 or 16	8	16-bit data	512
6	8 or 16	8	16-bit data	768
8	8 or 16	8	16-bit data	1024
12	8 or 16	8	16-bit data	1536
12	8 or 16	8	16-bit data	1536

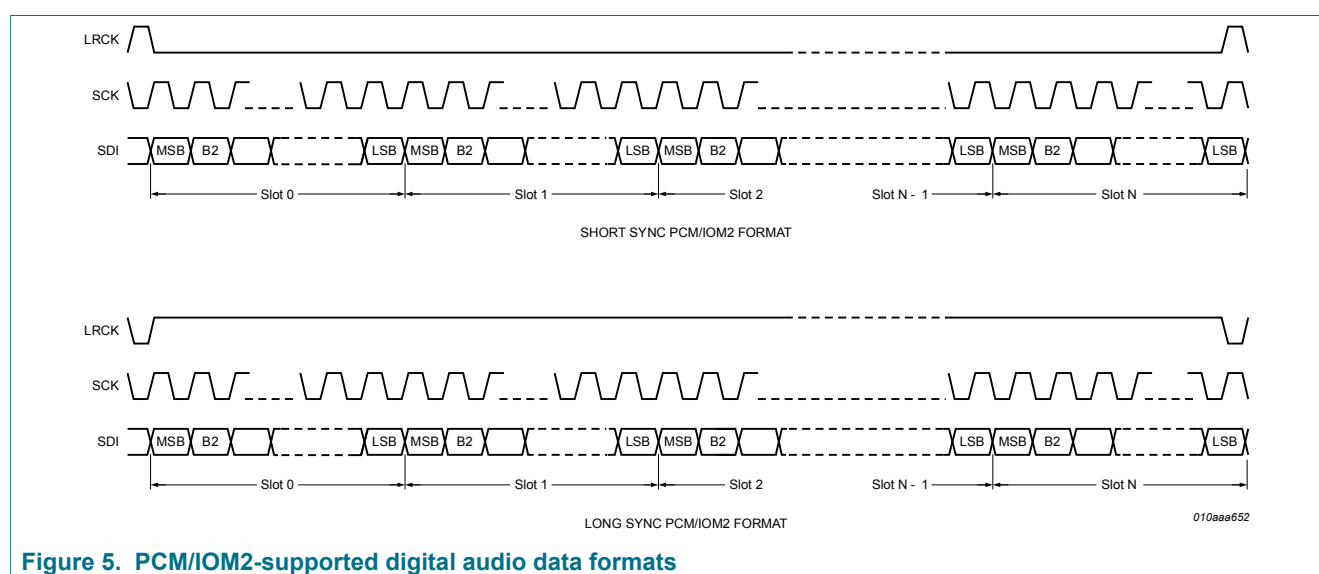


Figure 5. PCM/IOM2-supported digital audio data formats

8.2 Digital signal processor (DSP) features

8.2.1 Serial interface selection

The TFA8200 contains two serial interfaces. The active interface is selected via bit `INPUT_SEL` in the device control register (see [Table 21](#)). When this bit is toggled, the following sequence is initiated:

- Soft mute is activated for $128/f_s$ seconds
- The TFA8200 switches to off mode and the serial interface input is toggled
- The TFA8200 switches back to operating mode and soft mute is released

8.2.2 Mono selection

Mono selection is used to select the digital audio input channel to be amplified. The options are:

- Left channel
- Right channel
- Left + right channels (sum divided by two)

Separate mono selection is provided for the two serial interfaces via bits MONO_SEL in the serial interface control registers (addresses 01h and 03h; see [Table 22](#)).

8.2.3 Programmable high-pass filter

To block DC and low frequency signals, the TFA8200 features a first-order high-pass filter on the digital audio input. DC values at the output can damage the speaker.

The high-pass filter cut-off frequency is determined by:

- The high-pass filter control setting (bits HP_CTRL, see [Table 30](#))
- The sample frequency, f_s

The relationship between these parameters and the cut-off frequency is defined in [Equation 1](#):

$$f_{high(-3dB)} = \frac{-f_s \times \ln\left(\frac{4096-HP_CTRL}{4096}\right)}{2\pi} \quad (1)$$

HP_CTRL can be programmed to any integer value between 0 and 511 (see [Table 30](#)). If HP_CTRL = 0 or bit HPF_BP in the bypass control register is set to 1 (see [Table 27](#)), the high-pass filter is bypassed.

8.2.4 De-emphasis

Digital de-emphasis is sometimes required. To achieve good SNR over the complete audio band, the high frequency components of the audio signal were amplified prior to transmission (= emphasis).

The de-emphasis filter is a simple first order filter. The cut-off frequency of the de-emphasis low-pass filter is approximately 3.5 kHz. The TFA8200 de-emphasis filter is supported for four sample frequencies, as detailed in [Table 6](#).

Table 6. De-emphasis control

[1:0] Control value ^[1]	f_s (kHz)
00 ^[2]	de-emphasis inactive
01	32
10	44.1
11	48

[1] Value selected via bits DE_PHAS in the de-emphasis, soft/hard mute and power limiter control register (see [Table 32](#)).

[2] Default value.

8.2.5 Equalizer

The equalizer can be used for speaker curve compensation or for customer equalizer settings, such as jazz, pop, rock, or classical music. The equalizer function can be bypassed or configured as 5-band.

8.2.5.1 Equalizer band function

The following three filter parameters determine the shape of each parametric equalizer band:

- (Relative) center frequency

$$\omega = 2\pi (f_c / f_s) \quad (2)$$

- Quality factor Q
- Gain factor G

In [Equation 2](#), f_c is the center frequency and f_s is the sample frequency.

The definition of the quality factor is the center frequency divided by the 3 dB bandwidth (see [Equation 3](#)). In parametric equalizers, it is only valid when the gain is set very low (–30 dB).

$$Q = \frac{f_c}{f_2 - f_1}; \quad \begin{array}{ll} f_1: & 20 \log_{10} \left(\frac{Af_1}{Af_c} \right) = 3 \text{ dB}, f_c > f_1 \\ f_2: & 20 \log_{10} \left(\frac{Af_2}{Af_c} \right) = 3 \text{ dB}, f_2 > f_c \end{array} \quad (3)$$

Each band filter can be programmed to perform a band-suppression ($G < 1$) or a band-amplification ($G > 1$) function around the center frequency.

Each band of the TFA8200 equalizer has a second order regalia-mitra all-pass filter structure. The structure is shown in [Figure 6](#).

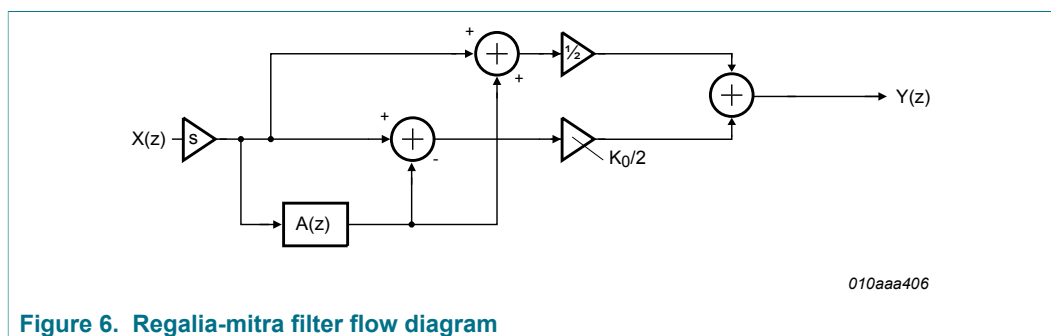


Figure 6. Regalia-mitra filter flow diagram

The transfer function of this all-pass filter is given in [Equation 4](#):

$$H(z) = 1 / 2 \cdot (1 + A(z)) + K_0 / 2 \cdot (1 - A(z)) \quad (4)$$

A(z) is the second-order filter structure. The transfer function of A(z) is given in [Equation 5](#):

$$A(z) = \frac{K_1 K_2 (1 + K_1) z^{-1} z^{-2}}{1 K_2 (1 + K_1) z^{-1} K_1 z^{-2}} \quad (5)$$

z^{-1} equals one f_s delay period. The relationship between the programmable parameters K_0 , K_1 , and K_2 and the filter parameters G , ω , and Q is shown in [Equation 6](#) and [Equation 7](#).

[Equation 6](#) can be used to calculate band suppression ($G < 1$) functions.

$$\left. \begin{aligned} K_0 &= G \\ K_1 &= -\cos \omega \\ K_2 &= (2Q \cdot G - \sin \omega) / (2Q \cdot G + \sin \omega) \end{aligned} \right|_{G < 1} \quad (6)$$

[Equation 7](#) can be used to calculate band amplification ($G \geq 1$) functions.

$$\left. \begin{aligned} K_0 &= G \\ K_1 &= -\cos \omega \\ K_2 &= (2Q - \sin \omega) / (2Q + \sin \omega) \end{aligned} \right|_{G \geq 1} \quad (7)$$

The ranges of the parametric equalizer settings for each band are:

- The gain, G , is from -30 dB to +12 dB.
- The center frequency, f_c , is from $0.0004 \cdot f_s$ to $0.49 \cdot f_s$.
- The quality factor, Q , is from 0.001 to 8.

Filter coefficients must be entered for each filter stage via the I²C-bus interface to configure the filters (see [Section 9.4.3](#)).

[Figure 7](#), [Figure 8](#), and [Figure 9](#) illustrate some possible equalizer band transfer functions. The relationships are symmetrical for the suppression and amplification functions. A skewing effect can be observed at higher frequencies.

For optimum numerical noise performance, different configurations are available for a given filter transfer function. The binary filter configuration parameters t_1 and t_2 control the actual configuration. They must be chosen according to [Equation 8](#).

$$\begin{aligned} t_1 &= \begin{cases} 0 & K_1 \leq 0 \\ 1 & K_1 > 0 \end{cases} \\ t_2 &= \begin{cases} 0 & K_2 \geq 0 \\ 1 & K_2 < 0 \end{cases} \end{aligned} \quad (8)$$

A maximum of 12 dB amplification, regarding the input signal, can be achieved per equalizer stage. The equalizer band signals are processed in sequence from the highest (Band A) to the lowest (Band E). Each band can attenuate the signal by 6 dB. So, to

prevent numerical clipping at filter settings of over 6 dB amplification, band filters can be scaled by 0 dB or -6 dB. For optimum numerical noise performance, steps of -6 dB amplification must be applied to the bands in sequence, starting with B and A, as long as they are able to amplify the signal without clipping.

A filter scale factor, s , is associated with each of the equalizer bands. It is set via the relevant EQx_s control bit (see [Table 25](#)).

Table 7. Equalizer filter scale factor settings

s	scale factor (dB)
0	0
1	-6

8.2.5.2 Equalizer band control

For compact representation with positive signed parameters, parameters k_1' and k_2' are introduced in [Equation 9](#).

$$\begin{aligned}
 k_0' &= K_0 \\
 k_1' &= \begin{cases} 1 - K_1 & t_1 = 0 \\ 1 + K_1 & t_1 = 1 \end{cases} \\
 k_2' &= \begin{cases} 1 - K_2 & t_2 = 0 \\ 1 + K_2 & t_2 = 1 \end{cases}
 \end{aligned} \tag{9}$$

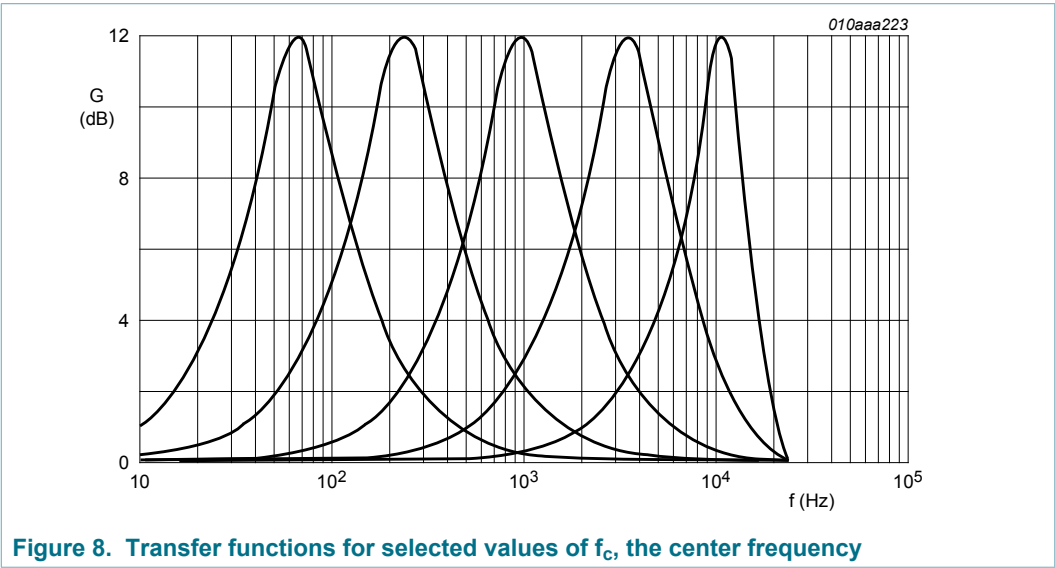
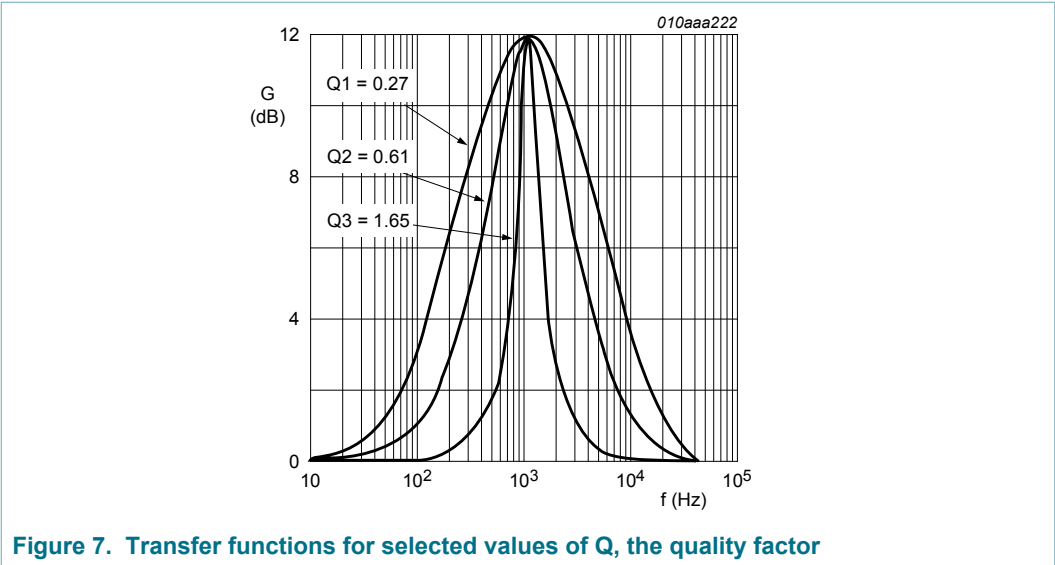
Parameters K_0 , k_1' , k_2' , t_1 , t_2 , and s must be combined in two 16-bit control words, word1 and word2 (see [Table 24](#) and [Table 25](#)), using the format shown in [Table 8](#). Parameters k_1' and k_2' are unsigned floating-point representations in [Equation 9](#).

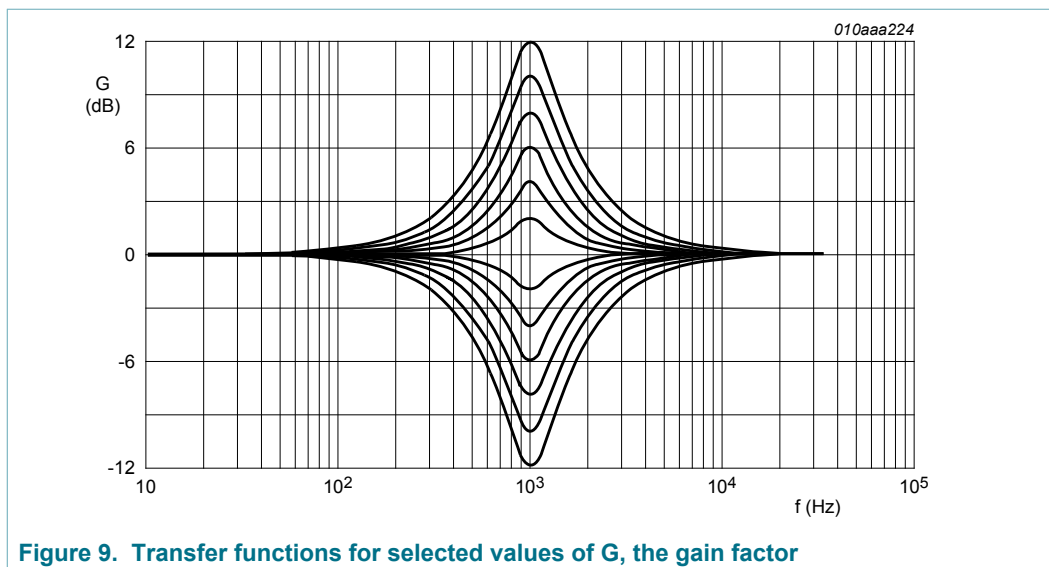
$$k_x' = M \cdot 2^{-E} \mid M < 1 \tag{10}$$

In [Equation 10](#), M is the unsigned mantissa and E the negative signed exponent. For example, in word2 bits [14:8] = [0111 010] represent $k_2' = (7 / 2^4) \times 2^{-2} = 1.09375 \times 10^{-1}$.

Table 8. Equalizer control word construction

Word	Section	Data
word1	15	t_1
word1	[14:4]	11 mantissa bits of k_1'
word1	[3:0]	four exponent bits of k_1'
word2	15	t_2
word2	[14:11]	four mantissa bits of k_2'
word2	[10:8]	three exponent bits of k_2'
word2	[7:1]	k_0'
word2	0	s





8.2.6 Bass and treble control

The TFA8200 contains first-order shelving filters for bass and treble control. The device can attenuate or boost the bass and high frequency signals independently in 2 dB steps within a -18 dB to +18 dB range. Attenuation and boosting depend on the audio signal zero crossing settings (see [Section 8.2.9](#) for further details). The bass and treble corner frequencies are adjustable.

The bass and treble corner frequencies, as a function of the I²C control settings and the sample rate, are given in [Table 9](#).

Table 9. Corner frequency settings for bass and treble control

Control value	f_s (kHz)	Corner frequency (Hz)	
		Bass ^[1]	Treble ^[2]
00	8, 16, 32, 64	181	1090
	11.025, 22.05, 44.1, 88.2	250	1500
	12, 24, 48, 96	272	1630
01 ^[3]	8, 16, 32, 64	218	2180
	11.025, 22.05, 44.1, 88.2	300	3000
	12, 24, 48, 96	326	3260
10	8, 16, 32, 64	300	3000
	11.025, 22.05, 44.1, 88.2	413	4130
	12, 24, 48, 96	450	4500
11	reserved	-	-

[1] Value selected via bits F BASS in the bass and treble control register (see [Table 29](#)).

[2] Value selected via bits F TREBLE in the bass and treble control register (see [Table 29](#)).

[3] Default value.

Figure 10 shows the bass function for a range of attenuation and boost settings with a sample rate of 48 kHz and a corner frequency of 272 Hz.

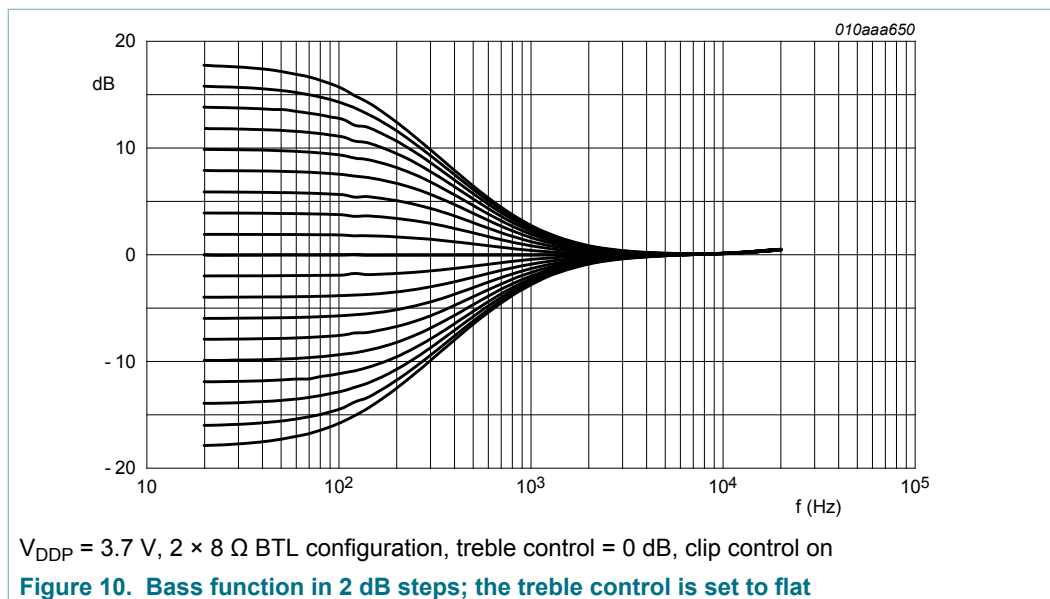
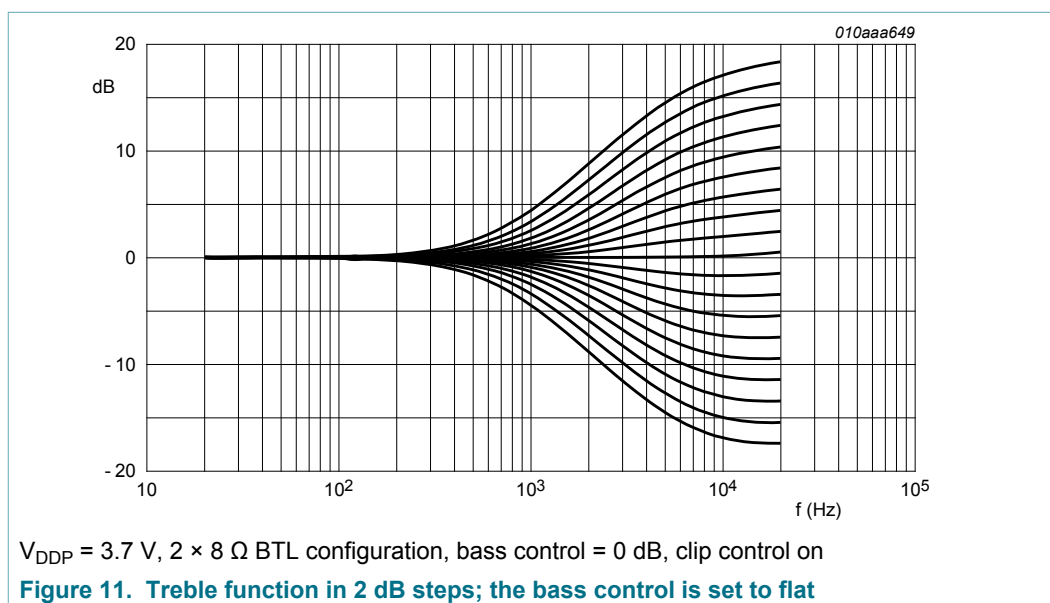


Figure 11 shows the treble function for a range of attenuation and boost settings with a sample rate of 48 kHz and a corner frequency of 1630 Hz.



8.2.7 Muting

The TFA8200 support two muting options, which are controlled via the I²C-bus interface:

- Soft muting
- Hard muting

Soft muting prevents audible pops. The function smoothly reduces the gain setting of the audio channel to the mute level according to a raised cosine shape. Soft muting is performed in $128 / f_s$ steps. Soft unmute results in a similar gain increase. Bit S_MUTE in Table 32 enables and disables the soft mute function.

The hard mute function immediately switches the outputs to 50 % duty cycle pulses. As a result, the input signals are abruptly blocked. Hard mute takes priority over soft mute. Hard mute is enabled and disabled via bit H_MUTE in [Table 32](#).

8.2.8 Digital volume control

The digital volume control has a range of –70 dB to +24 dB, programmable in 0.5 dB steps. The default setting is mute (0 × BD). Attenuation and boosting behavior is affected by the zero crossing volume setting (see [Section 8.2.9](#) for further details).

The volume control settings, and the resulting amplification or suppression factors, are detailed in [Table 10](#).

Table 10. Volume control amplification and suppression

Control value ^[1]	Gain (dB)
00h	+24
01h	+23.5
...	steps of 0.5 dB
BBh	–69.5
BCh	–70
BDh ^[2]	mute
...	mute
FFh	mute

[1] Control value is selected via bits VOL in the volume control register (see [Table 31](#)).

[2] Default value.

8.2.9 Zero-crossing volume control

To minimize pop noise when the volume or bass/treble control is changing, the TFA8200 employs zero-crossing volume control.

When zero-crossing volume control is enabled (ZR_CRSS = 1; see [Table 31](#)), the TFA8200 increases or decreases the gain only when the audio signal passes a zero crossing.

8.2.10 Dynamic range compressor (DRC)

The TFA8200 provides a DRC to adjust power levels automatically according to programmable attack and release levels. The attack level is related to the peak value of the signal. The release level is related to the RMS value of the signal. The attack level is programmable using 16 available levels in the range –12 dB to +10 dB. The release level is programmable using 16 available levels in the range –29 dB to 0 dB relative to the attack level. The signal level is measured after equalizer, bass, and treble processing, but before it reaches the power limiter.

The DRC can be bypassed via bit DRC_BP in [Table 27](#).

8.2.10.1 Functional description

The DRC compresses the dynamic range of the audio stream. The volume control, equalizer, or bass/treble controls can be set so that the audio stream exceeds the 0 dBFS clip level. The DRC can be programmed to compress the louder audio content when the audio stream exceeds the 0 dBFS clip level, while quieter sounds remain unaffected, i.e. the DRC soft clips the audio stream. It is useful when background noise overpowers quiet audio passages. Increasing the volume using the volume control can make quiet audio passages audible but can cause louder audio passages to be distorted by clipping. The DRC prevents that this distortion happens by reducing the volume during loud audio passages and increasing it again for quiet passages.

The design of the DRC feedback loop, incorporating the equalizer and bass and treble controls, is illustrated in [Figure 12](#).

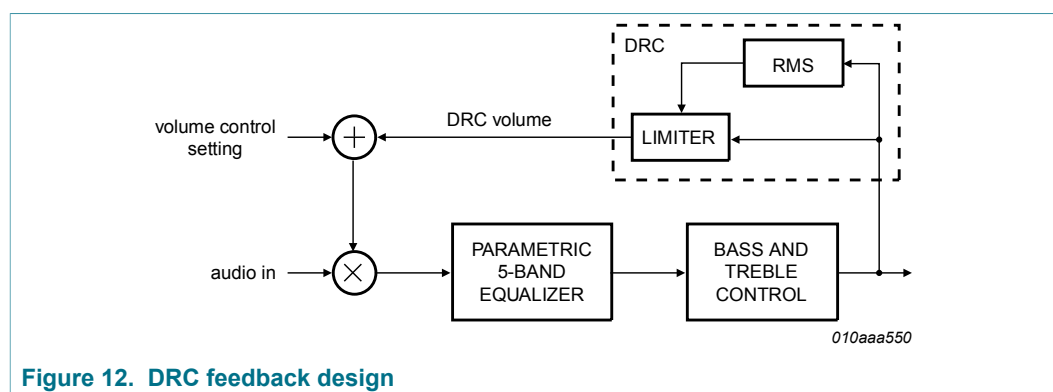


Figure 12. DRC feedback design

8.2.10.2 DRC control

The DRC has four programmable control settings:

- Attack level
- Attack rate
- Release level
- Release rate

When the audio signal level exceeds the attack level, the DRC reduces the volume. The attack level is based on the audio peak value. When the audio signal level drops below the attack level, the DRC stops reducing the volume. The rate of decrease is programmable via the attack rate. When the audio signal level drops to below the release level, the DRC increases it again. This level is based on the audio RMS-value and is related to the attack level. The rate of increase is programmable via the release level. When the audio signal level reaches the release level or the DRC volume drops to 0 dB, the DRC stops increasing the volume.

[Figure 13](#) shows the attack and release behavior of the DRC.

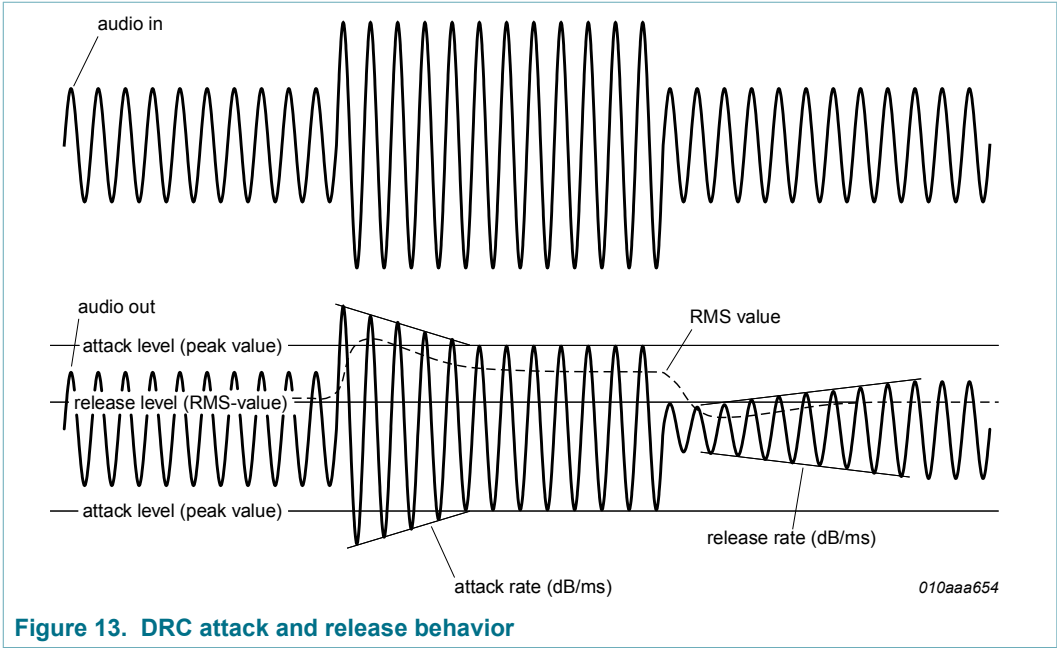


Figure 13. DRC attack and release behavior

Table 11. DRC attack and release levels

Control value: attack level ^[1]	Attack level based on peak value; absolute value (dBFS)	Control value: release level ^[2]	Release level based on RMS value (relative to the attack level ^[3]) (dB)
0000	-12	0000	-29
0001	-10	0001	-26
0010	-8	0010	-23
0011	-6	0011	-20
0100	-5	0100	-18
0101	-4	0101	-16
0110	-3	0110	-14
0111	-2	0111	-12
1000	-1	1000	-10
1001 ^[4]	0	1001	-8
1010	+1	1010	-6
1011	+2	1011 ^[4]	-4

Control value: attack level ^[1]	Attack level based on peak value; absolute value (dBFS)	Control value: release level ^[2]	Release level based on RMS value (relative to the attack level ^[3]) (dB)
1100	+4	1100	-3
1101	+6	1101	-2
1110	+8	1110	-1
1111	+10	1111	0

[1] The control value is selected via bits AT_LVL in the DRC control register (see [Table 28](#)).

[2] The control value is selected via bits RL_LVL in the DRC control register (see [Table 28](#)).

[3] 0 dB (RMS) release level equals 0 dB (peak) attack level.

[4] Default value.

Table 12. DRC attack and release rates

Control value: attack rate ^[1]	Attack rate (dB/ms)	Control value: release rate ^[2]	Release rate (dB/ms)
0000	3	0000	0.5
0001	2.7	0001	0.137
0010 ^[3]	2.25	0010	0.075
0011	1.8	0011	0.05
0100	1.35	0100	0.036
0101	0.9	0101	0.03
0110	0.45	0110	0.026
0111	0.225	0111	0.021
1000	0.15	1000	0.020
1001	0.11	1001	0.017
1010	0.09	1010 ^[3]	0.015
1011	0.075	1011	0.014
1100	0.065	1100	0.013
1101	0.06	1101	0.012
1110	0.055	1110	0.011
1111	0.05	1111	0.01

[1] The control value is selected via bits AT_RATE in the DRC control register (see [Table 28](#)).

[2] The control value is selected via bits RL_RATE in the DRC control register (see [Table 28](#)).

[3] Default value.

8.2.11 Power limiter

The power limiter controls the maximum output voltage in amplifier mode. This feature makes it possible to limit the output voltage across a peripheral (speaker) when necessary.

The TFA8200 output voltage depends on:

- The analog supply voltage on pin V_{DDP}
- The gain of the power limiter (G)
- The power limiter input signal (X_i)

The bass/treble output signal is connected to the power limiter input and is relative to the fraction of full scale (FFS), from -1 to +1.

[Equation 11](#) shows the relationship between these settings and the output voltage between pins OUTA and OUTB in the audio bandwidth:

$$V_o = \begin{cases} X_i \times G \times 5.91 & X_i \times G \times 5.91 < V_{DDP} \\ V_{DDP} & X_i \times G \times 5.91 \geq V_{DDP} \end{cases} \quad (V) \quad (11)$$

[Equation 11](#) only applies with no load and with clip control off (see [Section 8.3](#)). Clip control and the R_{DSon} of the power switches reduce the maximum clipped output signal. The power limiter gain can be reduced in 249 steps of 0.5 dB in the range 0 dB to -124 dB.

The maximum peak output voltage for the first ten power limiter gain settings is given in [Table 13](#).

Table 13. Power limiter control settings

All parameters are guaranteed for $V_{DDP} = 5\text{ V}$; no load; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; clip control off; $T_{amb} = 25\text{ °C}$ unless otherwise specified.

Control value ^[1]	Power limiter gain (dB)	Maximum peak output voltage (V)
00h ^[2]	0.0	V_{DDP}
01h	-0.5	V_{DDP}
02h	-1.0	V_{DDP}
03h	-1.5	V_{DDP}
04h	-2.0	4.7
05h	-2.5	4.4
06h	-3.0	4.2
07h	-3.5	4.0
08h	-4.0	3.7
09h	-4.5	3.5

[1] The control value is selected via bits P_LIM in the De-emphasis, soft/hard mute and power limiter control register (see [Table 32](#)).

[2] Default value.

8.3 Class-D amplification and clip control

A fourth order sigma delta PWM converter converts the digital audio streams into 3-level modulated PWM signals. The analog back end amplifies the two PWM signals in a BTL configuration with complementary output stages.

One of two clip control configurations can be selected:

- Smooth clipping, clip control on
- Maximum power, clip control off

If smooth clipping is selected (CLIPCTRL = 0; see [Table 27](#)), the clipping behavior has no artifacts. To obtain the maximum output power, the device can be set to maximum power.

The PWM frequency is related to the I²S input sample rate as detailed in [Table 4](#).

Table 14. Power limiter control settings

PWM frequency (kHz)	Sample rate (kHz)	SCK relative to sample rate
256	8, 16, 32, 64	32 ×, 64 ×
352.8	11.025, 22.05, 44.1, 88.2	32 ×, 64 ×
384	12, 24, 48, 96	32 ×, 64 ×

8.4 Protections

The TFA8200 incorporates a wide range of protection circuits to facilitate optimal and safe application.

The following protection circuits are included in the TFA8200:

- Overtemperature protection (OTP)
- Overcurrent protection (OCP)
- Underfrequency protection (UFP)
- Overfrequency protection (OFP)
- Invalid bit-clock protection (IBP)
- DC-blocking via high-pass filter (see [Section 8.2.3](#))

The reaction of the device to fault conditions differs depending on the protection circuit involved.

8.4.1 Overtemperature protection (OTP)

OTP is a 'hard' protection to prevent that heat damages the TFA8200. When the junction temperature exceeds 130 °C, overtemperature protection is triggered. When OTP is triggered, the output stages are set floating. OTP can be cleared automatically via a programmable timer or via the I²C-bus interface, after which the output stages start to operate normally again. The programmable timer settings, selected via bits L_OTP in the bypass control register ([Table 27](#)), are:

- 4.5 μs
- 100 ms
- 1 s

OTP can also be set to no recovery. When no recovery is selected, setting the TFA8200 to off mode and then to amplifier mode clears the OTP.

8.4.2 Overcurrent protection (OCP)

The output current of the class-D amplifiers is current limited. When an output stage exceeds a current in the range 1.3 A to 2.3 A, the output stages are set floating. OCP can be cleared automatically via a programmable timer or via the I²C-bus interface, after which the output stages start to operate normally again. The programmable timer settings, selected via bits L_OCP in the bypass control register ([Table 27](#)), are:

- 4.5 μ s
- 27.5 μ s
- 10 ms

The OCP can also be set to no recovery. When no recovery is selected, setting the TFA8200 to off mode and then to amplifier mode clears the OCP.

8.4.3 Underfrequency protection (UFP)

When the clock input source is too low ($< f_{UFP}$), UFP sets the output stages floating. It can happen if, for example, the selected sample frequency (bits I2S_FS in [Table 22](#)) is not in line with the applied sample rate. When the frequency of the input clock is lower than the selected sample frequency, the PWM switching frequency can become critically low. Without UFP, peripheral devices in an application may be damaged.

The UFP status can be monitored by polling the I²C status register ([Table 33](#)). When the input sample rate is too low, the alarm is raised.

8.4.4 Overfrequency protection (OFP)

When the clock input source is too high ($> f_{OFP}$), OFP sets the output stages floating. It can happen if, for example, the selected sample frequency (bits I2S_FS in [Table 22](#)) is not in line with the applied sample rate. When the frequency of the input clock is higher than the selected sample frequency, the PWM controller can become unstable. Without OFP, peripheral devices in an application may be damaged.

The OFP status can be monitored by polling the I²C status register ([Table 33](#)). When the input sample rate is too high, the alarm is raised.

8.4.5 Invalid bit-clock protection (IBP)

If the SCK-to-LRCK ratio is not supported, the audio signal is distorted. The reason it occurs is that the sound processing blocks are operating at frequencies out of synchronization with the sample rate.

If the IBP alarm is raised for the selected channel, IBP prevents that the audio signal becomes distorted by shutting down the TFA8200. It disconnects the digital audio path.

Valid SCK-to-LRCK ratios for PCM interface formats are 16, 32, 48, 64, 96, 128, and 192. For I²S interface formats, valid SCK-to-LRCK ratios are 32 and 64.

8.4.6 Overview of protection circuits

[Table 15](#) provides an overview of the protection circuits implemented.

Table 15. Overview of protection circuits

Protection circuits				
Symbol	Conditions	I ² C flag	Output	Recovery
OTP	$T_j > 130\text{ °C}$	OTP	floating	automatic when timer set to 4.5 μ s, 100 ms, or 1 s (via bits L_OTP in Table 27) and $T_j < 130\text{ °C}$; when no recovery is selected, via I ² C-bus
OCP	$I_O > I_{O(ocp)}$	OCP	floating	automatic when timer set to 4.5 μ s, 27.5 μ s, or 10 μ s (via bits L_OCP in Table 27) and $I_O < I_{O(ocp)}$; when no recovery is selected, via I ² C-bus
UFP	PWM frequency < 96 kHz	UFP	floating	restart (when PWM frequency > 96 kHz, fault to operating)
OFP	PWM frequency > 1031 kHz	OFP	floating	restart (when PWM frequency < 1031 kHz, fault to operating)
IBP	SCK/WS is not 16 ± 1 , 32 ± 1 , 48 ± 1 , 64 ± 1 , or 128 ± 1	IBP	floating	restart (when SCK/WS is 16 ± 1 , 32 ± 1 , 48 ± 1 , 64 ± 1 , or 128 ± 1 , fault to operating)

9 I²C-bus interface and register settings

9.1 I²C-bus interface

The TFA8200 supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control the TFA8200 and to transmit and receive data.

The TFA8200 can operate only in I²C slave mode, as a slave receiver or as a slave transmitter.

The TFA8200 is accessed via an 8-bit code (see [Table 16](#)). Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for multichannel applications. Applying the appropriate voltage to pins ADSEL1 (A1) and ADSEL2 (A2) select the required I²C address as detailed in [Table 16](#).

Table 16. I²C-bus device address

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
1	1	0	1	1	A2	A1	R/W

Table 17. I²C pin voltages in I²C control mode

Logic value	Voltage on pins ADSEL1 and ADSEL2
0	< V _{IL}
1	> V _{IH}

9.2 I²C-bus write cycle

The sequence of events that must be followed when writing data to the I²C-bus registers of the TFA8200 is detailed in [Table 18](#). One byte is transmitted at a time. Each register stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA8200, followed by the R/W bit set to 0.
3. The TFA8200 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA8200 register address to which the first data byte is written.
5. The TFA8200 asserts an acknowledge.
6. The microcontroller transmits the first byte (the most significant byte).
7. The TFA8200 asserts an acknowledge.
8. The microcontroller transmits the second byte (the least significant byte).
9. The TFA8200 asserts an acknowledge.
10. The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the TFA8200 auto-increments the targeted register address.

Table 18. I²C-bus write cycle

Start	TFA8200 Address	R/W		TFA8200 first register address		MSB		LSB		More data...	Stop
S	11011A ₂ A ₁	0	A	ADDR	A	MS1	A	LS1	A	<....>	P

9.3 I²C-bus read cycle

The sequence of events that must be followed when reading data from the I²C-bus registers of the TFA8200 is detailed in [Table 19](#). One byte is transmitted at a time. Each of the registers stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA8200, followed by the R/W bit set to 0.
3. The TFA8200 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA8200 register address from which the first data byte is read.
5. The TFA8200 asserts an acknowledge.
6. The microcontroller asserts a repeated start (Sr).
7. The microcontroller retransmits the device address followed by the R/W bit set to 1.
8. The TFA8200 asserts an acknowledge.
9. The TFA8200 transmits the first byte (the MSB).
10. The microcontroller asserts an acknowledge.
11. The TFA8200 transmits the second byte (the LSB).
12. The microcontroller asserts either an acknowledge or a negative acknowledge (NA).
 - If the microcontroller asserts an acknowledge, the TFA8200 auto-increases the target register address and steps 9 to 12 are repeated.
 - If the microcontroller asserts a negative acknowledge, the TFA8200 frees the I²C-bus and the microcontroller generates a stop condition (P).

Table 19. I²C-bus read cycle

Start	TFA8200 address	R/W		First register address			TFA8200 address	R/W		MSB		LSB		More data...		Stop
S	11011A ₂ A ₁	0	A	ADDR	A	Sr	11011A ₂ A ₁	1	A	MS1	A	LS1	A	<....>	NA	P

9.4 Top-level register map

[Table 20](#) describes the top-level assignment of register addresses to the functional control and status areas. There are 21 control registers and 1 status register.

Table 20. Top-level register map

Register address (hex)	Default (hex)	Access	Description
00h	0x0000	R/W	device control; see Table 21
01h	0x0A18	R/W	serial Interface input 1; see Table 22
02h	0x0007	R/W	PCM/IOM2 format input 1; see Table 23
03h	0x0A18	R/W	serial Interface input 2; see Table 22
04h	0x0007	R/W	PCM/IOM2 format input 2; see Table 23
05h	0x59DD	R/W	equalizer_A word_1; see Table 24
06h	0xC63E	R/W	equalizer_A word_2; see Table 25
07h	0x651A	R/W	equalizer_B word_1; see Table 24
08h	0xE53E	R/W	equalizer_B word_2; see Table 25
09h	0x4616	R/W	equalizer_C word_1; see Table 24
0Ah	0xD33E	R/W	equalizer_C word_2; see Table 25
0Bh	0x4DF3	R/W	equalizer_D word_1; see Table 24
0Ch	0xEA3E	R/W	equalizer_D word_2; see Table 25
0Dh	0x5EE0	R/W	equalizer_E word_1; see Table 24
0Eh	0xF93E	R/W	equalizer_E word_2; see Table 25
0Fh	0x0093	R/W	bypass control; see Table 27
10h	0x92BA	R/W	dynamic range compressor; see Table 28
11h	0x12A5	R/W	bass and treble; see Table 29
12h	0x0004	R/W	high-pass filter; see Table 30
13h	0x10BD	R/W	volume control; see Table 31
14h	0x0000	R/W	de-emphasis, soft/hard mute and power limiter; see Table 32
15h	-	R	miscellaneous status; see Table 33

The following subsections provide details of the bits in these registers and the control and status functionality assigned to each.

9.4.1 Device control

Table 21. Device control register (address 00h) bit description

Bit	Symbol	Access	Default	Description
15:5	reserved		0x000	
4	INPUT_SEL	R/W	0	serial interface input selection 0: serial interface input 1 1: serial interface input 2
3	OPMODE	R/W	0	operating mode selection 0: off mode 1: amplifier mode
2	reserved		0	
1	RESET	R/W	0	I ² C reset activation 0: reset inactive 1: reset active; 1 is written to generate a reset, after which the RESET bit is automatically reset to 0
0	POWERUP	R/W	0	Power-down mode selection 0: Power-down mode 1: operating mode (dependent on OPMODE)

9.4.2 Serial interface control

Table 22. Serial interface control registers (addresses 01h and 03h^[1]) bit description

Bit	Symbol	Access	Default	Description
15:12	reserved		0000	
11:10	MONO_SEL	R/W	10	mono selection
				00: left channel; left channel content is amplified in amplifier mode
				01: right channel; right channel content is amplified in amplifier mode
				10: left + right channels; sum of left and right channels, divided by two, is amplified in amplifier mode
				11: reserved
9:6	I2S_FS	R/W	1000	sample frequency (f_s) of digital-in signal
				0000: 8 kHz
				0001: 11.025 kHz
				0010: 12 kHz
				0011: 16 kHz
				0100: 22.05 kHz
				0101: 24 kHz
				0110: 32 kHz
				0111: 44.1 kHz
				1000: 48 kHz
				1001: 64 kHz
				1010: 88.2 kHz
				1011: 96 kHz
				1100 to 1111: reserved
5:3	I2S_SET	R/W	011	I ² S format selection
				000: reserved
				001: reserved
				010: MSB-justified data up to 24 bits
				011: I ² S data up to 24 bits
				100: LSB-justified 16-bit data
				101: LSB-justified 18-bit data
				110: LSB-justified 20-bit data
2	SCK_POL	R/W	0	enable SCK signal polarity inversion
				0: no SCK signal polarity inversion
				1: SCK signal polarity inversion enabled

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Bit	Symbol	Access	Default	Description
1:0	I_MODE	R/W	00	input audio mode selection
				00: I ² S mode
				01: PCM/IOM2 Short Frame Sync Format
				10: PCM/IOM2 Long Frame Sync Format
				11: reserved

[1] Serial interface 1 settings are controlled via register 01h; serial interface 2 settings are controlled via register 03h.

Table 23. PCM/IOM2 format control registers (addresses 02h and 04h^[1]) bit description

Bit	Symbol	Access	Default	Description
15:12	reserved		0000	
11	PCM_FS	R/W	0	PCM sample frequency
				0: 8 kHz
				1: 16 kHz
10	A_LAW	R/W	0	U-LAW/A-LAW decoding selection (depending on PCM_COMP)
				0: U-law decoding; default value
				1: A-law decoding
9	PCM_COMP	R/W	0	companded PCM data
				0: linear
				1: companded (U/A-law)
8	PCM_DL	R/W	0	PCM data length (number of bits per slot)
				0: 8-bit; default value
				1: 16-bit
7:4	D1_SLOT	R/W	0000	slot number position of the first sample (at 8 kHz and 16 kHz)
				0000: slot 0
				0001: slot 1
			
				1111: slot 15
3:0	D2_SLOT	R/W	0111	slot number position of the second sample (16 kHz)
				0000: slot 0
				0001: slot 1
			

Bit	Symbol	Access	Default	Description
3:0 (continued)				0111: slot 7
			
				1111: slot 15

[1] PCM/IOM2 format settings of serial interface 1 are controlled via register 02h; PCM/IOM2 format settings of serial interface 2 are controlled via register 04h.

9.4.3 Equalizer configuration

Table 24. Equalizer word1 control registers (addresses 05h, 07h, 09h, 0Bh, and 0Dh for equalizer bands A, B, C, D, and E respectively) bit description

'x' represents the equalizer band A, B, C, D, or E

Bit	Symbol	Access	Default ^[1]	Description
15	EQx_t1	R/W		filter configuration parameter t_1 (see Section 8.2.5.1)
14:4	EQx_k1m	R/W		11 mantissa bits of filter parameter k_1' (see Section 8.2.5.1)
3:0	EQx_k1e	R/W		four exponent bits of filter parameter k_1' (see Section 8.2.5.1)

[1] Default settings are given in [Table 20](#). The corresponding equalizer configuration is shown in [Table 26](#).

Table 25. Equalizer word2 control register (addresses 06h, 08h, 0Ah, 0Ch, and 0Eh for equalizer bands A, B, C, D, and E respectively) bit description

'x' represents the equalizer band A, B, C, D, or E

Bit	Symbol	Access	Default ^[1]	Description
15	EQx_t2	R/W		filter configuration parameter t_2 (see Section 8.2.5.1)
14:11	EQx_k2m	R/W		four mantissa bits of filter parameter k_2' (see Section 8.2.5.1)
10:8	EQx_k2e	R/W		three exponent bits of filter parameter k_2' (see Section 8.2.5.1)
7:1	EQx_K0	R/W		seven-bit of filter gain parameter K_0 (see Section 8.2.5.1)
0	EQx_s	R/W		filter scale-factor (s) (see Section 8.2.5.1)
				0: no scaling applied
				1: -6 dB amplification enabled

[1] Default settings are given in [Table 20](#). The corresponding equalizer configuration is shown in [Table 26](#).

Table 26. Default equalizer configuration for $f_s = 48$ kHz

Band	A	B	C	D	E
frequency (Hz)	100	300	1000	3000	10000
Q-factor	1.65	1.65	1.65	1.65	1.65
gain (dB)	0	0	0	0	0

9.4.4 Bypass control

Table 27. Bypass control register (addresses 0Fh) bit description

Bit	Symbol	Access	Default	Description
15:8	reserved		0x00	
7:6	L_OCP	R/W	10	overcurrent protection timer setting
				00: 4.5 μ s floating when an overcurrent is detected
				01: 27.5 μ s floating when an overcurrent is detected
				10: 10 ms floating when an overcurrent is detected
5:4	L_OTP	R/W	01	11: no recovery (stays floating) when an overcurrent is detected
				overtemperature protection timer setting
				00: 4.5 μ s floating when an overtemperature is detected
				01: 100 ms floating when an overtemperature is detected
3	CLIPCTRL	R/W	0	10: 1 s floating when an overtemperature is detected
				11: no recovery (stays floating) when an overtemperature is detected
				clip control bypass setting (see Section 8.3)
2	HPF_BP	R/W	0	0: clip control on (smooth clipping)
				1: clip control off (maximum power)
				high-pass filter bypass setting
1	DRC_BP	R/W	1	0: high-pass filter active
				1: high-pass filter bypassed
				dynamic range compressor bypass setting
0	EQ_BP	R/W	1	0: dynamic range compression active
				1: dynamic range compression bypassed
				equalizer bypass setting:
				0: equalizer active
				1: equalizer bypassed

9.4.5 Dynamic range compressor

Table 28. DRC control register (addresses 10h) bit description

Bit	Symbol	Access	Default	Description
15:12	AT_LVL	R/W	1001	dynamic range compressor attack level; see Table 11 for the attack level as a function of the value of AT_LTV.
11:8	AT_RATE	R/W	0010	dynamic range compressor attack rate; see Table 12 for the attack rate as a function of the value of AT_RATE
37:4	RL_LVL	R/W	1011	dynamic range compressor release level; see Table 11 for the release level as a function of the value of RL_LTV.
3:0	RL_RATE	R/W	1010	dynamic range compressor release rate; see Table 12 for the release rate as a function of the value of RL_RATE

9.4.6 Bass and treble control

Table 29. Bass and treble control register (addresses 11h) bit description

Bit	Symbol	Access	Default	Description
15:14	reserved			
13:9	G_TRBLE	R/W	01001	treble gain (2 dB steps)
				00000: -18 dB
				00001: -16 dB
			
				01001: 0 dB
			
				10001: +16 dB
				10010: +18 dB
				10011 to 11111: reserved
8:7	F_TRBLE	R/W	01	treble control corner frequency (see Table 9 for the corner frequency as a function of the value of F_TREBLE)
6:2	G_BASS	R/W	01001	bass gain (2 dB steps)
				-18 dB
				-16 dB
			
				01001: 0 dB
			
				+16 dB
				+16 dB
				reserved

Bit	Symbol	Access	Default	Description
1:0	F_BASS	R/W	01	bass control corner frequency (see Table 9 for the corner frequency as a function of the value of F_BASS)

9.4.7 High-pass filter

Table 30. High-pass filter control register (addresses 12h) bit description

Bit	Symbol	Access	Default	Description
15:9	reserved			
8:0	HP_CTRL	R/W	0x04 ^[1]	high-pass filter control (see Section 8.2.3 for a discussion of the high pass corner frequency as a function of the value of HP_CTRL)

[1] Default value is 04h. From [Equation 1](#), giving a high-pass cut-off frequency of approximately $1.6 \times f_s$.

9.4.8 Volume control

Table 31. Volume control register (address 13h) bit description

Bit	Symbol	Access	Default	Description
15:13	reserved		000	
12	ZR_CRSS	R/W	1	volume update at zero crossing audio stream 0: zero-crossing volume control disabled 1: zero-crossing volume control enabled; default value
11:8	reserved	R/W	0000	
7:0	VOL	R/W	0xBD	volume control (see Table 10 for the amplification and suppression factors as a function of the value of bits VOL)

9.4.9 De-emphasis, soft/hard mute, and power limiter

Table 32. De-emphasis, soft/hard mute and power limiter control register (address 14h) bit description

Bit	Symbol	Access	Default	Description
15:12	reserved		0000	
11:10	DE_PHAS	R/W	00	de-emphasis settings (see Table 6 for the de-emphasis configuration for four sample rates as a function of the value of DE_PHASE)
9	H_MUTE	R/W	0	hard mute 0: no hard mute; default value 1: hard mute enabled; implemented by PWM signal with 50 % duty cycle
8	S_MUTE	R/W	0	soft mute; default value 0: soft mute disabled using raised cosine 1: soft mute enabled using raised cosine

Bit	Symbol	Access	Default	Description
7:0	P_LIM	R/W	0xBD	power limiter control settings (see Table 13 for suppressions factors as a function of the value of P_LIM)

9.4.10 Miscellaneous status

Table 33. Miscellaneous status register (address 15h) bit description

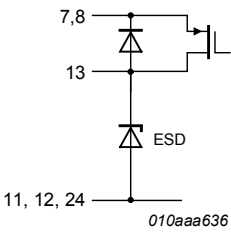
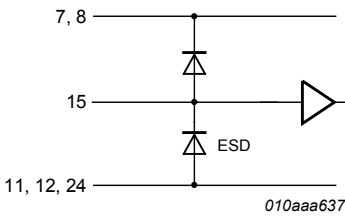
Bit	Symbol	Access	Description
15	reserved		
14	PS	R	power stage status <ul style="list-style-type: none"> 0: class-D audio amplifier power stage floating 1: class-D audio amplifier power stage switching; PWM signals on pins OUTA and OUTB
13	PORA	R	analog 1V8 regulator status <ul style="list-style-type: none"> 0: 1V8 analog regulator is off or output voltage level is too low 1: 1V8 analog regulator output is available and correct
12:11	reserved		
10:9	AMP	R	amplifier mode status <ul style="list-style-type: none"> 00: amplifier is off 01: startup 10: startup 11: amplifier is functional
8	IBP(2)	R	invalid bit clock protection on serial interface input 2 <ul style="list-style-type: none"> 0: the ratio in frequency between the signal on pin SCK2 and the signal on pin LRCK2 is valid for the selected interface format 1: the ratio in frequency between the signal on pin SCK2 and the signal on pin LRCK2 is invalid for the selected interface format
7	OFP(2)	R	overfrequency protection on serial interface input 2 <ul style="list-style-type: none"> 0: the frequency of the signal on pin LRCK2 is in line with (or lower than) the selected interface format 1: the frequency of the signal on pin LRCK2 is higher than the selected interface format
6	UFP(2)	R	underfrequency protection on serial interface input 2 <ul style="list-style-type: none"> 0: the frequency of the signal on pin LRCK2 is in line with (or higher than) the selected interface format 1: the frequency of the signal on pin LRCK2 is lower than the selected interface format

Bit	Symbol	Access	Description
5	IBP(1)	R	invalid bit clock protection on serial interface input 1
			0: the ratio in frequency between the signal on pin SCK1 and the signal on pin LRCK1 is valid for the selected interface format
			1: the ratio in frequency between the signal on pin SCK1 and the signal on pin LRCK1 is invalid for the selected interface format
4	OFP(1)	R	overfrequency protection on serial interface input 1
			0: the frequency of the signal on pin LRCK1 is in line with (or lower than) the selected interface format
			1: the frequency of the signal on pin LRCK1 is higher than the selected interface format
3	UFP(1)	R	underfrequency protection on serial interface input 1
			0: the frequency of the signal on pin LRCK1 is in line with (or higher than) the selected interface format
			1: the frequency of the signal on pin LRCK1 is lower than the selected interface format
2	OCPOKA	R	overcurrent protection on pin OUTA
			0: overcurrent protection on pin OUTA active
			1: overcurrent protection on pin OUTA inactive
1	OCPOKB	R	overcurrent protection on pin OUTB
			0: overcurrent protection on pin OUTB active
			1: overcurrent protection on pin OUTB inactive
0	OTPOK	R	overtemperature protection
			0: overtemperature protection active
			1: overtemperature protection inactive

10 Internal circuitry

Table 34. Internal circuitry

Pin	Symbol	Equivalent circuit
1	SDA	
2	SCL	
3	TEST1	
4	ADSEL2	
5	TEST3	
16	ADSEL1	
17	SDI2	
18	SCK2	
19	LRCK2	
20	SDI1	
21	SCK1	
22	LRCK2	
7; 8	V _{DDP}	
9	OUTB	
10	OUTA	

Pin	Symbol	Equivalent circuit
13	STABA	
15	TEST2	

11 Limiting values

Table 35. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage	on pin V_{DDP}	-0.3	+5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDP}	-0.3	+1.95	V
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-20	+85	°C
V_x	voltage on pin x	pins LRCKx, SCKx, SDIx, SDA, SCL, ADSEL1, ADSEL2, TEST1, and TEST3	-0.3	+3.6	V
		pin TEST2	-0.3	$V_{DDP} + 0.3$	V
		pins OUTA and OUTB	-0.6	$V_{DDP} + 0.6$	V
		pin STABA	-0.3	+1.95	V
V_{ESD}	electrostatic discharge voltage	according to human body model (HBM)	-2	+2	kV
		according to charge device model (CDM)	-500	+500	V

12 Thermal characteristics

Table 36. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with natural convection		
		JEDEC test board	^[1] 49	K/W
		2-layer application board	67	K/W
Ψ_{j-lead}	thermal characterization parameter from junction to lead		23	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		^[2] 6	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air with natural convection	5	K/W

[1] Measured on a JEDEC high K-factor test board (standard EIA/JESD 51-7).

[2] Value depends on where measurement is taken on package.

13 Characteristics

13.1 DC characteristics

Table 37. DC characteristics

All parameters are guaranteed for $V_{DDD} = 1.8\text{ V}$; $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$; $L_L = 44\ \mu\text{H}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; clip control off; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DDP}	power supply voltage	on pin V _{DDP}	2.5	-	5.5	V
V _{DDD}	digital supply voltage	on pin V _{DDD}	1.65	1.8	1.95	V
I _P	supply current	on pin V _{DDP} ; amplifier mode with load; soft mute on	-	5.7	-	mA
		on pin V _{DDP} ; power-down mode	-	-	20	μA
I _{DDD}	digital supply current	on pin V _{DDD} ; amplifier mode	-	1.2	-	mA
		on pin V _{DDD} ; power-down mode ^[1]	-	5	15	μA
Series resistance output power switches						
R _{DSon}	drain-source on-state resistance	lower switch (NMOS)	-	190	-	mΩ
		upper switch (PMOS)	-	260	-	mΩ
Amplifier output pins; OUTA and OUTB						
V _{O(offSet)}	output offset voltage		-15	0	+15	mV
Regulator; pin STABA						
V _{O(reg)}	regulator output voltage	STABA to GNDP	1.65	-	1.95	V
LRCK1, SCK1, SDI1, LRCK2, SCK2, SDI2, SDA, SCL, ADSEL1, and ADSEL2						
V _{IH}	HIGH-level input voltage		0.7V _{DDD}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DDD}	V
C _i	input capacitance		-	-	3	pF
V _{OL}	LOW-level output voltage	at I _{OL} = 2.6 mA	-	-	400	mV
Protection						
T _{act(th_prot)}	thermal protection activation temperature		130	-	-	°C
I _{O(ocp)}	overcurrent protection output current		1.3	-	2.3	A
f _{OFF}	overfrequency protection frequency	at PWM output frequency	-	710	1031	kHz
f _{UFP}	underfrequency protection frequency	at PWM output frequency	96	175	-	kHz

[1] After switching from Off/Amplifier mode to Power-down mode.

13.2 AC characteristics

Table 38. AC characteristics

All parameters are guaranteed for $V_{DD} = 1.8\text{ V}$; $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$; $L_L = 44\ \mu\text{H}$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; clip control off; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Class D amplifier						
$P_{o(RMS)}$	RMS output power	$R_L = 8\ \Omega$				
		THD+N = 1 %	0.65	0.7	-	W
		THD+N = 10 %	-	0.85	-	W
		$R_L = 4\ \Omega$				
		THD+N = 1 %	-	1.2	-	W
		THD+N = 10 %	-	1.5	-	W
		$R_L = 8\ \Omega$; $V_{DDP} = 4.2\text{ V}$				
		THD+N = 1 %	-	0.9	-	W
		THD+N = 10 %	-	1.1	-	W
		$R_L = 4\ \Omega$; $V_{DDP} = 4.2\text{ V}$				
		THD+N = 1 %	-	1.6	-	W
		THD+N = 10 %	-	1.95	-	W
		$R_L = 8\ \Omega$; $V_{DDP} = 5.0\text{ V}$				
		THD+N = 1 %	-	1.35	-	W
		THD+N = 10 %	-	1.6	-	W
		$R_L = 4\ \Omega$; $V_{DDP} = 5.0\text{ V}$				
		THD+N = 1 %	-	2.35	-	W
		THD+N = 10 %	-	2.75	-	W
η_{po}	output power efficiency	$P_{o(RMS)} = 850\text{ mW}$	-	92	-	%
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)} = 100\text{ mW}$	-	0.02	0.1	%
$V_{n(o)}$	output noise voltage	soft mute; a-weighted	-	60	-	μV
S/N	signal-to-noise ratio	$V_{PVDD} = 5\text{ V}$; $P_{o(RMS)} = 1.3\text{ W}$; a-weighted	-	94	-	dB
PSRR	power supply rejection ratio	$V_{ripple} = 200\text{ mV}$; $f_{ripple} = 217\text{ Hz}$	65	80	-	dB
$V_{o(RMS)}$	RMS output voltage	At -9 dBFS (RMS) digital input; volume control = 0 dB; bass and treble control = 0 dB; equalizer bypassed and DRC bypassed	1.9	2.1	2.3	V
Power-up, power-down, and propagation times						
$t_{d(on)}$	turn-on delay time	off mode to operating mode; soft demute excluded	-	-	5.6	ms
$t_{d(mute_off)}$	mute off delay time		-	-	2.67	ms
$t_{d(soft_mute)}$	soft mute delay time		-	-	2.67	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	propagation delay	bass and treble control = 0 dB; equalizer bypassed and DRC bypassed.	-	600	-	μs

13.3 I²C timing characteristics

Table 39. I²C-bus interface characteristics (see Figure 14)

All parameters are guaranteed for $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$; $L_L = 44\ \mu H$; $f_i = 1\text{ kHz}$; $f_s = 48\text{ kHz}$; clip control off; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{LOW}	LOW period of the SCL clock		1.3	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	μs
t_r	rise time	SDA and SCL signals	^[1] $20 + 0.1C_b$	-	-	ns
t_f	fall time	SDA and SCL signals	^[1] $20 + 0.1C_b$	-	-	ns
$t_{HD,STA}$	hold time (repeated) START condition		^[2] 0.6	-	-	μs
$t_{SU,STA}$	set-up time for a repeated START condition		0.6	-	-	μs
$t_{SU,STO}$	set-up time for STOP condition		0.6	-	-	μs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	μs
$t_{SU,DAT}$	data set-up time		100	-	-	ns
$t_{HD,DAT}$	data hold time		0	-	-	μs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns
C_b	capacitive load for each bus line		-	-	400	pF

[1] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.

[2] After this period, the first clock pulse is generated.

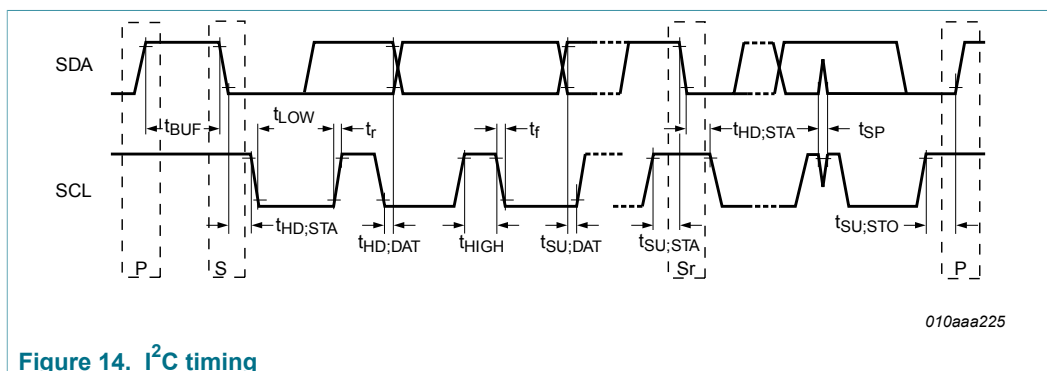


Figure 14. I²C timing

13.4 I²S timing characteristics

Table 40. I²S bus interface characteristics (see Figure 15)

All parameters are guaranteed for $V_{DD} = 1.8\text{ V}$; $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$; $L_L = 44\ \mu\text{H}$; $f_i = 1\text{ kHz}$; clip control off; $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency	on LRCK1 or LRCK2 pins	8	-	96	kHz
f_{clk}	clock frequency	on SCK1 or SCK2 pins	$32f_s$	-	$64f_s$	Hz
t_{su}	set-up time	LRCK edge to SCK HIGH	10	-	-	ns
		SDI edge to SCK HIGH	10	-	-	ns
t_h	hold time	SCK HIGH to LRCK edge	10	-	-	ns
		SCK HIGH to SDI edge	10	-	-	ns

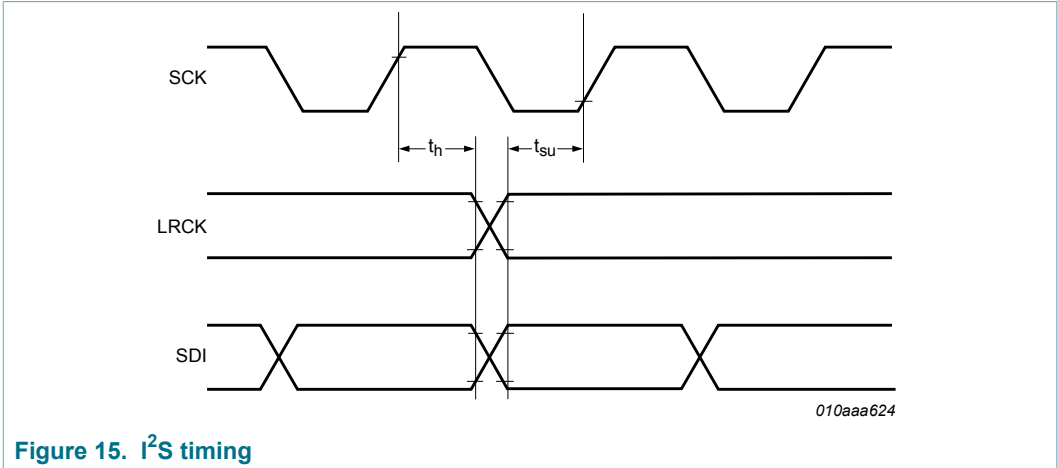


Figure 15. I²S timing

13.5 PCM/IOM2 timing characteristics

Table 41. PCM/IOM2 characteristics (see Figure 16)

All parameters are guaranteed for $V_{DD} = 1.8\text{ V}$; $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$; $L_L = 44\ \mu\text{H}$; $f_i = 1\text{ kHz}$; clip control off; $T_{amb} = 25\ ^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_p	pulse frequency	on LRCK1 or LRCK2 pins	-	-	8	kHz
f_{clk}	clock frequency	on SCK1 or SCK2 pin	$16f_p$	-	$192f_p$	Hz
t_{su}	set-up time	SCK HIGH to LRCK edge	10	-	-	ns
		SCK HIGH to SDI edge	10	-	-	ns
t_h	hold time	LRCK edge to SCK HIGH	10	-	-	ns
		SDI edge to SCK HIGH	10	-	-	ns
t_p	pulse duration	pulse on LRCK1 pin or LRCK2 pin	$1/f_{clk}$	-	-	s

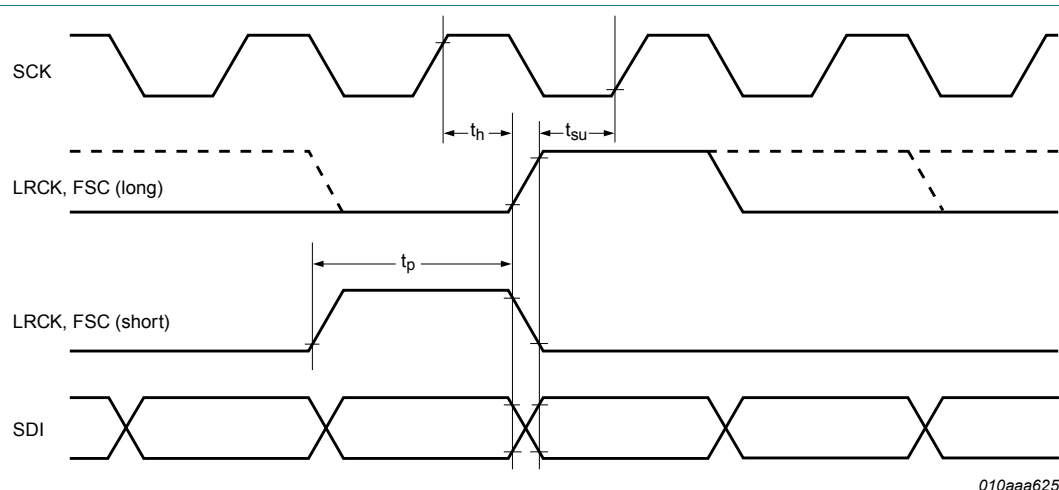


Figure 16. PCM/IOM2 timing

14 Application information

The TFA8200 is a filter-free BTL class-D amplifier that uses a fixed frequency PWM modulation scheme (see the simplified application schematic in [Figure 18](#)). When the TFA8200 is idle (no audio input signal), the voltage across the speaker is 0 V, generating no additional current. Even when the audio input signal modulates the PWM output, the out-of-band AC ripple current in the voice coil is very small compared to the audio current. The reason is the inductive behavior of the voice coil at the PWM switching frequency. A typical voice coil inductance is in the range 30 µH to 80 µH.

14.1 Power capability

14.1.1 Estimating the RMS output power ($P_{O(RMS)}$)

The RMS output power, $P_{O(RMS)}$, at THD+N = 1 % just before clipping can be estimated using [Equation 12](#), with clip-control off, or using [Equation 13](#), with clip-control on.

Clip control off:

$$P_{O(RMS)1\%} = \frac{\left(\left(\frac{R_L}{R_L + R_S + (2 \times R_{DSon})} \right) \times V_{DDP} \right)^2}{2 \times R_L} \quad (12)$$

Clip control on:

$$P_{O(RMS)1\%} = \frac{\left(\left(\frac{R_L}{R_L + R_S + (2 \times R_{DSon})} \right) \times M_{max} \times V_{DDP} \right)^2}{2 \times R_L} \quad (13)$$

Where:

R_L = load resistance (Ω)

R_S = total series resistance of application

R_{DSon} = on-resistance of power switch (typically 230 mΩ)

V_{DDP} = power supply voltage (V)

M_{max} = maximum modulation depth (clip control on; typically 0.9)

Example (clip control off):

With $V_{DDP} = 5 \text{ V}$; $R_{DSon} = 0.23 \text{ } \Omega$ (at $T_j = 25 \text{ } ^\circ\text{C}$); $R_S = 0.14 \text{ } \Omega$:

$P_{O(RMS)1\%} = 1.35 \text{ W}$ in an 8 Ω load

$P_{O(RMS)1\%} = 2.35 \text{ W}$ in a 4 Ω load

The RMS output power at THD+N = 10 % can be estimated using [Equation 14](#):

$$P_{O(RMS)10\%} = 1.25 \times P_{O(RMS)1\%} \quad (14)$$

14.1.2 Output current limiting

OCP internally limits the peak output current $I_{O(max)}$. The minimum OCP trigger level is 1.3 A. During normal operation, the output current must not exceed this threshold level, otherwise the audio signal is distorted. The peak output current in BTL configuration can be calculated using [Equation 15](#):

$$I_{O(max)} \leq I_{O(OCP)} \leq \frac{V_{DDP}}{2 \times R_{DSon} + R_L} \leq 1.3A \quad (15)$$

Where:

V_{DDP} = power supply voltage (V)

R_L = load resistance (Ω)

R_{DSon} = drain-source on-state resistance (Ω)

Example:

A 4 Ω speaker can be used with a 5 V supply without triggering OCP.

14.2 PWM output filtering

The TFA8200 PWM power stage is optimized to meet the legal limits (FCC) for radiated emissions without requiring an external filter (speaker cable < 5 cm). However, a low-pass LC filter is recommended if a long speaker cable cannot be avoided or other components in the application are sensitive to frequencies in the 10 MHz to 150 MHz range (for example, an FM tuner). The suggested differential low-pass filter consists of a ferrite bead inductor ($Z > 80 \Omega$ at 100 MHz) and a small ceramic capacitor of about 1 nF (see [Figure 17](#)).

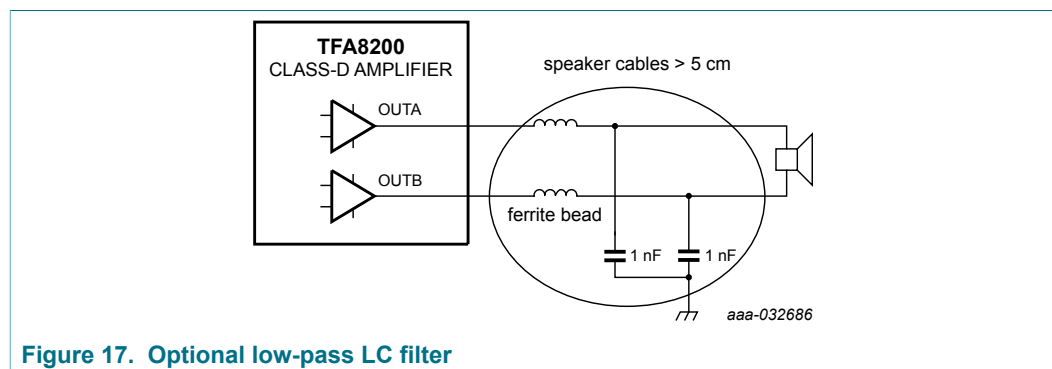


Figure 17. Optional low-pass LC filter

14.3 Supply decoupling and filtering

To minimize the size of the high-frequency current loop and therefore optimize EMC performance, a ceramic decoupling capacitor of between 1 μ F and 10 μ F must be placed close to the TFA8200. Optionally, to reduce the impedance further, a small 1 nF ceramic capacitor can be connected in parallel.

14.4 PCB layout considerations

When designing the PCB layout for a Class-D amplifier circuit, great care must be taken. The layout can affect the audio performance, the EMC performance, and/or the thermal performance. It can even affect the functionality of the TFA8200.

14.4.1 EMC considerations

The decoupling capacitors on pins V_{DD} , V_{DDP} , and STABA must be placed close to the TFA8200 and must be referenced to a solid ground plane. The exposed DAP must also be connected to this ground plane.

14.4.2 Thermal considerations

The TFA8200 is available in a thermally enhanced HVQFN24 (SOT616-3) package for reflow soldering. The HVQFN24 has an exposed DAP that significantly reduces the thermal resistance, $R_{th(j-a)}$. To achieve a lower overall thermal resistance, the exposed DAP must be soldered to a thermal copper plane. Increasing the area of the thermal plane, the number of planes, or the copper thickness can reduce the thermal resistance further. The typical thermal resistance (free air and natural convection) of a practical PCB implementation is:

$R_{th(j-a)} = 67^\circ\text{K/W}$ for a two-layer application board (18 mm × 22 mm, 35 μm copper, FR4 base material).

[Equation 16](#) describes the relationship between the maximum allowable power dissipation (P) and the thermal resistance from junction to ambient.

$$R_{th(j-a)} = \frac{T_{j(max)} - T_{amb}}{P} \quad (16)$$

Where:

$R_{th(j-a)}$ = thermal resistance from junction to ambient

$T_{j(max)}$ = maximum junction temperature (125 °C)

T_{amb} = ambient temperature

P = power dissipated in the TFA8200

To avoid thermal damage, OTP limits the maximum junction temperature to 130 °C.

14.5 Typical application diagram (simplified)

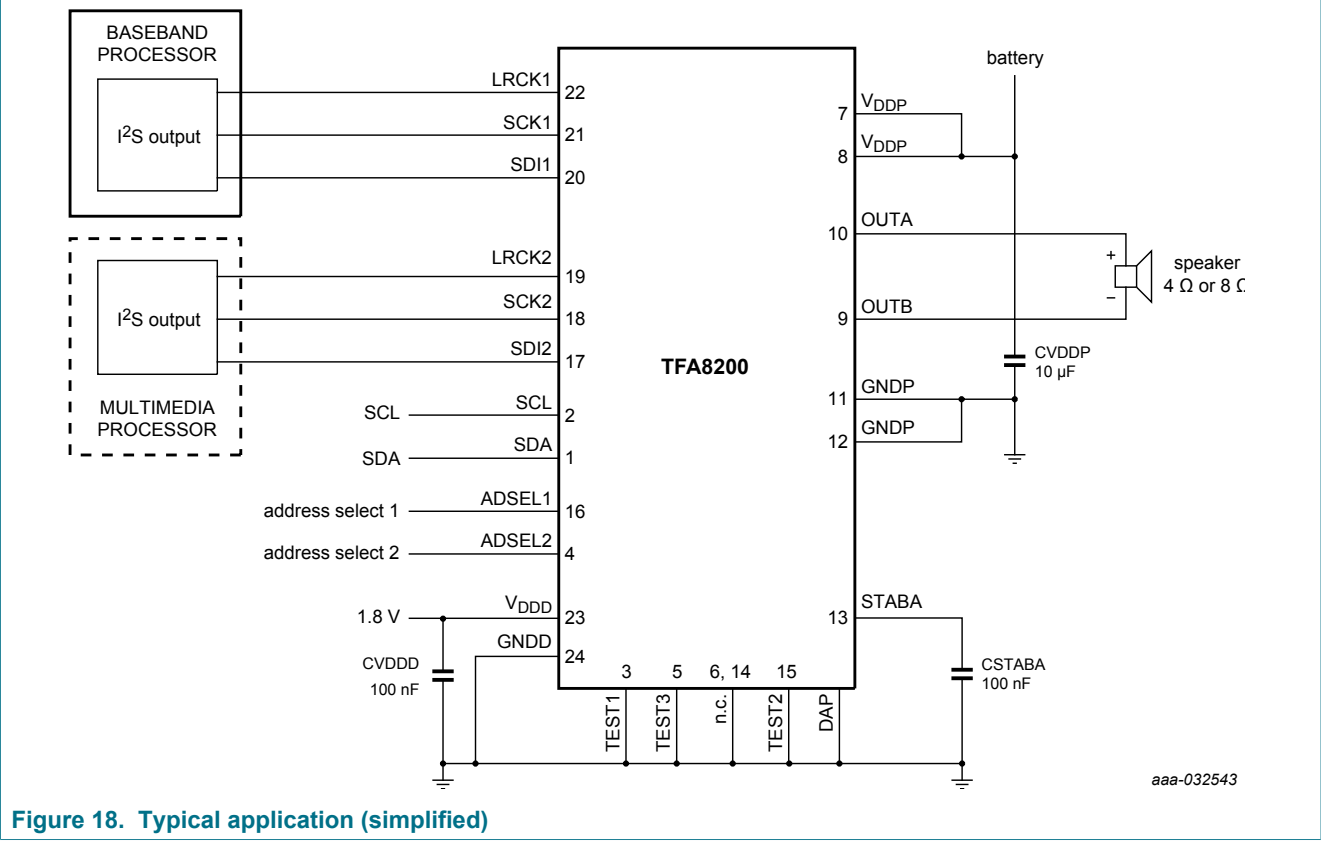
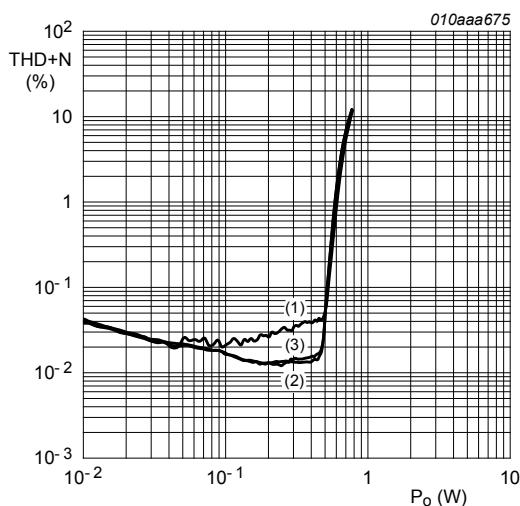


Figure 18. Typical application (simplified)

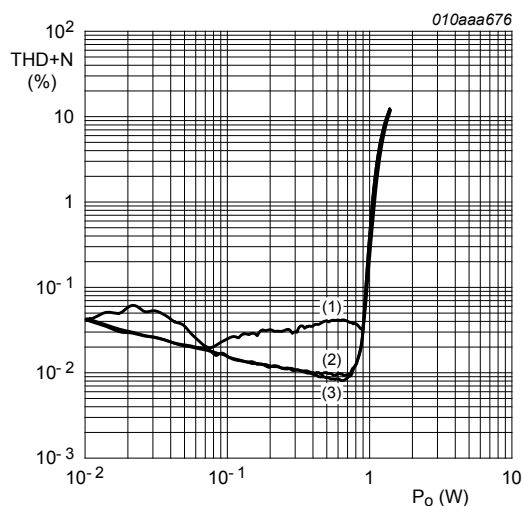
14.6 Curves measured in reference design (demonstration board)

All measurements were taken with $V_{DDP} = 1.8\text{ V}$; $f_s = 48\text{ kHz}$, clip control on; the high-pass filter off; unless otherwise specified.



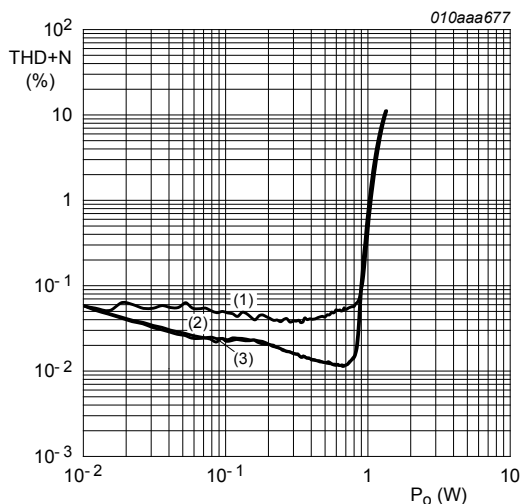
- (1) $f_i = 6\text{ kHz}$
- (2) $f_i = 1\text{ kHz}$
- (3) $f_i = 100\text{ Hz}$

a. $V_{DDP} = 3.7\text{ V}$; $R_L = 8\ \Omega$



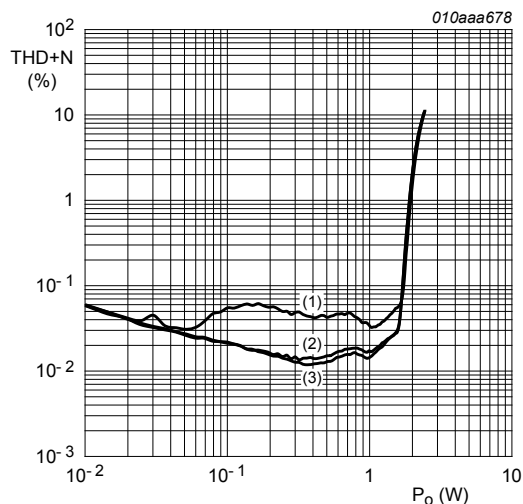
- (1) $f_i = 6\text{ kHz}$
- (2) $f_i = 1\text{ kHz}$
- (3) $f_i = 100\text{ Hz}$

b. $V_{DDP} = 5\text{ V}$; $R_L = 8\ \Omega$



- (1) $f_i = 6\text{ kHz}$
- (2) $f_i = 1\text{ kHz}$
- (3) $f_i = 100\text{ Hz}$

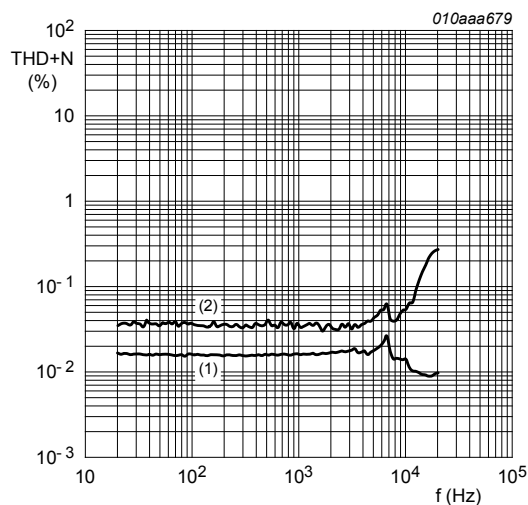
c. $V_{DDP} = 3.7\text{ V}$; $R_L = 4\ \Omega$



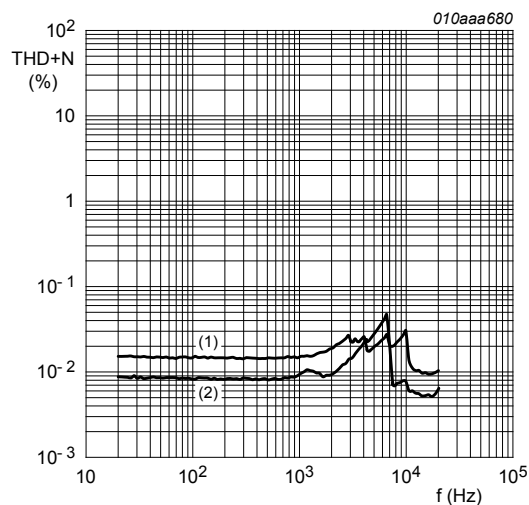
- (1) $f_i = 6\text{ kHz}$
- (2) $f_i = 1\text{ kHz}$
- (3) $f_i = 100\text{ Hz}$

d. $V_{DDP} = 5\text{ V}$; $R_L = 4\ \Omega$

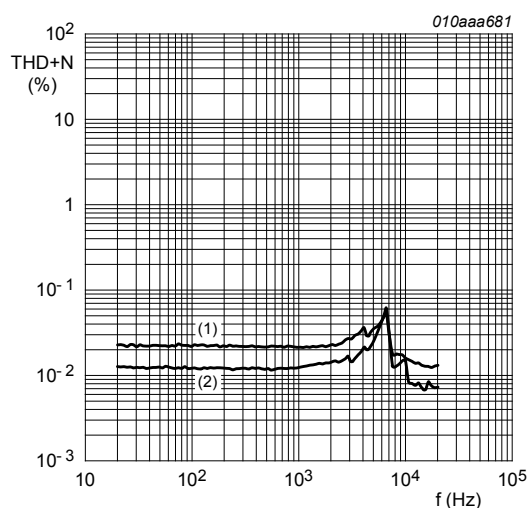
Figure 19. Total harmonic distortion-plus-noise as a function of output power



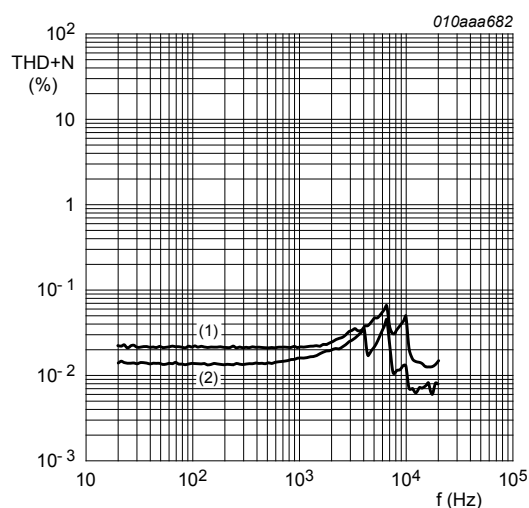
(1) $P_o = 100 \text{ mW}$
 (2) $P_o = 500 \text{ mW}$
 a. $V_{DDP} = 3.7 \text{ V}$; $R_L = 8 \Omega$



1. $P_o = 100 \text{ mW}$
 2. $P_o = 500 \text{ mW}$
 b. $V_{DDP} = 5 \text{ V}$; $R_L = 8 \Omega$

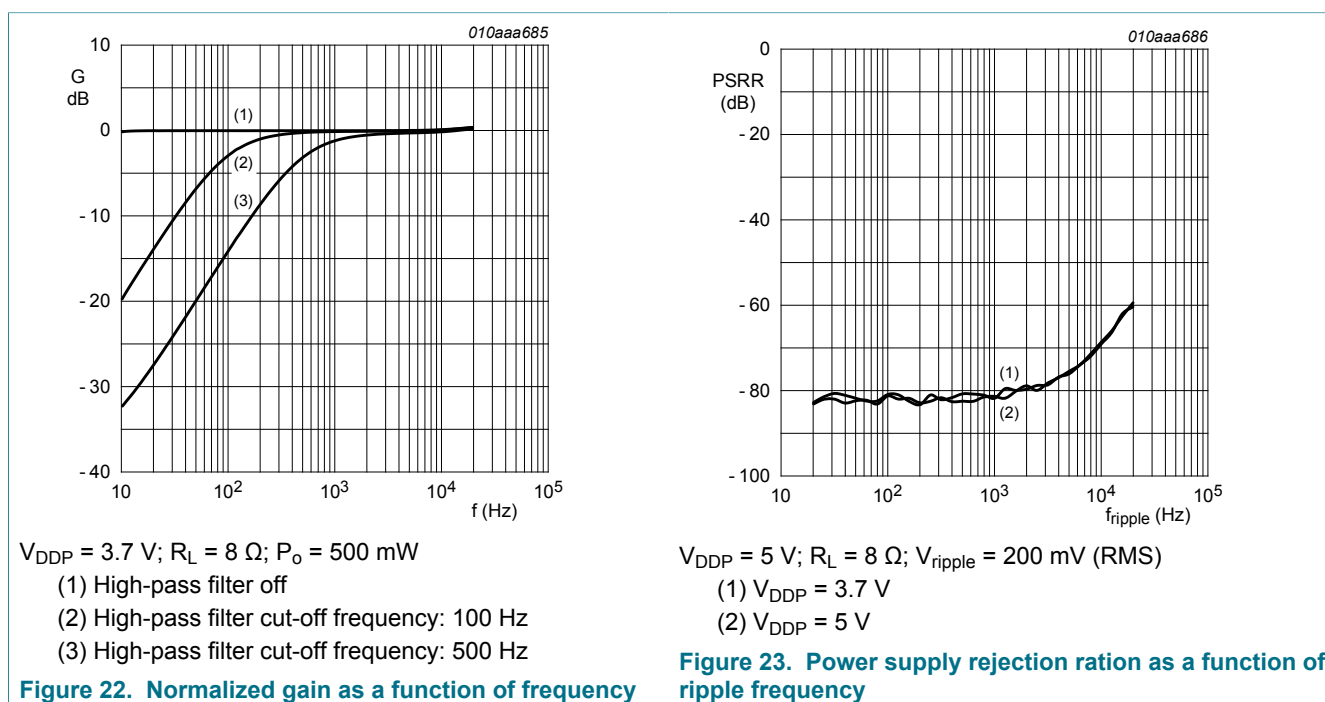
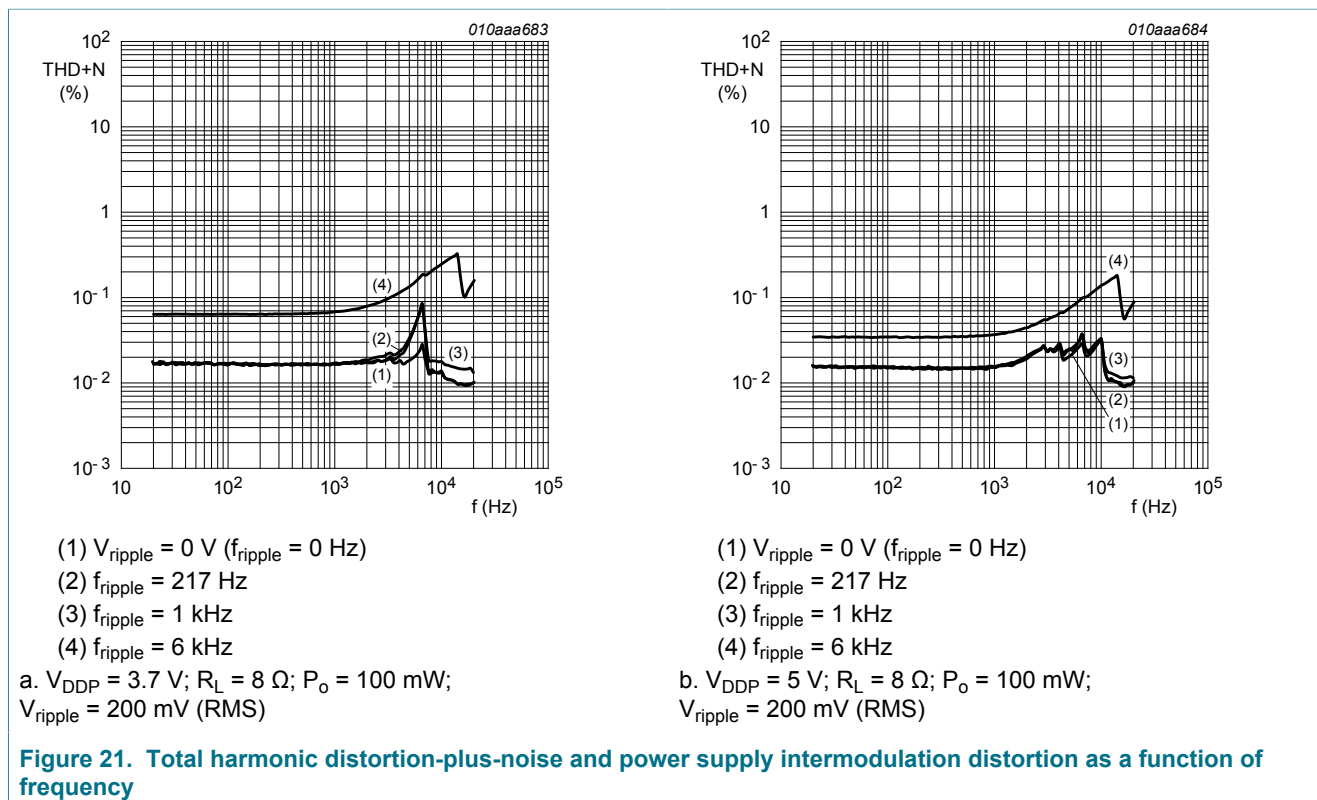


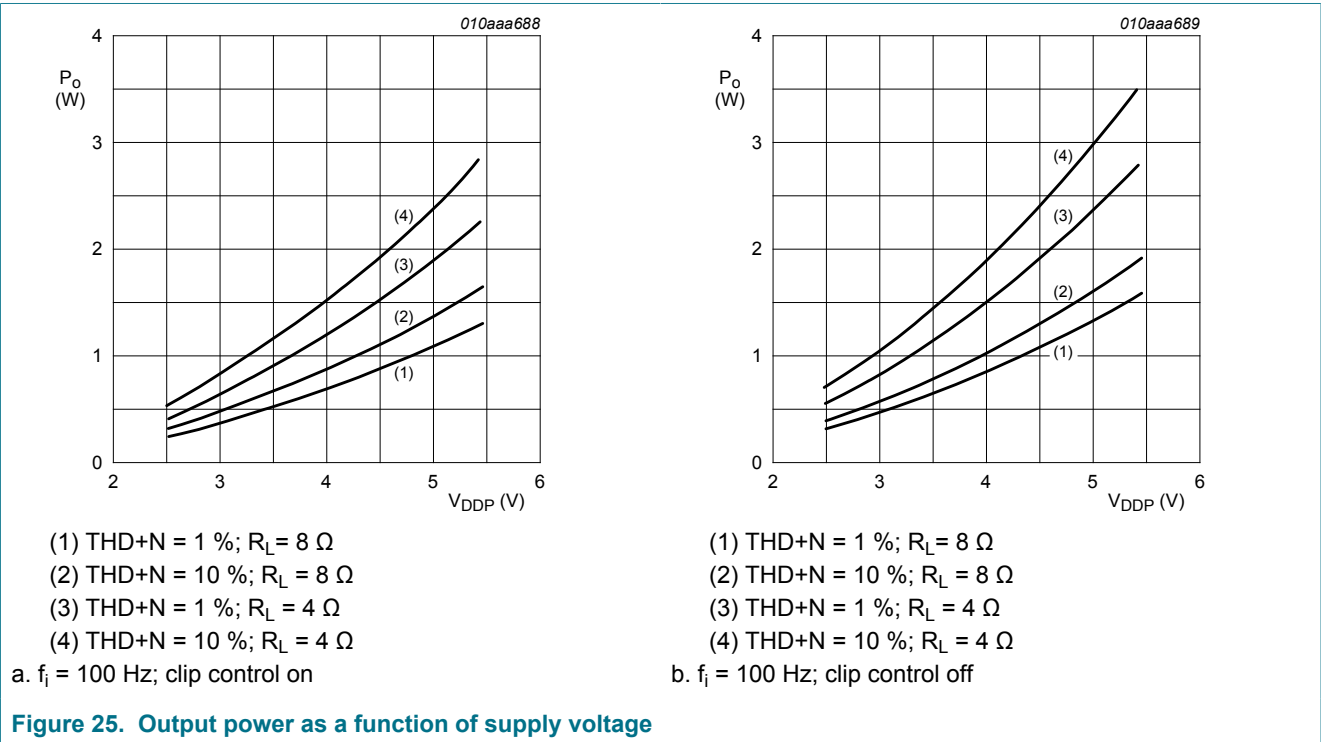
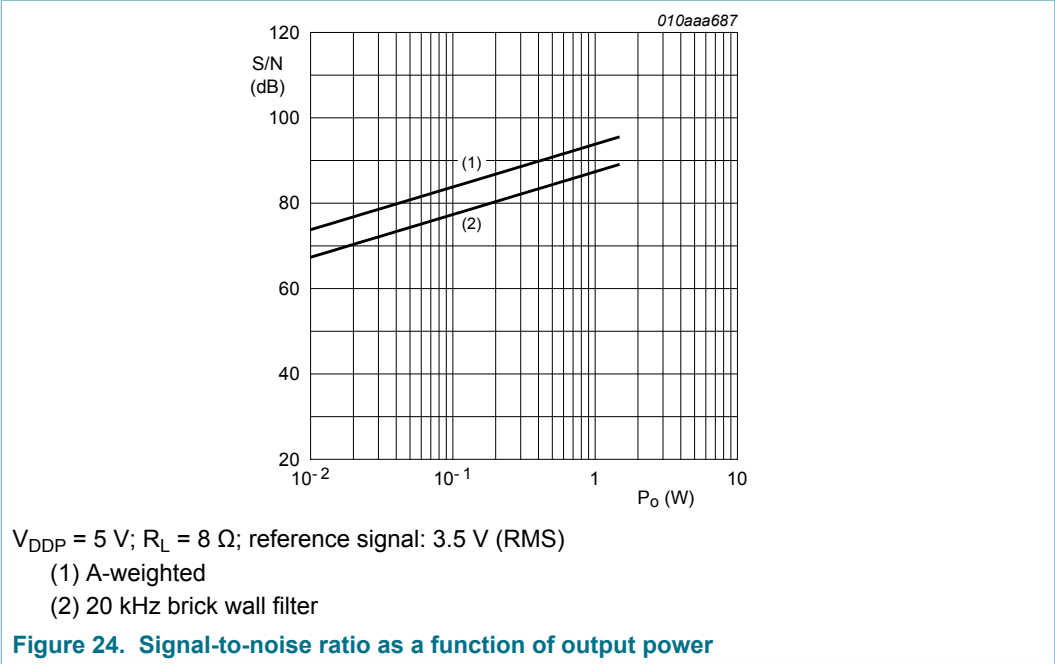
(1) $P_o = 100 \text{ mW}$
 (2) $P_o = 500 \text{ mW}$
 c. $V_{DDP} = 3.7 \text{ V}$; $R_L = 4 \Omega$

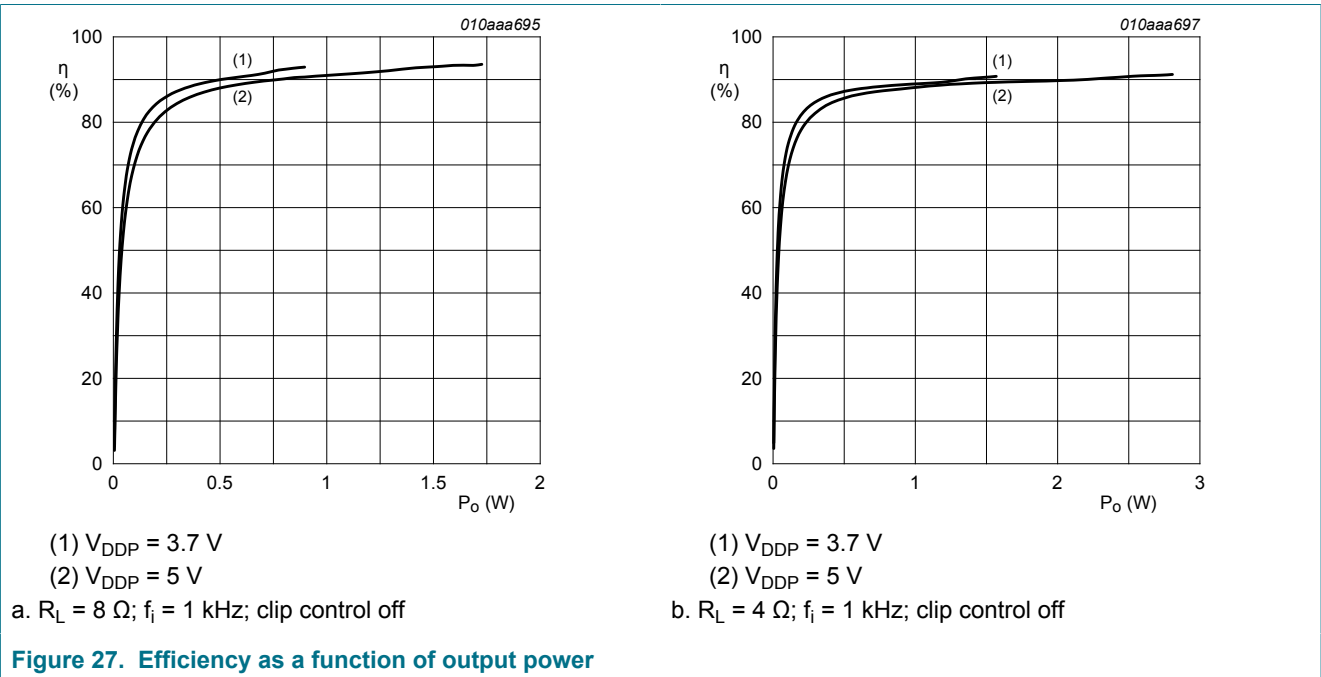
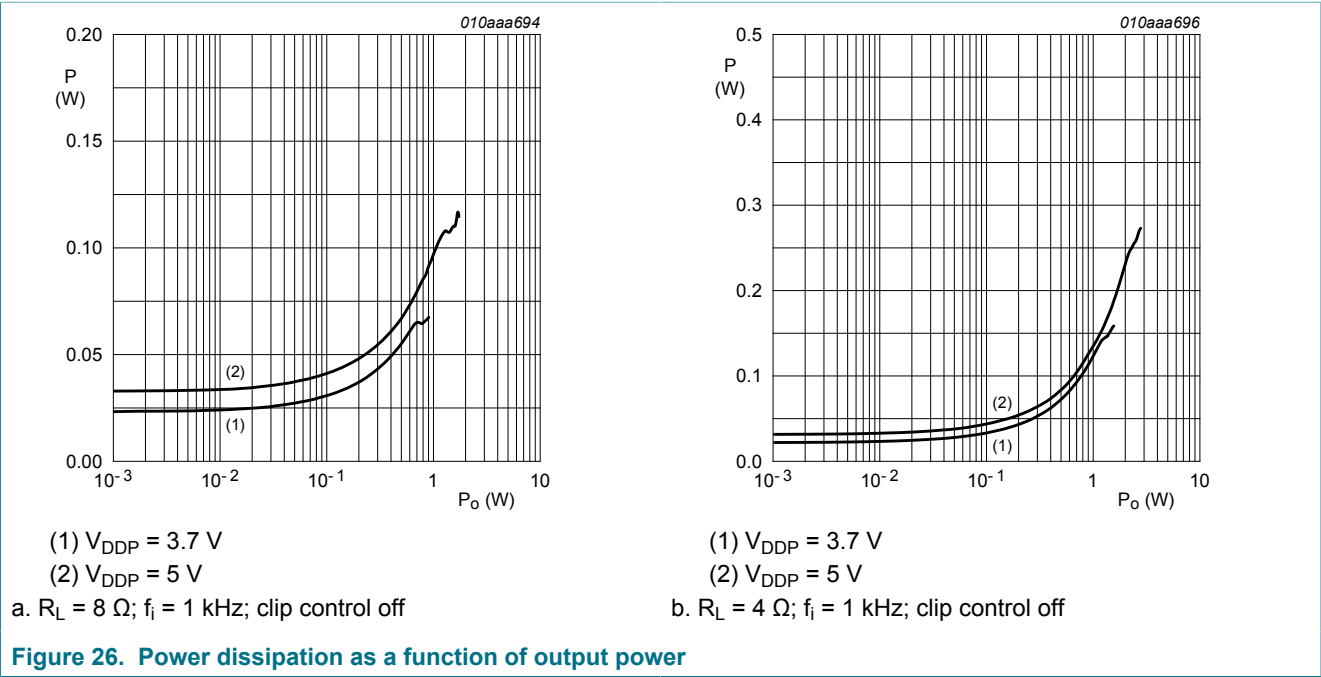


(1) $P_o = 100 \text{ mW}$
 (2) $P_o = 1 \text{ W}$
 d. $V_{DDP} = 5 \text{ V}$; $R_L = 4 \Omega$

Figure 20. Total harmonic distortion-plus-noise as a function of frequency







15 Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm

SOT616-3

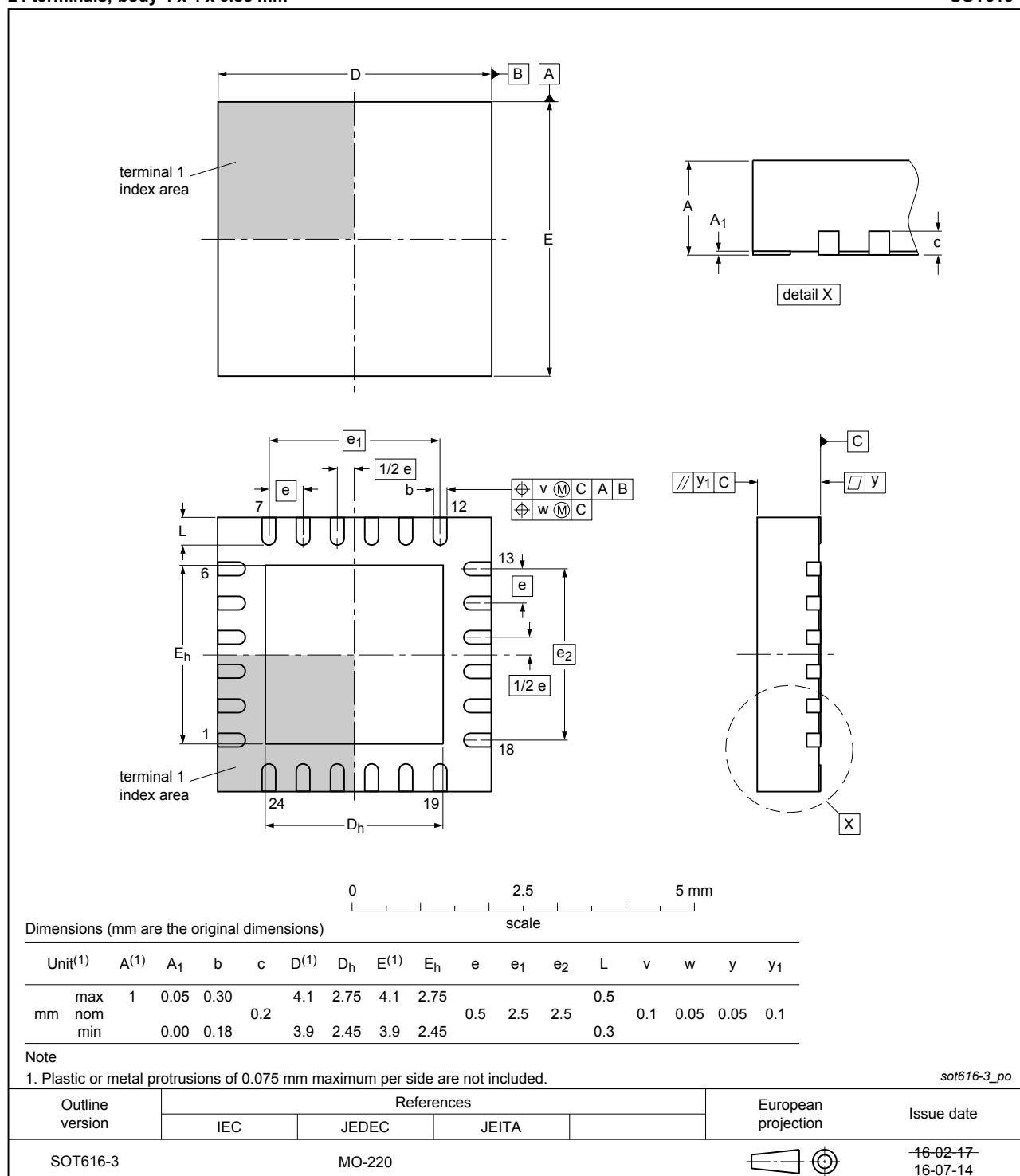


Figure 28. Package outline TFA8200 (HVQFN24)

16 Soldering of SMD packages

This section gives a very brief insight into a complex technology. An in-depth account of soldering ICs can be found in the "Surface mount reflow soldering description" application note (AN10365).

16.1 Introduction to soldering

To form electrical circuits, soldering is one of the most common methods through which packages are attached to printed-circuit boards (PCBs). The soldered joint provides the mechanical connection and the electrical connection. No single soldering method is ideal for all IC packages. When through-hole and surface mount devices (SMDs) are mixed on one printed wiring board, wave soldering is often preferred. However, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology with which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave-soldered. Packages with solder balls and some leadless packages which have solder lands underneath the body cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave soldering and reflow soldering are:

- Board specifications, including the board finish, solder masks, and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering
A lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 29](#)) than a SnPb process, therefore reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile
This profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough, so the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume. It is classified in accordance with [Table 42](#) and [Table 43](#).

Table 42. SnPb eutectic process (from J-STD-020D)

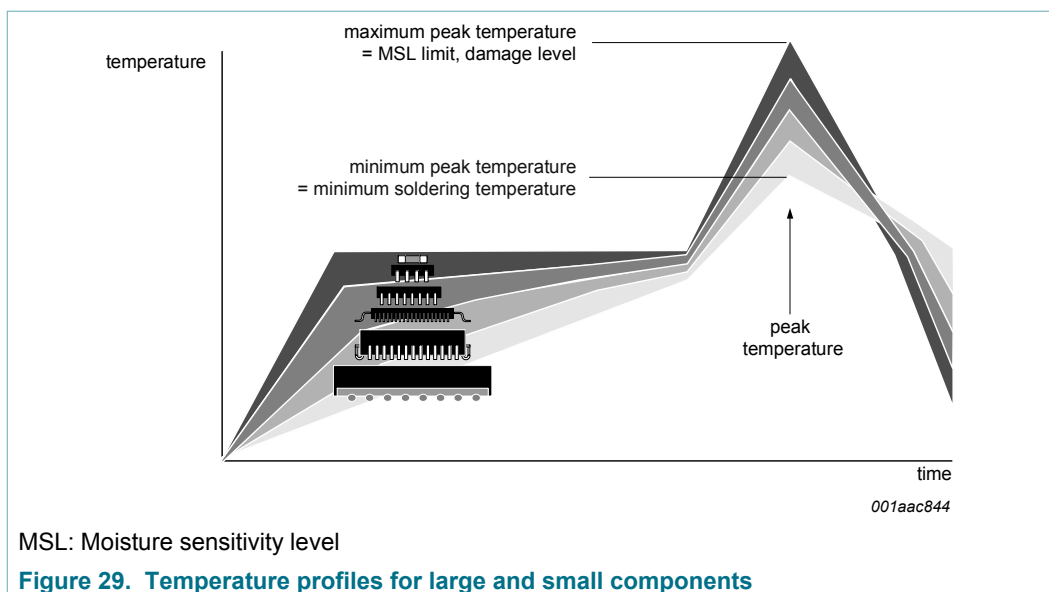
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 43. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must always be respected.

Studies have shown that small packages reach higher temperatures during reflow soldering (see [Figure 29](#)).



For further information on temperature profiles, refer to the "Surface mount reflow soldering description" application note (AN10365).

17 Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA8200 v.1	20190819	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Mono BTL class-D audio amplifier with digital inputs for IOT applications

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