

74LV74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 3 — 9 September 2013

Product data sheet

1. General description

The 74LV74 is a dual positive edge triggered, D-type flip-flop. It has individual data (nD) inputs, clock (nCP) inputs, set (nSD) and (nRD) inputs, and complementary nQ and nQ outputs.

The set and reset are asynchronous active LOW inputs that operate independently of the clock input. Information on the data input is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse. The nD inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114-A exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

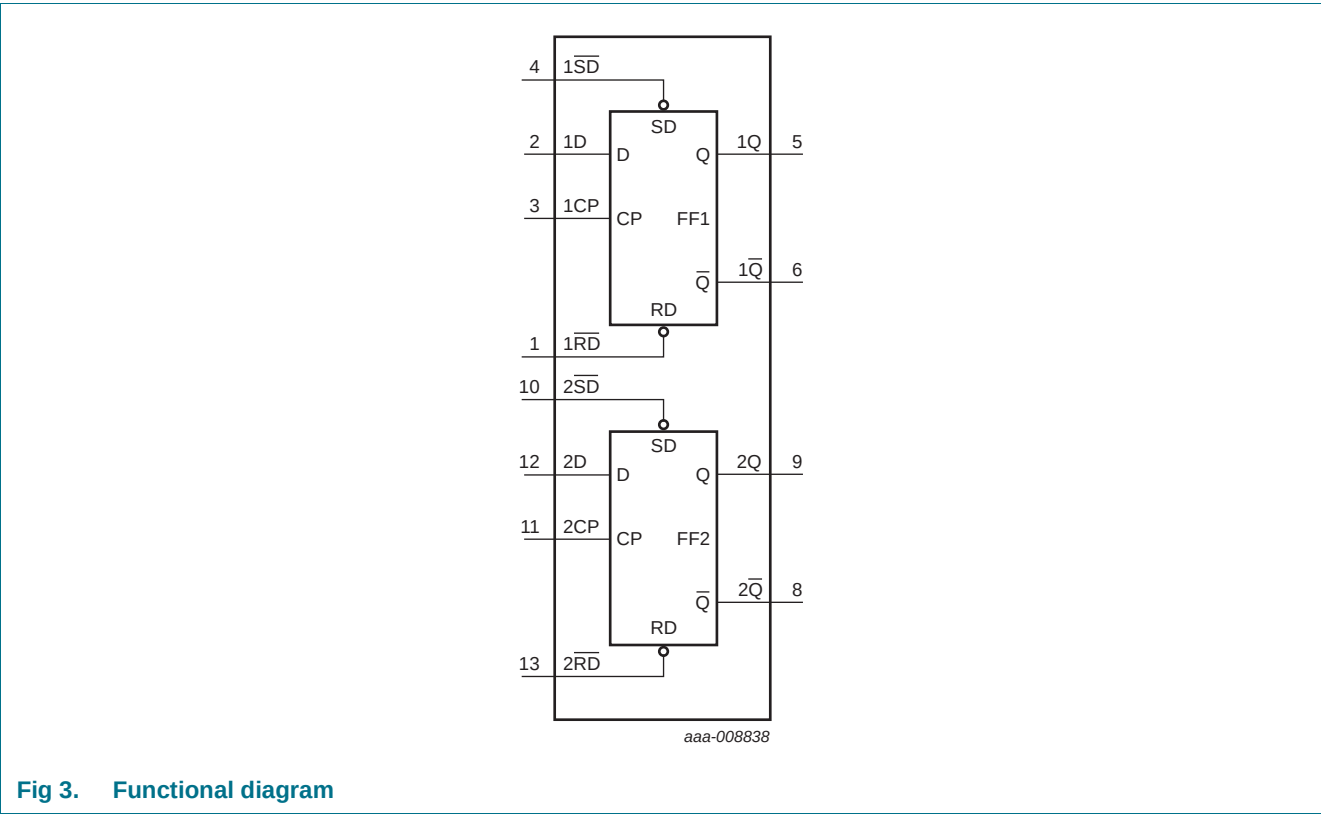
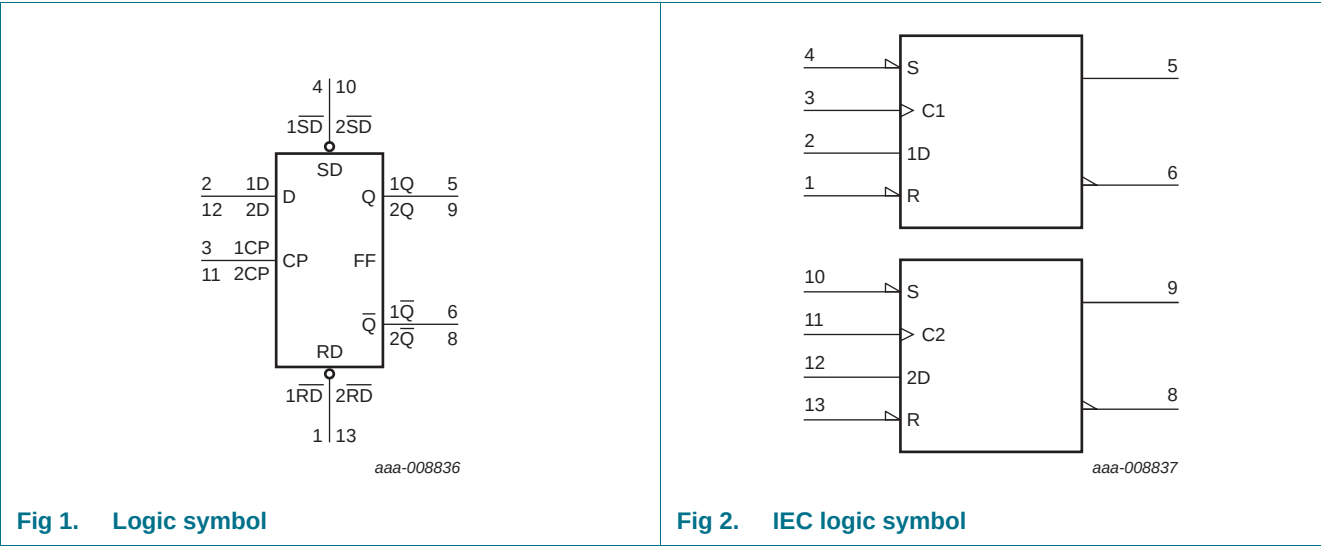
3. Ordering information

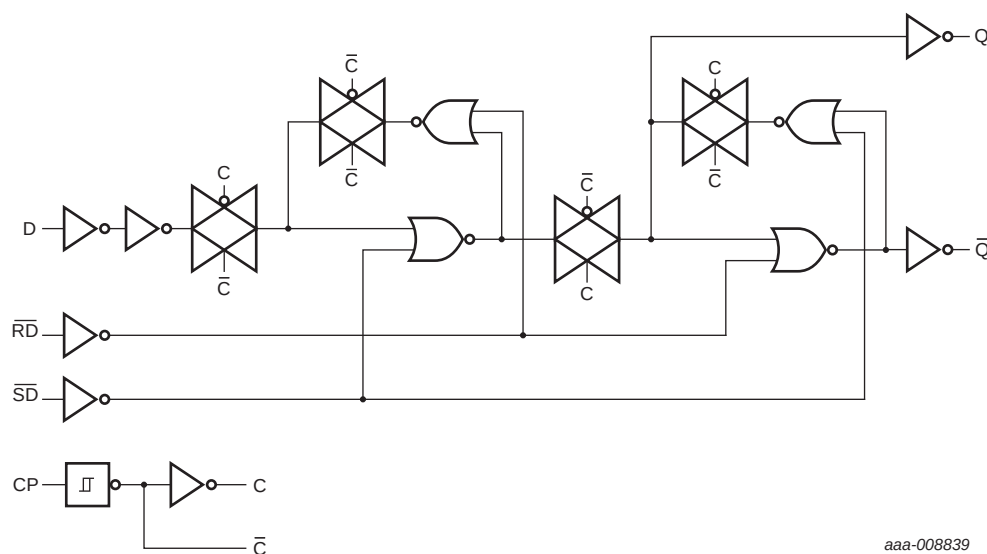
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV74N	-40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV74DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



4. Functional diagram





aaa-008839

Fig 4. Logic diagram (one flip-flop)

5. Pinning information

5.1 Pinning

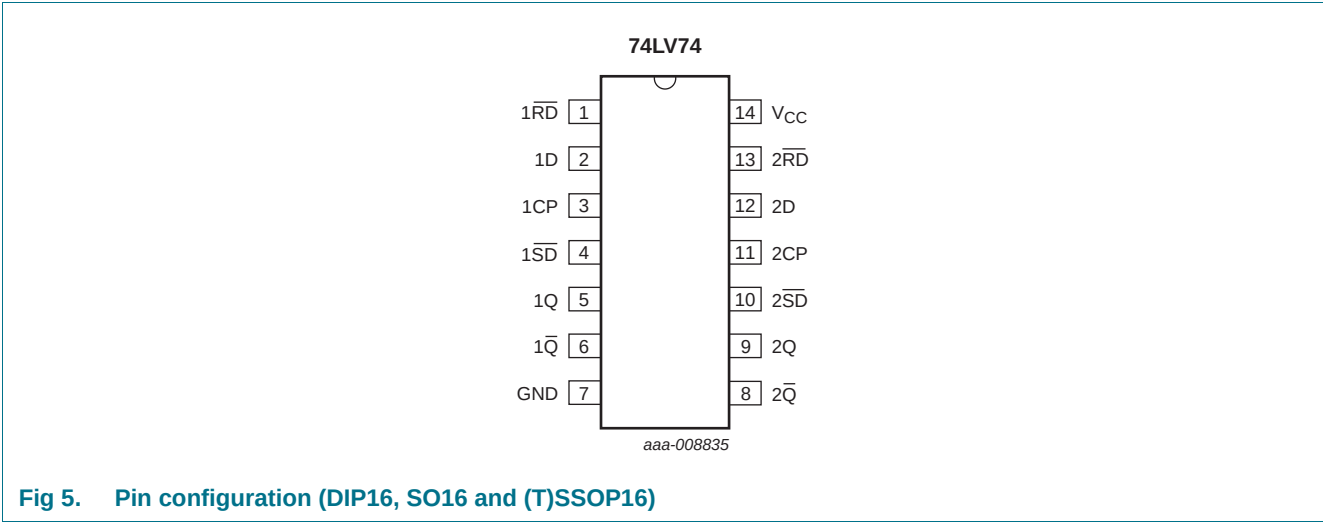


Fig 5. Pin configuration (DIP16, SO16 and (T)SSOP16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset-direct input (active-LOW)
1D	2	data inputs
1CP	3	clock input (LOW-to-HIGH), edge-triggered)
1SD	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop outputs
1Q	6	complement flip-flop outputs
GND	7	ground (0 V)
2Q	8	complement flip-flop outputs
2Q	9	true flip-flop outputs
2SD	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered)
2D	12	data inputs
2RD	13	asynchronous reset-direct input (active-LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input				Output			
nSD	nRD	nCP	nD	nQ	nQ̄	Q _{n+1}	nQ̄ _{n+1}
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 ↑ = LOW-to-HIGH clock transition;
 Q_{n+1} = state after the next LOW-to-HIGH CP transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	20	mA
V _I	input voltage		-0.5	+7	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	±50	mA
I _{GND}	ground current		-	±50	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		DIP16 package	^[2] -	750	mW
		SO16 package	^[3] -	500	mW
		(T)SSOP16 package	^[4] -	400	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] P_{tot} derates linearly with 12 mW/K above 70 °C.
 [3] P_{tot} derates linearly with 8 mW/K above 70 °C.
 [4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage ^[1]		1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	0	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	0	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	100	ns/V
		$V_{CC} = 3.6\text{ V to }5.5\text{ V}$	0	-	50	ns/V

[1] LV is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	0.7 × V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	-	0.3 × V _{CC}	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = –100 µA						
		V _{CC} = 1.2 V	-	1.2	-	-	-	
		V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		standard outputs: V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = –6 mA	2.40	2.82	-	2.20	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 100 µA						
		V _{CC} = 1.2 V	-	0	-	-	-	
		V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		standard outputs: V _I = V _{IH} or V _{IL}						
		V _{CC} = 3.0 V; I _O = 6 mA	-	0.25	0.40	-	0.50	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20	-	80	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} – 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	µA
C _I	input capacitance		-	3.5	-			pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see [Figure 8](#)

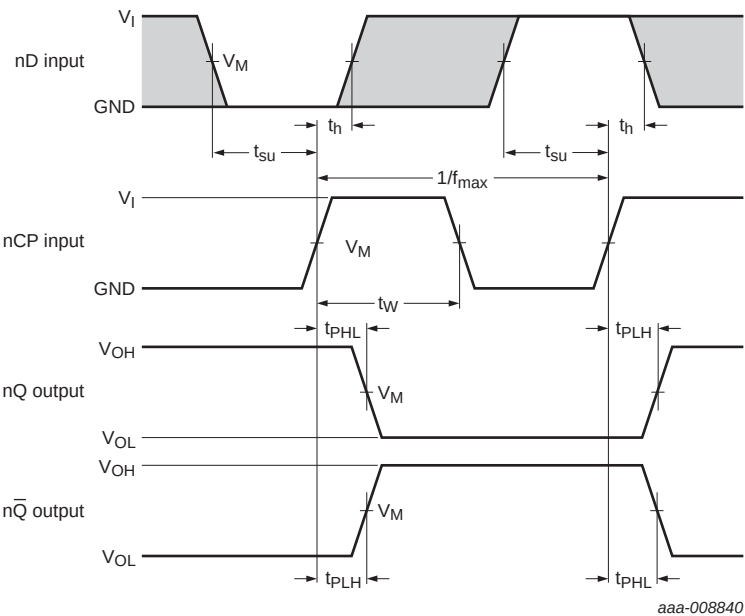
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n $\overline{Q}$; see Figure 6 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	70	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	24	44	-	56	ns
		$V_{CC} = 2.7\text{ V}$	-	18	28	-	41	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	13	26	-	33	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	11	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	-	9.5	17	-	23	ns
		n $\overline{SD}$ to nQ, n $\overline{Q}$; see Figure 7						
		$V_{CC} = 1.2\text{ V}$	-	90	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	31	46	-	58	ns
		$V_{CC} = 2.7\text{ V}$	-	23	34	-	43	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	17	27	-	34	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	14	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	-	12	19	-	24	ns
		n $\overline{RD}$ to nQ, n $\overline{Q}$; see Figure 7						
		$V_{CC} = 1.2\text{ V}$	-	90	-	-	-	ns
		$V_{CC} = 2.0\text{ V}$	-	31	46	-	58	ns
		$V_{CC} = 2.7\text{ V}$	-	23	34	-	43	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	-	17	27	-	34	ns
		$V_{CC} = 3.3\text{ V}; C_L = 15\text{ pF}$	-	14	-	-	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	-	12	19	-	24	ns
t_w	pulse width	nCP input HIGH to LOW; see Figure 6						
		$V_{CC} = 2.0\text{ V}$	34	10	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	20	7	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	15	6	-	18	-	ns
		n $\overline{SD}$ or n $\overline{RD}$ pulse width LOW; see Figure 7						
		$V_{CC} = 2.0\text{ V}$	34	10	-	41	-	ns
		$V_{CC} = 2.7\text{ V}$	25	8	-	30	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ^[3]	20	7	-	24	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ^[4]	15	6	-	18	-	ns

Table 7. Dynamic characteristics ...continuedGND (ground = 0 V): for test circuit, see [Figure 8](#)

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{rec}	recovery time	nRD; see Figure 7						
		V _{CC} = 1.2 V	-	5	-	-	-	ns
		V _{CC} = 2.0 V	14	2	-	15	-	ns
		V _{CC} = 2.7 V	10	1	-	11	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	8	1	-	9	-	ns
		V _{CC} = 4.5 V to 5.5 V ^[4]	6	1	-	7	-	ns
t _{su}	set-up time	nD to nCP; see Figure 6						
		V _{CC} = 1.2 V	-	10	-	-	-	ns
		V _{CC} = 2.0 V	22	4	-	26	-	ns
		V _{CC} = 2.7 V	12	3	-	15	-	ns
		V _{CC} = 3.0 V to 3.6 V ^[3]	8	2	-	10	-	ns
		V _{CC} = 4.5 V to 5.5 V ^[4]	6	1	-	8	-	ns
t _h	hold time	nD to nCP; see Figure 6						
		V _{CC} = 1.2 V	-	–10	-	-	-	ns
		V _{CC} = 2.0 V	3	–2	-	3	-	ns
		V _{CC} = 2.7 V	3	–2	-	3	-	ns
		V _{CC} = 3.0 V to 3.6 V	3	–2	-	3	-	ns
		V _{CC} = 4.5 V to 5.5 V	3	–2	-	3	-	ns
f _{max}	maximum frequency	nCP; see Figure 6						
		V _{CC} = 2.0 V	14	40	-	12	-	MHz
		V _{CC} = 2.7 V	50	90	-	40	-	MHz
		V _{CC} = 3.0 V to 3.6 V ^[3]	60	100	-	48	-	MHz
		V _{CC} = 4.5 V to 5.5 V ^[4]	70	110	-	56	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ^[5]	-	24	-	-	-	pF

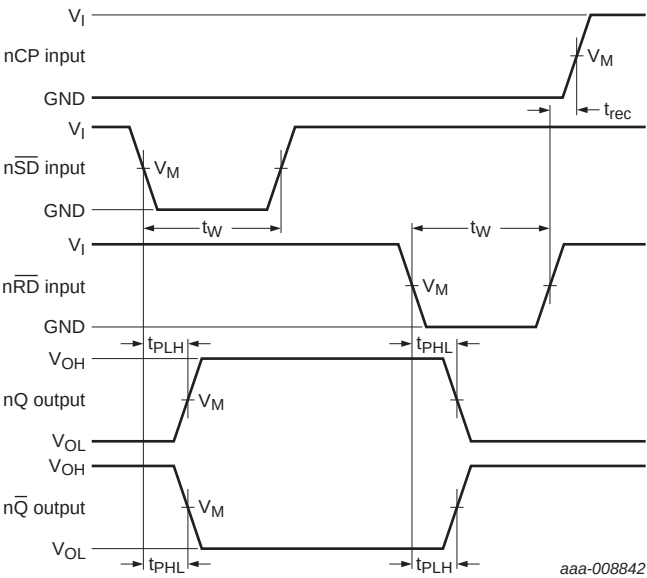
[1] Typical values are measured at T_{amb} = 25 °C.[2] t_{pd} is the same as t_{PHL} and t_{PLH}.[3] Typical value measured at V_{CC} = 3.3 V.[4] Typical values are measured at V_{CC} = 5.0 V.[5] C_{PD} is used to determine the dynamic power dissipation P_D = C_{PD} × V_{CC}² × f_i + Σ (C_L × V_{CC}² × f_o) (P_D in μW), where:f_i = input frequency in MHz;f_o = output frequency in MHz;Σ (C_L × V_{CC}² × f_o) = sum of outputs;C_L = output load capacitance in pF;V_{CC} = supply voltage in V.

11. Waveforms



Measurement points are given in [Table 8](#).
The shaded areas indicate when the input is permitted to change for predictable output performance.

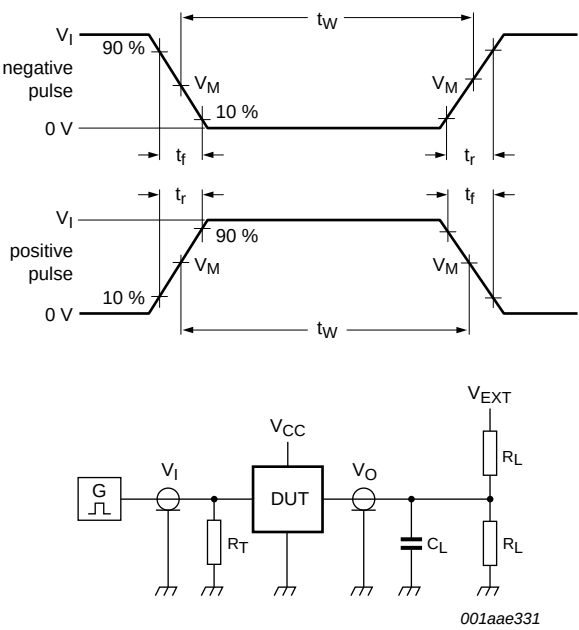
Fig 6. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width and maximum frequency



Measurement points are given in [Table 8](#).
Fig 7. The set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nRD to nCP recovery time

Table 8. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
< 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	0.5V _{CC}	0.5V _{CC}



001aae331

Test data is given in [Table 9](#).
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}
	V _I	t _r , t _f	C _L	R _L	t _{PHL} , t _{PLH}
< 2.7 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 kΩ	open
≥ 4.5 V	V _{CC}	2.5 ns	50 pF	1 kΩ	open

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

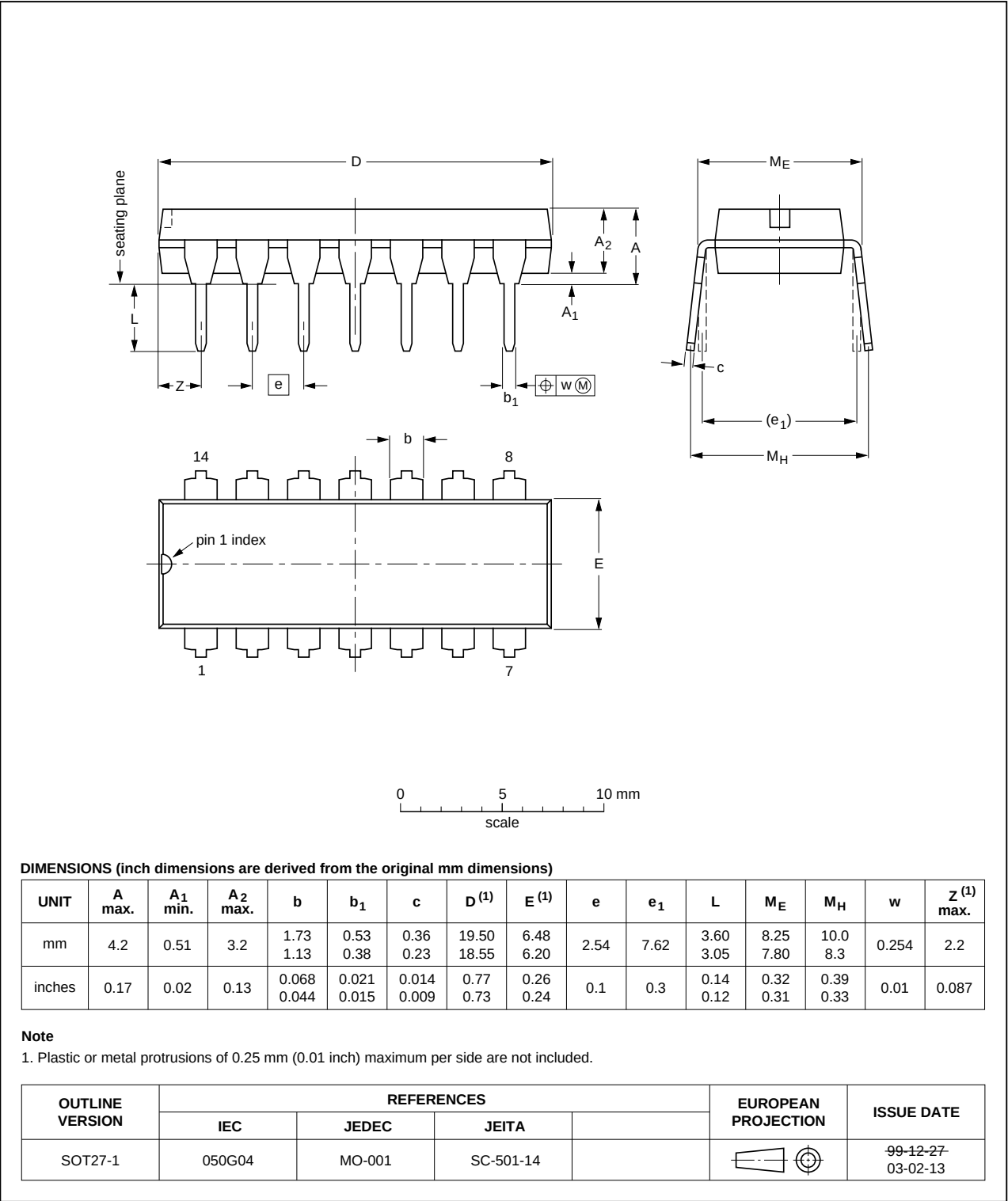


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

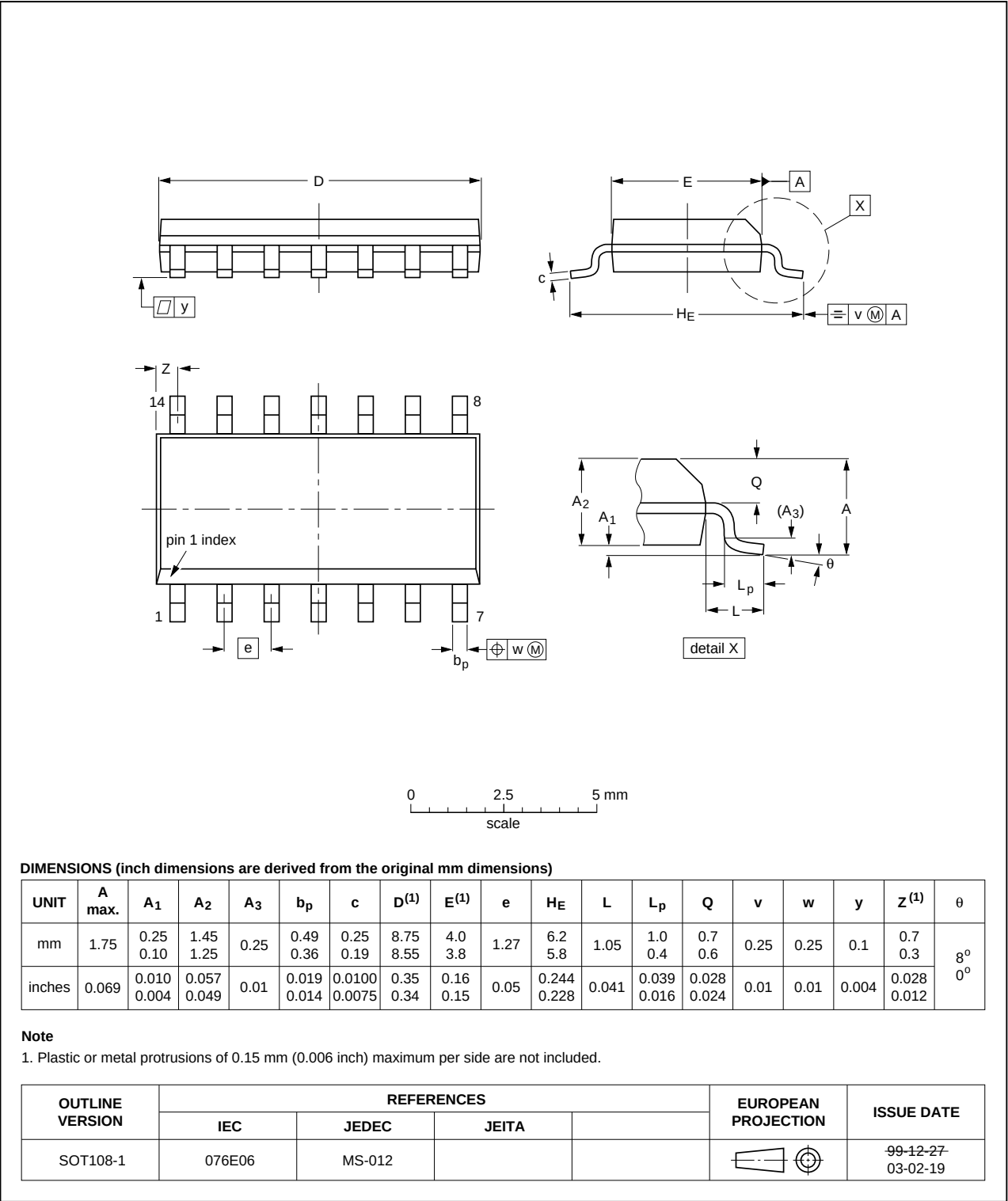


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

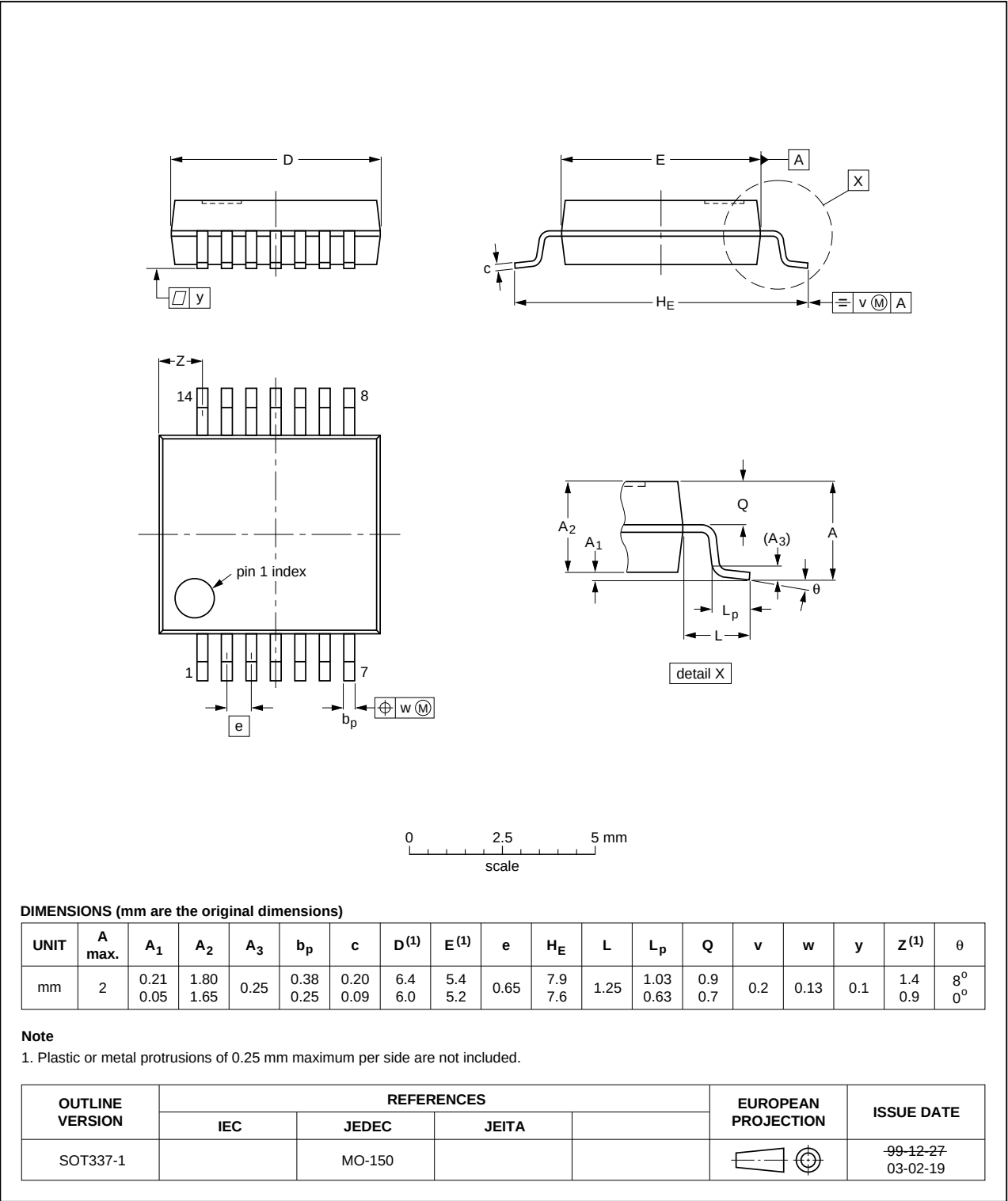


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

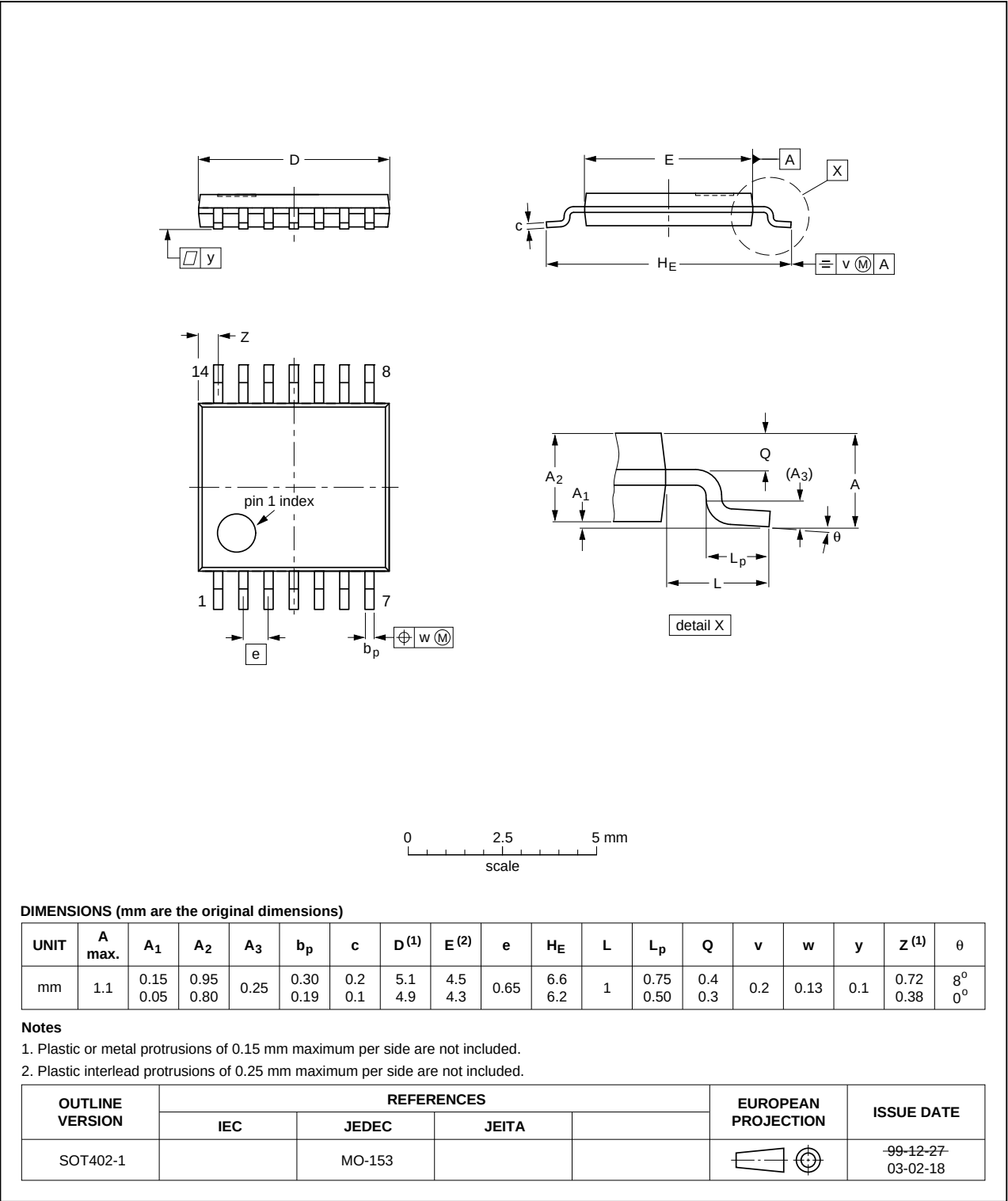


Fig 12. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74 v.3	20130909	Product data sheet	-	74LV74_CNV v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Family data added, see Section 9 "Static characteristics"			
74LV74_CNV v.2	April 1998	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
7	Limiting values	5
8	Recommended operating conditions	6
9	Static characteristics	7
10	Dynamic characteristics	8
11	Waveforms	10
12	Package outline	12
13	Abbreviations	16
14	Revision history	16
15	Legal information	17
15.1	Data sheet status	17
15.2	Definitions	17
15.3	Disclaimers	17
15.4	Trademarks	18
16	Contact information	18
17	Contents	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 September 2013

Document identifier: 74LV74