

LM831 Low Voltage Audio Power Amplifier

General Description

The LM831 is a dual audio power amplifier optimized for very low voltage operation. The LM831 has two independent amplifiers, giving stereo or higher power bridge (BTL) operation from two- or three-cell power supplies.

The LM831 uses a patented compensation technique to reduce high-frequency radiation for optimum performance in AM radio applications. This compensation also results in lower distortion and less wide-band noise.

The input is direct-coupled to the LM831, eliminating the usual coupling capacitor. Voltage gain is adjustable with a single resistor.

Features

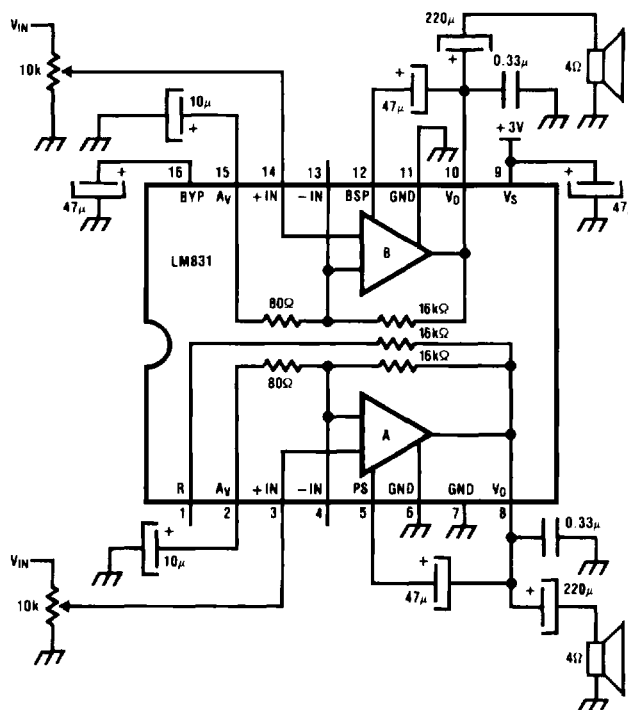
- Low voltage operation, 1.8V to 6.0V
- High power, 440 mW, 8 Ω , BTL, 3V
- Low AM radiation
- Low noise
- Low THD

Applications

- Portable tape recorders
- Portable radios
- Headphone stereo
- Portable speakers

Typical Application

Dual Amplifier with Minimum Parts



TL/H/6754-1

A_V 46 dB, BW $\pm$ 250 Hz to 35 kHz

P_{OUT} 220 mW/Ch, R_L 4 Ω

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	7.5V
Input Voltage, V_{IN}	$\pm 0.4V$
Power Dissipation (Note 1), P_D	1.3W (M Package) 1.4W (N Package)
Operating Temperature (Note 1), T_{opr}	40°C to $+85^\circ\text{C}$

Storage Temperature, T_{stg}	65°C to $+150^\circ\text{C}$
Junction Temperature, T_j	$+150^\circ\text{C}$
Lead Temp. (Soldering, 10 sec.), T_L	$+260^\circ\text{C}$
Thermal Resistance	
θ_{JC} (DIP)	27°C/W
θ_{JA} (DIP)	75°C/W
θ_{JC} (SO Package)	20°C/W
θ_{JA} (SO Package)	95°C/W

Electrical Characteristics

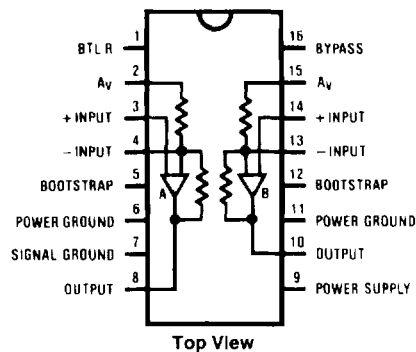
Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_S = 3V$, $f = 1\text{ kHz}$, test circuit is dual or BTL amplifier with minimum parts.

Symbol	Parameter	Conditions	Typ	Tested Limit	Unit (Limit)
V_S	Operating Voltage		3 3	1.8 6	V (Min) V (Max)
I_Q	Supply Current	$V_{IN} = 0$, Dual Mode $V_{IN} = 0$, BTL Mode	5 6	10 15	mA (Max) mA (Max)
V_{OS}	Output DC Offset	$V_{IN} = 0$, BTL Mode	10	50	mV (Max)
R_{IN}	Input Resistance		25	15 35	k (Min) k (Max)
A_v	Voltage Gain	$V_{IN} = 2.25\text{ mV}_{rms}$, $f = 1\text{ kHz}$, Dual Mode	46	44 48	dB (Min) dB (Max)
PSRR	Supply Rejection	$V_S = 3V + 200\text{ mV}_{rms}$ @ $f = 1\text{ kHz}$	46	30	dB (Min)
P_{OD}	Power Out	$V_S = 3V$, $R_L = 4\Omega$, 10% THD, Dual Mode	220	150	mW (Min)
P_{ODL}	Power Out Low, V_S	$V_S = 1.8V$, $R_L = 4\Omega$, 10% THD, Dual Mode	45	10	mW (Min)
P_{OB}	Power Out	$V_S = 3V$, $R_L = 8\Omega$, 10% THD, BTL Mode	440	300	mW (Min)
P_{OBL}	Power Out Low, V_S	$V_S = 1.8V$, $R_L = 8\Omega$, 10% THD, BTL Mode	90	20	mW (Min)
Sep	Channel Separation	Referenced to V_O 200 mV_{rms}	52	40	dB (Min)
I_B	Input Bias Current		1	2	μA (Max)
E_{n0}	Output Noise	Wide Band (250 ~ 35 kHz)	250	500	μV (Max)
THD	Distortion	$V_S = 3V$, $P_O = 50\text{ mW}$, $f = 1\text{ kHz}$, Dual	0.25	1	% (Max)

Note 1: For operation in ambient temperatures above 25°C , the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 98°C/W junction to ambient for the M package or 90°C/W junction to ambient for the N package.

Connection Diagram

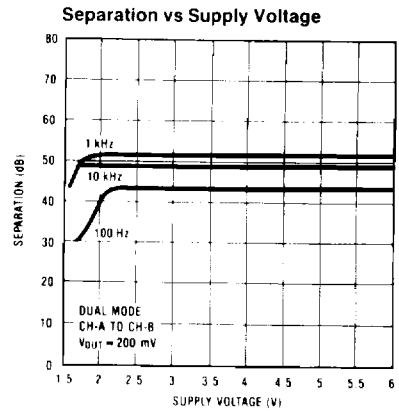
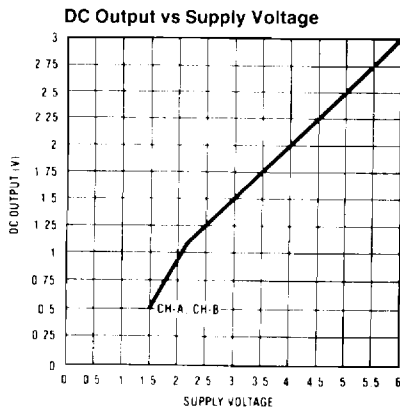
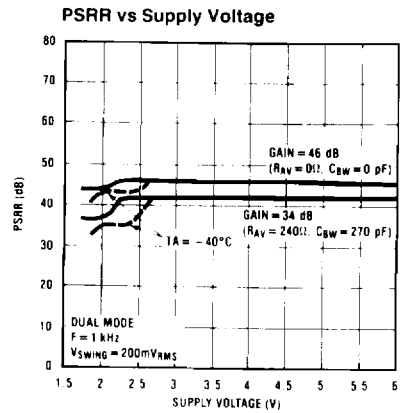
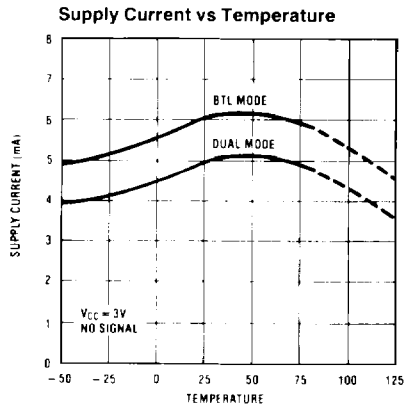
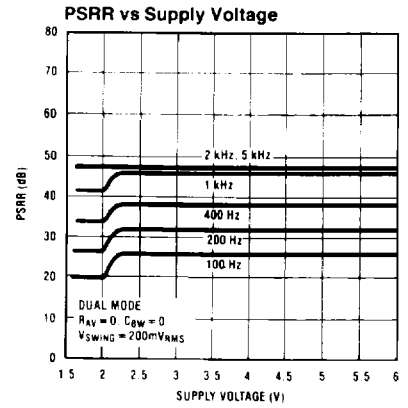
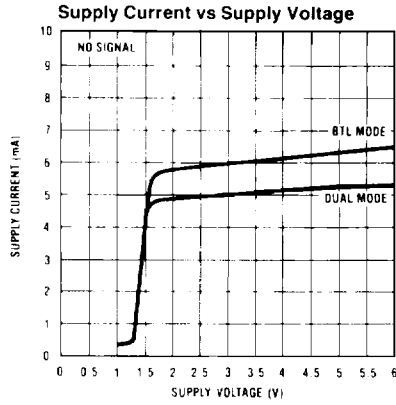
Dual-In-Line Package



Order Number LM831M or N
See NS Package Number M16B or N16E

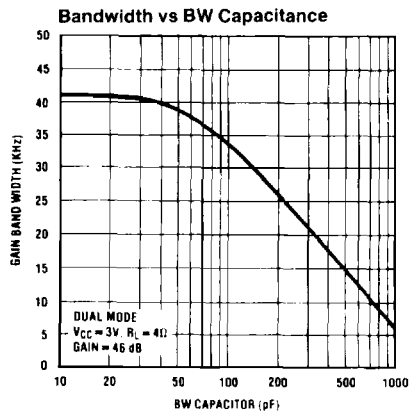
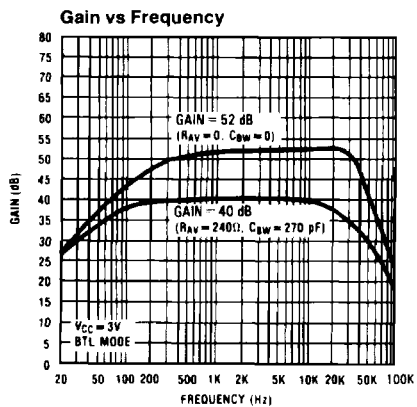
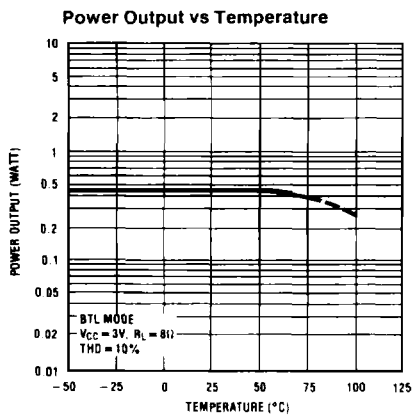
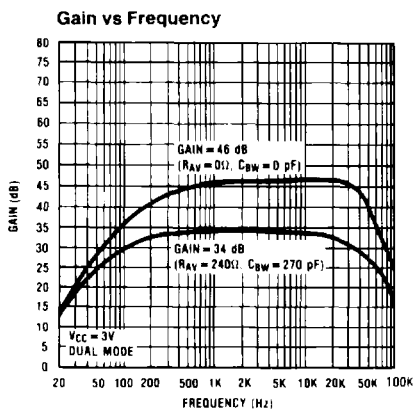
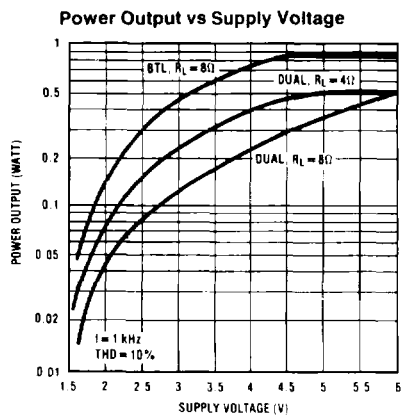
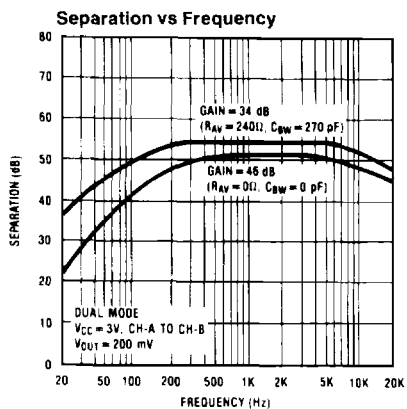
TL/H/6754-2

Typical Performance Characteristics



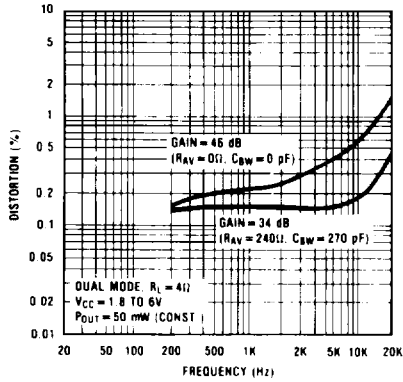
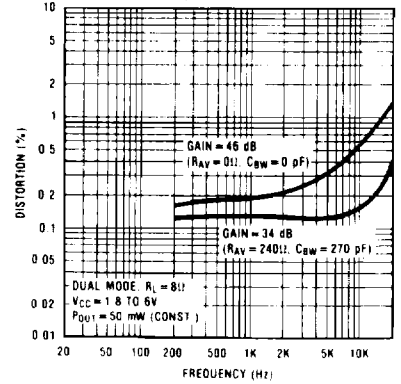
Typical Performance Characteristics (Continued)

LM831

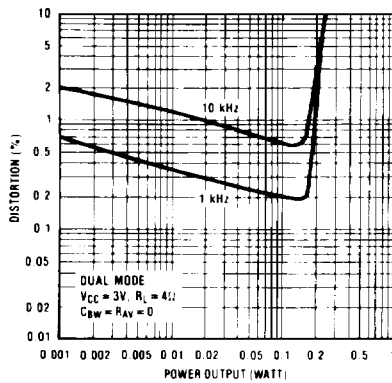


TL/H/6754-5

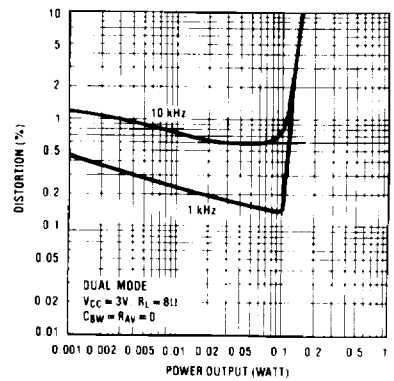
Typical Performance Characteristics (Continued)

Dual Mode, $R_L = 4\Omega$ Distortion vs FrequencyDual Mode, $R_L = 8\Omega$ Distortion vs Frequency

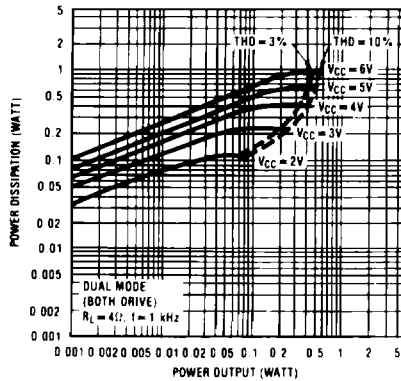
Distortion vs Power Output (Note 2)



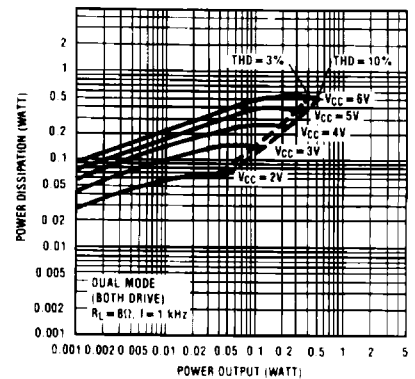
Distortion vs Power Output (Note 2)



Power Dissipation vs Power Output



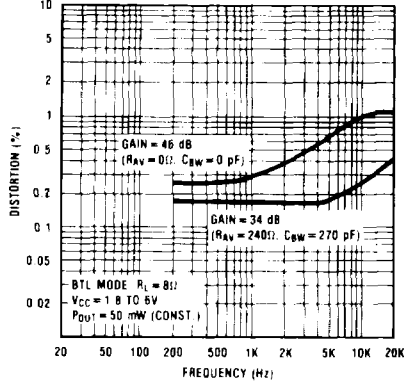
Power Dissipation vs Power Output



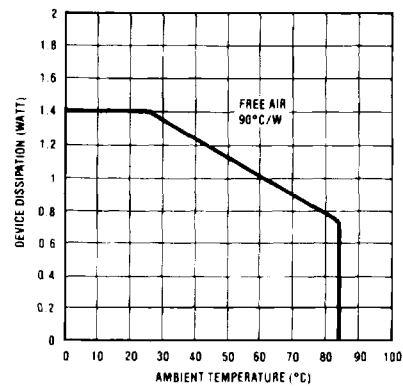
TL/H/6754-6

Typical Performance Characteristics (Continued)

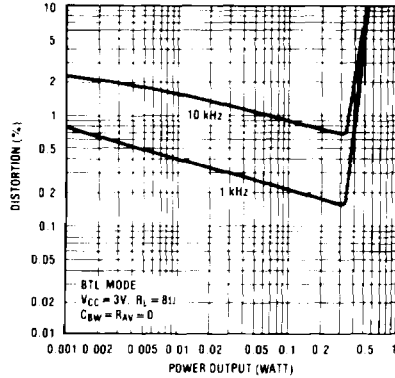
BTL Mode, $R_L = 8\Omega$ Distortion vs Frequency



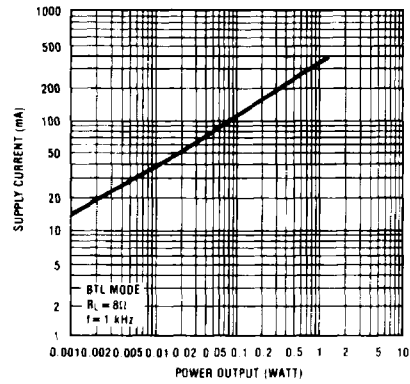
Device Dissipation vs Ambient Temperature



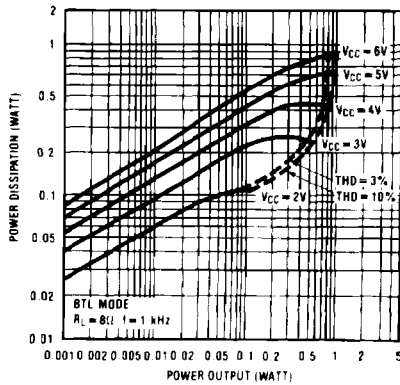
Distortion vs Power Output (Note 2)



Supply Current vs Power Output



Power Dissipation vs Power Output

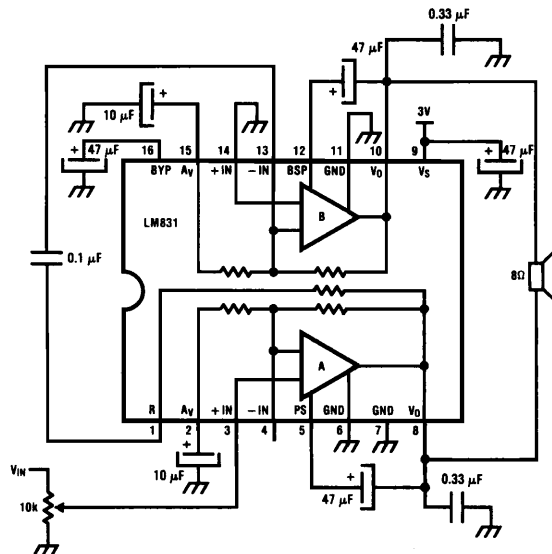


Note 2: 1 kHz curve is measured with 400 Hz–30 kHz Filter.

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Typical Applications

BTL Amplifier with Minimum Parts

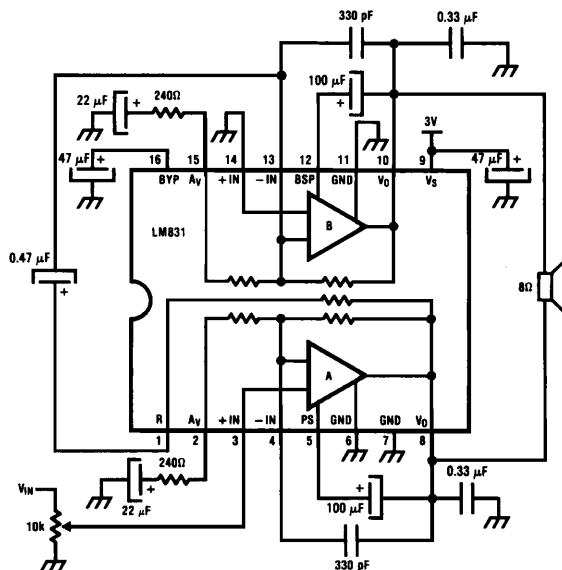


$A_V = 52 \text{ dB}$, $BW = 250 \text{ Hz to } 25 \text{ kHz}$

$P_{OUT} = 440 \text{ mW}$, $R_L = 8\Omega$

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BTL Amplifier for Hi-Fi Quality



$A_V = 40 \text{ dB}$, $BW = 20 \text{ Hz to } 20 \text{ kHz}$

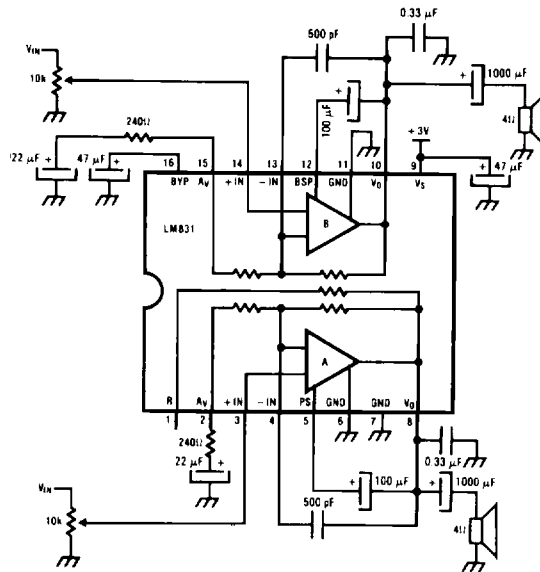
$P_{OUT} = 440 \text{ mW}$, $R_L = 8\Omega$

(Dynamic Range Over 80 dB)

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Typical Applications (Continued)

Dual Amplifier for Hi-Fi Quality

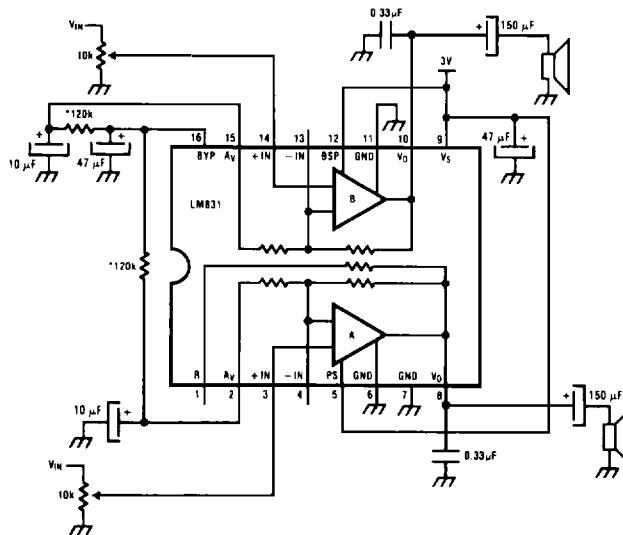


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 $A_V \approx 34 \text{ dB}$, $BW = 50 \text{ Hz to } 20 \text{ kHz}$
 $P_{OUT} = 220 \text{ mW/Ch}$, $R_L = 4\Omega$

(Dynamic Range Over 80 dB)

Low-Cost Power Amplifier (No Bootstrap)



TL/H/6754-11

 $P_{OUT} = 150 \text{ mW/Ch}$, $BW = 300 \text{ Hz to } 35 \text{ kHz}$

BTL Mode is also possible

*For 3-cell applications, the 120k resistor should be changed to 20k.

LM831 Circuit Description Refer to the external component diagram and equivalent schematic.

The power supply is applied to Pin 9 and is filtered by resistor R_1 and capacitor C_B on Pin 16. This filtered voltage at Pin 16 is used to bias all of the LM831 circuits except the power output stage. Resistor R_0 generates a biasing current that sets the output DC voltage for optimum output power for any given supply voltage.

Feedback is provided to the input transistor Q_1 emitter by R_6 and R_7 .

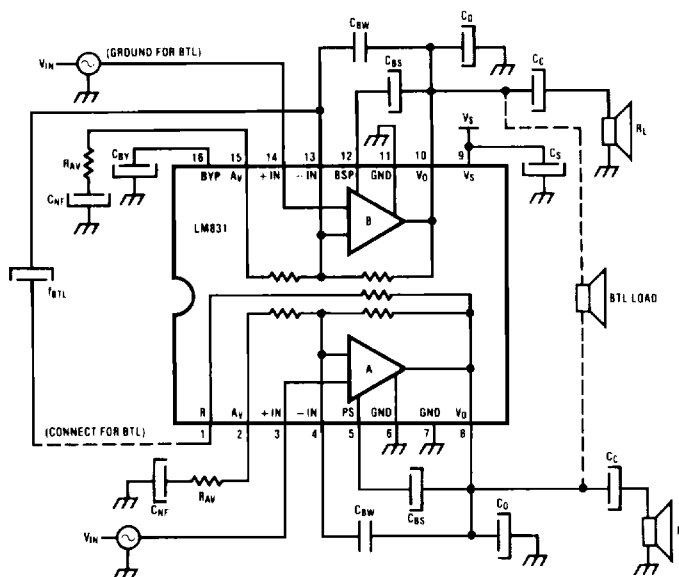
The capacitor C_{NF} on Pin 2 provides unity DC gain for maximum DC accuracy.

Q_2 provides voltage gain and the rest of the devices buffer the output load from Q_2 's collector.

Bootstrapping of Pin 5 by C_{BS} allows maximum output swing and improved supply rejection.

R₅ is provided for bridge (BTL) operation.

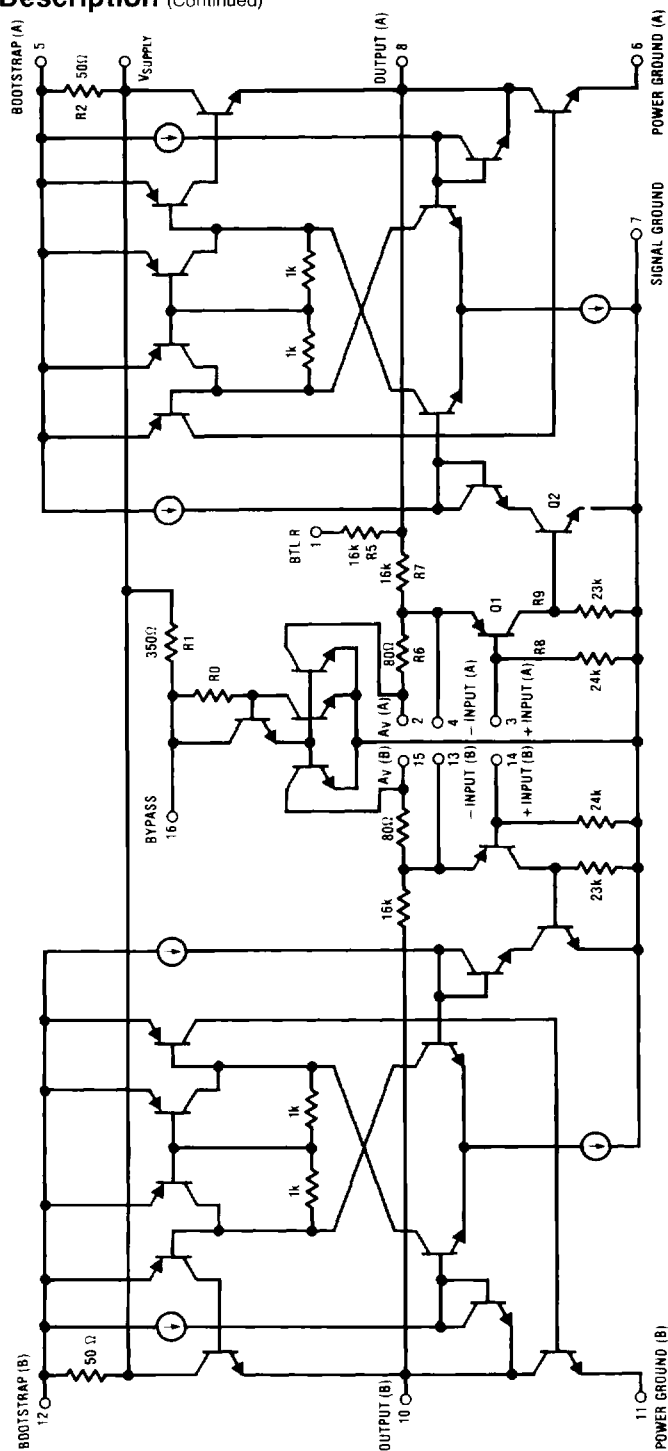
External Component Diagram



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LM831 Circuit Description (Continued)

LM831 Equivalent Schematic



TL/H/6754-13

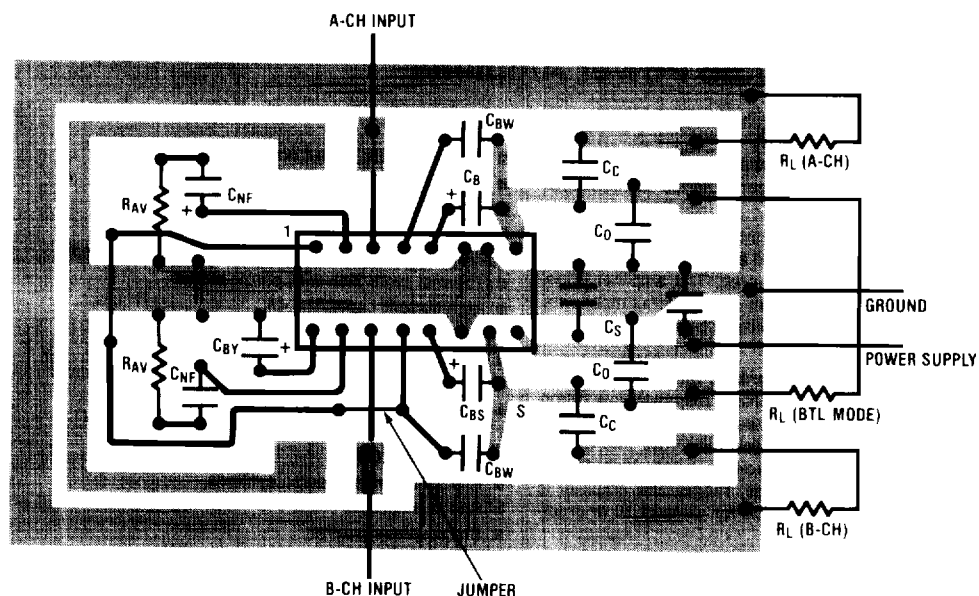
LM831

External Components (Refer to External Component Diagram)

Component	Comments	Min	Max
C _O	Required to stabilize output stage.	0.33 μF	1 μF
C _C	Output coupling capacitors for Dual Mode. Sets a low-frequency pole in the frequency response. $f_L = \frac{1}{2\pi C_C R_L}$	100 μF	10,000 μF
C _{BS}	Bootstrap capacitors. Sets a low-frequency pole in the power BW. Recommended value is $C_{BS} = \frac{1}{10 \cdot 2\pi \cdot f_L \cdot R_L}$	22 μF or (short Pins 4 & 12 to 9)	470 μF
C _S	Supply bypass. Larger values improve low-battery performance by reducing supply ripple.	47 μF	10,000 μF
C _{BY}	Filters the supply for improved low-voltage operation. Also sets turn-on delay.	47 μF	470 μF
C _{NF}	Sets a low-frequency response. Also affects turn-on delay. $f_L = \frac{1}{2\pi \cdot C_{NF} \cdot (R_{AV} + 80)}$ In BTL Mode, C _{NF} on Pin 15 can be reduced without affecting the frequency response. However, the turn-on "POP" will be worsened.	10 μF	100 μF
C _{BT}	Used only in the Bridge Mode. Connects the output of the first amplifier to the inverting input of the other through an internal resistor. Sets a low-frequency pole in one-half the frequency response. $f_L = \frac{1}{2\pi \cdot C_{BT} \cdot 16k}$	0.1 μF	1 μF
C _{BW}	Improves clipping waveform and sets the high-frequency bandwidth. Works with an internal 16k resistor. (This equation applies for R _{AV} ≠ 0. For 46 dB application, see BW–C _{BW} curve.) $f_H = \frac{1}{2\pi \cdot C_{BW} \cdot 16k}$	See table below	
R _{AV}	Used to reduce the gain and improve the distortion and signal to noise. If this is desired, C _{BW} must also be used.	See table below	

Typical A _v	R _{AV}	C _{BW}	
		Min	Max
46 dB	Short	Open	4700 pF
40 dB	82	100 pF	4700 pF
34 dB	240	270 pF	4700 pF
28 dB	560	500 pF	4700 pF

Printed Circuit Layout for LM831N (Foil Side View) Refer to External Component Diagram



TL/H/6754-14

Note: Power ground pattern should be as wide as possible. Supply bypass capacitor should be as close to the IC as possible. Output compensation capacitors should also be close to the IC.