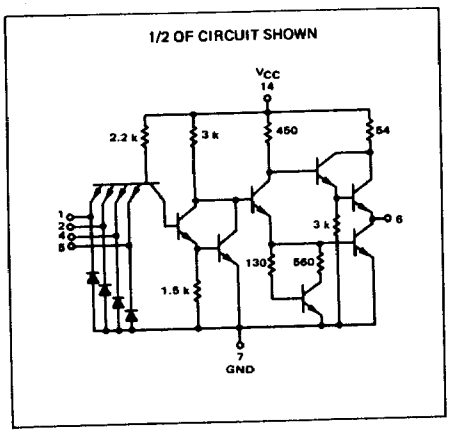
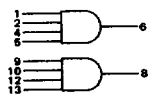
DUAL 4-INPUT "AND" POWER GATE

MC3126F • MC3026F
MC3126L • MC3026L,P



This device consists of two 4-input AND power gates. Each gate is designed for driving high fan-out loads (20).

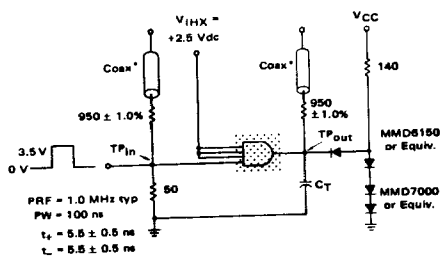


Positive Logic: $6 = 1 \cdot 2 \cdot 4 \cdot 5$
Negative Logic: $6 = 1 + 2 + 4 + 5$

Input Loading Factor = 1.3
Output Loading Factor = 20

Total Power Dissipation = 90 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

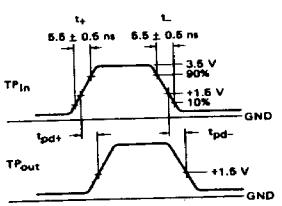
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

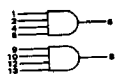
VOLTAGE WAVEFORMS AND DEFINITIONS



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3126 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3026 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Input Forward Current	I_F	1	-	-3.6	-	-3.6	-	-3.6	-	-3.6	-	-3.6	-	-3.6	mAdc
Leakage Current	I_R	1	-	50	-	50	-	50	-	50	-	50	-	50	μAdc
Breakdown Voltage	BV_{in}	1	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc
Clamp Voltage	V_D	1	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc
Output Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc
Short-Circuit Current	I_{SC}	6	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	-50	-125	mAdc
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	14	-	-	-	22	-	-	-	-	-	22	-	-	mAdc
Power Supply Drain	I_{PDH}	14	-	14	-	14	-	14	-	14	-	14	-	14	mAdc
	I_{PDL}	14	-	38	-	38	-	38	-	38	-	38	-	38	mAdc
Switching Parameters Turn-On Delay	t_{pd-}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns
Turn-Off Delay	t_{pd+}	1, 6	-	-	-	15	-	-	-	-	-	15	-	-	ns

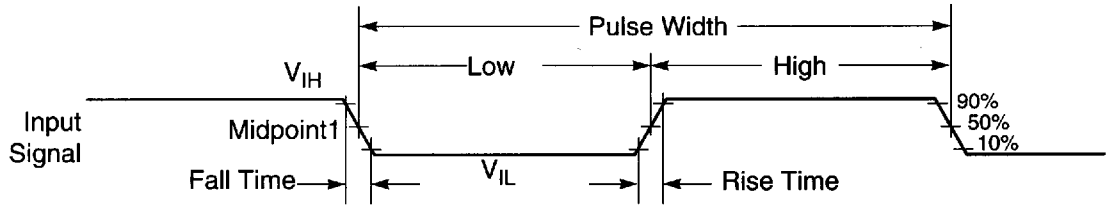
@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{BR}	V_{max}	V_{CC}	V_{CC1}	V_{CCH}	V_{BCC}
MC3126 −55°C	40	-4.0	-	-	1.1	2.0	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3126 +25°C	40	-4.0	1.0	-10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.5
MC3126 +125°C	40	-4.0	-	-	0.8	1.8	0.4	2.4	4.0	-	5.0	4.5	5.5	-
MC3026 0°C	40	-4.0	-	-	1.1	2.0	0.4	2.5	4.0	-	5.0	4.75	5.25	-
MC3026 +25°C	40	-4.0	1.0	-10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.5
MC3026 +75°C	40	-4.0	-	-	0.8	1.8	0.4	2.5	4.0	-	5.0	4.75	5.25	-

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{BR}	V_{max}	V_{CC}	V_{CC1}	V_{CCH}	V_{BCC}	Gnd
-	-	-	-	-	-	1	-	2, 4, 5 *	-	-	-	14	-	7
-	-	-	-	-	-	-	1	*	-	-	-	14	-	2, 4, 5, 7
-	-	1	-	-	-	-	-	*	-	-	-	14	-	2, 4, 5, 7
-	-	-	1	-	-	-	-	*	-	-	14	-	-	7
6	-	-	-	1	-	-	-	2, 4, 5 *	-	-	14	-	-	7
-	-	-	-	-	1	-	-	2, 4, 5 *	-	-	14	-	-	7
-	n	-	-	-	-	-	-	1, 2, 4, 5 *	-	14	-	-	-	6, 7
-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	14	-	-	-	-	7
-	-	-	-	-	-	-	-	1, 2, 4, 5, 9, 10, 12, 13	-	14	-	-	-	7
-	-	-	-	-	-	-	-	-	-	14	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13
Pulse In	Pulse Out													
1	6	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7
1	6	-	-	-	-	-	-	*	-	14	-	-	2, 4, 5	7

* Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH}.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms in the AC Electrical Characteristics are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These pins are tested using the input levels set forth in the DC Electrical Characteristics. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56002 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

AA0179

Figure 2-1 Signal Measurement Reference