Never stop thinking

SPI Power Controller

SPOC - BTS6480SF

For Advanced Front Light Control

Data Sheet

Rev. 1.0, 2010-04-12

Automotive Power

Table of Contents

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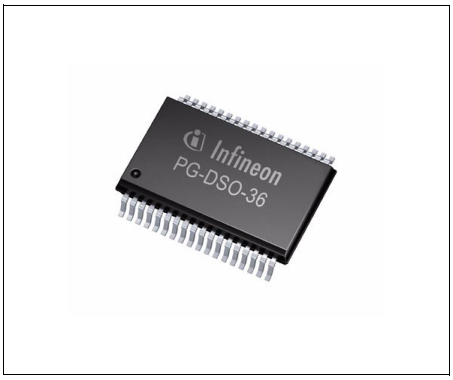
1 Overview



PG-DSO-36-43

Features

- 16 bit serial peripheral interface for control and diagnosis
- Integrated PWM generator
- Integrated control for two external smart power switches
- 3.3 V and 5 V compatible logic pins
- Very low stand-by current
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LEDs with increased slew rate
- Stable behavior at under voltage
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

Description

The SPOC - BTS6480SF is a four channel high-side smart power switch in PG-DSO-36-43 package providing embedded protective functions. It is especially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode for channel 2 and channel 3. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is specially designed to drive exterior lamps up to 65W, 27W and 10W and HIDL.

Product Summary

Operating Voltage Power Switch	V_{BB}	4.5 … 28 V
Logic Supply Voltage	V_{DD}	3.0 … 5.5 V
Supply Voltage for Load Dump Protection	$V_{BB(LD)}$	40 V
Maximum Stand-By Current at 25 °C	$I_{BB(STB)}$	4.5 µA
Typical On-State Resistance at T_j = 25 °C channel 0, 1 channel 2, 3	$R_{DS(ON,typ)}$	 3.5 mΩ 11 mΩ
Maximum On-State Resistance at T_j = 150 °C channel 0, 1 channel 2, 3	$R_{DS(ON,max)}$	 9 mΩ 28 mΩ
SPI Access Frequency	$f_{SCLK(max)}$	5 MHz

Type	Package	Marking
SPOC - BTS6480SF	PG-DSO-36-43	BTS6480SF

Configuration and status diagnosis are done via SPI. The SPI is daisy chain capable. The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over load and over temperature flag is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to V_{BB} diagnosis. In OFF state a current source can be switched to the output of one selected channel in order to detect an open load.

Additionally, there is an integrated PWM generator implemented, which allows autonomous PWM operation with programmable phase shifts, duty cycles and PWM frequencies. The status diagnosis and the current sense signal is available for each channel.

The device provides an external driver capability for two external devices. For each external driver there are two control outputs available: one output for controlling the input and one output for diagnosis enable input. The current sense output of the external smart power drivers can be connected to the IS pin. The external drivers can be controlled by the automatic PWM generator as well.

The SPOC - BTS6480SF provides a fail-safe feature via limp home input pin.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps.

Protective Functions

- Reverse battery protection with external components
- Reversave™ - Reverse battery protection by self turn on of channels 0, 1, 2 and 3
- Short circuit protection
- Over load protection
- Thermal shutdown with latch and dynamic temperature sensor
- Over current tripping
- Over voltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio (k_{ILIS}) configurable for LEDs or bulbs for channel 2 and 3
- Very fast diagnosis in LED mode
- Feedback on over temperature and over load via SPI
- Multiplexed switch bypass monitor provides short circuit to V_{BB} detection
- Integrated, in two steps programmable current source for open load in OFF-state detection

Application Specific Functions

- Fail-safe activation via LHI pin
- Control of two additional loads with external smart power switches

Applications

- High-side power switch for 12 V grounded loads in automotive applications
- Especially designed for standard exterior lighting like high beam, low beam, indicator, parking light and equivalent LEDs
- Load type configuration via SPI (bulbs or LEDs) for optimized load control
- Replaces electromechanical relays, fuses and discrete circuits

2 Block Diagram

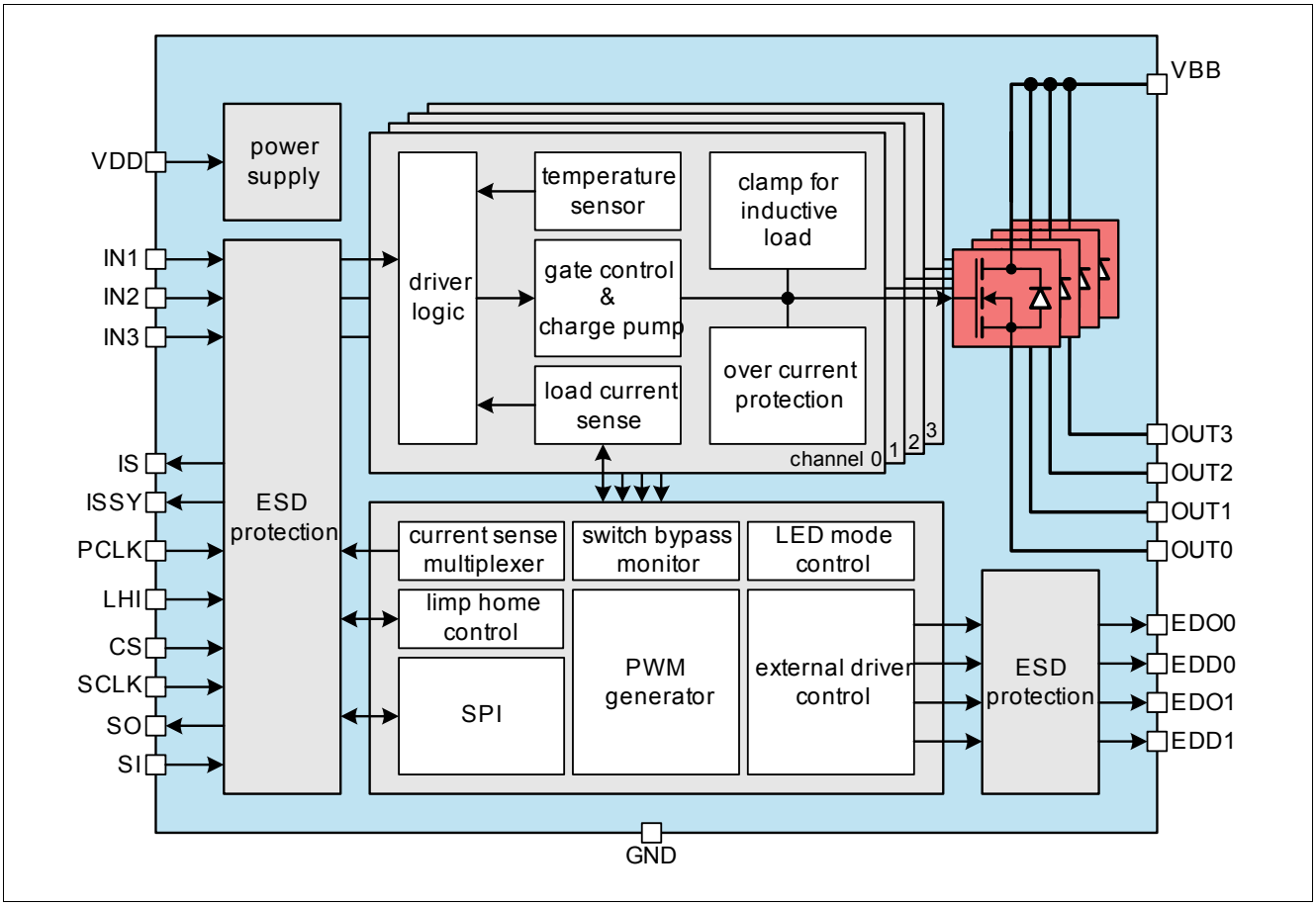


Figure 1 Block Diagram SPOC - BTS6480SF

2.1 Terms

Figure 2 shows all terms used in this data sheet.

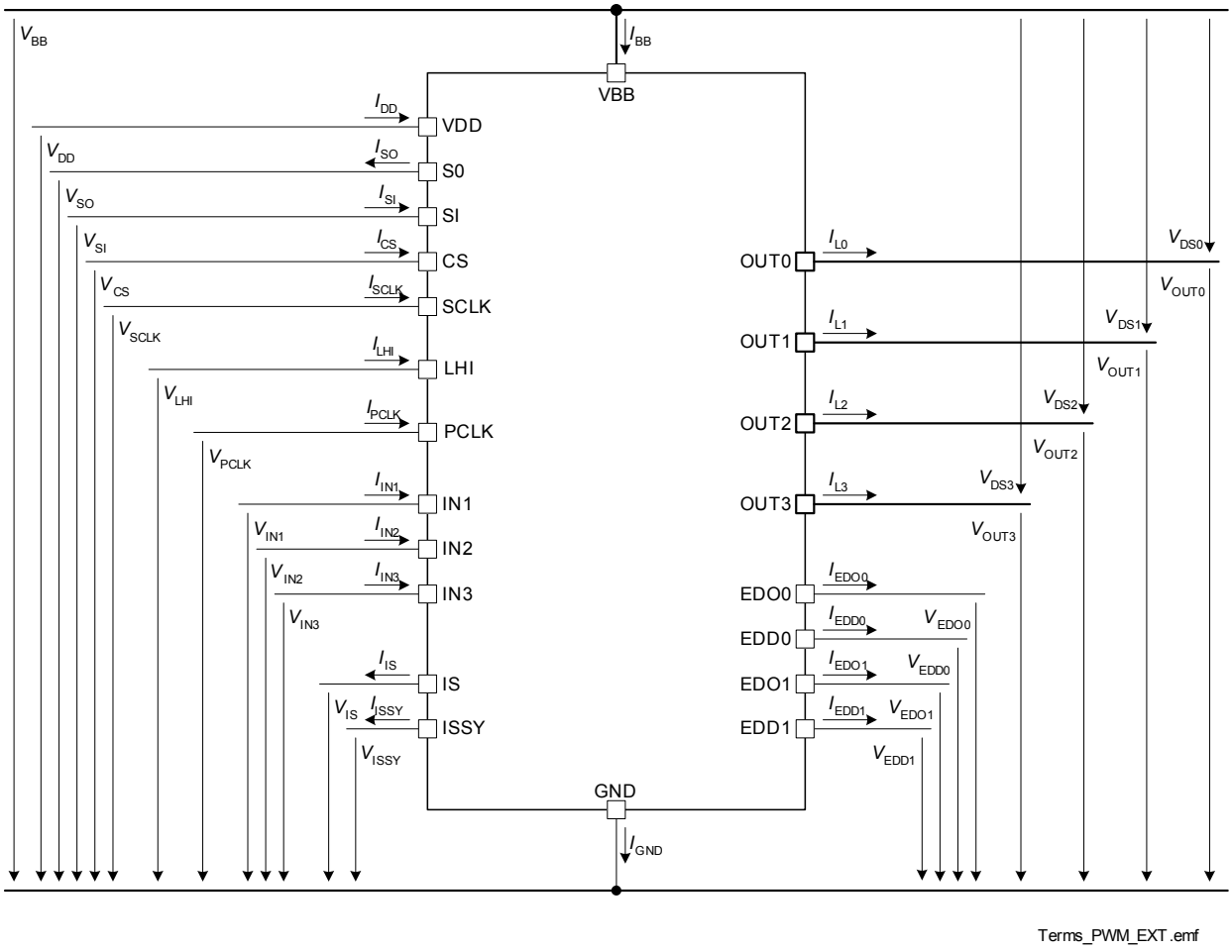


Figure 2 Terms

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} … V_{DS3}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.CL`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment SPOC - BTS6480SF

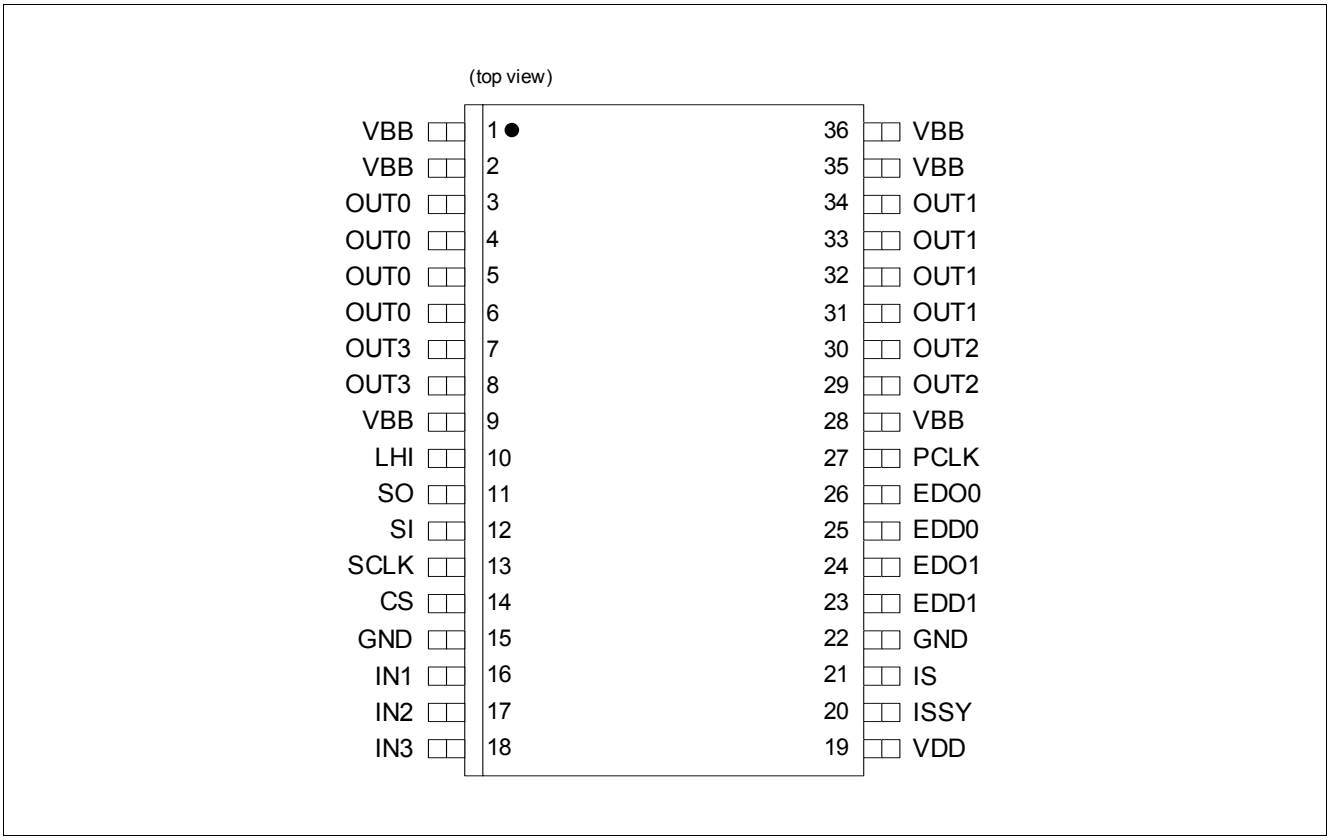


Figure 3 Pin Configuration PG-DSO-36-43

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
1, 2, 9, 28, 35, 36 [1]	VBB	–	Positive power supply for high-side power switch
19	VDD	–	Logic supply (5 V)
15, 22	GND	–	Ground connection
Parallel Input Pins (integrated pull-down, leave unused pins unconnected)			
16	IN1	I	Input signal of channel 1 (high active)
17	IN2	I	Input signal of channel 2 (high active)
18	IN3	I	Input signal of channel 3 (high active)
Power Output Pins			
3, 4, 5, 6 [2]	OUT0	O	Protected high-side power output of channel 0
31, 32, 33, 34 [2]	OUT1	O	Protected high-side power output of channel 1
29, 30 [2]	OUT2	O	Protected high-side power output of channel 2
7, 8 [2]	OUT3	O	Protected high-side power output of channel 3
SPI, PWM & Diagnosis Pins			
14	CS	I	Chip select of SPI interface (low active); Integrated pull up
13	SCLK	I	Serial clock of SPI interface
12	SI	I	Serial input of SPI interface (high active)
11	SO	O	Serial output of SPI interface
27	PCLK	I	PWM clock reference signal
21	IS	O	Current sense output signal
20	ISSY	O	Current sense synchronization signal
Limp Home Pin (integrated pull-down, pull-down resistor recommended)			
10	LHI	I	Limp home activation signal (high active)
External Driver Pins (integrated pull-down, leave unused external driver pins unconnected)			
26	EDO0	O	External driver output for activation of external driver 0
24	EDO1	O	External driver output for activation of external driver 1
25	EDD0	O	External driver diagnosis enable signal of external driver 0
23	EDD1	O	External driver diagnosis enable signal of external driver 1

1) All VBB pins have to be connected.

2) All outputs pins of each channel have to be connected.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
Supply Voltage						
4.1.1	Power supply voltage	V_{BB}	-0.3	28	V	–
4.1.2	Logic supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Reverse polarity voltage according **Figure 30**	$-V_{bat(rev)}$	–	16	V	T_{jStart} = 25 °C $t \leq$ 2 min. [2)]
4.1.4	Supply voltage for short circuit protection (single pulse)	$V_{BB(SC)}$			V	R_{ECU} = 20 mΩ l = 0 or 5 m [3)]
	channel 0, 1		0	24		R_{Cable} = 6 mΩ/m L_{Cable} = 1 µH/m
	channel 2, 3		0	24		R_{Cable} = 16 mΩ/m L_{Cable} = 1 µH/m
4.1.5	Supply voltage for load dump protection with connected loads	$V_{BB(LD)}$	–	40	V	R_I = 2 Ω [4)] t = 400 ms
4.1.6	Current through ground pin	I_{GND}	–	25	mA	$t \leq$ 2 min.
4.1.7	Current through VDD pin	I_{DD}	-25	12	mA	$t \leq$ 2 min.
Power Stages						
4.1.8	Load current	I_L	$-I_{L(LIM)}$	$I_{L(LIM)}$	A	[5)]
4.1.9	Maximum energy dissipation single pulse	E_{AS}			mJ	[6)] $T_{j(0)}$ = 150 °C
	channel 0, 1		–	180		$I_{L(0)}$ = 5 A
	channel 2, 3		–	45		$I_{L(0)}$ = 2 A
Diagnosis Pin						
4.1.10	Current through sense pin IS	I_{IS}	-8	8	mA	$t \leq$ 2 min.
Input Pins						
4.1.11	Voltage at input pins	V_{IN}	-0.3	5.5	V	–
4.1.12	Current through input pins	I_{IN}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
SPI Pins						
4.1.13	Voltage at chip select pin	V_{CS}	-0.3	V_{DD} + 0.3	V	–
4.1.14	Current through chip select pin	I_{CS}	-2.0	2.0	mA	$t \leq$ 2 min.
4.1.15	Voltage at serial input pin	V_{SI}	-0.3	V_{DD} + 0.3	V	–
4.1.16	Current through serial input pin	I_{SI}	-2.0	2.0	mA	$t \leq$ 2 min.
4.1.17	Voltage at serial clock pin	V_{SCLK}	-0.3	V_{DD} + 0.3	V	–
4.1.18	Current through serial clock pin	I_{SCLK}	-2.0	2.0	mA	$t \leq$ 2 min.
4.1.19	Voltage at serial out pin	V_{SO}	-0.3	V_{DD} + 0.3	V	–

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 to +150 °C; all voltages with respect to ground

(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
4.1.20	Current through serial output pin SO	I_{SO}	-2.0	2.0	mA	$t \leq 2$ min.
PWM Clock and Sense Synchronization Pin						
4.1.21	Voltage at PWM clock input pin	V_{PCLK}	-0.3	V_{DD} + 0.3	V	–
4.1.22	Current through PWM clock input pin	I_{PLCK}	-0.75 -2.0	0.75 2.0	mA	– $t \leq 2$ min.
4.1.23	Voltage at sense synchronization pin	V_{ISSY}	-0.3	V_{DD} + 0.3	V	–
4.1.24	Current through sense synchronization pin	I_{ISSY}	-2.0	2.0	mA	$t \leq 2$ min.
Limp Home Pin						
4.1.25	Voltage at limp home input pin	V_{LHI}	-0.3	5.5	V	–
4.1.26	Current through limp home input pin	I_{LHI}	-0.75 -2.0	0.75 2.0	mA	– $t \leq 2$ min.
External Driver Pins						
4.1.27	Voltage at external driver output	V_{EDO}	-0.3	V_{DD} + 0.3	V	–
4.1.28	Current through external driver output	I_{EDO}	-1.0	1.0	mA	$t \leq 2$ min.
4.1.29	Voltage at external driver diagnosis enable	V_{EDD}	-0.3	V_{DD} + 0.3	V	–
4.1.30	Current through external driver diagnosis enable	I_{EDD}	-1.0	1.0	mA	$t \leq 2$ min.
Temperatures						
4.1.31	Junction temperature	T_j	-40	150	°C	–
4.1.32	Dynamic temperature increase while switching	ΔT_j	–	60	K	–
4.1.33	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.34	ESD susceptibility HBM	V_{ESD}			kV	HBM [7)]
	OUT pins vs. VBB		-4	4		–
	other pins incl. OUT vs. GND		-2	2		–

1) Not subject to production test, specified by design.

2) Device is mounted on an FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) In accordance to AEC Q100-012 and AEC Q101-006.

4) R_I is the internal resistance of the load dump pulse generator.

5) Over current protection is a protection feature. Operation in over current protection is considered as "outside" normal operating range. Protection features are not designed for continuous repetitive operation.

6) Pulse shape represents inductive switch off: $I_{D(t)} = I_{D}(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

7) ESD resistivity, HBM according to EIA/JESD 22-A 114B (1.5 kΩ, 100 pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Junction to Soldering Point [1]	R_{thJSP}	–	–	20	K/W	measured to pin 1, 2, 9, 28, 35, 36
4.2.2	Junction to Ambient [1]	R_{thJA}	–	35	–	K/W	[2]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} values is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

5 Power Supply

The SPOC - BTS6480SF is supplied by two supply voltages V_{BB} and V_{DD}. The V_{BB} supply line is used by the power switches. The V_{DD} supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins VDD and GND is recommended as shown in **Figure 30**.

There is a power-on reset function implemented for the V_{DD} logic power supply. After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as V_{DD} is provided in the specified range independent of V_{BB}. First SPI data are the output register values with TER = 1.

Specified parameters are valid for the supply voltage range according $V_{BB(nor)}$ or otherwise specified. For the extended supply voltage range according $V_{BB(ext)}$ device functionality (switching, diagnosis and protection functions) are still given, parameter deviations are possible.

5.1 Power Supply Modes

The following table shows all possible power supply modes for V_{BB}, V_{DD} and the pin LHI.

Power Supply Modes	Off	Off	SPI on	Reset	Off	On via INx	Limp Home mode without SPI	Normal operation	Limp Home mode with SPI [1]
V_{BB}	0 V	0 V	0 V	0 V	13.5 V	13.5 V	13.5 V	13.5 V	13.5 V
V_{DD}	0 V	0 V	5 V	5 V	0 V	0 V	0 V	5 V	5 V
LHI	0 V	5 V	0 V	5 V	0 V	0 V	5 V	0 V	5 V
Power stage, protection	–	–	–	–	–	✓[2]	✓[2]	✓	✓[2]
Limp home	–	–	–	–	–	–	✓	–	✓
SPI (logic)	–	–	✓	✓	reset	reset	reset	✓	reset[3]
Stand-by current	–	–	–	–	✓	✓[4]	–	✓[5]	–
Idle current	–	–	–	–	–	–	–	✓[6]	–
Diagnosis	–	–	–	–	–	–	–	✓	✓[7]

1) SPI read only
2) Channel 1, 2 and/or 3 activated according to the state of INx
3) SPI reset only with applied V_{BB} voltage
4) When INx = low
5) When DCR.MUX = 111_b, INx = low and PCR.PST = 0_b
6) When all channels are in OFF-state and DCR.MUX ≠ 111_b
7) Current sense disabled in limp home mode

5.1.1 Stand-by Mode and Device Wake-up Mechanisms

Stand-by mode is entered as soon as the current sense multiplexer (DCR.MUX) is in default (stand-by) position, the PWM start bit is reset (PCR.PST = 0_b) and all input pins are not set. All error latches are cleared automatically in stand-by mode. As soon as stand-by mode is entered, register HWCR.STB is set. To wake-up the device, the current sense multiplexer (DCR.MUX) is programmed different to default (stand-by) position or the PWM start bit is set (PCR.PST = 1_b). The power-on wake up time $t_{WU(PO)}$ has to be considered for both cases.

Idle mode parameters are valid, when all channels are switched off, but the current sense multiplexer is not in default position, and V_{DD} supply is available.

Note: A transition from operation to stand-by mode does not reset the SPI registers. So, if V_{DD} is present and SPI is programmed, a changing to MUX = 111_b does not reset the SPI registers. An activation of the channels via the input pin INx will wake up the device with the former SPI register settings.

Activating one of the outputs via the input pins (INx = high) will wake-up the device out of stand-by mode. The power stages are working without VDD supply according to the table above. The output turn-on times will be extended by the stand-by channel wake up time $t_{WU(STCH)}$ as long as no other channel is active. If one channel is active already before channel turn-on times t_{on} (**6.6.12**) can be considered.

Note: In the operation with V_{DD} = 0 V and INx = high a switching off of all input signals will turn the device in stand-by mode. In stand-by mode the error latches are cleared.

Limp home (LHI = high) applied for a time longer than $t_{LH(ac)}$ will wake-up the device out of stand-by mode after the power-on wake up time $t_{WU(PO)}$ and it is working without VDD supply. Channels 1, 2 and 3 can be activated via the input pins INx. The error latches can be cleared by a low-high transition at the according input pin.

5.2 Reset

There are several reset trigger implemented in the device. They reset the SPI registers including the over temperature latches to their default values. The power stages will switch off, if they are activated via the SPI register `OUT.n`. If the power stages are activated via the parallel input pins they are not affected by the reset signals. The ERR-flags are cleared by those reset triggers. The over temperature protection and latches are functional after a reset trigger.

Note: During a reset only the channels 1, 2 and 3 can be activated via the according input pins. The input assigned mode is not available during a reset.

The first SPI transmission after any kind of reset contains at pin SO the read information from the standard diagnosis, the transmission error bit `TER` is set.

Power-On Reset

The power-on reset is released, when V_{DD} voltage level is higher than $V_{DD(PO)}$. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `HWCR.RST = 1`$_b$, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time $t_{CS(td)}$.

Limp Home Mode

The limp home mode will be activated as soon as the pin LHI is set to high for a time longer than $t_{LH(ac)}$. The SPI write-registers are reset with applied V_{BB} voltage. The outputs OUTx can be activated via the input pins also during activated limp home mode. The error latches can be cleared by a low-high transition at the according input pin. For application example see **Figure 30**. The SPI interface is operating normally, so the limp home register bit LHI as well as the error flags can be read, but any write command will be ignored.

5.3 Electrical Characteristics

Electrical Characteristics Power Supply

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
5.3.1	Supply voltage range for normal operation power switch	$V_{BB(nor)}$	8	–	17	V	–
5.3.2	Extended supply voltage range for operation power switch	$V_{BB(ext)}$	4.5	–	28[1)]	V	Parameter deviations possible
5.3.3	Stand-by current for whole device with loads	$I_{BB(STB)}$	 – –	 – –	 4.5 28	µA	V_{DD} = 0 V V_{LHI} = 0 V 1) T_j = 25 °C 1) $T_j \leq$ 85 °C
5.3.4	Idle current for whole device with loads, all channels off	$I_{BB(idle)}$	–	7	–	mA	V_{DD} = 5 V DCR.MUX = 110
5.3.5	Logic supply voltage	V_{DD}	3.0	–	5.5	V	–
5.3.6	Logic supply current	I_{DD}	 – –	 140 280	 – –	µA	V_{CS} = V_{LHI} = 0 V R_{IS} = 2.7 kΩ V_{IS} = 0 V f_{SCLK} = 0 Hz f_{SCLK} = 5 MHz
5.3.7	Logic idle current	$I_{DD(idle)}$	–	25	–	µA	V_{CS} = V_{DD} f_{SCLK} = 0 Hz Chip in Standby
5.3.8	Operating current for whole device active	I_{GND}	–	10	25	mA	f_{SCLK} = 0 Hz
LHI Input Characteristics							
5.3.9	L-input level at LHI pin	$V_{LHI(L)}$	0	–	0.8	V	–
5.3.10	H-input level at LHI pin	$V_{LHI(H)}$	1.8	–	5.5	V	–
5.3.11	L-input current through LHI pin	$I_{LHI(L)}$	3	12	80	µA	1) V_{LHI} = 0.4 V
5.3.12	H-input current through LHI pin	$I_{LHI(H)}$	10	40	80	µA	V_{LHI} = 5 V
Reset							
5.3.13	Power-On reset threshold voltage	$V_{DD(PO)}$	–	–	2.4	V	–
5.3.14	Power-On wake up time	$t_{WU(PO)}$	–	–	200	µs	1)
5.3.15	Stand-by channel wake up time	$t_{WU(STCH)}$	–	–	200	µs	1)
5.3.16	Limp home acknowledgement time	$t_{LH(ac)}$	5	–	200	µs	1)

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature.

5.4 Command Description

HWCR
Hardware Configuration Register [1)]

W/$\overline{R}$ [2)]	RB[2)]		ADDR[2)]			9	8	7	6	5	4	3	2	1	0
read	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**STB**	**CL**
write	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**RST**	**CL**

1) Shaded cells not mentioned in this chapter.
2) W/$\overline{R}$ Write/Read, RB Register Bank, ADDR Address

Field	Bits	Type	Description
RST	1	w	**Reset Command** **0** [1)] Normal operation 1 Execute reset command
STB	1	r	**Stand-by** 0 Device is awake **1** Device is in stand-by mode

1) Bold letters indicate the default values.

6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs (DMOS) with charge pumps. There are four channels implemented in the device. Channels can be switched on via an input pin (please refer to **Section 6.2**) or via SPI register OUT.

6.1 Output ON-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage V_{BB} as well as on the junction temperature T_j. **Figure 4** shows those dependencies. The behavior in reverse polarity mode is described in **Section 8.5**.

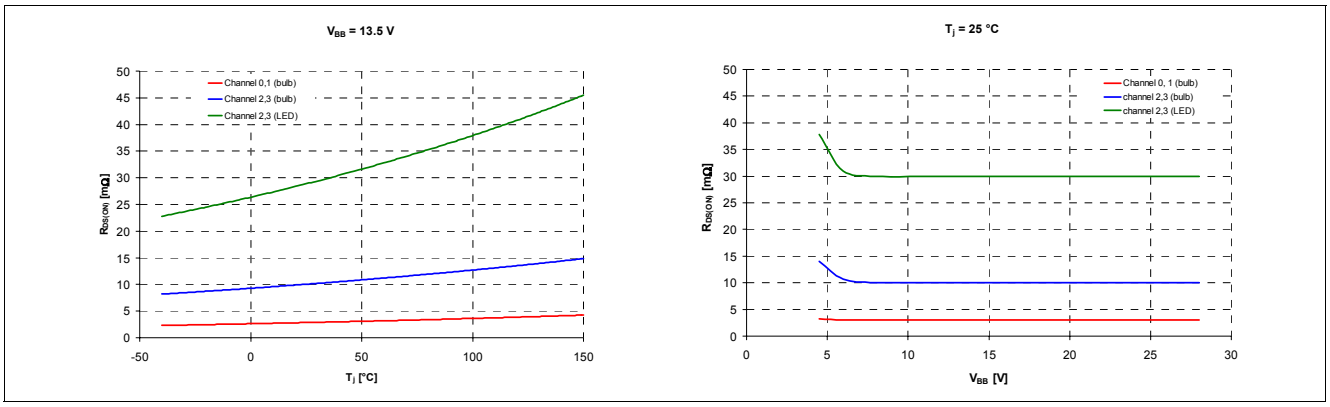


Figure 4 Typical On-State Resistance

6.2 Input Circuit

The outputs of the SPOC - BTS6480SF can be activated either via the SPI register OUT.OUTn or via the dedicated input pins. There are two different ways to use the input pins, the direct drive mode and the assigned drive mode. The default setting is the direct drive mode. To activate the assigned drive mode the register bit IECR.INCG needs to be set.

Additionally, there are two ways of using the input pins in combination with the OUT register by programming the IECR.COL parameter.

- IECR.COL = 0_b: A channel is switched on either by the according OUT register bit or the input pin.
- IECR.COL = 1_b: A channel is switched on by the according OUT register bit only, when the input pin is high. In this configuration, a PWM signal can be applied to the input pin and the channel is activated by the SPI register OUT.

Figure 5 shows the complete input switch matrix.

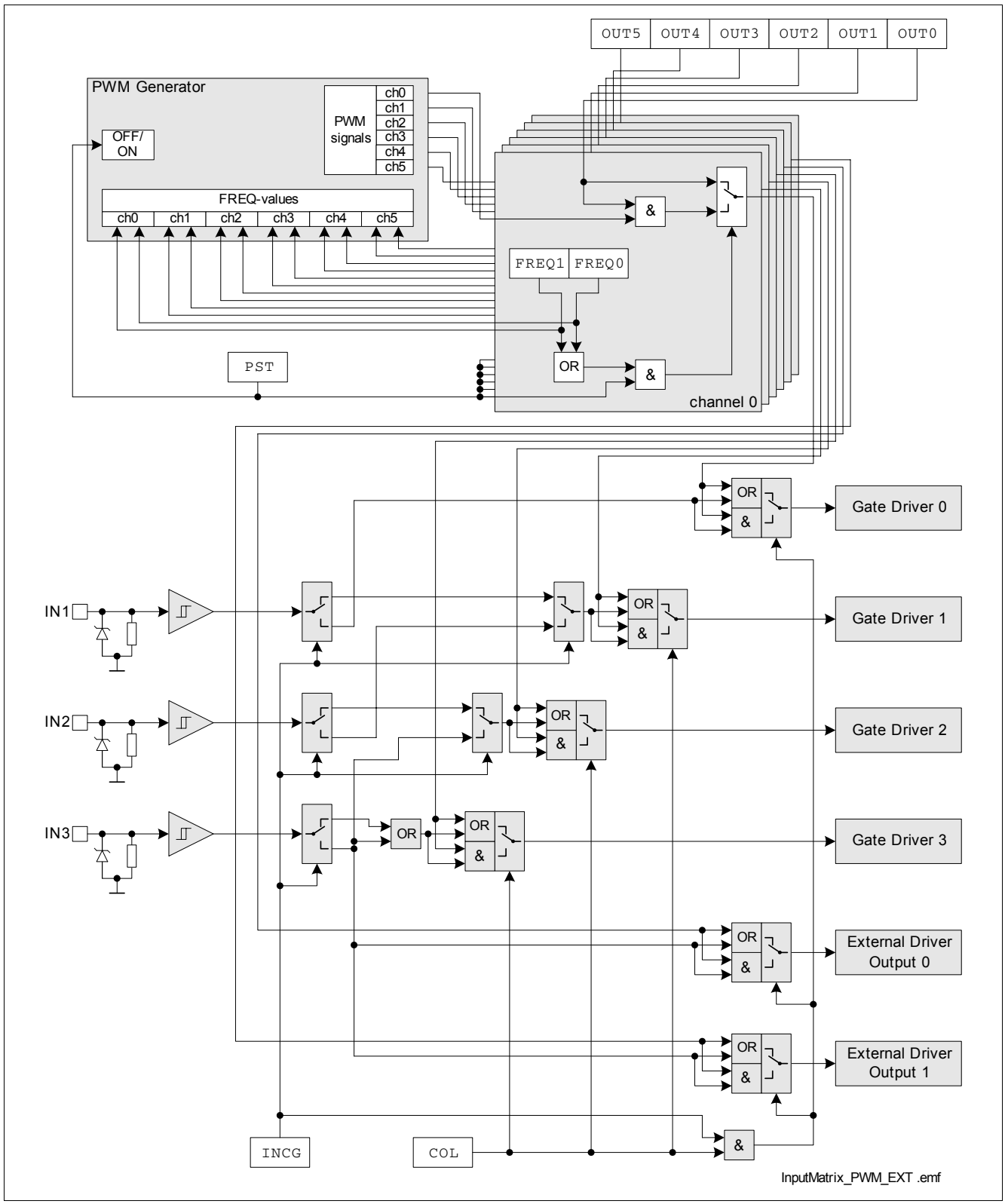


Figure 5 Input Switch Matrix

The current sink to ground ensures that the input signal is low in case of an open input pin. The zener diode protects the input circuit against ESD pulses.

6.2.1 Input Direct Drive

This mode is the default after the device's wake up and reset. The input pins activate the channels during normal operation (with default setting of bit `IECR.INCG`), stand-by mode and limp home mode. Channel 0 and the external drivers can be activated only via the SPI-bit `OUT.OUTn` in direct drive mode. The inputs are linked directly to the channels according to:

Table 1 Direct Drive Mode

Input Pin	**Assigned channel**, if `IECR.INCG` = 0_b
IN1	Channel 1
IN2	Channel 2
IN3	Channel 3

6.2.2 Input Assigned Drive

To activate the assigned drive function the register bit `IECR.INCG` needs to be set. In this mode all output channels can be activated via the input pins. Channel 2, 3 and the two external drivers are assigned to only one input pin. The following mapping is used:

Table 2 Assigned Drive Mode

Input Pin	**Assigned channel**, if `IECR.INCG` = 1_b
IN1	Channel 0
IN2	Channel 1
IN3	Channel 2, channel 3, external driver 0, external driver 1

6.3 Power Stage Output

The power stages are built to be used in high side configuration (**Figure 6**).

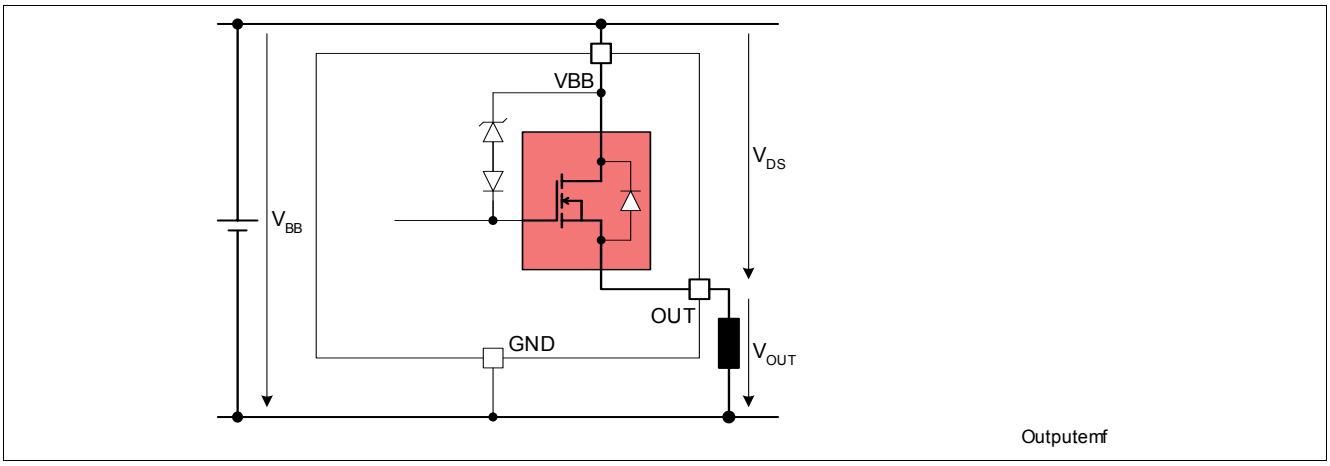


Figure 6 Power Stage Output

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission. Defined slew rates and edge shaping allow lowest EMC emissions during PWM operation at low switching losses.

6.3.1 Bulb and LED mode

Channel 2 and channel 3 can be configured in bulb and LED mode via the SPI registers HWCR.LEDn. During LED mode following parameters are changed for an optimized functionality with LED loads: On-state resistance $R_{DS(ON)}$, switching timings ($t_{delay(ON)}$, $t_{delay(OFF)}$, t_{ON}, t_{OFF}), slew rates dV/dt_{ON} and dV/dt_{OFF}, current protections $I_{L(trip)}$ and current sense ratio k_{ILIS}.

6.3.2 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.

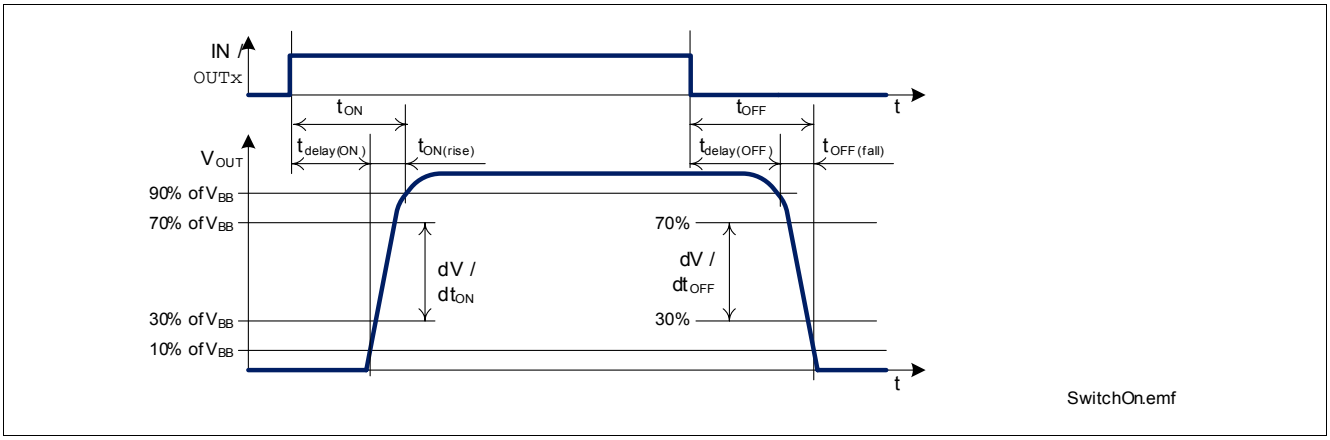


Figure 7 Switching a Load (resistive)

6.3.3 Switching Inductive Loads

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a voltage clamp mechanism implemented, which limits that negative output voltage to a certain level ($V_{DS(CL)}$ (**6.6.2**)). See **Figure 6** for details. The device provides SmartClamp functionality. To increase the energy capability, the clamp voltage $V_{DS(CL)}$ increases with the junction temperature T_j and load current I_L. Please refer also to **Section 8.6**. The maximum allowed load inductance is limited.

6.4 Inverse Current Behavior

During inverse currents (V_{OUT} > V_{BB}) the affected channel stays in ON- or in OFF-state. Furthermore, during applied inverse currents no ERR-flag is set.

The functionality of unaffected channels is not influenced by inverse currents applied to other channels (except effects due to junction temperature increase). Influences on the diagnostic function of unaffected channels are possible only for the current sense ratio, please refer to $\Delta k_{ILIS(IC)}$ (**9.8.3**).

Note: No protection mechanism like temperature protection or current protection is active during applied inverse currents. Inverse currents cause power losses inside the DMOS, which increase the overall device temperature, which could lead to a switch off of the unaffected channels due to over temperature.

6.5 External Driver Control

Two external smart power drivers can be driven by the SPOC - BTS6480SF via the external driver control block. For each external driver there are two control outputs available: one output for controlling the input (EDOx) and one output for diagnosis enable input (EDDx). The current sense output of the external smart power drivers can be connected to the IS pin. For details please refer to **Figure 30**.

The external driver outputs can be used only with applied V_{DD} voltage. The external driver outputs are internally pulled down. The external drivers can be activated via SPI-bits `OUT.OUT4` and `OUT.OUT5` or via the input pin IN3 in assigned drive mode. They will be served as well by the integrated automatic PWM-generation. Therefore, the according PWM-frequency and duty cycle needs to be programmed.

For performing diagnosis on the external drivers they can be selected via the SPI register `DCR.MUX`. For being compliant to PROFET+ diagnostic functions, it is possible to configure pin EDD0 as DEN and EDD1 as DSEL. Therefore, the bit `IECR.PRO+` needs to be set. The DSEL will be set depending on the multiplexer setting `DCR.MUX`.

Table 3 PROFET+ Compliancy

MUX Setting `DCR.MUX`	EDD0 used as DEN	EDD1 used as DSEL
100_b	1	0
101_b	1	1

Note: The usable duty cycle range and diagnostic timings for the external drivers depend on the external driver's characteristics.

6.6 Electrical Characteristics

Electrical Characteristics Power Stages

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output Characteristics							
6.6.1	On-state resistance	$R_{DS(ON)}$				mΩ	
	channel 0, 1						I_L = 7.5 A
			–	3.5	–		1) T_j = 25 °C
			–	7	9		T_j = 150 °C
	channel 2, 3						HWCR.LEDn = 0
							I_L = 2.6 A
			–	11	–		1) T_j = 25 °C
			–	22	28		T_j = 150 °C
							HWCR.LEDn = 1
							I_L = 0.6 A
			–	39	–		1) T_j = 25 °C
			–	78	100		T_j = 150 °C
6.6.2	Output clamp	$V_{DS(CL)}$				V	
	channel 0, 1		32	–	54		T_j = 25 °C I_L = 20 mA
			40	–	55		1) T_j = 150 °C I_L = 6 A
	channel 2, 3		32	–	54		T_j = 25 °C I_L = 20 mA
			40	–	55		1) T_j = 150 °C I_L = 2 A
6.6.3	Output leakage current per channel in stand-by	$I_{L(OFFSTB)}$				µA	OUT.OUTn = 0 DCR.MUX = 111
	channel 0, 1		–	–	2		T_j = 25 °C
			–	–	10		1) T_j = 85 °C
			–	–	50		1) T_j = 105 °C
	channel 2, 3		–	–	1		T_j = 25 °C
			–	–	4		1) T_j = 85 °C
			–	–	20		1) T_j = 105 °C
6.6.4	Output leakage current per channel in idle mode	$I_{L(OFFidle)}$				µA	OUT.OUTn = 0 DCR.MUX ≠ 111
	channel 0, 1		–	–	60		1) T_j = 85 °C
			–	–	80		1) T_j = 105 °C
			–	–	530		T_j = 150 °C
	channel 2, 3		–	–	45		1) T_j = 85 °C
			–	–	50		1) T_j = 105 °C
			–	–	230		T_j = 150 °C

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
6.6.5	Inverse current capability per channel channel 0, 1 channel 2, 3	$-I_{L(IC)}$	 6 2	 – –	 – –	A	[1] No influences on switching functionality of unaffected channels, k_{ILIS} influence according $\Delta k_{ILIS(IC)}$ (9.8.3)
Input Characteristics							
6.6.6	L-input level	$V_{IN(L)}$	0	–	0.8	V	–
6.6.7	H-input level	$V_{IN(H)}$	1.8	–	5.5	V	–
6.6.8	L-input current	$I_{IN(L)}$	3	12	80	µA	[1] V_{IN} = 0.4 V
6.6.9	H-input current	$I_{IN(H)}$	10	40	80	µA	V_{IN} = 5 V

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Timings							
6.6.10	Turn-ON delay to 10% V_{BB}	$t_{delay(ON)}$				µs	[1] V_{BB} = 13.5 V
	channel 0, 1		–	25	–		–
	channel 2, 3		–	20	–		HWCR.LEDn = 0
			–	12	–		HWCR.LEDn = 1
6.6.11	Turn-OFF delay to 90% V_{BB}	$t_{delay(OFF)}$				µs	[1] V_{BB} = 13.5 V
	channel 0, 1		–	75	–		–
	channel 2, 3		–	50	–		HWCR.LEDn = 0
			–	20	–		HWCR.LEDn = 1
6.6.12	Turn-ON time to 90% V_{BB} including turn-ON delay	t_{ON}				µs	V_{BB} = 13.5 V DCR.MUX ≠ 111
	channel 0, 1		–	–	100		R_L = 2.2 Ω
	channel 2, 3		–	–	100		HWCR.LEDn = 0 R_L = 6.8 Ω
			–	–	50		HWCR.LEDn = 1 R_L = 33 Ω
6.6.13	Turn-OFF time to 10% V_{BB} including turn-OFF delay	t_{OFF}				µs	V_{BB} = 13.5 V
	channel 0, 1		–	–	150		R_L = 2.2 Ω
	channel 2, 3		–	–	110		HWCR.LEDn = 0 R_L = 6.8 Ω
			–	–	50		HWCR.LEDn = 1 R_L = 33 Ω
6.6.14	Turn-ON rise time from 10% to 90% V_{BB}	$t_{ON(rise)}$				µs	V_{BB} = 13.5 V DCR.MUX ≠ 111
	channel 0, 1		–	–	55		R_L = 2.2 Ω
	channel 2, 3		–	–	55		HWCR.LEDn = 0 R_L = 6.8 Ω
			–	–	11		HWCR.LEDn = 1 R_L = 33 Ω
6.6.15	Turn-OFF fall time from 90% to 10% V_{BB}	$t_{OFF(fall)}$				µs	V_{BB} = 13.5 V
	channel 0, 1		–	–	55		R_L = 2.2 Ω
	channel 2, 3		–	–	55		HWCR.LEDn = 0 R_L = 6.8 Ω
			–	–	11		HWCR.LEDn = 1 R_L = 33 Ω

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
6.6.16	Turn-ON/OFF matching	$\lvert t_{ON} - t_{OFF} \rvert$				µs	V_{BB} = 13.5 V
	channel 0, 1		–	–	90		R_L = 2.2 Ω
	channel 2, 3		–	–	70		HWCR.LEDn = 0 R_L = 6.8 Ω
			–	–	50		HWCR.LEDn = 1 R_L = 33 Ω
6.6.17	Turn-ON slew rate 30% to 70% V_{BB}	dV/dt_{ON}				V/µs	V_{BB} = 13.5 V
	channel 0, 1		0.2	0.7	2.0		R_L = 2.2 Ω
	channel 2, 3		0.2	0.9	2.5		HWCR.LEDn = 0 R_L = 6.8 Ω
			0.6	2.5	6.0		HWCR.LEDn = 1 R_L = 33 Ω
6.6.18	Turn-OFF slew rate 70% to 30% V_{BB}	$-dV/dt_{OFF}$				V/µs	V_{BB} = 13.5 V
	channel 0, 1		0.2	0.7	2.0		R_L = 2.2 Ω
	channel 2, 3		0.2	0.9	2.5		HWCR.LEDn = 0 R_L = 6.8 Ω
			0.6	2.5	6.0		HWCR.LEDn = 1 R_L = 33 Ω
External Driver Control							
6.6.19	L level external driver output voltage	$V_{EDO(L)}$	0	–	0.4	V	I_{EDO} = -0.5 mA
6.6.20	H level external driver output voltage	$V_{EDO(H)}$	V_{DD} - 0.4V	–	V_{DD}	V	I_{EDO} = 0.5 mA V_{DD} = 4.3 V
6.6.21	External driver output enable time	$t_{EDO(en)}$	–	–	4	µs	1) C_L = 20 pF
6.6.22	External driver output disable time	$t_{EDO(dis)}$	–	–	4	µs	1) C_L = 20 pF
6.6.23	L level external driver diagnosis enable voltage	$V_{EDD(L)}$	0	–	0.4	V	I_{EDD} = -0.5 mA
6.6.24	H level external driver diagnosis enable voltage	$V_{EDD(H)}$	V_{DD} - 0.4V	–	V_{DD}	V	I_{EDD} = 0.5 mA V_{DD} = 4.3 V
6.6.25	External driver diagnosis enable enable time	$t_{EDD(en)}$	–	–	4	µs	1) C_L = 20 pF
6.6.26	External driver diagnosis enable disable time	$t_{EDD(dis)}$	–	–	4	µs	1) C_L = 20 pF

1) Not subject to production test, specified by design.

6.7 Command Description

OUT
Output Configuration Registers

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**

Field	Bits	Type	Description
OUTn n = 5 to 0	n	rw	**Set Output Mode for Channel n** **0** Channel n is switched off 1 Channel n is switched on [1]

1) Channel status depends on automatic PWM generator configuration. For more details, please refer to **Section 7**.

HWCR
Hardware Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**STB**	**CL**

Field	Bits	Type	Description
LEDn n = 3 to 2	n	rw	**Set LED Mode for Channel n** **0** Channel n is in bulb mode 1 Channel n is in LED mode

IECR
Input, External Drive and Current Source Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**COL**	**INCG**	**CSL**	**PRO+**

Field	Bits	Type	Description
PRO+	0	rw	**Configuration of EDD0 and EDD1 to be Compliant to PROFET+** **0** Normal mode 1 EDD0=DEN, EDD1=DSEL
INCG	2	rw	**Input Drive Configuration** **0** Direct drive mode 1 Assigned drive mode
COL	3	rw	**Input Combinatorial Logic Configuration** **0** Input signal OR-combined with according OUT register bit 1 Input signal AND-combined with according OUT register bit

7 Automatic PWM Generator

The SPOC - BTS6480SF has an automatic PWM generator implemented, which allows to operate the channels in PWM mode with drastically reduced micro controller attention compared to a conventional PWM generation via SPI. After the initializing phase, where different settings are done, the PWM generator works autonomously. The only required information from the micro controller is the PWM duty cycle and the channel states (ON-state or OFF-state).

For details about the current sense diagnosis please refer to **Chapter 9**.

7.1 PWM Setup

The PWM operation mode is available for each output. The register CHCRn.FREQ is used to switch from normal mode to automatic PWM generation mode. With CHCRn.FREQ = 00_b the output state is following the OUTn register value. For details please refer to **Figure 5**.

To start the automatic PWM generation the bit PCR.PST has to be set. For details please refer to **Figure 8**.

The device can be woken up also out of stand-by mode by setting the bit PCR.PST. Therefore, the power-on wake up time $t_{WU(PO)}$ (**5.3.14**) has to be considered as delay until the automatic PWM generation will start.

7.2 PWM Clock

The output PWM frequency f_{PWM} can be derived from an external clock f_{PCLK}, which is applied at the pin PCLK, or from an internal clock f_{INT}. The source for the PWM clock can be selected by the SPI register HWCR.CLK.

Note: For avoiding skews it is recommended to change from external to internal clock source or vice versa only during deactivated PWM generator (PCR.PST = 0_b).

7.2.1 External PWM Clock

The output PWM frequency is generated from the PWM clock input signal f_{PCLK} (applied at the pin PCLK), if HWCR.CLK is set to 0_b. The resulting output PWM frequency clock f_{PWM} is:

$$f_{PWM} = \frac{f_{PCLK}}{256 \cdot \text{prescaler}} \quad (1)$$

The prescaler is set via the register CHCRn.FREQ according to:

Table 4 Prescaler Setting

Prescaler Setting CHCRn.FREQ	Resulting Prescaler
00_b	Normal mode without automatic PWM generation
01_b	Prescaler 1: f_{PCLK} (or f_{INT}) / 256
10_b	Prescaler 2: f_{PCLK} (or f_{INT}) / 512
11_b	Prescaler 4: f_{PCLK} (or f_{INT}) / 1024

For example: with f_{in} =102,400 Hz

- CHCRn.FREQ = 01_b: f_{PWM} = 400 Hz
- CHCRn.FREQ = 10_b: f_{PWM} = 200 Hz
- CHCRn.FREQ = 11_b: f_{PWM} = 100 Hz

Note: For avoiding skews it is recommended to change the prescaler setting only during deactivated PWM generator (PCR.PST = 0_b).

The applied clock signal can be monitored via SPI in the standard diagnosis. The standard diagnosis bit CLE provides the information in device operation mode (not during stand-by), if the applied clock is above or below the threshold $f_{PCLK(TH)}$ according to the following table. The bit CLE will be reset after every successful standard diagnosis readout. The reset of the bit CLE is performed only, if the bit CLE is set.

Table 5 External Clock Monitoring

External Clock Status CLE	Clock Frequency
0_b	$f_{PCLK} > f_{PCLK(TH)}$
1_b	$f_{PCLK} < f_{PCLK(TH)}$

Note: A changing of the HWCR.CLKTRIM will also change the CLE thresholds.

7.2.2 Internal PWM Clock

The SPOC - BTS6480SF provides also an internal clock signal f_{INT}. The internal clock frequency is used by setting the register HWCR.CLK to 1_b.

For adjusting the clock signal, a trimming of f_{INT} via the SPI register HWCR.CLK_TRIM can be done. f_{PWM} can be decreased or increased in steps of k_{TRIM}.

$$f_{PWM} = \frac{f_{INT} \pm (x \cdot k_{TRIM})}{256 \cdot \text{prescaler}} \quad (2)$$

7.3 PWM Duty Cycle

The PWM duty cycle of each output is defined by the SPI register DCCRn.DC register from 0 to 256. The ON-state duty cycle is (in %):

$$DC_{PWM} = \frac{\text{DCCRn.DC} \cdot 100}{256} \quad (3)$$

The minimum duty cycle, which can be set (except from 0 %), is according to **Equation (3)** 0.39 %. The duty cycle of the output voltage depends on the switching times t_{ON}, t_{OFF} and the connected load. Therefore, the observed output duty cycle can differ from the set duty cycle.

7.4 Channel Phase Shift

For optimized EMC performances phase shifts between all channels can be programmed via the SPI register CHCRn.PHS. The phase shifts refer to one common start point. Please refer to **Figure 8**. Up to eight different phase shifts can be selected.

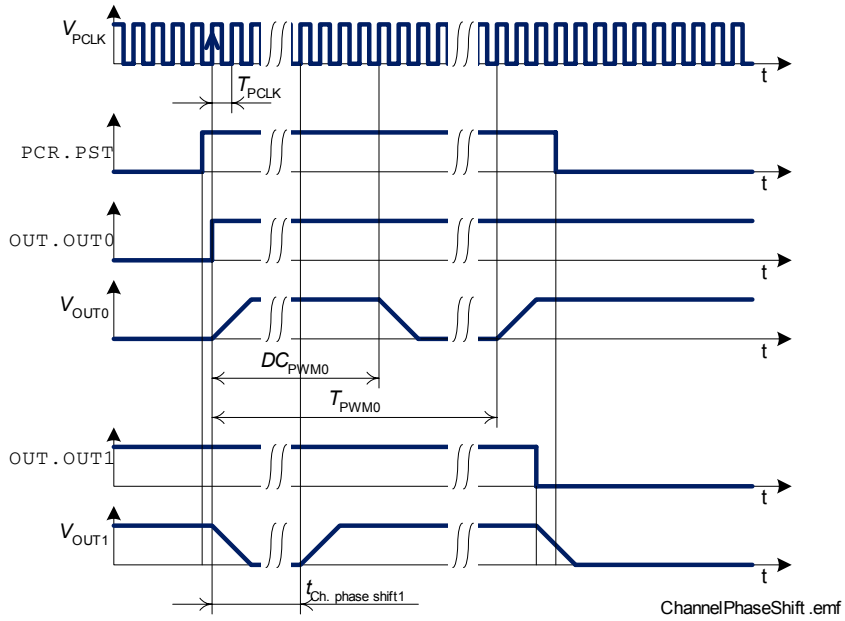


Figure 8 Phase Shifts between Channels

7.5 Daisy Chain Operation with PWM Generator

The SPI of SPOC - BTS6480SF provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. This allows the usage of only one PWM clock input signal f_{PCLK}. To avoid a synchronous activation of channels of the different devices, device phase shift can be programmed at the register PCR.DPSH.

7.5.1 Activation of Several SPOC Devices with PWM Generation

For the usage of several SPOC devices in daisy chain configuration with automatic PWM generation the following procedure is recommended:

- Wake up the devices by setting the DCR.MUX ≠ 111_b
- Set the PWM frequencies, duty cycles, phase shifts of all channels
- Set the device phase shift for each SPOC device differently
- Activate the automatic PWM generator of all devices by setting PCR.PST within one $\overline{MCS}$-frame
- Activate the channels via the SPI registers OUT.OUTn

With the next rising edge of the PWM clock signal f_{PWM} the automatic PWM generation will start. Please see **Figure 9** for details.

Note: If the PWM generator is started during stand-by, the power-on wake up time $t_{WU(PO)}$ (**5.3.14**) has to be considered as delay until the automatic PWM generation will start.

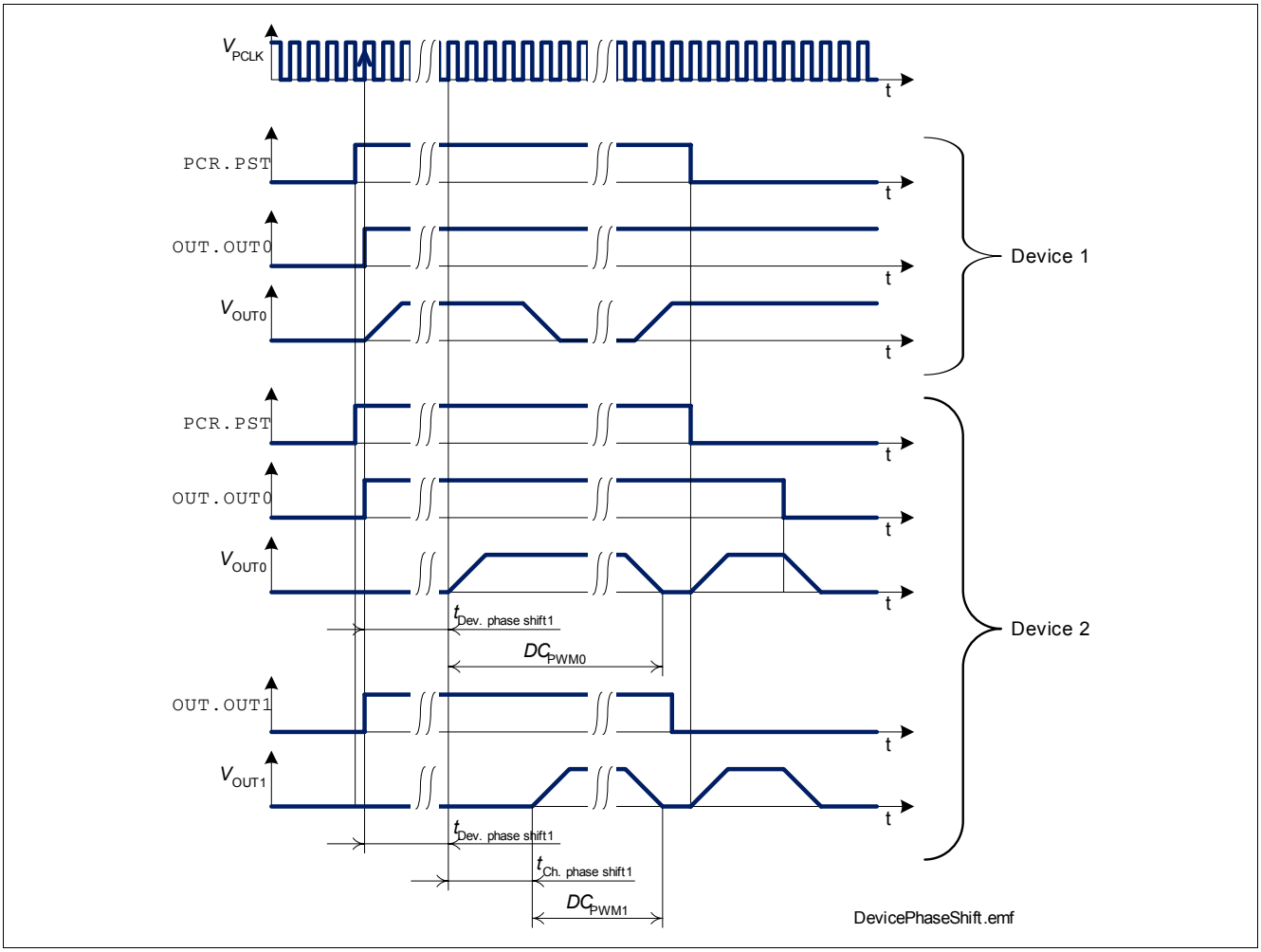


Figure 9 Phase Shifts between Devices

7.5.2 How to resynchronize a Reset SPOC

In case of a reset SPOC device or a SPOC device in stand-by mode the synchronization can be done as follows:

- Set the PWM frequencies, duty cycles, phase shifts of the reset device
- Set the device phase shift for the reset SPOC device
- Deactivate the automatic PWM generation of all SPOC devices in this daisy chain
- With the next SPI transmission activate the automatic PWM generator of all SPOC devices by setting `PCR.PST` within one $\overline{\text{MCS}}$-frame
- Activate the channels of the reset SPOC device via the SPI register `OUT.OUTn`

With the next rising edge of the PWM clock signal f_{PWM} the automatic PWM generation will start again synchronously.

7.6 Electrical Characteristics

Electrical Characteristics Power Stages

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Automatic PWM Generator							
7.6.1	External PWM clock threshold	$f_{PCLK(TH)}$	22	–	46	kHz	HWCR.CLKTRIM = 100
7.6.2	External PWM clock	f_{PCLK}	–	–	250	kHz	–
7.6.3	External PWM clock period	$t_{PCLK(P)}$	4	–	–	µs	1)
7.6.4	External PWM clock high time	$t_{PCLK(H)}$	2	–	–	µs	1)
7.6.5	External PWM clock low time	$t_{PCLK(L)}$	2	–	–	µs	1)
7.6.6	External PWM clock duty cycle range	DC_{PCLK}	30 %	–	70 %		1)
7.6.7	Internal PWM clock	f_{INT}	75	105	135	kHz	HWCR.CLKTRIM = 100
7.6.8	Internal PWM clock trimming step	k_{TRIM}	–	5 %	–		2)

1) Not subject to production test, specified by design. Functional test is performed at f_{PCLK} = 250kHz.

2) Not subject to production test, specified by design.

7.7 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
read	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**STB**	**CL**
write	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**RST**	**CL**

Field	Bits	Type	Description
CLK	5	rw	**Clock Mode** [1] 0 External clock input PCLK is used for PWM mode **1** Internal clock is used for PWM mode
CLKTRIM	8:6	rw	**Internal Clock Trim** 000 f_{INT} - 4 k_{TRIM} ... 011 f_{INT} - 1 k_{TRIM} **100** f_{INT} without trimming 101 f_{INT} + 1 k_{TRIM} ... 111 f_{INT} + 3 k_{TRIM}

1) For avoiding skews it is recommended to change from external to internal clock source or vice versa only during deactivated PWM generator (`PCR.PST` = 0_b).

Standard Diagnosis

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	**0**	**LHI**	**SBM**	**x**	**CLE**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**ERR3**	**ERR2**	**ERR1**	**ERR0**

Field	Bits	Type	Description
CLE	11	r	**External Clock Status** [1] **0** $f_{PCLK} > f_{PCLK(TH)}$ 1 $f_{PCLK} < f_{PCLK(TH)}$

1) Invalid in stand-by mode

CHCRn
Channel Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**1**	**1**	**x**	**x**	**x**	**0**	**0**	**0**	**PHSn**			**SYDELn**		**FREQn**	

Field	Bits	Type	Description
FREQn n = 0 to 5	1:0	rw	**PWM Frequency Prescaler Setting for Channel n** **00** Normal mode without automatic PWM generation 01 Prescaler 1: f_{PCLK} (or f_{INT}) / 256 10 Prescaler 2: f_{PCLK} (or f_{INT}) / 512 11 Prescaler 4: f_{PCLK} (or f_{INT}) / 1024
SYDELn n = 0 to 5	3:2	rw	**Delay of Current Sense Synchronization Signal for Channel n** **00** No synchronization signal delay 01 Synchronization signal delay 1: 8 / (f_{PCLK} (or f_{INT})) 10 Synchronization signal delay 2: 16 / (f_{PCLK} (or f_{INT})) 11 Synchronization signal delay 3: 24 / (f_{PCLK} (or f_{INT}))
PSHn n = 0 to 5	6:4	rw	**Channel Phase Shift for Channel n** **000** No phase shift 001 Phase shift 1: 32 / (f_{PCLK} (or f_{INT})) 010 Phase shift 2: 64 / (f_{PCLK} (or f_{INT})) ... 110 Phase shift 6: 192 / (f_{PCLK} (or f_{INT})) 111 Phase shift 7: 224 / (f_{PCLK} (or f_{INT}))

PCR
PWM Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**DCS**	**DPSH**		**PST**

Field	Bits	Type	Description
PST	0	rw	**Automatic PWM Generation** **0** No automatic PWM generation 1 Automatic PWM generation
DPSH	2:1	rw	**Device Phase Shift** **00** No phase shift 01 Phase shift 1: 8 / (f_{PCLK} (or f_{INT})) 10 Phase shift 2: 16 / (f_{PCLK} (or f_{INT})) 11 Phase shift 3: 24 / (f_{PCLK} (or f_{INT}))
DCS	3	rw	**Single Duty Cycle for all Channels** **0** Duty cycle setting of channel 0 used for all channels 1 Individual duty cycle setting used for each channel

DCCRn
Duty Cycle Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**0**	**1**	**x**	**x**	**x**	**0**	**DCn**								

Field	Bits	Type	Description
DCn n = 0 to 5	8:0	rw	**Duty Cycle for Channel n during Automatic PWM Generation** **000000000** DC value: 0 (channel off) 000000001 DC value: (1 / 256) * 100 000000010 DC value: (2 / 256) * 100 ... 011111111 DC value: (255 / 256) * 100 1xxxxxxxx DC value: 1 (channel 100% on)

8 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

8.1 Over Current Protection

The maximum load current I_L is switched off in case of exceeding the over current trip level $I_{L(trip)}$ by the device itself. Depending on the total short circuit impedance higher current over shoots may occur. A limited auto-restart function is implemented. The number of restarts is dependent of the V_{DS} voltage. Please refer to following figures for details.

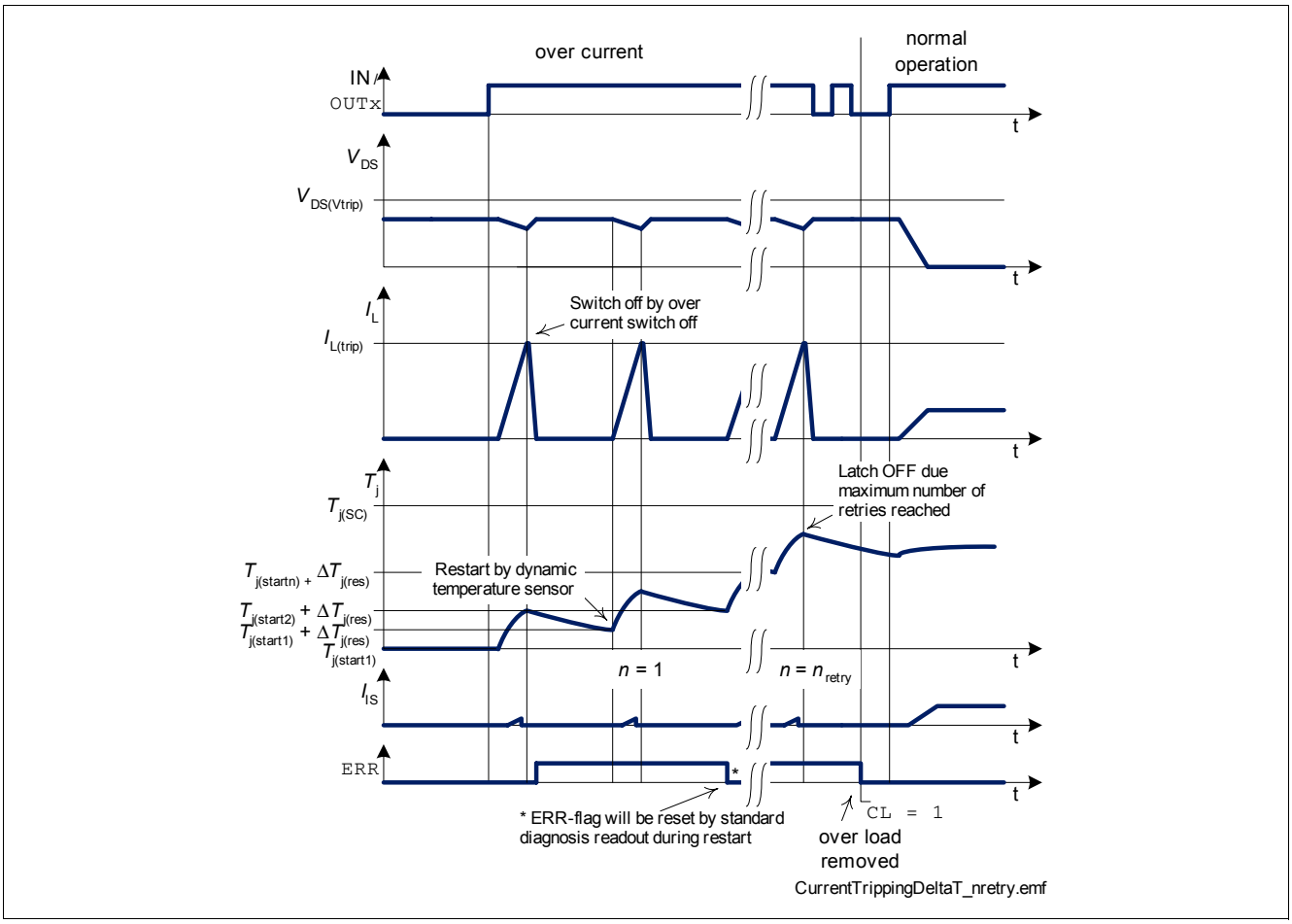


Figure 10 Over current protection with latch due to reaching maximum number of retries n_{retry}

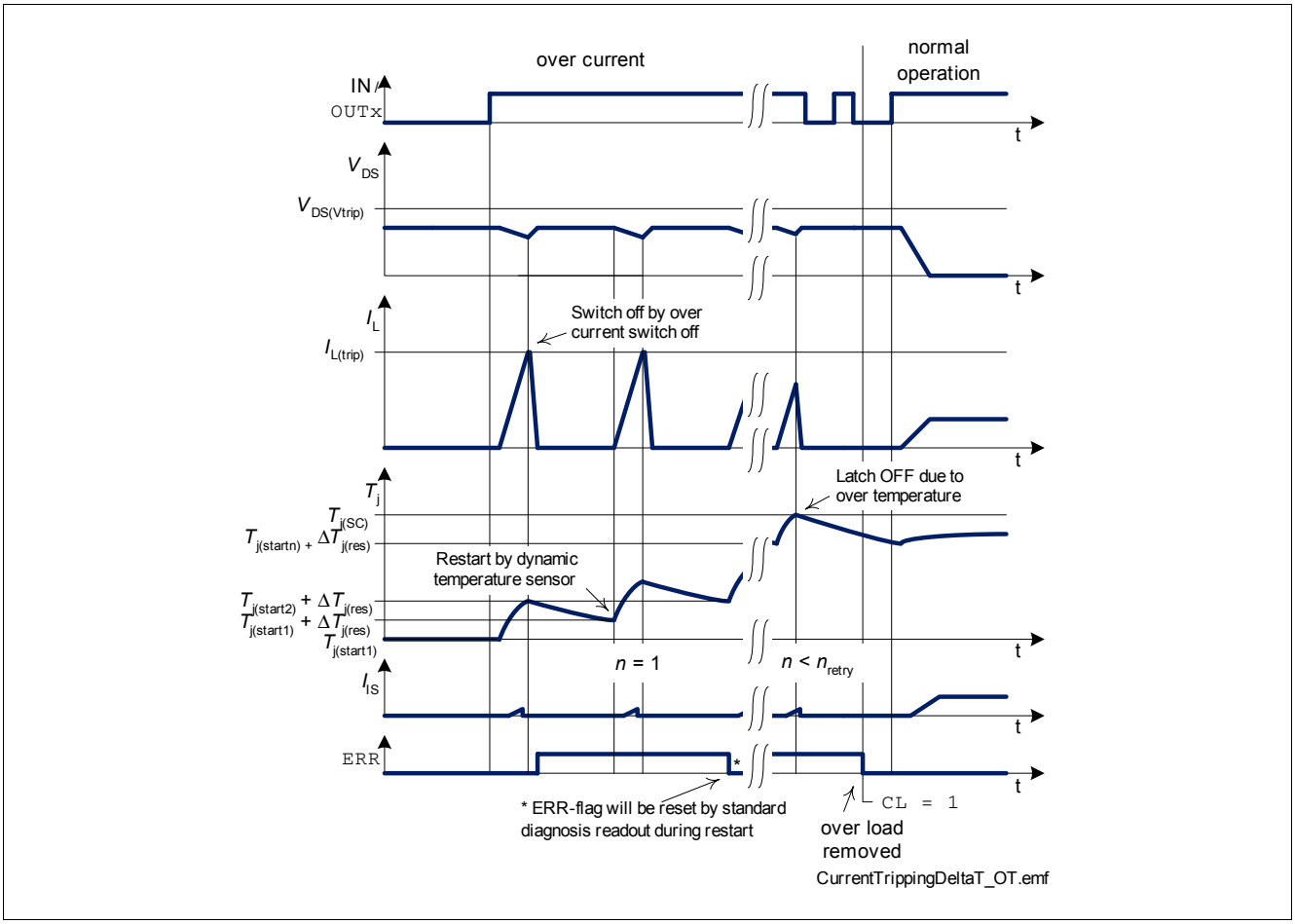


Figure 11 Over current protection with latch due to reaching over temperature $T_{j(SC)}$

The ERR-flag will be set during over current shut down. It can be reset by reading the ERR-flag. If the channel is still in over current shut down, the ERR-flag will be set again. During the automatic restart of the channel the ERR-flag can be cleared by reading the ERR-flag. It will be set again as soon as the over current protection is activated again.

The number of restarts n_{retry} is depending on the V_{DS} voltage according to the following figure and **Chapter 8.2**.

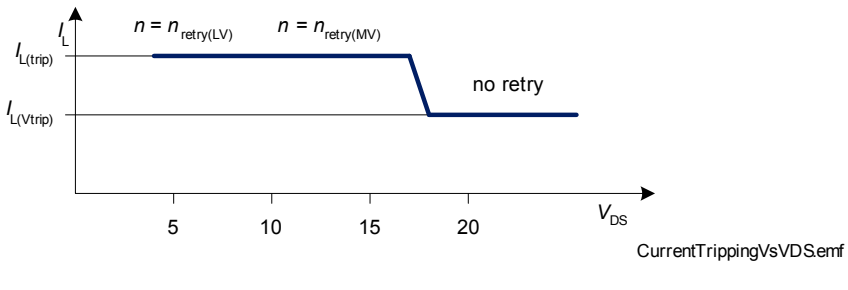


Figure 12 Number of retries and trip levels dependent of V_{DS}

The retry latch or over temperature latch is cleared by SPI command `HWCR.CL = 1b`. If the input pin or the bit in the SPI register `OUT` is still set, the channel will be turned on immediately (or according to the automatic PWM generator setting) after the command `HWCR.CL = 1b`.

8.2 Over Current Protection at high V_{DS}

The SPOC - BTS6480SF provides an over current protection for V_{DS} > $V_{DS(Vtrip)}$ (8.9.5). For V_{DS} > $V_{DS(Vtrip)}$ and I_L > $I_{L(Vtrip)}$ during turn on the channel switches off and latches immediately. For details please refer to parameter $I_{L(VTRIP)}$ (8.9.4).

The current trip level $I_{L(Vtrip)}$ is below the current trip level $I_{L(trip)}$ at V_{DS} = 7V. The ratio between $I_{L(trip)}$ and $I_{L(Vtrip)}$ is defined by the parameter Δk_{TR} (8.9.6).

The over current latch is cleared by SPI command HWCR.CL = 1_b. If the input pin or the bit in the SPI register OUT is still set, the channel will be turned on immediately (or according to the automatic PWM generator setting) after the command HWCR.CL = 1_b.

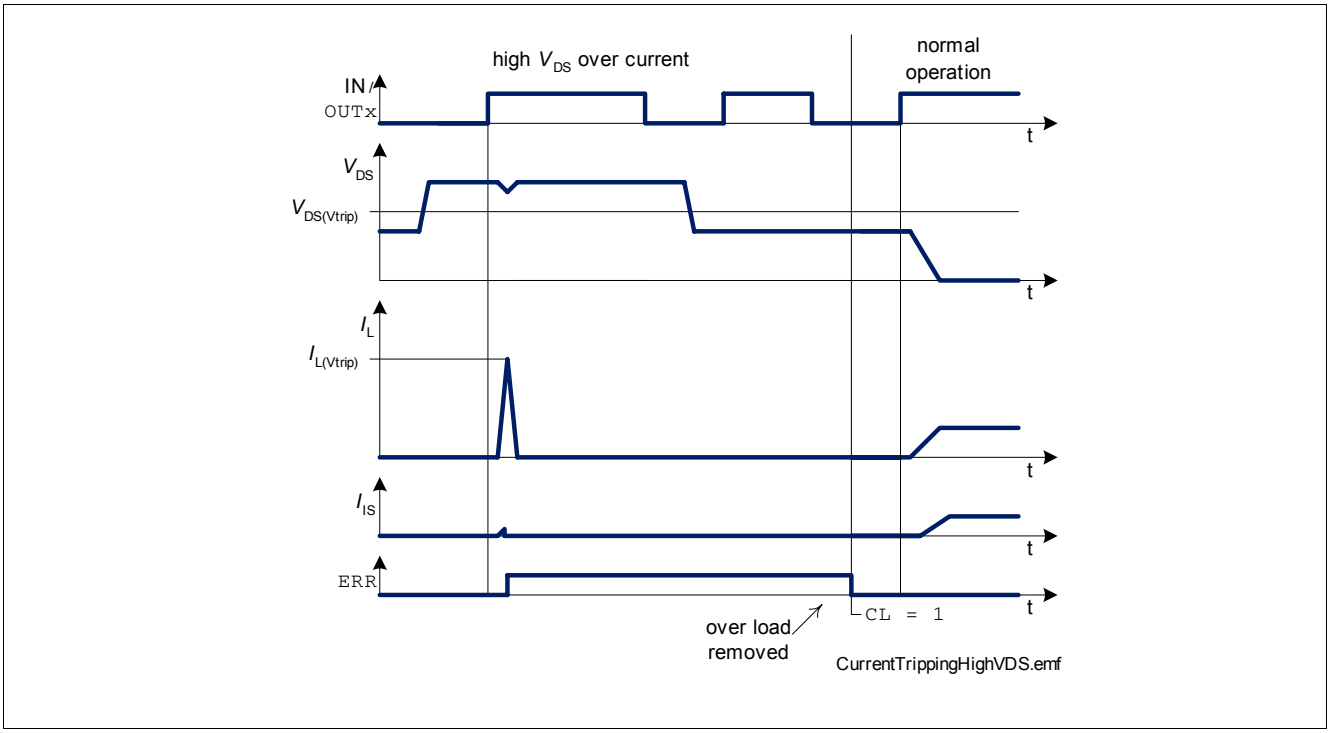


Figure 13 Over current protection in case of high V_{DS} voltages

8.3 Over Current Protection for Short Circuit Type 2 Protection

After activation of the channels without over temperature shutdown and after the delay time $t_{delay(trip)}$ (8.9.2) the over current protection threshold $I_{L(trip)}$ is reduced to $I_{L(Itrip)}$. The delay time $t_{delay(trip)}$ is reset by an dynamic temperature sensor or over current shutdown and any IN, OUTx or automatic PWM generator signal transition. In case of a short circuit to GND event with I_L > $I_{L(Itrip)}$ (8.9.3), which occurs in the on state, the channel is switched off and latched immediately. For more details, please refer to the figure Figure 14.

The current trip level $I_{L(Itrip)}$ is below the current trip level $I_{L(trip)}$ at V_{DS} = 7V. The ratio between $I_{L(trip)}$ and $I_{L(Itrip)}$ is defined by the parameter Δk_{TR} (8.9.6).

The over current latch is cleared by SPI command HWCR.CL = 1_b. If the input pin or the bit in the SPI register OUT is still set, the channel will be turned on immediately (or according to the automatic PWM generator setting) after the command HWCR.CL = 1_b.

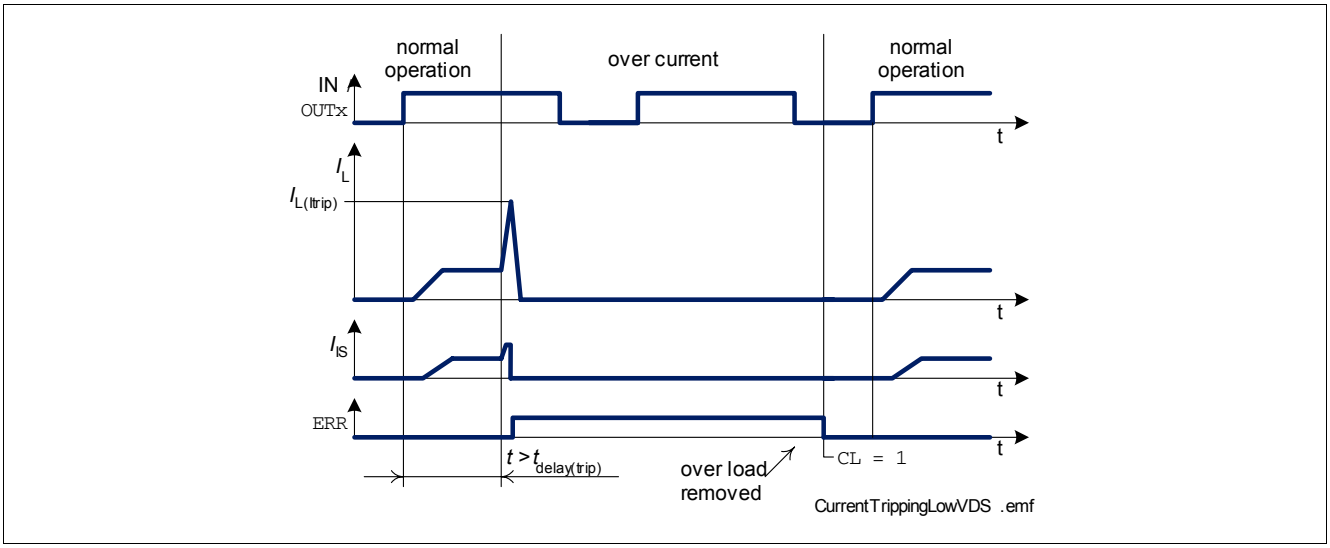


Figure 14 Shut Down by Over Current due to Short Circuit Type 2

8.4 Over Temperature Protection

Each channel has its own temperature sensor. If the temperature at the channel exceeds the thermal shutdown temperature $T_{j(SC)}$, the channel will switch off and latch to prevent destruction (also in case of V_{DD} = 0V). In order to reactivate the channel, the temperature at the output must drop by at least the thermal hysteresis ΔT_j and the over temperature latch must be cleared by SPI command `HWCR.CL = 1b`. If the input pin or the bit in the SPI register `OUT` is still set, the channel will be turned on immediately (or according to the automatic PWM generator setting) after the command `HWCR.CL = 1b`.

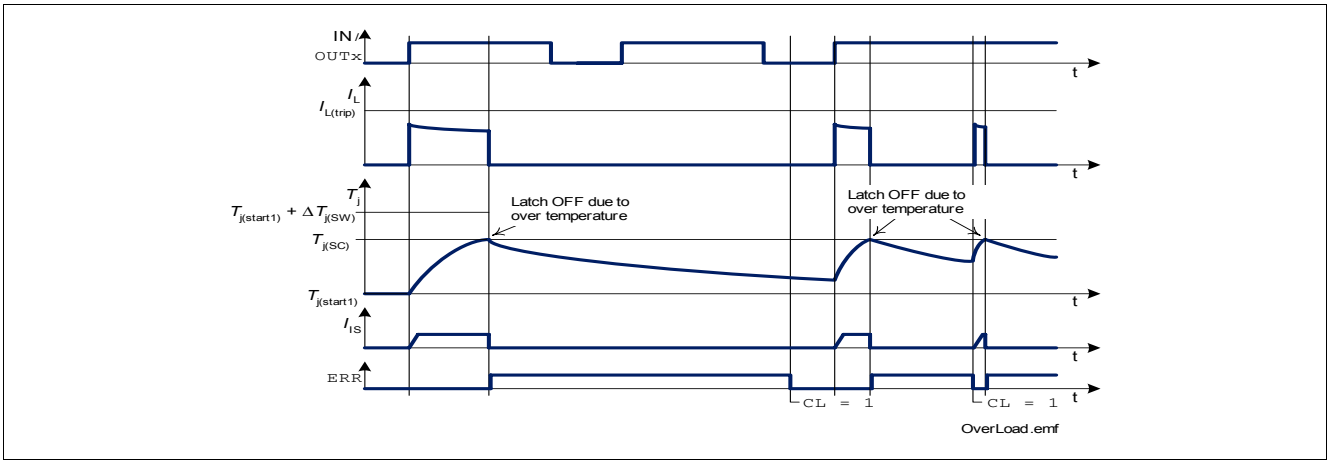


Figure 15 Shut Down by Over Temperature

8.4.1 Dynamic Temperature Sensor Protection

Additionally, each channel has its own dynamic temperature sensor. The dynamic temperature sensor improves short circuit robustness by limiting sudden increases in the junction temperature. The dynamic temperature sensor turns off the channel if its sudden temperature increase exceeds the dynamic temperature sensor threshold $\Delta T_{j(SW)}$. The number of automatic reactivations is limited by n_{retry} (8.9.7). If this number of retries is exceeded the channel turns off and latches. The retry latch is cleared by SPI command `HWCR.CL = 1b`. If the input pin or the bit in the SPI register `OUT` is still set, the channel will be turned on immediately (or according to the automatic PWM generator setting) after the command `HWCR.CL = 1b`. For the condition $n < n_{retry}$ the counter of automatic reactivations will be reset by every low to high transition on the input pin or the bit in SPI register `OUT`.

For automatic PWM generation the counter will be reset also in case of duty cycles < 100% during the off-state. Please refer to **Figure 14** for details.

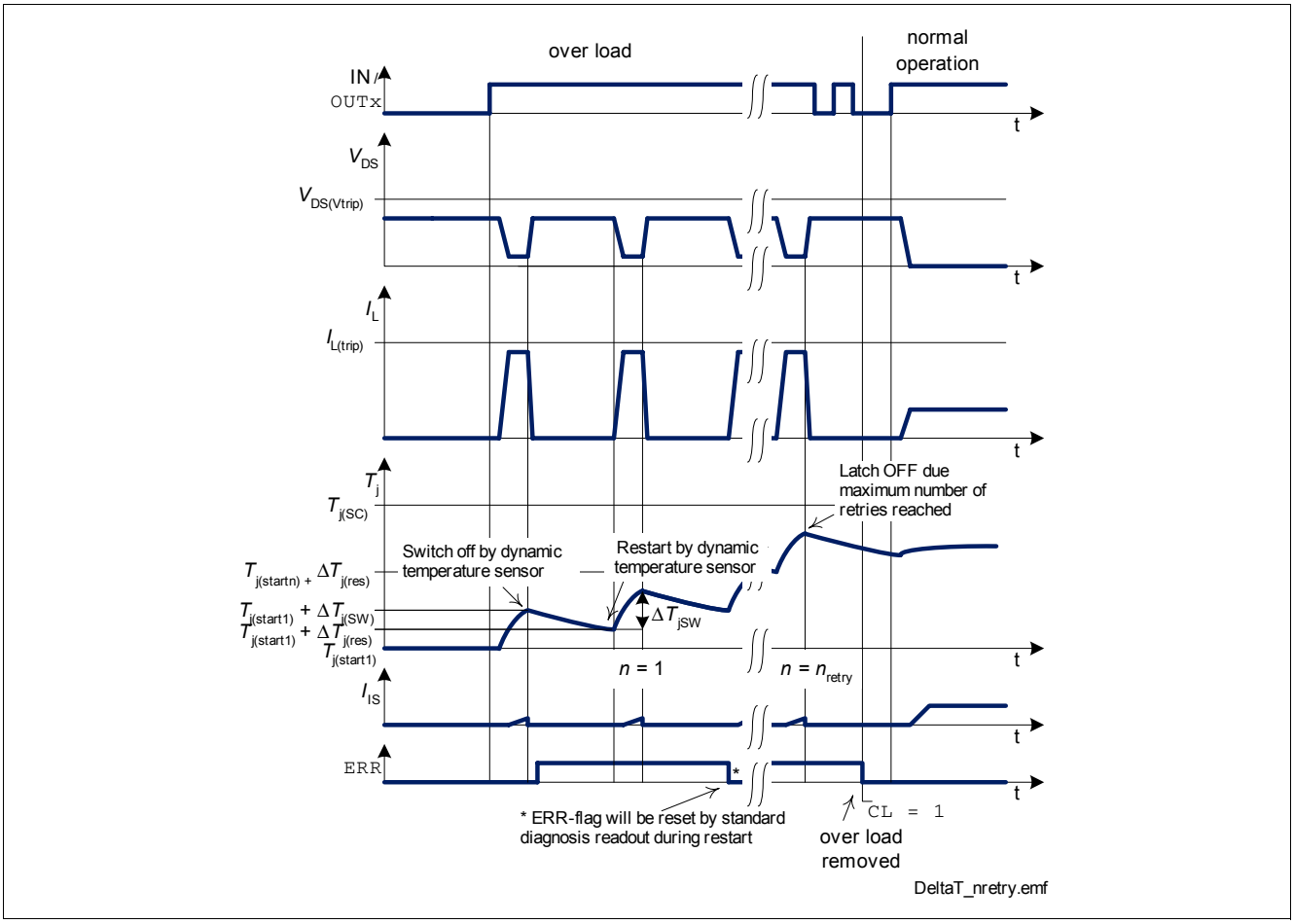


Figure 16 Dynamic Temperature Sensor Operations with latch due to reaching maximum number of retries n_{retry}

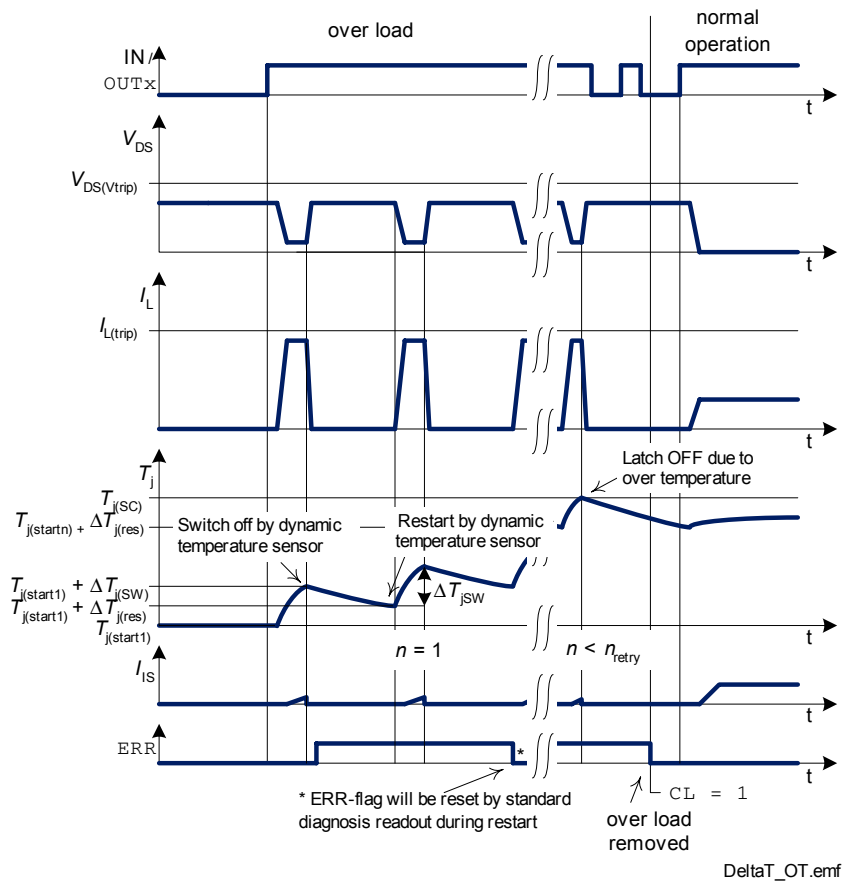


Figure 17 Dynamic Temperature Sensor Operations with latch due to reaching over temperature $T_{j(SC)}$

The ERR-flag will be set during dynamic temperature sensor shut down. It can be reset by reading the ERR-flag. If the channel is still in dynamic temperature sensor shut down, the ERR-flag will be set again. During the automatic restart of the channel the ERR-flag can be cleared by reading the ERR-flag. It will be set again as soon as the dynamic temperature sensor is activated again.

8.5 Reverse Polarity Protection

In reverse polarity mode, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads.The current through the ground pin, sense pin IS, current sense synchronization pin, the logic power supply pin VDD, the SPI pins, input pins, external driver pins, clock input pin and the limp home input pin has to be limited as well (please refer to the maximum ratings listed on **Page 10**).

For reducing the power loss during reverse polarity Reversave™ functionality is implemented for all channels. They are turned on to almost forward condition in reverse polarity condition, see parameter $R_{DS(REV)}$.

Note: No protection mechanism like temperature protection or current protection is active during reverse polarity.

8.6 Over Voltage Protection

In the case of supply voltages between $V_{BB(SC)\,max}$ and $V_{BB(CL)}$ the output transistors are still operational and follow the input or the OUT register. Parameters are not warranted and lifetime is reduced compared to normal mode.

In addition to the output clamp for inductive loads as described in **Section 6.3**, there is a clamp mechanism available for over voltage protection for the logic and all channels.

8.7 Loss of Ground

In case of complete loss of the device ground connections, but connected load ground, the SPOC - BTS6480SF securely changes to or stays in OFF-state.

8.8 Loss of V_{BB}

In case of loss of V_{BB} connection in on-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from VBB to ground. For example, a suppressor diode is recommended between VBB and GND.

8.9 Electrical Characteristics

Electrical Characteristics Protection Functions

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
8.9.1	Load current trip level	$I_{L(trip)}$				A	V_{DS} < 7 V
	channel 0, 1		71	–	120		T_j = -40 °C
			–	90	–		1) T_j = 25 °C
			67	–	100		T_j = 150 °C
	channel 2, 3						HWCR.LEDn = 0
			29	–	44		T_j = -40 °C
			–	30	–		1) T_j = 25 °C
			23	–	39		T_j = 150 °C
							HWCR.LEDn = 1
			7	–	12		T_j = -40 °C
			–	8.5	–		1) T_j = 25 °C
			5.5	–	11		T_j = 150 °C
Over Current Protection							
8.9.2	Over current tripping activation time	$t_{delay(trip)}$	7	–	14	ms	1)
8.9.3	Load current trip level after $t_{delay(trip)}$	$I_{L(Itrip)}$				A	
	channel 0, 1		40	–	78		T_j = -40 °C
			35	–	70		T_j = 150 °C
	channel 2, 3						HWCR.LEDn = 0
			17	–	35		T_j = -40 °C
			15.5	–	30		T_j = 150 °C
							HWCR.LEDn = 1
			3.8	–	9		T_j = -40 °C
			3.8	–	8		T_j = 150 °C
8.9.4	Load current trip level at high V_{DS}	$I_{L(Vtrip)}$				A	1)
	channel 0, 1		40	–	78		T_j = -40 °C
			35	–	70		T_j = 150 °C
	channel 2, 3						HWCR.LEDn = 0
			17	–	35		T_j = -40 °C
			15.5	–	30		T_j = 150 °C
							HWCR.LEDn = 1
			3.8	–	9		T_j = -40 °C
			3.8	–	8		T_j = 150 °C
8.9.5	Over current tripping at high V_{DS} activation level	$V_{DS(Vtrip)}$	15	–	–	V	1)
8.9.6	Current trip at V_{DS} = 7 V to current trip at V_{DS} = 20 V ratio	Δk_{TR}	1.2	1.5	–		1)

Electrical Characteristics Protection Functions (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Temperature Protection							
8.9.7	Number of automatic retries at over current or dynamic temperature sensor shut down at low V_{DS}	$n_{retry(LV)}$	–	32	–		1) V_{DS} = 9 V
8.9.8	Number of automatic retries at over current or dynamic temperature sensor shut down at medium V_{DS}	$n_{retry(MV)}$	–	8	–		1) V_{DS} = 13 V
8.9.9	Thermal shut down temperature	$T_{j(SC)}$	150	175	195	°C	1)
8.9.10	Thermal hysteresis of thermal shutdown	ΔT_j	–	10	–	K	1)
8.9.11	Dynamic temperature increase limitation while switching	$\Delta T_{j(SW)}$	–	60	–	K	1)
8.9.12	Dynamic temperature sensor restart	$\Delta T_{j(res)}$	–	20	–	K	1)
Reverse Battery							
8.9.13	On-state resistance	$R_{DS(REV)}$				mΩ	1) V_{BB} = -13.5 V
	channel 0, 1						I_L = -7.5 A
			–	4.7	–		T_j = 25 °C
			–	9.5	–		T_j = 150 °C
	channel 2, 3						I_L = -2.6 A
			–	14.7	–		T_j = 25 °C
			–	29.5	–		T_j = 150 °C
Over Voltage							
8.9.14	Over voltage protection	$V_{BB(CL)}$				V	
	VBB to GND		40	55	70		I_{GND} = 5 mA
	channel 0, 1		32	–	54		T_j = 25 °C I_L = 20 mA
			40	–	55		1) T_j = 150 °C I_L = 6 A
	channel 2, 3		32	–	54		T_j = 25 °C I_L = 20 mA
			40	–	55		1) T_j = 150 °C I_L = 2 A

1) Not subject to production test, specified by design.

8.10 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
read	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**STB**	**CL**
write	**1**	**0**	**0**	**1**	**0**	**0**	**CLKTRIM**			**CLK**	**0**	**LED3**	**LED2**	**RST**	**CL**

Field	Bits	Type	Description
CL	0	rw	**Clear Latch** **0** Thermal and over current latches are untouched 1 Command: Clear all thermal and over current latches

Standard Diagnosis

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	**0**	**LHI**	**SBM**	**x**	**CLE**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**ERR3**	**ERR2**	**ERR1**	**ERR0**

Field	Bits	Type	Description
ERRn n = 0 to 3	3:0	r	**Error Flag for Channel n** **0** No error 1 Error occurred

9 Diagnosis

For diagnosis purpose, the SPOC - BTS6480SF provides a current sense signal at pin IS and the diagnosis word via SPI. There is a current sense multiplexer implemented that is controlled via SPI. The sense signal can also be disabled by SPI command. A switch bypass monitor allows to detect a short circuit between the output pin and the battery voltage.

In OFF-state a current source is able to be switched on for a selected channel with the DCR.CSOL bit. This allows open load / short circuit detection to V_{BB} in OFF-state. The current value can be configured to a low or a high value by programming the bit IECR.CSL. Please refer to parameter $I_{L(OL)}$ (9.8.15).

Note: Please note: All below stated parameters and functions are valid for the internal channels. The behavior of the current sense of the two external channel is restricted to the behavior of the external drivers.

Please refer to **Figure 18** for details on diagnosis function:

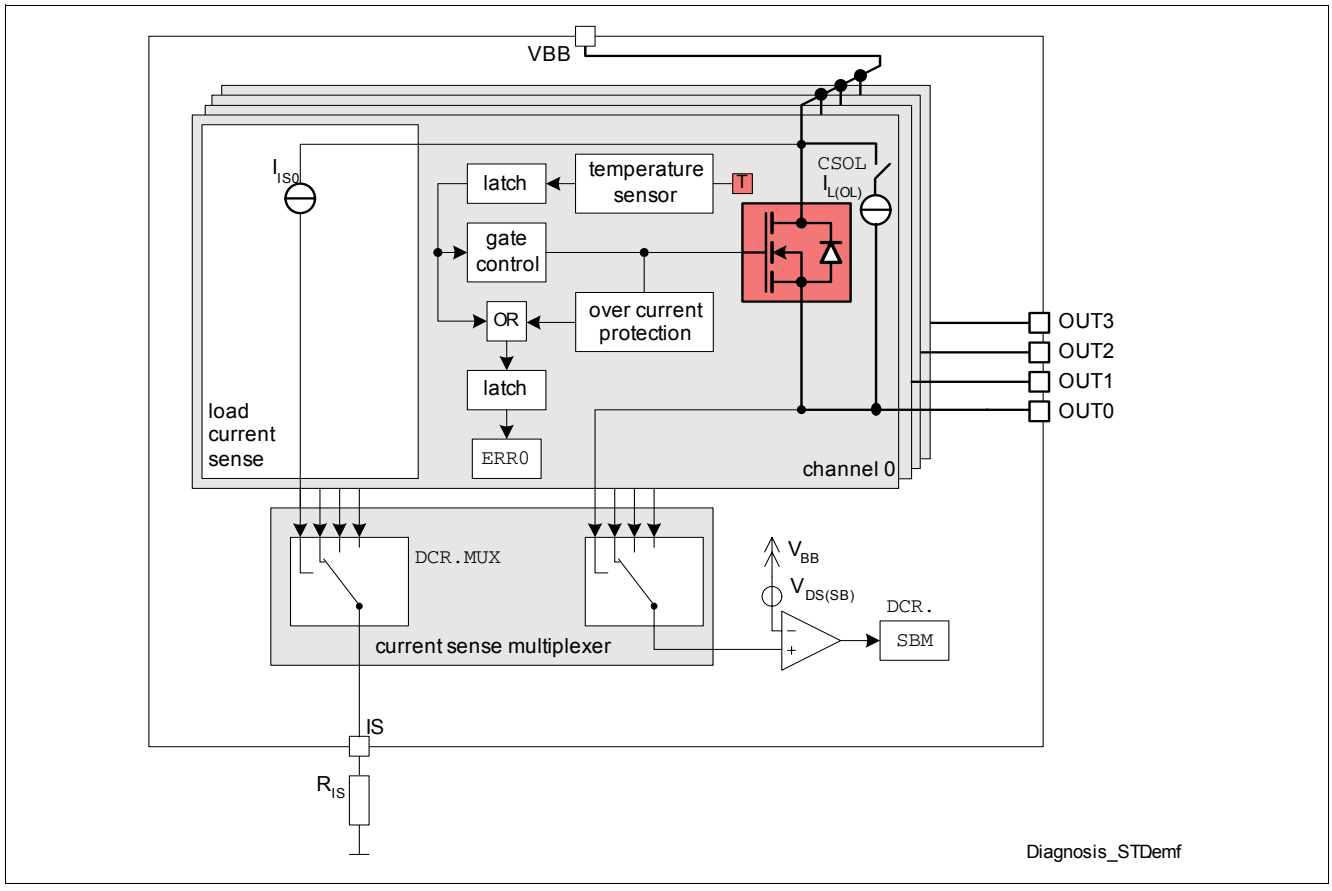


Figure 18 Block diagram: Diagnosis

For diagnosis feedback at different operation modes, please see following table.

Table 6 Operation Modes [1)]

Operation Mode	Input Level OUT.OUTn	Output Level V_{OUT}	Current Sense I_{IS}	Error Flag ERRn[2)]	SBM DCR.SBM
Normal Operation (OFF)	L / 0 (OFF-state)	GND	Z	0	1
Short Circuit to GND		GND	Z	0	1
Thermal shut down		Z	Z	0	x
Short Circuit to V_{BB}		V_{BB}	Z	0	0
Open Load		Z	Z	0	0[3)]
Inverse Current		> V_{BB}	Z	0	0[4)]
Normal Operation (ON)	H / 1 (ON-state)	~ V_{BB}	I_L / k_{ILIS}	0	0
Short Circuit to GND		~ GND	Z	1	1
Dynamic Temperature Sensor shut down		Z	Z	1	x
Over Current shut down		Z	Z	1[5)]	x
Thermal shut down		Z	Z	1[6)]	x
Short Circuit to V_{BB}		V_{BB}	< I_L / k_{ILIS}	0	0
Open Load		V_{BB}	Z	0	0
Inverse Current		> V_{BB}	Z	0	0

1) L = low level, H = high level, Z = high impedance, potential depends on leakage currents and external circuit x = undefined
2) The error flags are latched until they are transmitted in the standard diagnosis word via SPI
3) If the current sense multiplexer is set to Channel 0 to 3 and DRC.CSOL bit set
4) If the current sense multiplexer is set to Channel 0 to 3
5) The over current latch off flag is set latched and can be cleared by SPI command HWCR.CL
6) The over temperature flag is set latched and can be cleared by SPI command HWCR.CL

9.1 Diagnosis Word at SPI

The standard diagnosis at the SPI interface provides information about each channel. The error flags, an OR combination of the over temperature flags and the over load monitoring signals are provided in the SPI standard diagnosis bits ERRn.

The over load monitoring signals are latched in the error flags and cleared each time the standard diagnosis is transmitted via SPI. In detail, they are cleared between the second and third raising edge of the SCLK signal.

The over temperature flags, which cause an overheated channel to latch off, are latched directly at the gate control block. The over current flags, which cause an channel 0 or 1 driving a too high current to switch off, are latched like the over temperature flags. Those latches are cleared by SPI command HWCR.CL.

Please note: The over temperature and over current information is latched twice. When transmitting a clear latch command (HWCR.CL), the error flag is cleared during command transmission of the next SPI frame and ready for latching after the third raising edge of the SCLK signal. As a result, the first standard diagnosis information after a CL command will indicate a failure mode at the previously affected channels although the thermal latches have been cleared already. In case of continuous over load, the error flags are set again immediately because of the over load monitoring signal.

9.2 Load Current Sense Diagnosis

There is a current sense signal available at pin IS which provides a current proportional to the load current of one selected channel. The selection is done by a multiplexer which is configured via SPI.

Current Sense Signal

The current sense signal (ratio $k_{ILIS} = I_L / I_S$) is provided during on-state as long as no failure mode occurs.The ratio k_{ILIS} can be adjusted to the load type (LED or bulb) via SPI register HWCR for channel 2 and 3. The accuracy of the ratio k_{ILIS} depends on the load current.Usually a resistor R_{IS} is connected to the current sense pin. It is recommended to use resistors 1.5 kΩ < R_{IS} < 5 kΩ. A typical value is 2.7 kΩ.

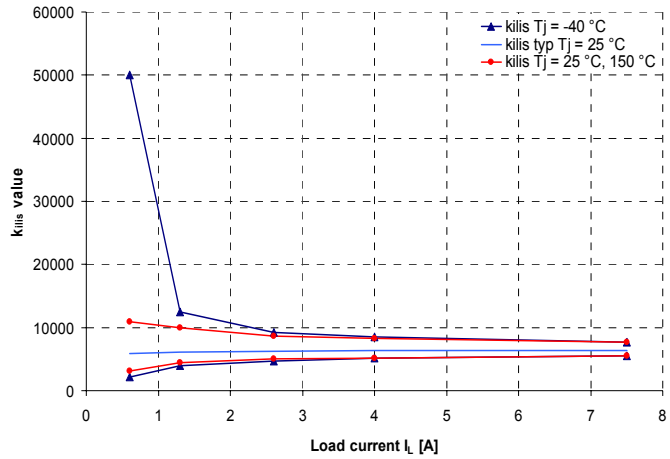


Figure 19 Current Sense Ratio k_{ILIS} Channel 0, 1 [1)]

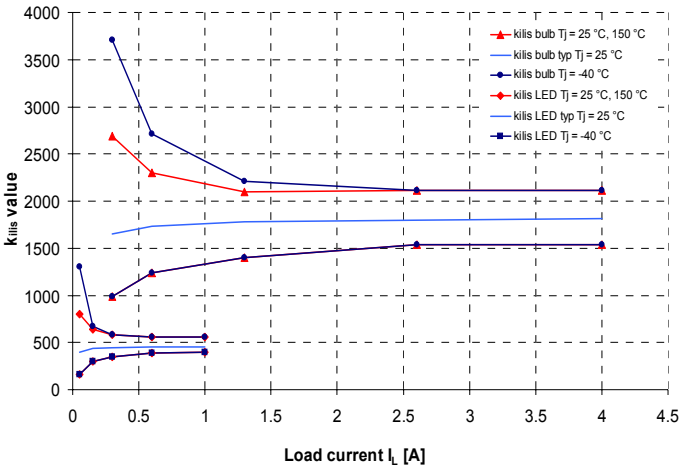


Figure 20 Current Sense Ratio k_{ILIS} Channel 2, 3 [2)]

In case of off-state, over current, dynamic temperature sensor shut down ($n < n_{retry}$), dynamic temperature sensor latch ($n = n_{retry}$) as well as over temperature, the current sense signal of the affected channel is switched off. To distinguish between over temperature or over current and over load, the SPI diagnosis word can be used. Whereas the over load and dynamic temperature sensor shut down ($n < n_{retry}$) flag is cleared every time the diagnosis is transmitted. The over temperature, dynamic temperature sensor latch ($n = n_{retry}$) and over current flag is cleared by a dedicated SPI command (HWCR.CL).

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 9.8** (Position **9.8.1**).

2) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 9.8** (Position **9.8.1**).

Details about timings between the current sense signal I_{IS} and the output voltage V_{OUT} and the load current I_L can be found in **Figure 21**.

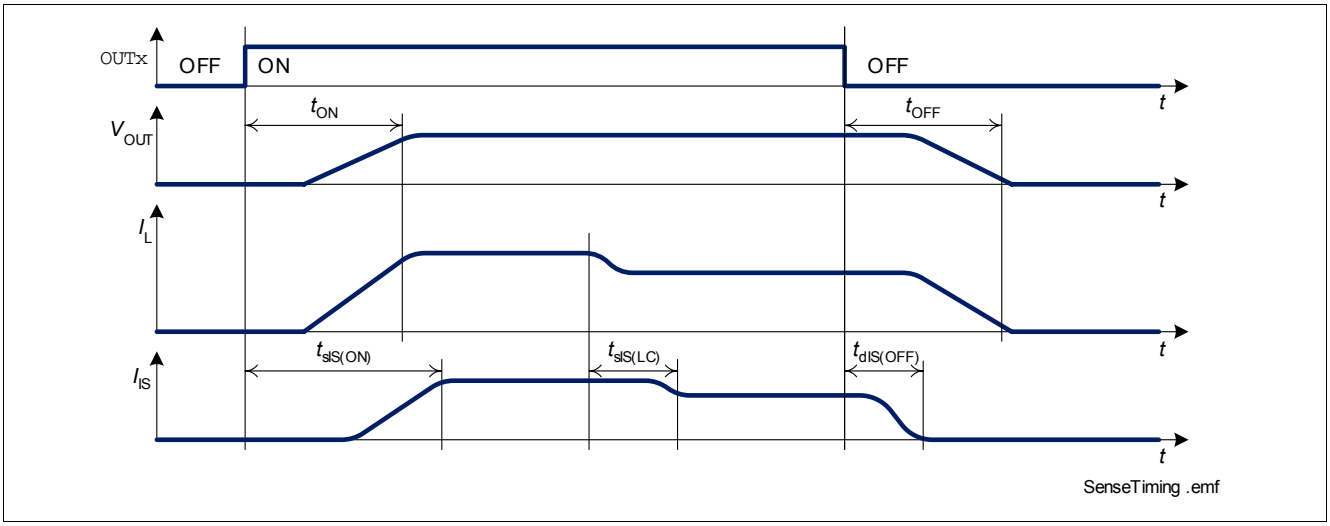


Figure 21 Timing of Current Sense Signal

Current Sense Multiplexer

There is a current sense multiplexer implemented in the SPOC - BTS6480SF that routes the sense current of the selected channel to the diagnosis pin IS. The channel is selected via SPI register `DCR.MUX`. The sense current also can be disabled by SPI register `DCR.MUX`. For details on timing of the current sense multiplexer, please refer to **Figure 22**.

The current sense diagnosis enable signal for the external smart power drivers also can be selected via the SPI register `DCR.MUX`. For being compliant to PROFET+ diagnostic functions, it is possible to configure pin EDD0 as DEN and EDD1 as DSEL. Therefore, the bit `IECR.PRO+` needs to be set.

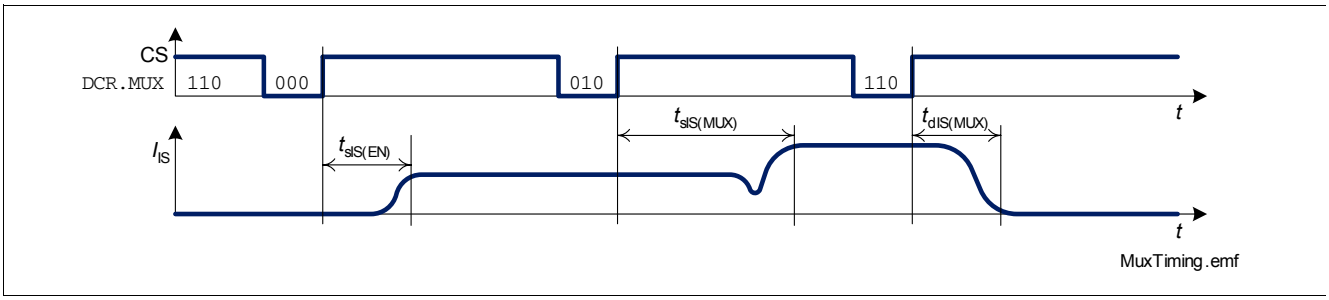


Figure 22 Timing of Current Sense Multiplexer

9.3 Sense Synchronization during Automatic PWM Generation

For performing current sense measurements there is a current sense synchronization signal at the pin ISSY available. This signal indicates the possible start of V_{IS} measurement. The synchronization signal will be activated after the time $t_{Measurement\ delay}$ after channel's activation. The delay time can be configured via SPI register `CHCRn.SYDEL`. The current sense synchronization signal is only available during the automatic PWM generation, i.e. the bit `PCR.PST` is set.

Figure 23 shows the functionality of the current sense synchronization signal.

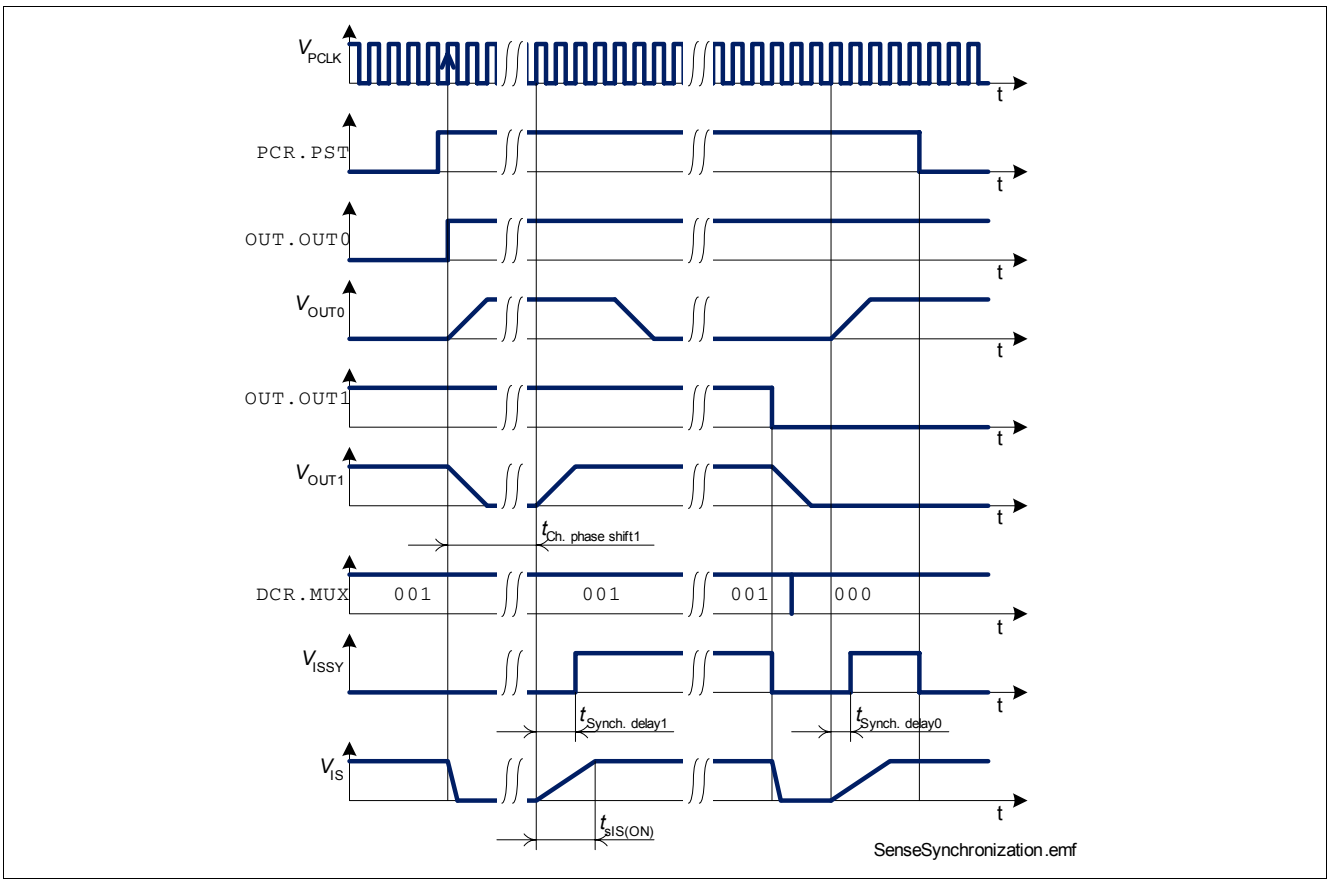


Figure 23 Current Sense Synchronization

9.4 Sense Measurement without Synchronization Signal

The SPOC - BTS6480SF refers all the channel activations to the clock signal f_{PCLK} or f_{INT}. In case of using the external clock f_{PCLK} the state (ON- or OFF-state) is known by the micro controller, which allows a time based processing.

In case of micro controller's loss of the PCLK synchrony the automatic PWM generation can be started again by resetting and setting of the bit PCR.PST. After that the micro controller is synchronous to the automatic PWM generation.

9.5 Automatic Current Sense Multiplexer Switching

The device provides for current sense measurements a function, which changes the current sense multiplexer sequentially and automatically. The function starts after the PWM reference point has passed, which happens each 1024 clock cycles (f_{PCLK} or f_{INT}). For more details please refer to figure **Figure 24**. The current sense multiplexer is switched first to the channel 0. When the current sense synchronization signal at the pin ISSY is finished, the multiplexer is programmed automatically to channel 1 (one clock cycle after the high low transition of the ISSY signal) and so on. The current sense synchronization signal at the pin ISSY will be set for eight clock cycles, if the channel duty cycle is 0 % < DC <100 %. For the scenario, where the channel is continuously on (DC = 100 %) or off (DC = 0 %), or the $t_{ISSY\ delay} > t_{duty\ cycle}$ (delay longer than on-state of channel) the sense synchronization signal will be set for nine clock cycles (f_{PCLK} or f_{INT}). Furthermore, to shorten the ISSY burst length for channels continuously in ON- or OFF-state, the ISSY signal will be started 11 clock cycles after the previous ISSY pulse.

If the synchronization delay is programmed to 11_b the following channel needs at minimum a synchronization delay ≥ = 01_b, otherwise the next ISSY signal will be delayed by one period of the following channel.

This multiplexer switching loop is done only once after the bit DCR.AMUX is set. After the completed loop the bit will be set to DCR.AMUX = 0_b automatically. For more details please refer to **Figure 24**.

The automatic multiplexer switching can be stopped manually by setting the bit DCR.AMUX = 0_b.

Note: The phase shifts between the channels have to be programmed in ascending order (channel 0 with minimum phase shift, channel 1 with a higher phase shift than channel 0, channel 2 with a higher phase shift than channel 1, ...) to get a short AMUX burst duration. Otherwise the duration for a complete automatic multiplexer cycle will increase until a new PWM reference point has passed and the channel is activated. During the activated AMUX bit any command, which should change the multiplexer, will be ignored. If a channel is switched continuously off, the current sense multiplexer will be switched to high impedance during the sense synchronization pulse.

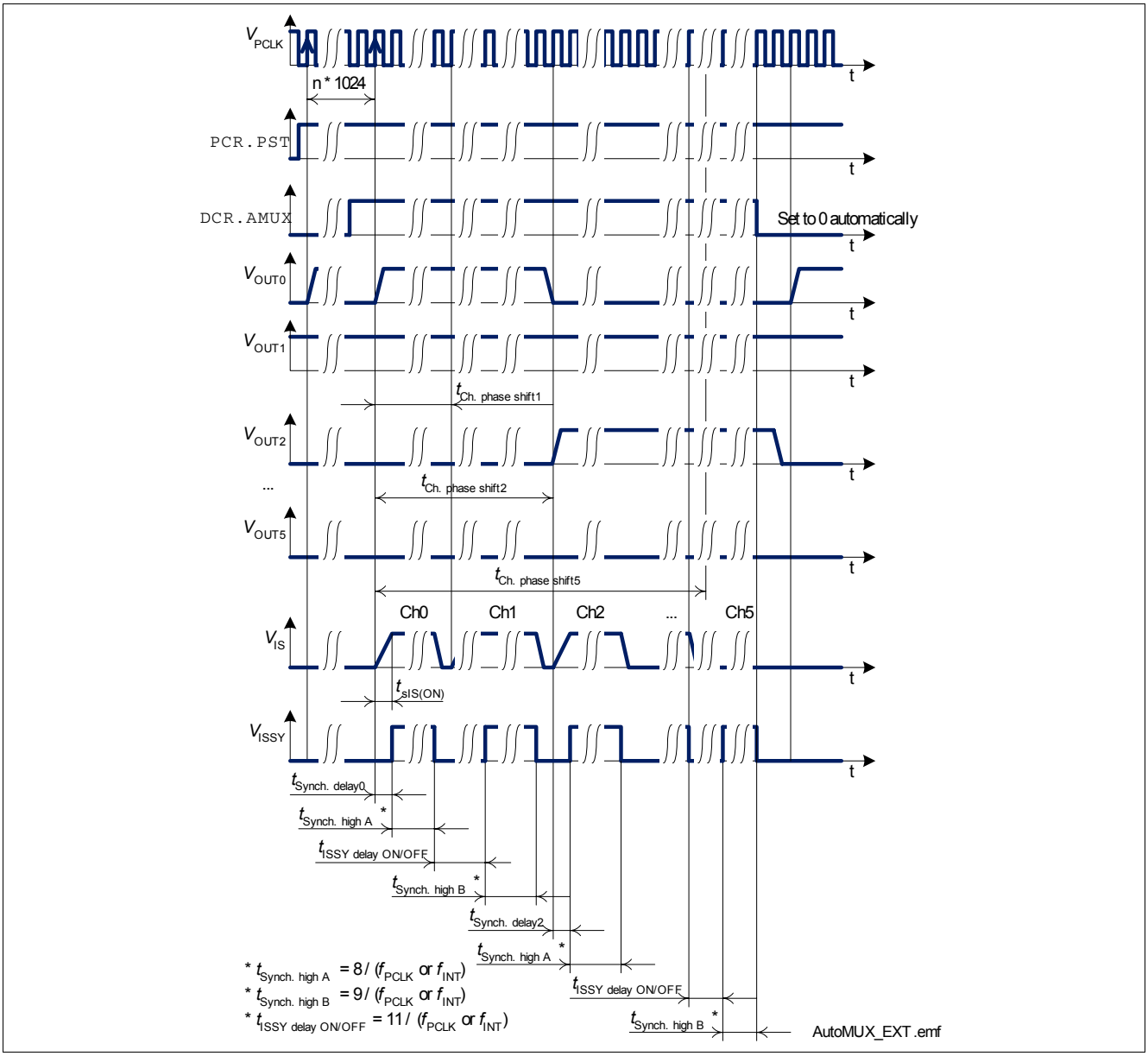


Figure 24 Automatic Current Sense Multiplexer Switching

9.6 Switch Bypass Diagnosis

To detect short circuit to V_{BB}, there is a switch bypass monitor implemented for all internal channels. In case of short circuit between the output pin OUT and V_{BB} in ON-state, the current will flow through the power transistor as well as through the short circuit (bypass) with undefined ratio. As a result, the current sense signal will show lower values than expected by the load current. In OFF-state, the output voltage will stay close to V_{BB} potential which means a small V_{DS}.

The switch bypass monitor compares the voltage V_{DS} across the power transistor of that channel, which is selected by the current sense multiplexer (DCR.MUX) with threshold $V_{DS(SB)}$. The result of comparison can be read in SPI register DCR.SBM or in the standard diagnosis.

9.7 Open Load in OFF-State

For performing a dedicated open load in OFF-state detection a current source can be switched in parallel to the DMOS according to the **Figure 18**. The current source current can be programmed in two steps by the bit IECR.CSL.

The following procedure is recommended to use:

- Select the dedicated channel with the multiplexer
- Enable the open load current with the DCR.CSOL bit
- Read the DCR.SBM or the standard diagnosis
- Disable the open load current with the DCR.CSOL bit

9.8 Electrical Characteristics

Electrical Characteristics Diagnosis

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Load Current Sense							
9.8.1	Current sense ratio	k_{ILIS}					T_j = -40 °C
	channel 0, 1:						
	0.600 A		2190	5840	50010		–
	1.3 A		3990	6140	12510		–
	2.6 A		4690	6350	9210		–
	4.0 A		5130	6430	8510		–
	7.5 A		5490	6480	7710		–
	channel 2, 3 (bulb):						HWCR.LEDn = 0
	0.300 A		990	1670	3710		–
	0.600 A		1240	1750	2710		–
	1.3 A		1400	1800	2210		–
	2.6 A		1540	1830	2110		–
	4.0 A		1540	1840	2110		–
	channel 2, 3 (LED):						HWCR.LEDn = 1
	0.050 A		165	400	1305		–
	0.150 A		300	440	675		–
	0.300 A		350	450	580		–
	0.600 A		385	460	555		–
	1.0 A		400	500	555		–
9.8.2	Current sense ratio	k_{ILIS}					T_j = 25 °C to 150 °C
	channel 0, 1:						
	0.600 A		3120	5840	10960		–
	1.3 A		4420	6140	10010		–
	2.6 A		5030	6350	8660		–
	4.0 A		5130	6430	8240		–
	7.5 A		5490	6480	7710		–
	channel 2, 3 (bulb):						HWCR.LEDn = 0
	0.300 A		990	1670	2690		–
	0.600 A		1240	1750	2300		–
	1.3 A		1400	1800	2100		–
	2.6 A		1540	1830	2110		–
	4.0 A		1540	1840	2110		–
	channel 2, 3 (LED):						HWCR.LEDn = 1
	0.050 A		165	400	805		–
	0.150 A		300	440	640		–
	0.300 A		350	450	580		–
	0.600 A		385	460	555		–
	1.0 A		400	500	555		–

Electrical Characteristics Diagnosis (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
9.8.3	Current sense drift of unaffected channel during inverse current of other channels	$\Delta k_{ILIS(IC)}$					1) DCR.MUX ≠ 111
	channel 0, 1						$I_{L0,1}$ = 7.5 A
			-20 %	–	20 %		$I_{L1,0\,(IC)}$ = 7.5 A
			-20 %	–	20 %		$I_{L2,3\,(IC)}$ = 2.6 A
	channel 2, 3 (bulb)						HWCR.LEDn = 0
							$I_{L2,3}$ = 2.6 A
			-20 %	–	20 %		$I_{L0,1\,(IC)}$ = 7.5 A
			-20 %	–	20 %		$I_{L3,2\,(IC)}$ = 2.6 A
	channel 2, 3 (LED)						HWCR.LEDn = 1
							$I_{L2,3}$ = 0.6 A
			-20 %	–	20 %		$I_{L0,1\,(IC)}$ = 7.5 A
			-20 %	–	20 %		$I_{L3,2\,(IC)}$ = 2.6 A
9.8.4	Current sense voltage limitation	$V_{IS(LIM)}$	0.9 × V_{DD}	V_{DD}	1.1 × V_{DD}	V	DCR.MUX = 011 I_{L3} = 2 A R_{IS} = 2.7 kΩ
9.8.5	Maximum steady state current sense output current	$I_{IS(MAX)}$	5.5	–	–	mA	1) V_{IS} = 0 V
9.8.6	Current sense leakage / offset current	$I_{IS(en)}$				µA	I_L = 0 A DCR.MUX ≠ 111
	channel 0, 1		–	–	76		
	channel 2, 3		–	–	76		
9.8.7	Current sense leakage, while diagnosis disabled	$I_{IS(dis)}$	–	–	1	µA	DCR.MUX = 110
9.8.8	Current sense settling time after channel activation	$t_{sIS(ON)}$				µs	V_{BB} = 13.5 V R_{IS} = 2.7 kΩ
	channel 0, 1		–	–	150		R_L = 2.2 Ω
	channel 2, 3						HWCR.LEDn = 0
			–	–	150		R_L = 6.8 Ω
							HWCR.LEDn = 1
			–	–	100		R_L = 33 Ω
9.8.9	Current sense desettling time after channel deactivation	$t_{dIS(OFF)}$				µs	1) V_{BB} = 13.5 V R_{IS} = 2.7 kΩ
			–	–	25		HWCR.LEDn = 0
			–	–	25		HWCR.LEDn = 1
9.8.10	Current sense settling time after change of load current	$t_{sIS(LC)}$				µs	1) V_{BB} = 13.5 V R_{IS} = 2.7 kΩ
	channel 0, 1		–	–	30		I_L = 7.5 A to 4.0 A
	channel 2, 3						HWCR.LEDn = 0
			–	–	30		I_L = 2.6 A to 1.3 A
							HWCR.LEDn = 1
			–	–	30		I_L = 0.6 A to 0.3 A

Electrical Characteristics Diagnosis (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
9.8.11	Current sense settling time after current sense activation	$t_{sIS(EN)}$	–	–	25	µs	R_{IS} = 2.7 kΩ DCR.MUX: 110 -> 000
9.8.12	Current sense settling time after multiplexer channel change	$t_{sIS(MUX)}$	–	–	30	µs	R_{IS} = 2.7 kΩ R_{L0} = 2.2 Ω R_{L2} = 33 Ω DCR.MUX: 010 -> 000
9.8.13	Current sense deactivation time	$t_{dIS(MUX)}$	–	–	25	µs	1) R_{IS} = 2.7 kΩ DCR.MUX: 000 -> 110
Switch Bypass Monitor							
9.8.14	Switch bypass monitor threshold	$V_{DS(SB)}$	1.5	–	4	V	–
Open load in off current source							
9.8.15	Current source in OFF-state	$I_{L(OL)}$	100 3.0	– –	450 7.5	µA mA	IECR.CSL = 0 IECR.CSL = 1
Current Sense Synchronization Signal							
9.8.16	L level signal voltage	$V_{ISSY(L)}$	0	–	0.4	V	I_{ISSY} = -0.5 mA
9.8.17	H level signal voltage	$V_{ISSY(H)}$	V_{DD} - 0.4 V	–	V_{DD}	V	1) I_{ISSY} = 0.5 mA V_{DD} = 4.3 V
9.8.18	Signal enable time	$t_{ISSY(en)}$	–	–	4	µs	1) C_L = 20 pF
9.8.19	Signal disable time	$t_{ISSY(dis)}$	–	–	4	µs	1) C_L = 20 pF

1) Not subject to production test, specified by design.

9.9 Command Description

DCR
Diagnosis Control Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
read	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**AMUX**	**SBM**	**MUX**		
write	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**AMUX**	**CSOL**	**MUX**		

Output state OUT.OUTn	Field	Bits	Type	Description
0 (OFF-state)	MUX	2:0	r/w	**Set Current Sense Multiplexer Configuration** 000 IS pin is high impedance 001 IS pin is high impedance 010 IS pin is high impedance 011 IS pin is high impedance 100 IECR.PRO+ = 0: Diagnosis enable of external driver 0 activated (EDD0 = 1) 101 IECR.PRO+ = 0: Diagnosis enable of external driver 1 activated (EDD1 = 1) 100 IECR.PRO+ = 1: EDD0 = 1, EDD1 = 0 101 IECR.PRO+ = 1: EDD0 = 1, EDD1 = 1 110 IS pin is high impedance **111** Stand-by mode (IS pin is high impedance)
	SBM	3	r	**Switch Bypass Monitor** [1] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$
1 (ON-state)	MUX	2:0	r/w	**Set Current Sense Multiplexer Configuration** 000 Current sense of channel 0 is routed to IS pin 001 Current sense of channel 1 is routed to IS pin 010 Current sense of channel 2 is routed to IS pin 011 Current sense of channel 3 is routed to IS pin 100 IECR.PRO+ = 0: Diagnosis enable of external driver 0 activated (EDD0 = 1) 101 IECR.PRO+ = 0: Diagnosis enable of external driver 1 activated (EDD1 = 1) 100 IECR.PRO+ = 1: EDD0 = 1, EDD1 = 0 101 IECR.PRO+ = 1: EDD0 = 1, EDD1 = 1 110 IS pin is high impedance **111** Stand-by mode (IS pin is high impedance))
	SBM	3	r	**Switch Bypass Monitor** [1] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$

1) Invalid in stand-by mode

Field	Bits	Type	Description
CSOL	3	w	**Current Source Switch for Open Load Detection** **0** OFF 1 ON
AMUX	4	rw	**Automatic Current Sense Multiplexer Switching during Automatic PWM Generation** **0** OFF 1 ON

CHCRn
Channel Configuration Register

W/$\overline{R}$	RB			ADDR		9	8	7	6	5	4	3	2	1	0
r/w	**1**	**1**	**1**	**x**	**x**	**0**	**0**	**0**	**PHSn**			**SYDELn**		**FREQn**	

Field	Bits	Type	Description
SYDELn n = 0 to 5	3:2	rw	**Delay of Current Sense Synchronization Signal for Channel n** **00** No synchronization signal delay 01 Synchronization signal delay 1: 8 / (f_{PCLK} (or f_{INT})) 10 Synchronization signal delay 2: 16 / (f_{PCLK} (or f_{INT})) 11 Synchronization signal delay 3: 24 / (f_{PCLK} (or f_{INT}))

Standard Diagnosis

CS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	**0**	**LHI**	**SBM**	**x**	**CLE**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**ERR3**	**ERR2**	**ERR1**	**ERR0**

Field	Bits	Type	Description
ERRn n = 3 to 0	n	r	**Error flag Channel n** 0 normal operation 1 failure mode occurred
SBM	13	r	**Switch Bypass Monitor** [1] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$

1) Invalid in stand-by mode

IECR

Input, External Drive and Current Source Configuration Register

W/$\overline{R}$	RB	ADDR				9	8	7	6	5	4	3	2	1	0
r/w	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**COL**	**INCG**	**CSL**	**PRO+**

Field	Bits	Type	Description
PRO+	0	rw	**Configuration of EDD0 and EDD1 to be Compliant to PROFET+** **0** Normal mode 1 EDD0=DEN, EDD1=DSEL
CSL	1	rw	**Level for Current Source for Open Load Detection** **0** Low level 1 High level

10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred, while the minimum of 16 bit is also taken into consideration. Therefore the interface provides daisy chain capability even with 8 bit SPI devices.

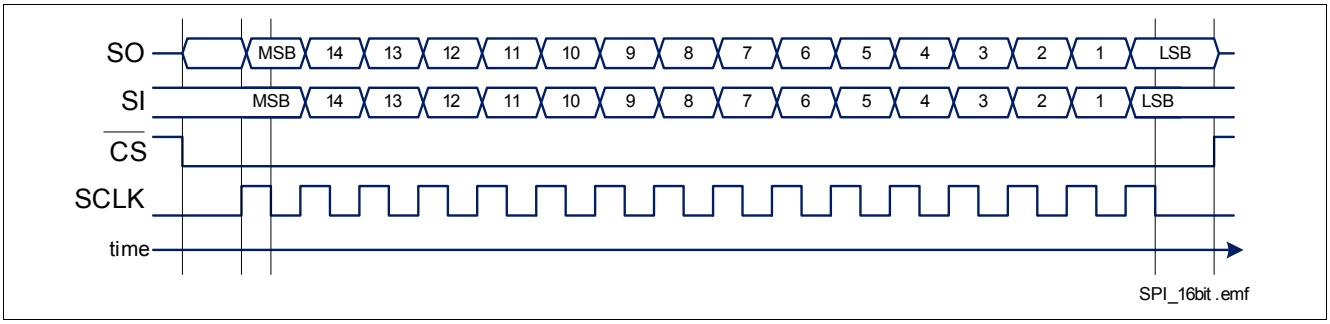


Figure 25 Serial Peripheral Interface

10.1 SPI Signal Description

$\overline{CS}$ - Chip Select:

The system micro controller selects the SPOC - BTS6480SF by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition:

- The requested information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. This information stays available to the first rising edge of SCLK.

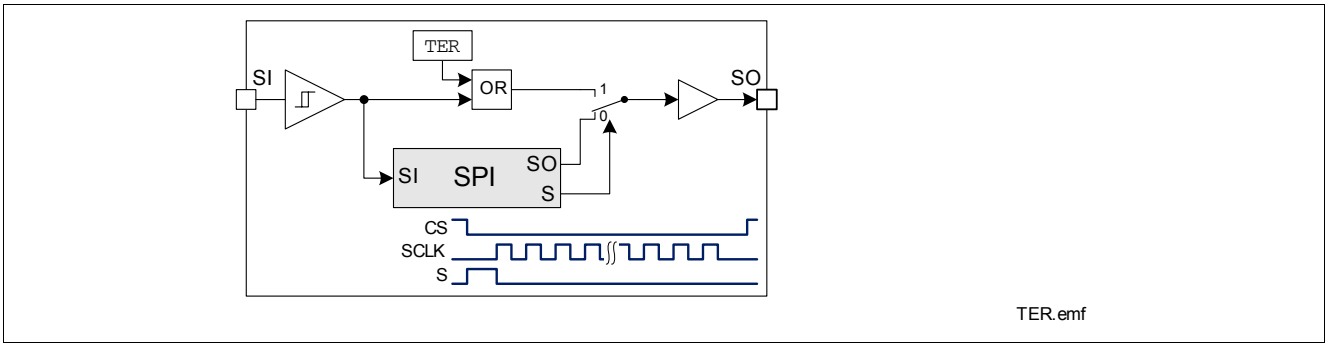


Figure 26 Combinatorial Logic for TER Flag

$\overline{CS}$ Low to High transition:

- Command decoding is only done, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (TER) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

SCLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input:

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to **Section 10.5** for further information.

SO Serial Output:

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 10.5** for further information.

10.2 Daisy Chain Capability

The SPI of SPOC - BTS6480SF provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 27**), in order to build a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

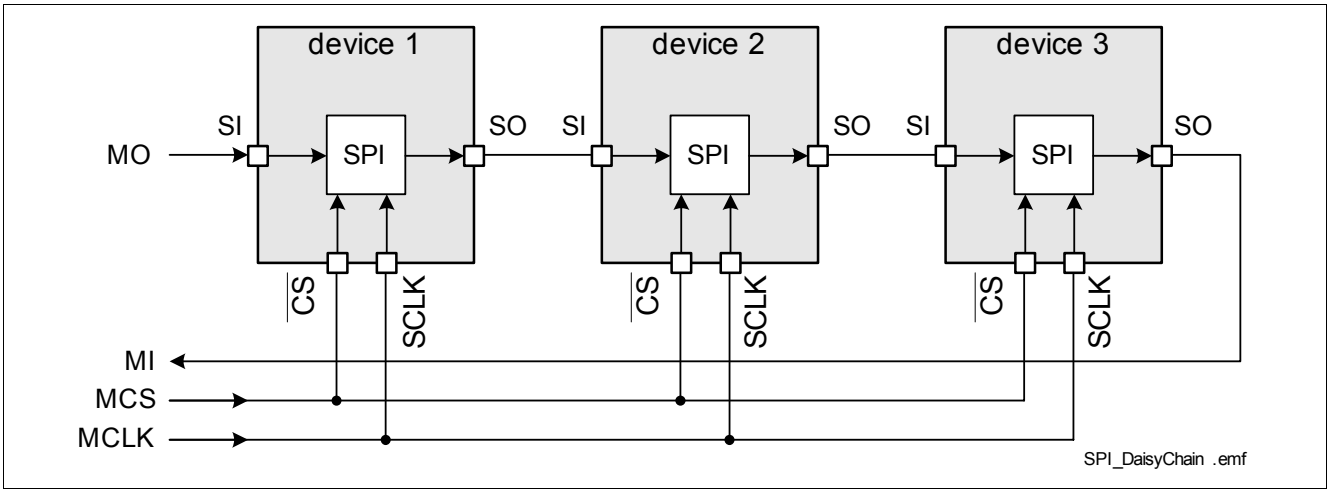


Figure 27 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After eight SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must turn high to make the device accept the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, three times 16 (or e.g. 16 + 8 +16) bits have to be shifted through the devices. After that, the $\overline{MCS}$ line must turn high (see **Figure 28**).

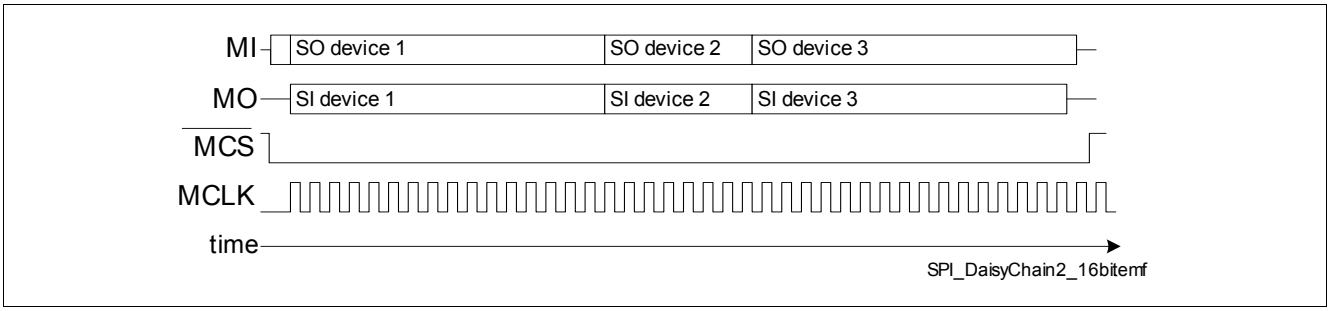


Figure 28 Data Transfer in Daisy Chain Configuration

10.3 Timing Diagrams

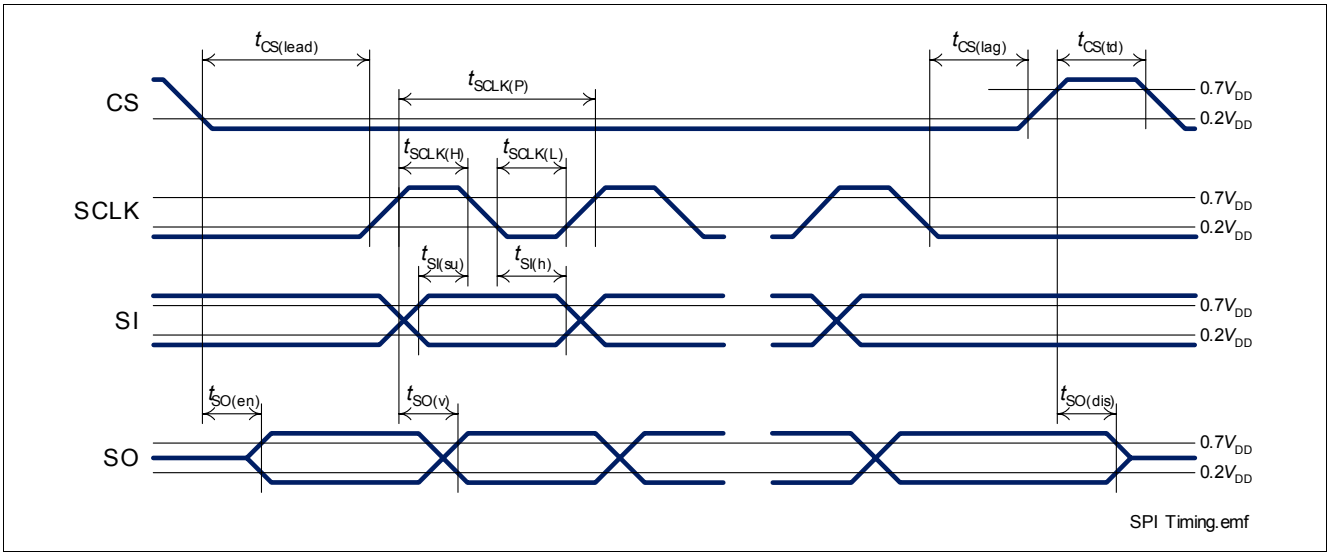


Figure 29 Timing Diagram SPI Access

10.4 Electrical Characteristics

Electrical Characteristics Serial Peripheral Interface (SPI)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
10.4.1	L level of pin $\overline{CS}$ SCLK SI	 $V_{CS(L)}$ $V_{SCLK(L)}$ $V_{SI(L)}$	0	–	0.2* V_{DD}	V	V_{DD} = 4.3 V
10.4.2	H level of pin $\overline{CS}$ SCLK SI	 $V_{CS(H)}$ $V_{SCLK(H)}$ $V_{SI(H)}$	0.4* V_{DD}	–	V_{DD}	V	V_{DD} = 4.3 V
10.4.3	Pull-up resistor at $\overline{CS}$ pin	R_{CS}	50	120	180	kΩ	I_{CS} = 100 µA
10.4.4	Pull-down resistor at pin SCLK SI	 R_{SCLK} R_{SI}	50	120	180	kΩ	– I_{SCLK} = 100 µA I_{SI} = 100 µA
Output Characteristics (SO)							
10.4.5	L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = -0.5 mA
10.4.6	H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4 V	–	V_{DD}	V	I_{SO} = 0.5 mA V_{DD} = 4.3 V
10.4.7	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} = V_{DD}
Timings							
10.4.8	Serial clock frequency	f_{SCLK}	0 0	– –	5 3	MHz	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.9	Serial clock period	$t_{SCLK(P)}$	200 333	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.10	Serial clock high time	$t_{SCLK(H)}$	100 166	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.11	Serial clock low time	$t_{SCLK(L)}$	100 166	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.12	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	200 333	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.13	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	200 333	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.14	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	200 333	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.15	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20 33	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V
10.4.16	Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20 33	– –	– –	ns	1) V_{DD} = 4.3 V 2) V_{DD} = 3.0 V

Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)

Unless otherwise specified: V_{BB} = 8 V to 17 V, V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
10.4.17	Output enable time (falling $\overline{CS}$ to SO valid)	$t_{SO(en)}$				ns	2) C_L = 20 pF
			–	–	200		V_{DD} = 4.3 V
			–	–	333		V_{DD} = 3.0 V
10.4.18	Output disable time (rising $\overline{CS}$ to SO tri-state)	$t_{SO(dis)}$				ns	2) C_L = 20 pF
			–	–	200		V_{DD} = 4.3 V
			–	–	333		V_{DD} = 3.0 V
10.4.19	Output data valid time with capacitive load	$t_{SO(v)}$				ns	2) C_L = 20 pF
			–	–	100		V_{DD} = 4.3 V
			–	–	166		V_{DD} = 3.0 V

1) Not subject to production test, specified by design. SPI functional test is performed at f_{SCLK} = 5 MHz.

2) Not subject to production test, specified by design.

10.5 SPI Protocol 16Bit

	CS[1]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Write OUT Register															
SI		1	0	0	0	0	0	0	0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
		Read OUT Register															
SI		0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	0
		Write Configuration and Control Registers															
SI		1	x	ADDR				DATA									
		Read Configuration and Control Registers															
SI		0	x	ADDR				x	x	x	x	x	x	x	x	x	0
		Read Standard Diagnosis															
SI		0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1
		Standard Diagnosis															
SO	TER	0	LHI	SBM	x	CLE	x	x	x	x	x	x	x	ERR3	ERR2	ERR1	ERR0
		Second Frame of Read Command															
SO	TER	1	0	0	0	0	0	x	x	x	x	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
SO	TER	1	x	ADDR				DATA									

1) The SO pin shows this information between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame the output at SPI signal SO will contain the requested information. A new command can be executed in the second frame. The standard diagnosis can be accessed either by sending the standard diagnosis read command or it is transmitted after each write command.

Field	Bits	Type	Description
W/$\overline{R}$	15	w	0 Read 1 Write
RB	14	rw	**Register Bank** **0** Read / write to register bank 0 1 Read / write to register bank 1
TER	CS	r	**Transmission Error** **0** Previous transmission was successful (modulo 16 clocks received) 1 Previous transmission failed or first transmission after reset
OUTn n = 5 to 0	n	w	**Output Control Register of Channel n** **0** OFF 1 ON
ADDR	13:10	rw	**Address** Pointer to register for read and write command
DATA	9:0	rw	**Data** Data written to or read from register selected by address ADDR
ERRn n = 3 to 0	n	r	**Diagnosis of Channel n** [1] **0** No failure 1 Over temperature, over load or short circuit

Field	Bits	Type	Description
CLE	11	r	**External Clock Status** [2] **0** $f_{PCLK} > f_{PCLK(TH)}$ 1 $f_{PCLK} < f_{PCLK(TH)}$
SBM	13	r	**Switch Bypass Monitor** [2] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$
LHI	14	r	**Limp Home Enable** [3] 0 H-input signal at pin LHI 1 L-input signal at pin LHI

1) No ERR-flags available for external drivers
2) Invalid in stand-by mode
3) Not latching information, read of LHI-status during falling CS

10.6 Register Overview

Register Bank 0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**W/$\overline{R}$**	**RB**	**ADDR**				**DATA**									
OUT	W/R	0	0	0	0	0	0	0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
PCR	W/R	0	0	1	1	1	0	0	0	0	0	0	DCS	DPSH		PST
DCCR0	W/R	0	1	0	0	0	0	DC0								
DCCR1	W/R	0	1	0	0	1	0	DC1								
DCCR2	W/R	0	1	0	1	0	0	DC2								
DCCR3	W/R	0	1	0	1	1	0	DC3								
DCCR4	W/R	0	1	1	0	0	0	DC4								
DCCR5	W/R	0	1	1	0	1	0	DC5								

Note: A readout of an unused register will return the standard diagnosis.

Field	Bits	Type	Description
RB	6	-	**Read Bit** **0** Read / write to register bank 0 1 Read / write to register bank 1
ADDR	5:4	w	**Address** Pointer to register for read and write command
DATA	3:0	rw	**Data** Data written to or read from register selected by address ADDR
OUTn n = 5 to 0	n	rw	**Set Output Mode for Channel n** **0** Channel n is switched off 1 Channel n is switched on
PST	0	rw	**Automatic PWM Generation** **0** No automatic PWM generation 1 Automatic PWM generation
DPSH	6:4	rw	**Device Phase Shift** **00** No phase shift 01 Phase shift 1: 8 / (f_{PCLK} (or f_{INT})) 10 Phase shift 2: 16 / (f_{PCLK} (or f_{INT})) 11 Phase shift 3: 24 / (f_{PCLK} (or f_{INT}))
DCS	0	rw	**Single Duty Cycle for all Channels** **0** Duty cycle setting of channel 0 used for all channels 1 Individual duty cycle setting used for each channel
DCn n = 0 to 5	8:0	rw	**Duty Cycle for Channel n during Automatic PWM Generation** **000000000** DC value: 0 (channel off) 000000001 DC value: (1 / 256) * 100 000000010 DC value: (2 / 256) * 100 ... 011111111 DC value: (255 / 256) * 100 1xxxxxxxx DC value: 1 (channel 100% on)

Register Bank 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**W/$\overline{R}$**	**RB**	**ADDR**				**DATA**									
IECR	W/R	1	0	0	0	1	0	0	0	0	0	0	COL	INCG	CSL	PRO+
HWCR	R	1	0	0	1	0	0	CLKTRIM			CLK	0	LED3	LED2	STB	CL
	W	1	0	0	1	0	0	CLKTRIM			CLK	0	LED3	LED2	RST	CL
DCR	R	1	0	0	1	1	0	0	0	0	0	AMUX	SBM	MUX		
	W	1	0	0	1	1	0	0	0	0	0	AMUX	CSOL	MUX		
CHCR0	W/R	1	1	0	0	0	0	0	0	PSH0			SYDEL0		FREQ0	
CHCR1	W/R	1	1	0	0	1	0	0	0	PSH1			SYDEL1		FREQ1	
CHCR2	W/R	1	1	0	1	0	0	0	0	PSH2			SYDEL2		FREQ2	
CHCR3	W/R	1	1	0	1	1	0	0	0	PSH3			SYDEL3		FREQ3	
CHCR4	W/R	1	1	1	0	0	0	0	0	PSH4			SYDEL4		FREQ4	
CHCR5	W/R	1	1	1	0	1	0	0	0	PSH5			SYDEL5		FREQ5	

Note: A readout of an unused register will return the standard diagnosis.

Field	Bits	Type	Description
PRO+	0	rw	**Configuration of EDD0 and EDD1 to be Compliant to PROFET+ Concept** **0** Normal mode 1 EDD0=DEN, EDD1=DSEL
CSL	1	rw	**Level for Current Source for Open Load Detection** **0** Low level 1 High level
INCG	2	rw	**Input Drive Configuration** **0** Direct drive mode 1 Assigned drive mode
COL	3	rw	**Input Combinatorial Logic Configuration** **0** Input signal OR-combined with according OUT register bit 1 Input signal AND-combined with according OUT register bit
CL	0	rw	**Clear Latch** **0** Thermal and over current latches are untouched 1 Command: Clear all thermal and over current latches
RST	1	w	**Reset Command** **0** Normal operation 1 Execute reset command
STB	1	r	**Standby Mode** 0 Device is awake **1** Device is in Standby mode
LEDn n = 3 to 2	n	rw	**Set LED Mode for Channel n** **0** Channel n is in bulb mode 1 Channel n is in LED mode

Field	Bits	Type	Description
CLK	5	rw	**Clock Mode** [1] 0 External Clock input PCLK is used for PWM Mode **1** Internal Clock is used for PWM Mode
CLKTRIM	8:6	rw	**Internal Clock Trim** 000 f_{INT} - 4 k_{TRIM} ... 011 f_{INT} - 1 k_{TRIM} **100** f_{INT} without trimming 101 f_{INT} + 1 k_{TRIM} ... 111 f_{INT} + 3 k_{TRIM}
MUX	2:0	rw	**Set Current Sense Multiplexer Configuration in OFF-state** 000 IS pin is high impedance 001 IS pin is high impedance 010 IS pin is high impedance 011 IS pin is high impedance 100 `IECR.PRO+ = 0:` Diagnosis enable of external driver 0 activated (EDD0 = 1) 101 `IECR.PRO+ = 0:` Diagnosis enable of external driver 1 activated (EDD1 = 1) 100 `IECR.PRO+ = 1:` EDD0 = 1, EDD1 = 0 101 `IECR.PRO+ = 1:` EDD0 = 1, EDD1 = 1 110 IS pin is high impedance **111** Stand-by mode (IS pin is high impedance) **Set Multiplexer Configuration in ON-state** 000 Current sense of channel 0 is routed to IS pin 001 Current sense of channel 1 is routed to IS pin 010 Current sense of channel 2 is routed to IS pin 011 Current sense of channel 3 is routed to IS pin 100 `IECR.PRO+ = 0:` Diagnosis enable of external driver 0 activated (EDD0 = 1) 101 `IECR.PRO+ = 0:` Diagnosis enable of external driver 1 activated (EDD1 = 1) 100 `IECR.PRO+ = 1:` EDD0 = 1, EDD1 = 0 101 `IECR.PRO+ = 1:` EDD0 = 1, EDD1 = 1 110 IS pin is high impedance **111** Stand-by mode (IS pin is high impedance))
SBM	3	r	**Switch Bypass Monitor** [2] 0 $V_{DS} < V_{DS(SB)}$ 1 $V_{DS} > V_{DS(SB)}$
CSOL	3	w	**Current Source Switch for Open Load Detection** **0** OFF 1 ON
AMUX	5:4	w	**Automatic Current Sense Multiplexer Switching (single loop)** **0** Automatic current sense multiplexer switching not activated 1 Automatic current sense multiplexer switching activated and proceeding

Field	Bits	Type	Description
FREQn n = 0 to 5	1:0	rw	**PWM Frequency Prescaler Setting for Channel n** **00** Normal mode without automatic PWM generation 01 Prescaler 1: f_{PCLK} (or f_{INT}) / 256 10 Prescaler 2: f_{PCLK} (or f_{INT}) / 512 11 Prescaler 4: f_{PCLK} (or f_{INT}) / 1024
SYDELn n = 0 to 5	3:2	rw	**Delay of Current Sense Synchronization Signal for Channel n** **00** No synchronization signal delay 01 Synchronization signal delay 1: 8 / (f_{PCLK} (or f_{INT})) 10 Synchronization signal delay 2: 16 / (f_{PCLK} (or f_{INT})) 11 Synchronization signal delay 3: 24 / (f_{PCLK} (or f_{INT}))
PSHn n = 0 to 5	6:4	rw	**Channel Phase Shift for Channel n** **000** No phase shift 001 Phase shift 1: 32/ (f_{PCLK} (or f_{INT})) 010 Phase shift 2: 64 / (f_{PCLK} (or f_{INT})) ... 110 Phase shift 6: 192 / (f_{PCLK} (or f_{INT})) 111 Phase shift 7: 224 / (f_{PCLK} (or f_{INT}))

1) For avoiding skews it is recommended to change from external to internal clock source or vice versa only during deactivated PWM generator (`PCR.PST = 0b`).

2) Invalid in stand-by mode

11 Application Description

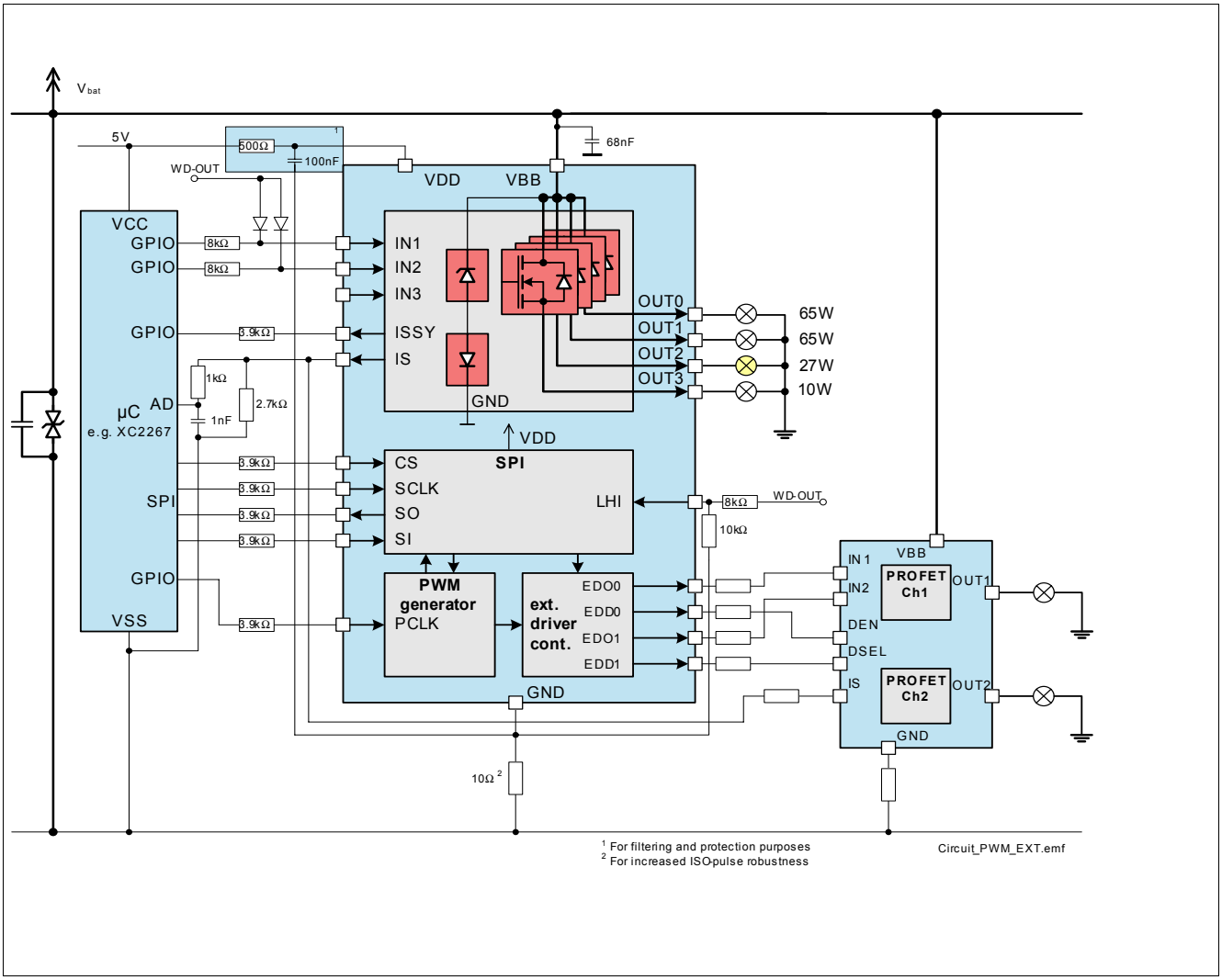


Figure 30 Application Circuit Example

12 Package Outlines SPOC - BTS6480SF

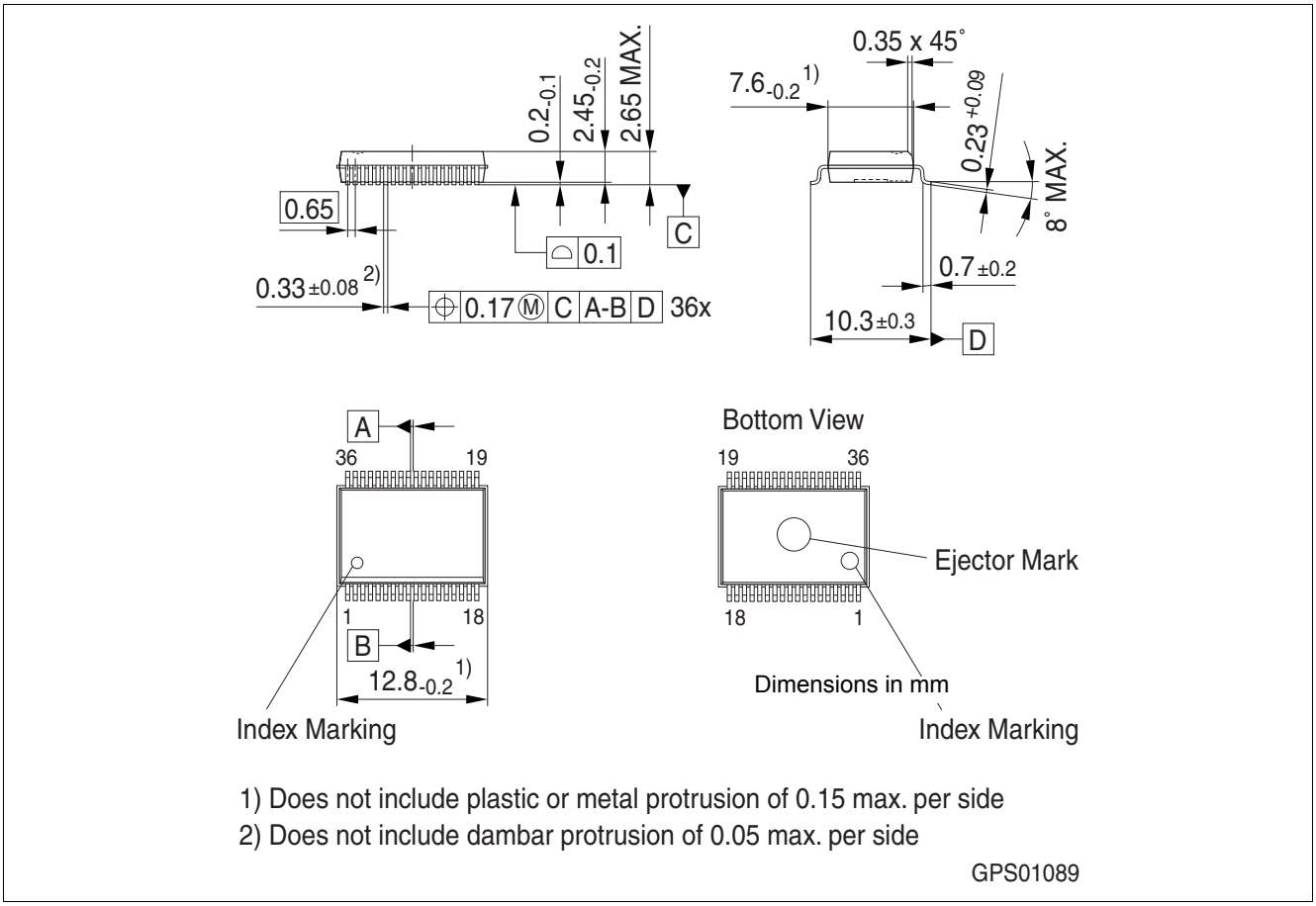


Figure 31 PG-DSO-36-43 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.

13 Revision History

Revision	Date	Changes
1.0	2010-04-12	Initial Data Sheet

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