

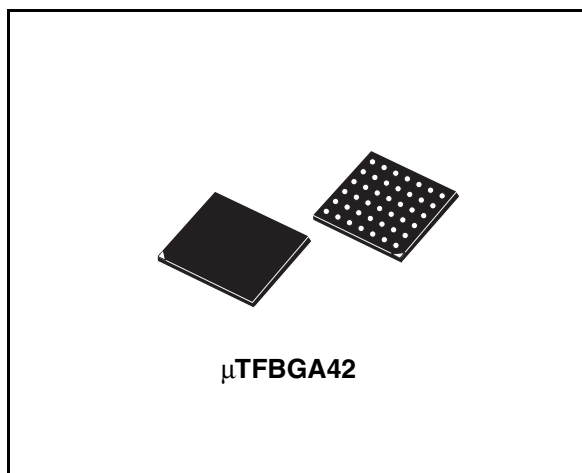


ST16C32245

14-bit dual supply bus transceiver level translator A side series resistor, 2-bit I²C lines

Features

- High speed: $t_{PD} = 4.4 \text{ ns (max)}$ at $T_A = 85 \text{ }^{\circ}\text{C}$
 $V_{CCA} = 3.0 \text{ V}$ and $V_{CCB} = 2.3 \text{ V}$
- Low power dissipation:
 $I_{CCA} = I_{CCB} = 20 \text{ } \mu\text{A(max)}$ at $T_A = 85 \text{ }^{\circ}\text{C}$
- Symmetrical output impedance:
 $|I_{OHA}| = |I_{OLA}| = 8 \text{ mA min}$
($V_{CCA} = 3.0 \text{ V}$; $V_{CCB} = 1.65 \text{ V}$ or 2.3 V)
 $|I_{OHB}| = |I_{OLB}| = 6 \text{ mA min}$
($V_{CCB} = 1.65 \text{ V}$ $V_{CCA} = 3.0 \text{ V}$;)
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Power down protection on inputs and outputs
- $26 \text{ } \Omega$ series resistor on A side outputs
- Operating voltage range:
 $V_{CCA} \text{ (opr)} = 2.3 \text{ V to } 3.6 \text{ V}$
 $V_{CCB} \text{ (opr)} = 1.65 \text{ V to } 2.7 \text{ V}$
- Fast I²C lines 1.8 V/2.8 V level translator:
400 KHz guaranteed data rate at $C_L = 15 \text{ pF}$
- Bus hold provided on data input both side
- Latch-up performance exceeds 500mA
(JESD 17)
- ESD performance:
HBM > 2000 V (MIL STD 883 method 3015);
MM > 200 V



Description

The ST16C32245 is a dual supply low voltage CMOS 14-bit bus transceiver fabricated with sub-micron silicon gate and five-layer metal wiring C²MOS technology. Designed for use as an interface between a 3.3 V bus and a 2.5 V or 1.8 V bus in a mixed 3.3 V/1.8 V, 3.3 V/2.5 V and 2.5 V/1.8 V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation and it includes 2-bit I²C level translation. This IC is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by nDIR inputs. The enable inputs n $\overline{\text{G}}$ can be used to disable the device so that the buses are effectively isolated. The A-port interfaces with the 3 V bus, the B-port with the 2.5 V and 1.8 V bus. All inputs are equipped with protection circuits against static discharge, giving them 2 KV ESD immunity and transient excess voltage. All floating bus terminals during high Z state do not need external pull-up or pull-down resistor.

Table 1. Device summary

Order code	Package	Packaging
ST16C32245TBR	μ TFBGA42	Tape and reel

Contents

1	General description	3
2	Pin settings	5
2.1	Pin connection	5
2.2	I2C bus function	6
3	Maximum rating	7
3.1	Recommended operating conditions	8
4	Electrical characteristics	9
5	Test circuit	16
6	Waveforms	17
7	Package mechanical data	19
8	Revision history	22

1 General description

Figure 1. Logic diagram

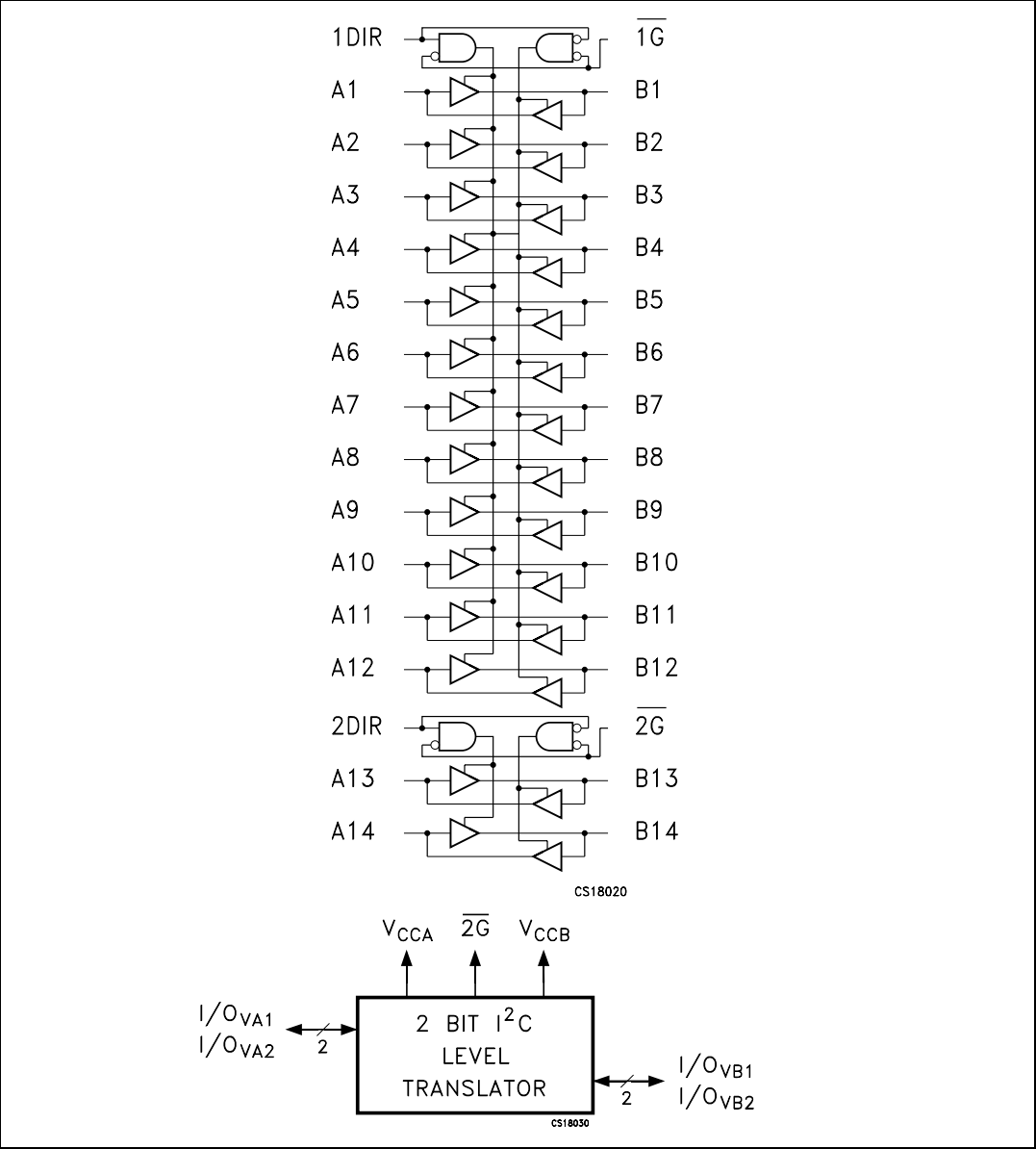
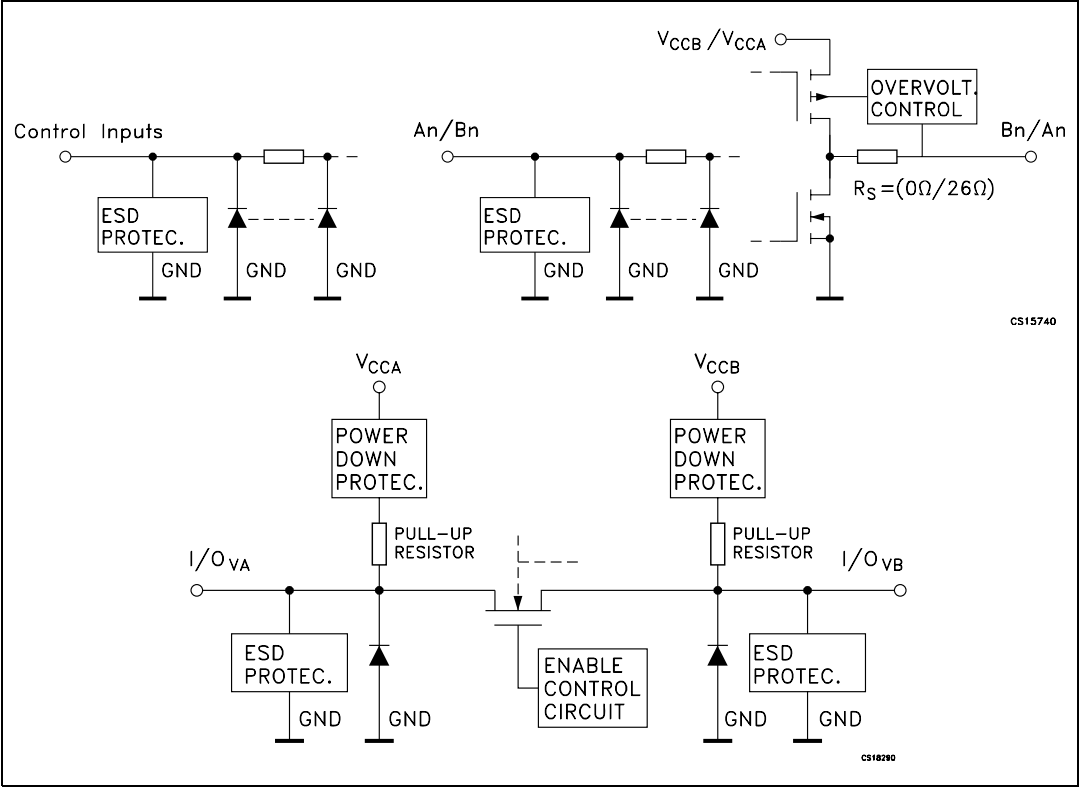


Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view)

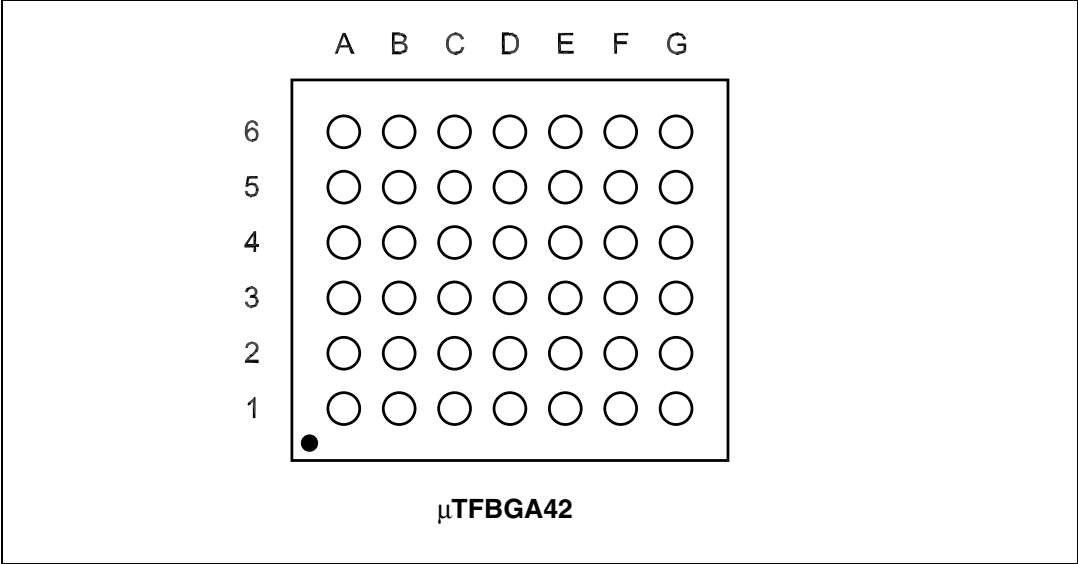


Table 2. Pin description

Pin number	Symbol	Name and function
B3	1DIR	Directional controls
F3	2DIR	Directional controls
A4, A5, A6, B5, B6, C5, C6, D5	A1, A2, A3, A4, A5, A6, A7, A8	Data Inputs/outputs
D6, E5, E6, F5, F6, G6	A9, A10, A11, A12, A13, A14	Data Inputs/outputs
A3, A2, A1, B2, B1, C2, C1, D2	B1, B2, B3, B4, B5, B6, B7, B8	Data Inputs/outputs
D1, E2, E1, F2, F1, G1	B9, B10, B11, B12, B13, B14	Data Inputs/outputs
F4	$\overline{2G}$	Output enable inputs
B4	$\overline{1G}$	Output enable inputs
C3, C4, E3, E4	GND	Ground (0V)
-	NC	No connected
D4	V_{CCA}	Positive supply voltage
D3	V_{CCB}	Positive supply voltage
G5, G4	$I/O_{VA1}, I/O_{VA2}$	I ² C Line (V_{CCA} referred)
G2, G3	$I/O_{VB1}, I/O_{VB2}$	I ² C Line (V_{CCB} referred)

Table 3. Truth table

Inputs		Function		Output
$\overline{G}$	DIR	A bus	B bus	
L	L	Output	Input	A = B
L	H	Input	Output	B = A
H	X	Z	Z	Z

Note: X = don't care; Z = high Impedance

2.2 I²C bus function

Table 4. I²C Bus function table

$\overline{2G}$	$\overline{1G}$, 1DIR, 2DIR	I/O input		Function
		I/O _{VA}	I/O _{VB}	
H	X	Z	Z	I ² C disabled
L	X	L	L	I ² C comm.
L	X	V _{CCA}	V _{CCB}	I ² C comm.
L	X	Open	V _{CCB}	I ² C comm.
L	X	V _{CCA}	Open	I ² C comm.

Note: Open: If I/O_{VA} is not driven then the I/O_{VB} goes in high level V_{CCB} by embedded 10 kΩ pull-up resistor. If I/O_{VB} is not driven then the I/O_{VA} will go in high level V_{CCB} by embedded 10 kΩ pull-up resistor.

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	-0.5 to +4.6	V
V_{CCB}	Supply voltage	-0.5 to +4.6	V
V_I	DC input voltage	-0.5 to +4.6	V
$V_{I/OA}$	DC I/O voltage (Output disabled)	-0.5 to +4.6	V
$V_{I/OB}$	DC I/O voltage (Output disabled)	-0.5 to +4.6	V
$V_{I/OA}$	DC I/O voltage	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OB}$	DC I/O voltage	-0.5 to $V_{CCB} + 0.5$	V
$V_{I/OVA}$	Level input voltage (I/O_{VA})	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OVB}$	Level input voltage (I/O_{VB})	-0.5 to $V_{CCB} + 0.5$	V
I_{IK}	DC input diode current	-20	mA
I_{OK}	DC output diode current	-50	mA
I_{OA}	DC output current	± 50	mA
I_{OB}	DC output current	± 50	mA
I_{CCA}	DC V_{CC} or ground current	± 100	mA
I_{CCB}	DC V_{CC} or ground current	± 100	mA
P_d	Power dissipation	400	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	260	°C

3.1 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	2.3 to 3.6	V
V_{CCB}	Supply voltage	1.65 to 2.7	V
V_I	Input voltage (Dir, $\overline{G}$)	0 to V_{CCB}	V
$V_{I/OA}$	I/O voltage	0 to V_{CCA}	V
$V_{I/OB}$	I/O voltage	0 to V_{CCB}	V
$V_{I/OVA}$	Level input voltage (I/O_{VA})	0 to V_{CCA}	V
$V_{I/OVB}$	Level input voltage (I/O_{VB})	0 to V_{CCB}	V
T_{op}	Operating temperature	-40 to +85	°C
dt/dv	Input rise and fall time	0 to 10	ns/V

4 Electrical characteristics

Table 7. DC specification for V_{CCA}

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
V _{IHA}	High level input voltage (A _n) ⁽¹⁾	1.8	2.5		1.6		1.6		V
		1.8	3.3		2.0		2.0		
		2.5	3.3		2.0		2.0		
V _{ILA}	Low level input voltage (A _n) ⁽¹⁾	1.8	2.5			0.7		0.7	V
		1.8	3.3			0.8		0.8	
		2.5	3.3			0.8		0.8	
V _{OHA}	High level output voltage	2.3	3.0	I _O = -100 μA	2.8		2.8		V
		2.3	3.0	I _O = -8 mA	2.4		2.4		
		1.65	3.0	I _O = -8 mA	2.4		2.4		
		1.65	2.3	I _O = -6 mA	1.8		1.8		
V _{OLA}	Low level output voltage	2.3	3.0	I _O = 100 μA		0.2		0.2	V
		2.3	3.0	I _O = 8 mA		0.55		0.55	
		1.65	3.0	I _O = 8 mA		0.55		0.55	
		1.65	2.3	I _O = 6 mA		0.40		0.40	
I _{IA}	Input leakage current	2.7	3.6	V _I = V _{CC} or GND		±0.5		±5	μA
I _{IA(HOLD)}	Input hold current	1.65	2.3	V _I = 0.7 V	45		45		μA
		1.65	2.3	V _I = 1.6 V	-45		-45		
		1.65	3.0	V _I = 0.8 V	75		75		
		1.65	3.0	V _I = 2.0 V	-75		-75		
		2.3	3.0	V _I = 0.8 V	75		75		
		2.3	3.0	V _I = 2.0 V	-75		-75		
		2.7	3.6	V _I = 0 to 3.6 V				±500	
I _{OZA}	High impedance output leakage current	2.7	3.6	V _{IA} = GND or 3.6 V V _{IB} = V _{IHB} or V _{ILB} G̅ = V _{CCB}		±1.0		±10	μA
I _{OFF}	Power off leakage current	0	0	V _{IA} = GND to 3.6 V V _{IB} = GND to 3.6 V G̅, Dir = GND to 3.6 V		±1.0		±10	μA

Table 7. DC specification for V_{CCA} (continued)

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
I _{OFFI2C}	Power Off I ² C line leakage current	1.65 to 2.7	0	I/O _{VA1,2} = GND or V _{CCA} ; I/O _{VB1,2} = GND or V _{CCB} ; $\overline{2G}$ = V _{CCB}		1.0		5	μA
I _{CCtA}	Quiescent supply current	1.95	3.6	V _{IA} = V _{CCA} or GND		2		20	μA
		1.95	2.7	V _{IB} = V _{CCB} or GND					
		2.7	3.6	I/O _{VA1,2} = V _{CCA} or Open; Dir, $\overline{G}$ = GND or V _{CCB}					
ΔI _{CCtA}	Maximum quiescent supply current / Input (An)	2.7	3.6	V _{IA} = V _{CCA} - 0.6V V _{IB} = V _{CCB} or GND				0.75	mA
		1.95	3.6						
		1.95	2.7						

1. V_{CC} range = 3.3 ± 0.3 ; $2.5 \pm 0.2\text{V}$ and $2.8 \pm 0.1\text{V}$; $1.8 \pm 0.15\text{V}$

Table 8. DC specification for V_{CCB}

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
V _{IHB}	High level input voltage (Bn, Dir, $\overline{G}$) ⁽¹⁾	1.8	2.5		0.65V _{CCB}		0.65V _{CCB}		V
		1.8	3.3		0.65V _{CCB}		0.65V _{CCB}		
		2.5	3.3		1.6		1.6		
V _{ILB}	Low level input voltage (Bn, Dir, $\overline{G}$) ⁽¹⁾	1.8	2.5			0.35V _{CCB}		0.35V _{CCB}	V
		1.8	3.3			0.35V _{CCB}		0.35V _{CCB}	
		2.5	3.3			0.7		0.7	
V _{OHB}	High level output voltage	2.3	3.0	I _O =-100μA	2.1		2.1		V
		2.3	3.0	I _O =-18mA	1.7		1.7		
		1.65	3.0	I _O =-6mA	1.25		1.25		
		1.65	2.3	I _O =-6mA	1.25		1.25		
V _{OLB}	Low level output voltage	2.3	3.0	I _O =100μA		0.2		0.2	V
		2.3	3.0	I _O =18mA		0.60		0.60	
		1.65	3.0	I _O =6mA		0.30		0.30	
		1.65	2.3	I _O =6mA		0.30		0.30	
I _{IB}	Input leakage current	2.7	3.6	V _I = V _{CC} or GND		±0.5		±5	μA

Table 8. DC specification for V_{CCB} (continued)

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C		-40 to 85°C		
					Min	Max	Min	Max	
I _{IB(HOLD)}	Input hold current	1.65	2.3	V _I = 0.57 V	25		25		μA
		1.65	2.3	V _I = 1.07 V	-25		-25		
		1.65	3.0	V _I = 0.57 V	25		25		
		1.65	3.0	V _I = 1.07 V	-25		-25		
		2.3	3.0	V _I = 0.7 V	45		45		
		2.3	3.0	V _I = 1.6 V	-45		-45		
		2.7	3.6	V _I = 0 to 2.7 V				±500	
I _{OZB}	High impedance output leakage current	2.7	3.6	V _{IA} = V _{IHA} or V _{ILA} V _{IB} = GND or 2.7V $\overline{G}$ = V _{CCB}		±1.0		±10	μA
I _{CCtB}	Quiescent supply current	1.95	3.6	V _{IA} =V _{CCA} or GND		2		20	μA
		1.95	2.7	V _{IB} =V _{CCB} or GND					
		2.7	3.6	Dir or $\overline{G}$ =V _{CCB} or GND I/O _{VA1,2} =V _{CCA} or Open					
ΔI _{CCtB}	Maximum quiescent supply current / Input (Bn, DIR, $\overline{G}$)	2.7	3.6	V _{IB} =V _{CCB} - 0.6V V _{IA} =V _{CCA} or GND				0.75	mA
		1.95	3.6						
		1.95	2.7						

1. V_{CC} range = 3.3 ± 0.3 ; $2.5\pm 0.2\text{ V}$ and $2.8\pm 0.1\text{ V}$; $1.8\pm 0.15\text{ V}$

Table 9. Dynamic switching characteristics

Symbol	Parameter	Test condition			Value					Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max.	
V _{OLPA}	Dynamic low level quiet An output	1.8	2.5	C _L = 30 pF V _{IL} = 0 V V _{IH} = V _{CC}		0.25				V
		1.8	3.3			0.35				
		2.5	3.3			0.35				
V _{OLPB}	Dynamic low level quiet Bn output	1.8	2.5	C _L = 30 pF V _{IL} = 0 V V _{IH} = V _{CC}		0.25				V
		1.8	3.3			0.25				
		2.5	3.3			0.6				
V _{OLVA}	Dynamic low level quiet An output	1.8	2.5	C _L = 30 pF V _{IL} = 0 V V _{IH} = V _{CC}		-0.25				V
		1.8	3.3			-0.35				
		2.5	3.3			-0.35				
V _{OLVB}	Dynamic low level quiet Bn output	1.8	2.5	C _L = 30 pF V _{IL} = 0 V V _{IH} = V _{CC}		-0.25				V
		1.8	3.3			-0.25				
		2.5	3.3			-0.6				
V _{OHVA}	Dynamic high level quiet An output	1.8	2.5	C _L = 30 pF V _{IL} = 0 V V _{IH} = V _{CC}		2.1				V
		1.8	3.3			2.6				
		2.5	3.3			2.6				
V _{OHVB}	Dynamic high level quiet Bn output	1.8	2.5	C _L = 30 pF V _{IL} = 0 V V _{IH} = V _{CC}		1.7				V
		1.8	3.3			1.7				
		2.5	3.3			2.0				

Table 10. DC specification I²C lines

Symbol	Parameter	Test condition			Value				Unit
		V _{CCB} (V) (1)	V _{CCA} (V)		T _A = 25 °C		-40 to 85 °C		
					Min.	Max.	Min.	Max.	
V _{IH2}	High level input voltage (I/O _{VB1} , I/O _{VB2})	1.8	2.65 to 3.6		0.7 V _{CCB}	V _{CCB}	0.7 V _{CCB}	V _{CCB}	V
		1.8	2.65 to 3.6		0.7 V _{CCB}	V _{CCB}	0.7 V _{CCB}	V _{CCB}	
	High level input voltage (I/O _{VA1} , I/O _{VA2})	1.8	2.65 to 3.6		0.7 V _{CCA}	V _{CCA}	0.7 V _{CCA}	V _{CCA}	
		1.8	2.65 to 3.6		0.7 V _{CCA}	V _{CCA}	0.7 V _{CCA}	V _{CCA}	
V _{IL2}	Low level input voltage (I/O _{VB1} , I/O _{VB2})	1.8	2.65 to 3.6		0	0.25	0	0.25	V
		1.8	2.65 to 3.6		0	0.25	0	0.25	
	Low level input voltage (I/O _{VA1} , I/O _{VA2})	1.8	2.65 to 3.6		0	0.25	0	0.25	
		1.8	2.65 to 3.6		0	0.25	0	0.25	
V _{OH2}	High level output voltage (I/O _{VB1} , I/O _{VB2})	1.65	2.3	I _{OH} = -20 μA; V _{I/OVA} =V _{CCA}	V _{CCB} -0.4		V _{CCB} -0.4		V
	High level output voltage (I/O _{VA1} , I/O _{VA2})	1.65	2.3	I _{OH} = -20 μA; V _{I/OVB} =V _{CCB}	V _{CCA} -0.4		V _{CCA} -0.4		
V _{OL2}	Low level output voltage (I/O _{VB1} , I/O _{VB2}), (I/O _{VA1} , I/O _{VA2})	1.65	2.3	I _{OL} = 1 mA; V _{I/OVB} or V _{I/OVA} =GND		0.35		0.35	V

1. V_{CC} range = 1.8±0.15 V

Table 11. AC electrical characteristics

Symbol	Parameter	Test condition			Value		Unit
		V _{CCB} (V)	V _{CCA} (V)		-40 to 85 °C		
					Min	Max	
t _{PLH} t _{PHL}	Propagation delay time An to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0	5.8	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	6.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t _{PLH} t _{PHL}	Propagation delay time Bn to An ⁽¹⁾	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0	5.5	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t _{PZL} t _{PZH}	Output enable time G̅ to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0	5.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t _{PZL} t _{PZH}	Output enable time G̅ to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0	8.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	8.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.6	
t _{PLZ} t _{PHZ}	Output disable time G̅ to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0	5.2	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.6	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.8	
t _{PLZ} t _{PHZ}	Output disable time G̅ to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω	1.0	4.6	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	4.5	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t _{OSLH} t _{OSHL}	Output to output skew time ⁽²⁾ ⁽³⁾	1.8 ± 0.15	2.5 ± 0.2	C _L = 30 pF R _L = 500 Ω		0.5	ns
		1.8 ± 0.15	3.3 ± 0.3			0.5	
		2.5 ± 0.2	3.3 ± 0.3			0.75	

1. To add 2.5 ns at t_{PLH} , t_{PHL} max propagation delay time Bn to An at $V_{CCB} = 1.8 \pm 0.15 \text{ V}$; $V_{CCA} = 2.8 \pm 0.1 \text{ V}$; $R_L = 500 \Omega$ when $C_L = 60 \text{ pF}$.
2. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$).
3. Parameter guaranteed by design.

Table 12. AC I²C electrical characteristics

Symbol	Parameter	Test condition			Value		Unit
		V _{CCB} (V) ⁽¹⁾	V _{CCA} (V) ⁽¹⁾		-40 to 85 °C		
					Min.	Max.	
t _{rl/O}	Rise time I ² C input/output voltage (20% to 80%)	1.8 ± 0.15	2.5 ± 0.2	C _L = 15 pF t _{rl/O} = 15 ns		250	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
t _{fl/O}	Fall time I ² C input/output voltage (80% to 20%)	1.8 ± 0.15	2.5 ± 0.2	C _L = 15 pF t _{fl/O} = 15 ns		250	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
t _{PLH}	Propagation delay time I ² C I/O voltage (20% to 80%) (low to high)	1.8 ± 0.15	2.5 ± 0.2	C _L = 15 pF t _{rl/O} = 15 ns		100	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
t _{PHL}	Propagation delay time I ² C I/O voltage (20% to 80%) high to low)	1.8 ± 0.15	2.5 ± 0.2	C _L = 15 pF t _{rl/O} = 15 ns		100	ns
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				
f _{I/OVA} , f _{I/OVB}	I ² C lines data rate	1.8 ± 0.15	2.5 ± 0.2	C _L = 15 pF t _{rl/O} = 15 ns	400		KHz
		1.8 ± 0.15	3.3 ± 0.3				
		2.5 ± 0.2	3.3 ± 0.3				

1. V_{CC} range = 3.3±0.3; 2.5±0.2 V and 2.8 ±0.1 V; 1.8 ±0.15 V

Table 13. Capacitance characteristics

Symbol	Parameter	Test condition			Value					Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
C _{INB}	Input capacitance	open	open			5				pF
C _{I/O}	Input/Output capacitance	2.5	3.3			6				pF
C _{PD} ⁽¹⁾	Power dissipation capacitance	2.5	3.3	f = 10MHz		28				pF
		1.8	3.3			28				pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average current can be obtained by the following equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/14 \text{ (per circuit)}$$

5 Test circuit

Figure 4. Test circuit

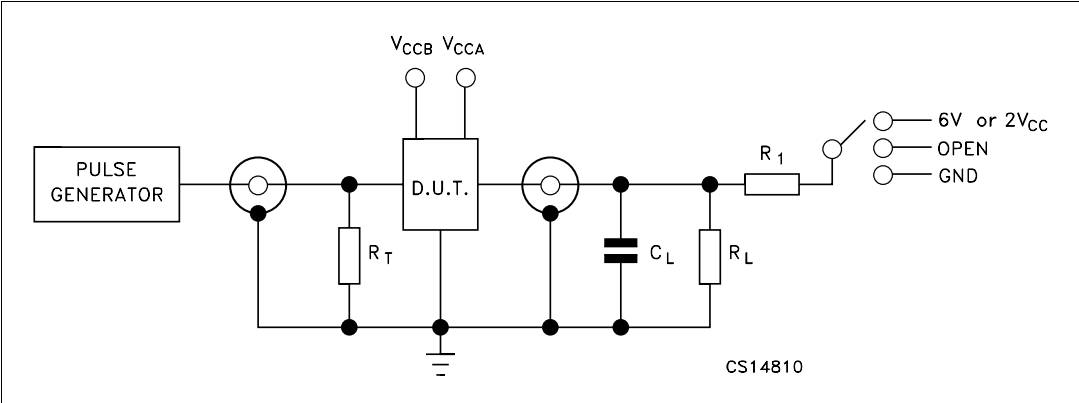


Table 14. Test circuit

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ} ($V_{CC} = 3.0$ to 3.6 V)	6 V
t_{PZL} , t_{PLZ} ($V_{CC} = 2.3$ to 2.7 V or $V_{CC} = 1.65$ to 1.95 V)	$2V_{CC}$
t_{PZH} , t_{PHZ}	GND

$C_L = 10/30$ pF or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500\Omega$ or equivalent

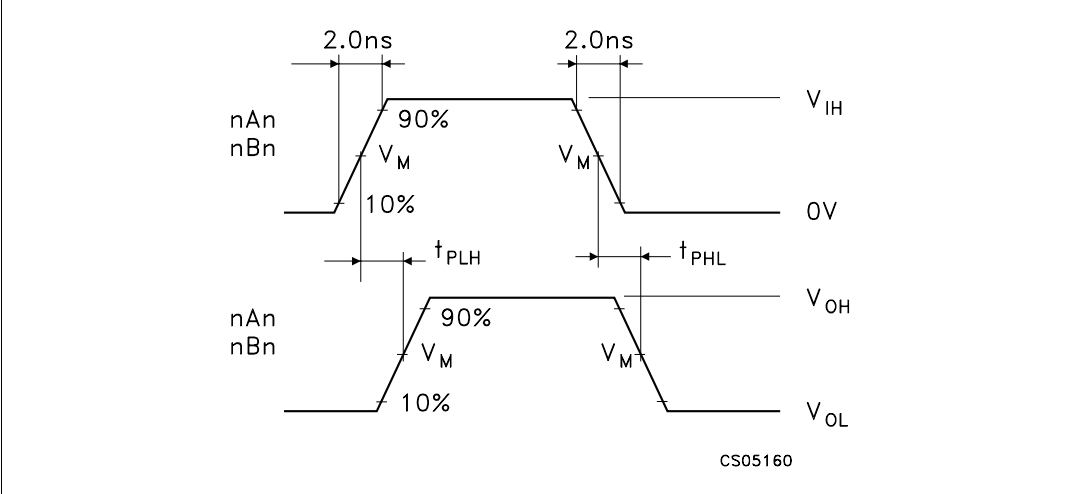
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

6 Waveforms

Table 15. Waveform symbol value

Symbol	V _{CC}		
	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V
V _{IH}	V _{CC}	V _{CC}	V _{CC}
V _M	1.5V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} +0.3V	V _{OL} +0.15V	V _{OL} +0.15V
V _Y	V _{OL} -0.3V	V _{OL} -0.15V	V _{OL} -0.15V

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)



The timing diagram illustrates the input and output signals for the SC13231 device. It features three main signal traces: $\overline{nG}$, nAn / nBn , and nAn / nBn .

- $\overline{nG}$ (Input):** A square wave signal. The high level is V_{IH} and the low level is GND. The signal transitions from high to low and low to high. The transition time is marked as 2.0ns. The signal levels are defined as 90% V_M and 10% V_M .
- nAn / nBn (Output):** A square wave signal. The high level is V_{OH} and the low level is GND. The signal transitions from low to high and high to low. The transition time is marked as 2.0ns. The signal levels are defined as 90% V_M and 10% V_M .
- nAn / nBn (Output):** A square wave signal. The high level is 3.0V or V_{CC} and the low level is V_{OL} . The signal transitions from high to low and low to high. The transition time is marked as 2.0ns. The signal levels are defined as 90% V_M and 10% V_M .

Timing parameters are indicated by arrows:

- t_{PZH} (Propagation delay from $\overline{nG}$ high to nAn / nBn high)
- t_{PHZ} (Propagation delay from $\overline{nG}$ high to nAn / nBn high)
- t_{PZL} (Propagation delay from $\overline{nG}$ low to nAn / nBn low)
- t_{PLZ} (Propagation delay from $\overline{nG}$ low to nAn / nBn low)

SC13231

The diagram illustrates the timing characteristics of the CS18070 device. It shows two signal transitions: a rising edge (left) and a falling edge (right).

Top Waveform (Input/Output):

- Input:** Labeled $I/O_{VA}, I/O_{VB}$. It shows a rising edge with propagation delay $t_{rI/O}$ and a falling edge with propagation delay $t_{fI/O}$. The signal levels are V_{CCA}, V_{CCB} and $0V$.
- Output:** Labeled $I/O_{VB}, I/O_{VA}$. It shows a rising edge with propagation delay t_{PLH} and a falling edge with propagation delay t_{PHZ} . The signal levels are V_{OH} and V_{OL} .

Timing Parameters:

- $t_{rI/O}$: Input rise time.
- $t_{fI/O}$: Input fall time.
- t_{PLH} : Propagation delay from input low to output high.
- t_{PHZ} : Propagation delay from input high to output high-impedance.

Signal Levels:

- V_{CCA}, V_{CCB} : Input high level.
- $0V$: Input low level.
- V_{OH} : Output high level.
- V_{OL} : Output low level.

Percentage Markers: The waveforms are marked with 20%, 50%, and 80% to indicate the points used for timing measurements.

CS18070

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 8. μ TFBGA42 mechanical data

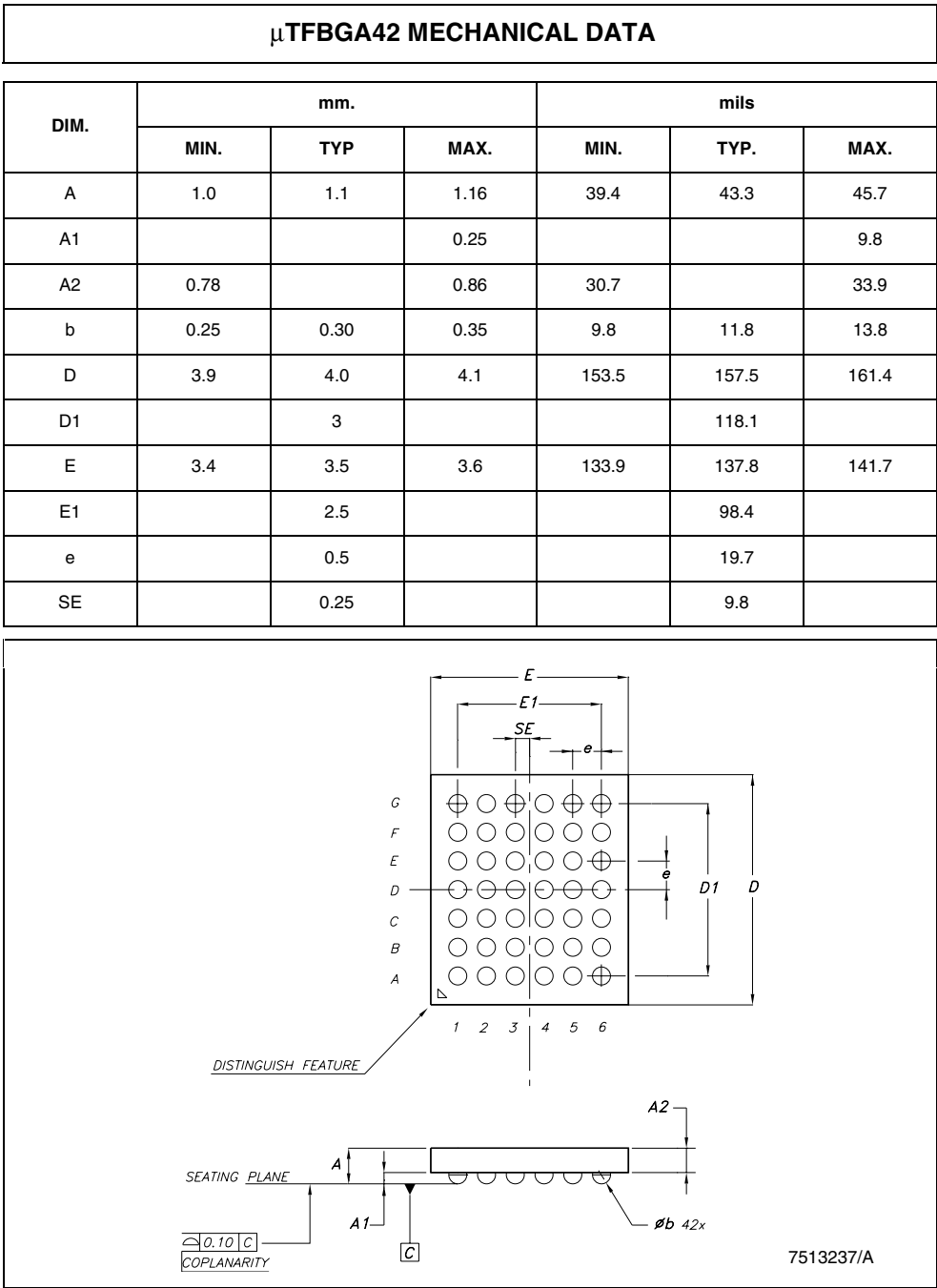
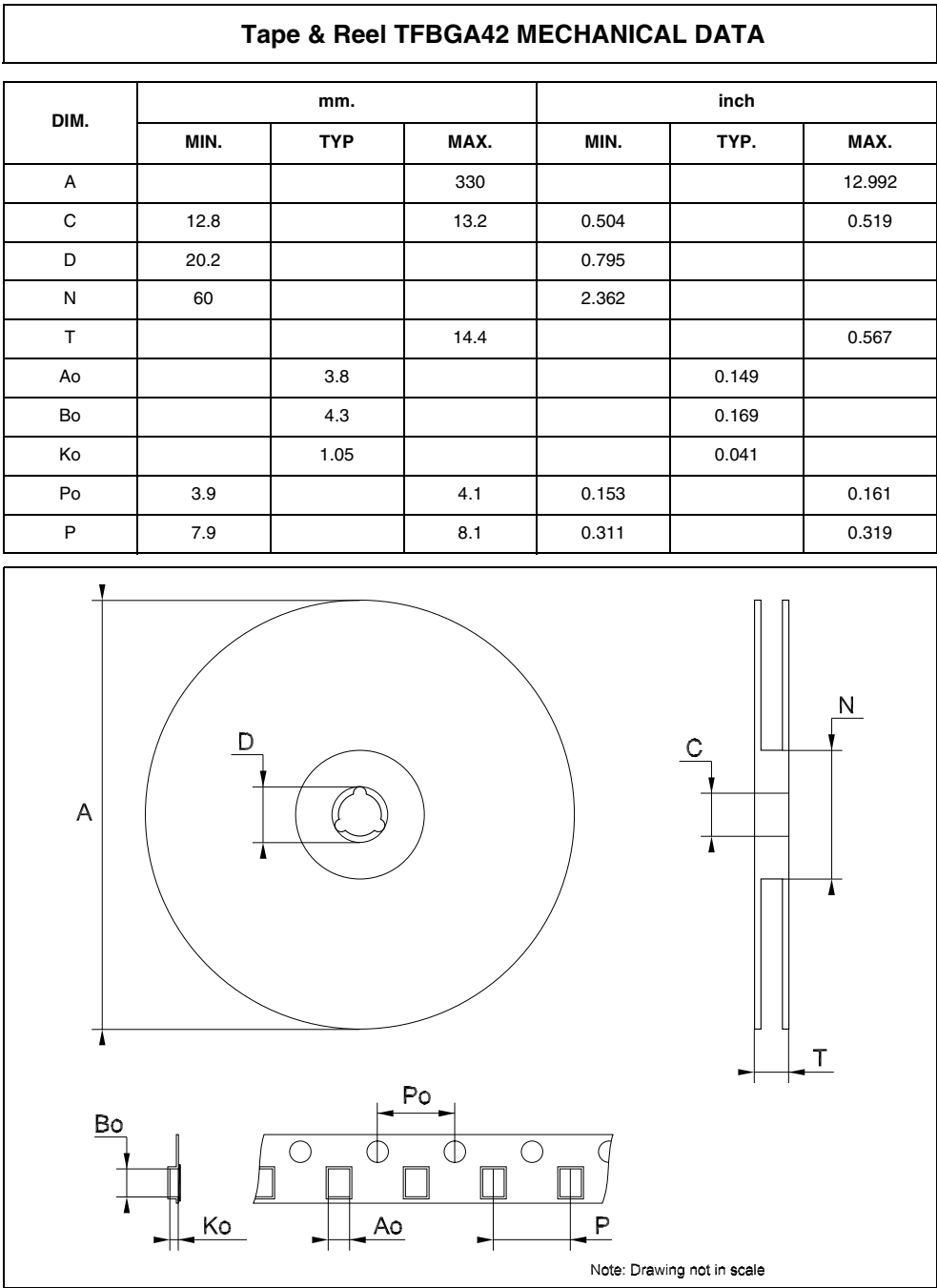


Figure 9. μ TFBGA42 tape and reel



8 Revision history

Table 16. Document revision history

Date	Revision	Changes
01-Oct-2004	1	Initial release.
31-Mar-2005	2	Document status promoted from preliminary data to datasheet.
04-Mar-2009	3	Document reformatted. TSSOP and TFBGA54 packages removed.

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