élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2142C

Differential Line Receiver

Features

- Differential input range ±2.3V
- 150MHz 3dB bandwidth
- 400V/μs slewrate
- ±5V supplies or single supply
- 50mA minimum output current
- Output swing (100Ω load) to within 1.5V of supplies
- Low power -11mA typical

Applications

- Twisted pair receiver
- Differential line receiver
- VGA over twisted pair
- ADSL/HDSL receiver
- Differential to single ended amplification.
- Reception of analog signals in a noisy environment.

Ordering Information

Part No.	Package	Tape & Reel	Outline #
EL2142CN	DIP-8	-	MDP0031
EL2142CS	SO-8	-	MDP0027
EL2142CS-T7	SO-8	7 in	MDP0027
EL2142CS-T13	SO-8	13 in	MDP0027

General Description

The EL2142C is a very high bandwidth amplifier designed to extract the difference signal from noisy environments, and is thus primarily targeted for applications such as receiving signals from twisted pair lines, or any application where common mode noise injection is likely to occur.

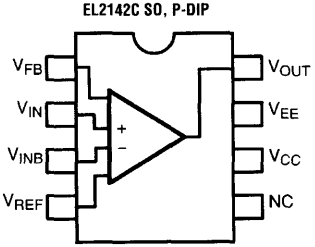
The EL2142C is stable for a gain of one, and requires two external resistors to set the voltage gain.

The output common mode level is set by the reference pin (V_{REF}), which has a -3dB bandwidth of over 100MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The output can deliver a minimum of ±50mA and is short circuit protected to withstand a temporary overload condition.

Connection Diagrams

EL2142C SO, P-DIP



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Absolute Maximum Ratings (T_A = 25 °C)

Supply Voltage (V_{CC}–V_{EE})	12.6V	Operating Junction Temperature	+150°C
Maximum Output Current	±60mA	Lead Temperature (<5 sec)	+300°C
Storage Temperature Range	-65°C to +150°C	Recommended Operating Temperature	-40° C to +85°C

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Characteristics

(V_{CC}=+5V, V_{EE} = -5V, T_A = 25C, V_{IN} = 0V, R_L = 100, unless otherwise specified)

Parameter	Description	Min	Typ	Max	Units
V_{supply}	Supply Operating Range (V_{CC} –V_{EE})	±3.0	±5.0	±6.3	V
I_S	Power Supply Current (no load)		11	14	mA
V_{OS}	Input Referred Offset Voltage	-25	10	40	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB}, V_{REF})	-20	6	20	µA
Z_{IN}	Differential Input Resistance		400		kΩ
C_{IN}	Differential Input Capacitance		1		pF
V_{DIFF}	Differential Input Range	±2.0	±2.3		V
A_{VOL}	Open Loop Voltage Gain		75		dB
V_{IN}	Input Common Mode Voltage Range	-2.6		+4.0	V
V_{OUT}	Output Voltage Swing (50Ω load to GND)	±2.9	±3.1		V
I_{OUT}(min)	Minimum Output Current	50	60		mA
V_N	Input Referred Voltage Noise		36		nV/√Hz
V_{REF}	Output Voltage Control Range	-2.5		+3.3	V
PSRR	Power Supply Rejection Ratio	60	70		dB
CMRR2	Input Common Mode Rejection Ratio (V_{IN}= ±2V)	60	70		dB
CMRR1	Input Common Mode Rejection Ratio (full V_{IN} range)	50	60		dB

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AC Electrical Characteristics

(V_{CC}=+5V, V_{EE}=-5V, T_A=25C, V_{IN}=0V, R_{LOAD}=100, unless otherwise specified)

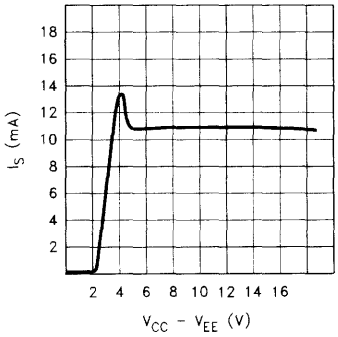
Parameter	Description	Min	Typ	Max	Units
BW(-3dB)	-3dB Bandwidth (Gain =1)		150		MHz
SR	Slewrate		400		V/µs
T_{stl}	Settling time to 1%		15		ns
GBWP	Gain bandwidth product		200		MHz
V_{REF}BW(-3dB)	V_{REF} -3dB Bandwidth		130		MHz
V_{REF}SR	V_{REF} Slewrate		100		V/µsec
dG	Differential gain at 3.58MHz		0.2		%
dθ	Differential phase at 3.58MHz		0.2		°

Pin Description

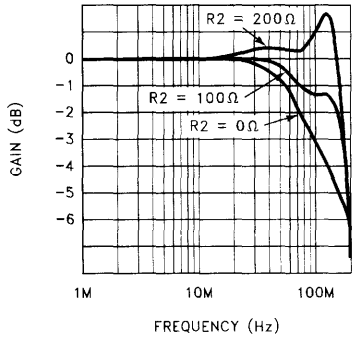
Pin Number	Pin Name	Function
1	V_{FB}	Feedback input
2	V_{IN}	Non-inverting input
3	V_{INB}	Inverting input
4	V_{REF}	Sets output voltage level to V_{REF} when V_{IN}=V_{INB}
5	NC	
6	V_{CC}	Positive supply voltage
7	V_{EE}	Negative supply voltage
8	V_{OUT}	Output voltage

Typical Performance Curves

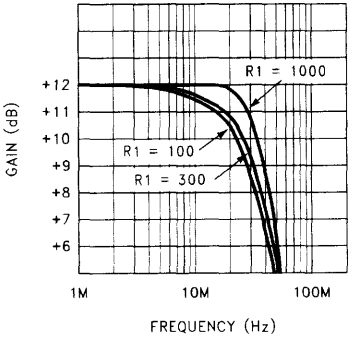
I_S vs Supply Voltage



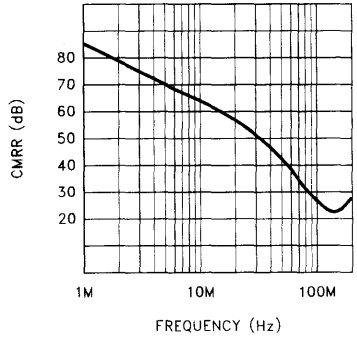
Frequency Response (Gain = 1)



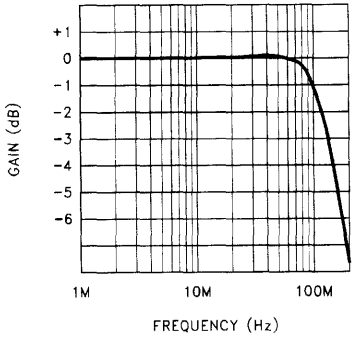
Frequency Response vs Resistor R1 (Gain = 4)



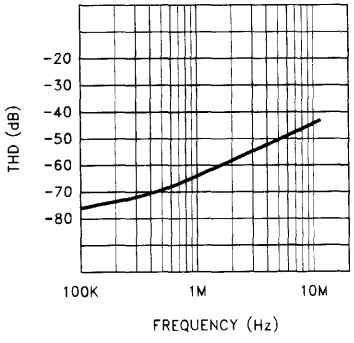
CMRR vs Frequency



V_{REF} Frequency Response



Distortion vs Frequency (GAIN = 3, R_{LOAD} = 100Ω) V_{IN} = 2V pk/pk



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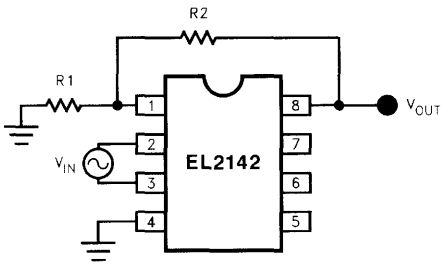
Applications Information



Gain Equation

$V_{OUT} = ((R2+R1)/R1) \times (V_{IN}-V_{INB}+V_{REF})$ when R1 tied to GND

$V_{OUT} = ((R2+R1)/R1) \times (V_{IN}-V_{INB})$ when R1 tied to V_{REF}

Choice of Feedback Resistor

For a gain of one, V_{OUT} may be shorted back to V_{FB}, but 100Ω to 200Ω improves the bandwidth. For gains greater than one, there is little to be gained from choosing resistor R1 value below 200Ω, for it would only result in increased power dissipation and potential signal distortion. Above 200Ω, the bandwidth response will develop some peaking (for a gain of one), but substantially higher R1 values may be used for higher voltage gains, such as up to 1kΩ at a gain of four before peaking will develop.

Capacitance Considerations

As with many high bandwidth amplifiers, the EL2142C prefers not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} is kept below 10pF if the user does not want gain peaking to develop. The V_{FB} node forms a potential pole in the feedback loop, so capacitance should be minimized on this node for maximum bandwidth.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

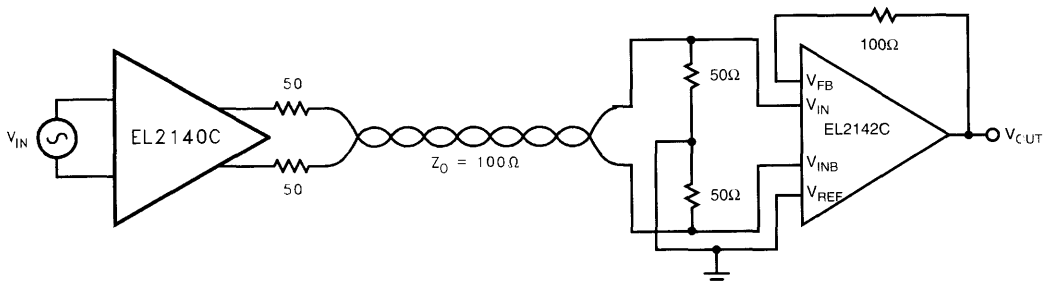


Figure 1. Typical Twisted Pair Application

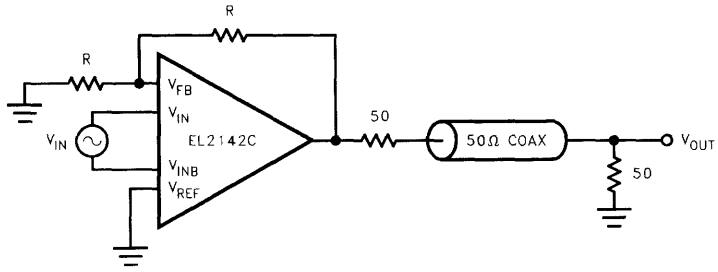


Figure 2. Coaxial Cable Driver Pair Application

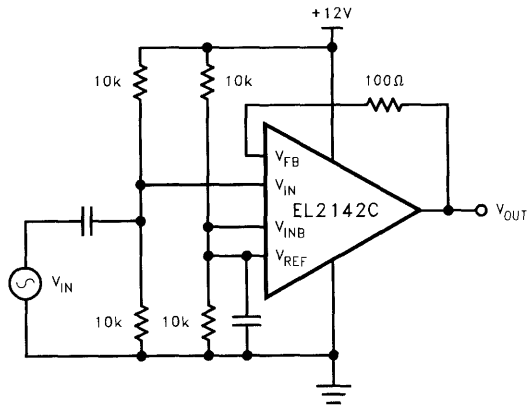


Figure 3. Single Supply Receiver

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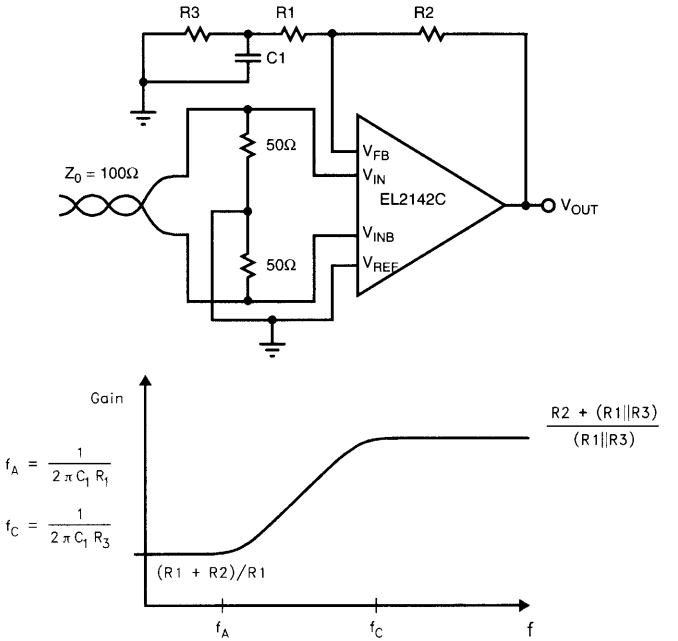

Figure 4. Compensated Line Receiver

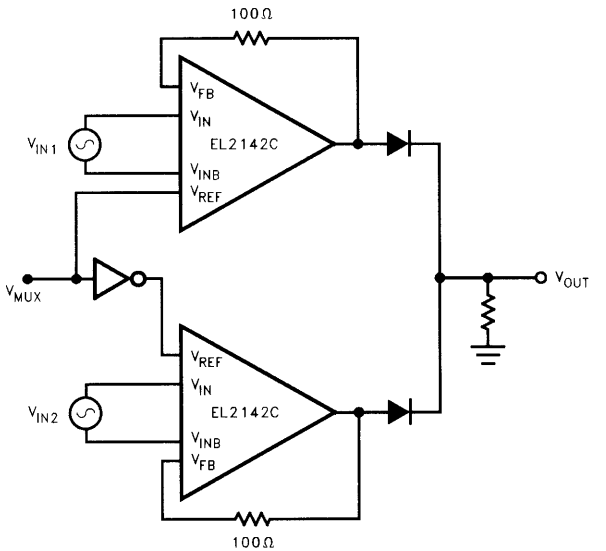

Figure 5. Two Channel Multiplexer