

✓ **54LS/74LS273** 011564 **8-BIT REGISTER** (With Clear)

DESCRIPTION — The '273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

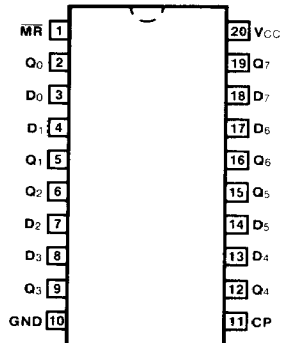
- **EDGE-TRIGGERED**
- **8-BIT HIGH SPEED REGISTER**
- **PARALLEL IN AND OUT**
- **COMMON CLOCK AND MASTER RESET**

ORDERING CODE: See Section 9

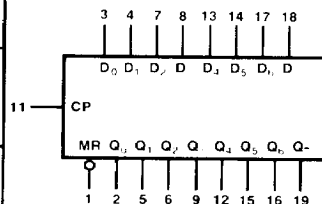
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C to } +70^\circ \text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ \text{C to } +125^\circ \text{C}$	
Plastic DIP (P)	A	74LS273PC		9Z
Ceramic DIP (D)	A	74LS273DC	54LS273DM	4E
Flatpak (F)	A	74LS273FC	54LS273FM	4F

CONNECTION DIAGRAM

PINOUT A



LOGIC SYMBOL

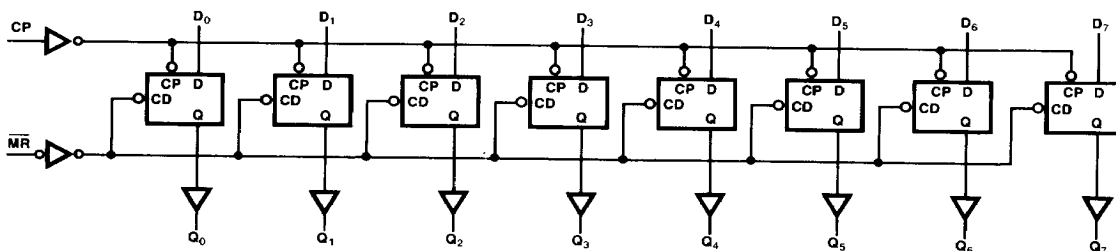


$V_{CC} = \text{Pin } 20$
 $GND = \text{Pin } 10$

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$D_0 - D_7$	Data Inputs	0.5/0.25
MR	Asynchronous Master Reset Input (Active LOW)	0.5/0.25
$Q_0 - Q_7$	Flip-flop Outputs	10/5.0 (2.5)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The '273 is an 8-bit parallel register with a common Clock and common Master Reset. When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

TRUTH TABLE

INPUTS			OUTPUTS
MR	CP	D _n	Q _n
L	X	X	L
H		H	H
H		L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I _{CC}	Power Supply Current	27		mA	V _{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		CL = 15 pF			
		Min	Max		
fmax	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
tPLH	Propagation Delay	24		ns	Figs. 3-1, 3-8
tPHL	CP to Qn	24			
tPHL	Propagation Delay MR to Qn	27		ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t _s (H)	Setup Time HIGH or LOW	15		ns	Fig. 3-6
t _s (L)	D _n to CP	15		ns	
t _h (H)	Hold Time HIGH or LOW	5.0		ns	Fig. 3-8
t _h (L)	D _n to CP	5.0		ns	
t _w (H)	CP Pulse Width HIGH or LOW	20		ns	Fig. 3-16
t _w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	
t _{rec}	Recovery Time	15		ns	Fig. 3-16
	$\overline{MR}$ to CP				