8 Pin Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 18-Bit Resolution
- 94 dB Dynamic Range
- 0.003% THD
- Low Clock Jitter Sensitivity
- Single +3 V or +5 V Power Supply
- Filtered Line Level Outputs Linear Phase Filtering
- On-Chip Digital De-emphasis

Description

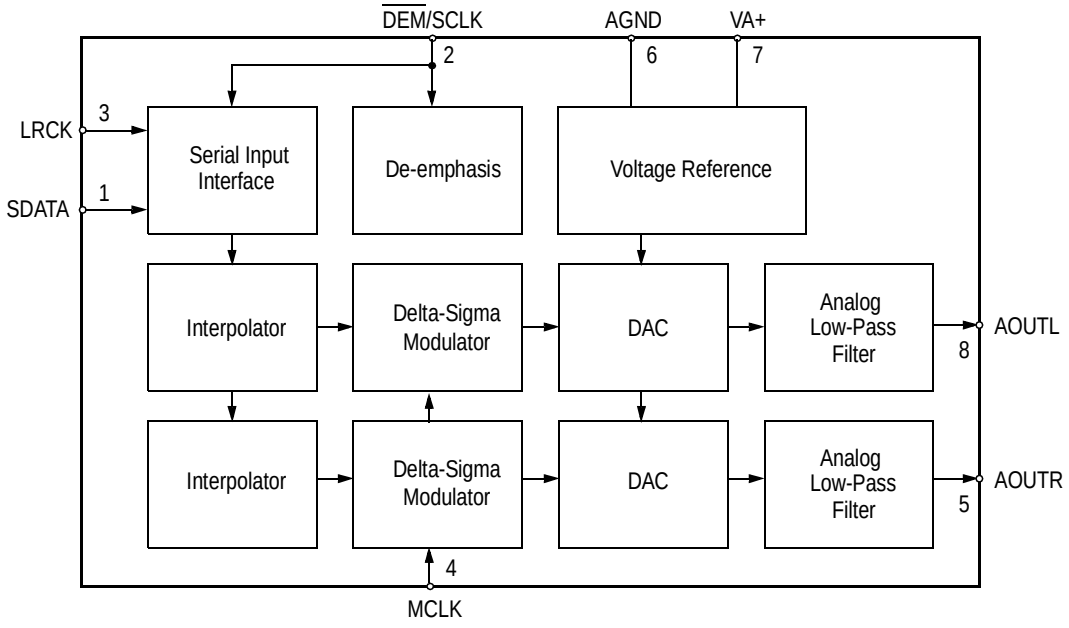
The CS4330, CS4331 and CS4333 are complete, stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering in an 8-pin package. These devices differ in the serial interface format used to input audio data.

The CS4330, CS4331 and CS4333 are based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4330, CS4331 and CS4333 contain on-chip digital de-emphasis, operate from a single +3 V or +5 V power supply, and consume only 60mW of power with a 3 V power supply. These features make them ideal for portable CD players and other portable playback systems.

ORDERING INFORMATION

See page 21.



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ANALOG CHARACTERISTICS (T_A = 25°C; Logic "1" = VA+; Logic "0" = AGND; MCLK = 12.288 MHz; Full-Scale Output Sine Wave, 991 Hz; Input Sample Rate = 48 kHz; Input Data = 18 Bits; SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz, unweighted; unless otherwise specified. Resistive load = 20 kΩ, capacitive load = 100 pF)

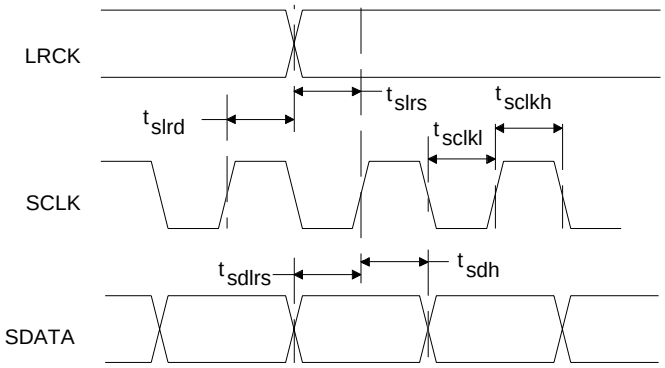
Parameter	Symbol	CS4330/31/33-KS VA +5V			CS4330/31/33-KS VA +3V			CS4330/31/33-BS VA +5V only			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range	T_A	-10	to	70	-10	to	70	-40	to	+85	°C
Resolution		-	-	18	-	-	18	-	-	18	Bits
Dynamic Performance											
Dynamic Range (A-weighted)		90	94	-	-	89	-	88	94	-	dB
Total Harmonic Distortion		-	0.003	0.007	-	0.003	-	-	.003	.008	%
Total Harmonic Distortion + Noise	THD+N										
0 dB Output,		-	-86	-81	-	-85	-80	-88	-86	-79	dB
-20 dB Output,		-	-72	-68	-	-67	-	-	-72	-66	dB
-60 dB Output		-	-32	-28	-	-27	-	-	-32	-26	dB
Deviation From Linear Phase (Note 1)		-	± 0.5	-	-	± 0.5	-	-	± 0.5	-	deg
Passband: to 0.05 dB corner (Note 2,3)		0	to	21.77	0	to	21.77	0	to	21.77	kHz
Frequency Response 10 Hz to 20 kHz (Note 1)		-	± 0.1	-	-	± 0.1	-	-	± 0.1	-	dB
Passband Ripple (Note 3)		-	-	±0.05	-	-	±0.05	-	-	±0.05	dB
StopBand (Notes 2,3)		26.23			26.23			26.23	-	-	kHz
StopBand Attenuation (Note 4)		60	-	-	60	-	-	60	-	-	dB
Group Delay (Fs = Input Sample Rate)	tgd	-	16 / Fs	-	-	16 / Fs	-	-	16 / Fs	-	s
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	-	90	-	dB
dc Accuracy											
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	-	0.1	-	dB
Gain Error		-	-	± 10	-	-	± 10	-	-	± 10	%
Gain Drift		-	250	-	-	250	-	-	250	-	ppm/°C
Analog Output											
Full Scale Output Voltage		3.33	3.70	4.07	1.66	1.85	2.03	3.33	3.70	4.07	Vpp
Output Common Mode Voltage		-	2.3	-	-	1.3	-	-	2.3	-	VDC
Minimum Resistive Load		-	10	-	-	10	-	-	20	-	kΩ
Maximum Capacitive Load		-	100	-	-	100	-	-	100	-	pF
Power Supplies											
Power Supply Current: normal operation	IA+	-	28	32	-	20	25	-	28	32	mA
power-down	IA+	-	60	-	-	20	-	-	60	-	µA
Power Dissipation normal operation		-	140	160	-	60	75	-	140	160	mW
power-down		-	0.3	-	-	0.06	-	-	0.3	-	mW
Power Supply Rejection Ratio (1 kHz)	PSRR	-	50	-	-	50	-	-	50	-	dB

Notes: 1. Combined digital and analog filter characteristics.
2. The passband and stopband edges scale with frequency. For input sample rates, Fs, other than 48 kHz, the 0.05 dB passband edge is 0.4535×Fs and the stopband edge is 0.5465×Fs.
3. Digital filter characteristics.
4. Measurement Bandwidth is 10 Hz to Fs (kHz)

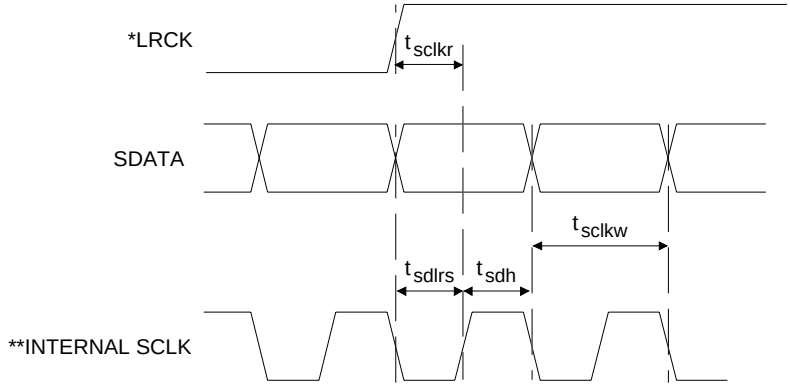
SWITCHING CHARACTERISTICS (TA = 25 °C; VA+ = 2.7V - 5.5V; Inputs: Logic 0 = 0V, Logic 1 = VA+, CL = 20 pF) Switching characteristics are guaranteed by characterization.

Parameter		Symbol	Min	Typ	Max	Units
Input Sample Rate		Fs	2	-	50	kHz
LRCK Duty Cycle (External SCLK only)	(Note 5)		30	50	70	%
MCLK Pulse Width High	MCLK / LRCK = 512		10	-	1000	ns
MCLK Pulse Width Low	MCLK / LRCK = 512		15	-	1000	ns
MCLK Pulse Width High	MCLK / LRCK = 384		21	-	1000	ns
MCLK Pulse Width Low	MCLK / LRCK = 384		21	-	1000	ns
MCLK Pulse Width High	MCLK / LRCK = 256		35	-	1000	ns
MCLK Pulse Width Low	MCLK / LRCK = 256		39	-	1000	ns
External SCLK Mode						
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period		t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	-	ns
Internal SCLK Mode						
SCLK Period	(Note 6)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	ns
SCLK rising to LRCK edge		t_{sclkr}	-	$\frac{t_{sclkw}}{2}$	-	µs
SDATA valid to SCLK rising setup time		t_{sdlrs}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time	MCLK / LRCK = 256 or 512	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time	MCLK / LRCK = 384	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 5. In Internal SCLK Mode, the Duty Cycle must be 50% ±1/2 MCLK Period.
6. The SCLK / LRCK ratio may be either 32, 48, or 64.



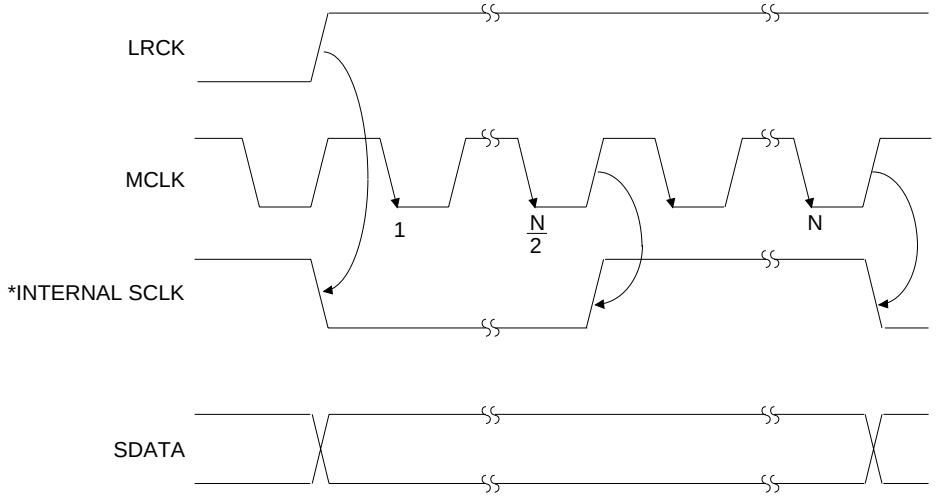
External Serial Mode Input Timing



Internal Serial Mode Input Timing

* LRCK for CS4331

** The SCLK pulses shown are internal to the CS4330/31/33.



Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4330/31/33.
N equals MCLK divided by SCLK

DIGITAL CHARACTERISTICS (TA = 25 °C; VA+ = 2.7V - 5.5V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(VA+ = 5.5V)	V_{IH}	2.4	-	-	V
	(VA+ = 5.0V)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
Input Leakage Current	(Note 7)	I_{in}	-	-	±10	µA

Notes: 7. I_{in} for CS4331 LRCK is ± 20 µA max.

ABSOLUTE MAXIMUM RATINGS (AGND = 0V; all voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
DC Power Supply:	VA+	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	(VA+)+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply:	(3V mode)	VA+	2.7	3.0	4.0	V
	(5V mode)	VA+	4.75	5.0	5.5	V

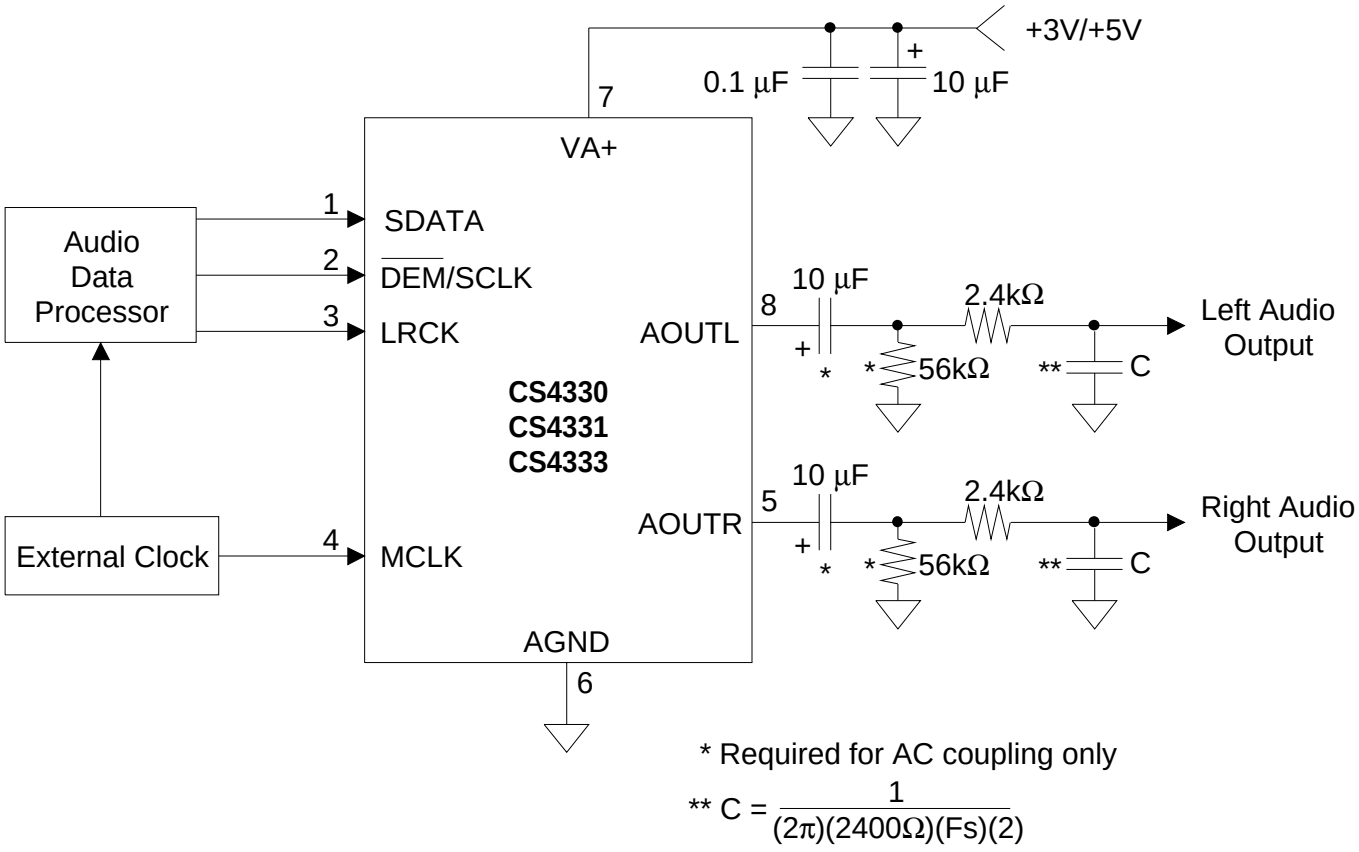


Figure 1. Recommended Connection Diagram

GENERAL DESCRIPTION

The CS4330, CS4331, and CS4333 are complete stereo digital-to-analog systems including digital interpolation, 128× third-order delta-sigma digital-to-analog conversion, digital de-emphasis and analog filtering, Figure 2. This architecture provides a high tolerance to clock jitter.

The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of laser trimmed resistive digital-to-analog converter architectures by using an inherently linear 1-bit digital-to-analog converter. The advantages of a 1-bit digital-to-analog converter include: ideal differential linearity, no distortion mechanisms due to resistor matching errors and no linearity drift over time and temperature due to variations in resistor values.

Digital Interpolation Filter

The digital interpolation filter increases the sample rate by a factor of 32 and is followed by a 4× digital sample-and-hold to effectively achieve a 128× interpolation filter. This filter eliminates images of the baseband audio signal which exist at multiples of the input sample rate, Fs. This allows for the selection of a less complex analog filter based on out-of-band noise attenuation requirements rather than anti-image filtering.

Following the interpolation filter, the resulting frequency spectrum has images of the input signal at multiples of 128× the input sample rate. These images are removed by the external analog filter.

Delta-Sigma Modulator

The interpolation filter is followed by a third-order delta-sigma modulator which converts the 22-bit interpolation filter output into 1-bit data at 128× .

Switched-Capacitor Filter

The delta-sigma modulator is followed by a digital-to-analog converter which translates the 1-bit data into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit signal. This technique greatly reduces the sensitivity to clock jitter and is a major improvement over earlier generations of 1-bit digital-to-analog converters.

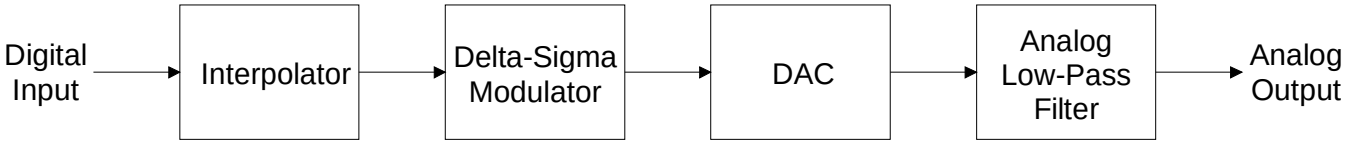


Figure 2. System Block Diagram

SYSTEM DESIGN

The CS4330/31/33 accept data at standard audio frequencies including 48 kHz, 44.1 kHz and 32 kHz. Audio data is input via the serial data input pin (SDATA). The Left/Right Clock (LRCK) defines the channel and delineation of data and the Serial Clock (SCLK) clocks audio data into the input data buffer. The CS4330, CS4331 and CS4333 differ in the serial data format as shown in Figures 4-7. The Master Clock (MCLK) is used to operate the digital interpolation filter and the delta-sigma modulator.

Master Clock

The MCLK must be either 256×, 384×, or 512× the desired input sample rate, Fs. Fs is the frequency at which words for each channel are input to the digital-to-analog converter, and is equal to the LRCK frequency. The MCLK to LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are set to generate the proper clocks for the digital filter, delta-sigma modulator and switched-capacitor filter. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 1. Common Clock Frequencies

Serial Clock

The serial clock controls the shifting of data into the input data buffers. The CS4330/31/33 support both external and internal serial clock generation modes. Refer to Figures 4-7 for data formats.

External Serial Clock Mode

The CS4330/31/33 will enter the External Serial Clock Mode when 4 low to high transitions are detected on the $\overline{\text{DEM}}$/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The CS4330/31/33 must return to Power-Down to exit this mode. Refer to Figure 8.

Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, or 64. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figure 8.

While the Internal Serial Clock Mode is provided to allow access to the de-emphasis filter, the Internal Serial Clock Mode also eliminates possible clock interference from an external SCLK. Use of Internal Serial Clock Mode is always preferred, even when de-emphasis filtering is not required.

De-Emphasis

The CS4330/31/33 include on-chip digital de-emphasis. Figure 3 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the $\overline{\text{DEM}}$/SCLK pin is low (high) for 8 consecutive falling edges of LRCK. This function is available only in the internal serial clock mode.

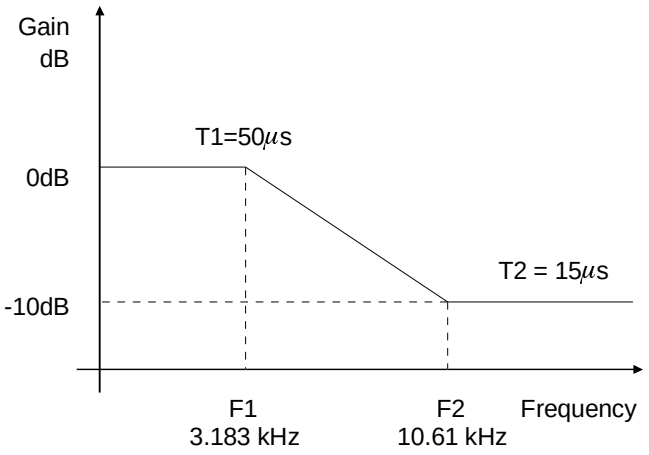


Figure 3. De-Emphasis Curve (Fs = 44.1kHz)

Initialization and Power-Down

The Initialization and Power-Down sequence flow chart is shown in Figure 8. The CS4330/31/33 enter the Power-Down mode upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, one-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down mode until MCLK and LRCK are presented. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference and the +5 or +3 Volt power supply mode is determined. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will move to approximately 2.3V (1.3V in 3V mode). This process requires approximately 1ms plus 1024 cycles of LRCK.

The CS4330/31/33 enter the Power-Down mode within 1 period of LRCK if either MCLK or LRCK is removed. The initialization sequence begins when MCLK and LRCK are restored. If the MCLK/LRCK frequency ratio or the VA+ voltage changes during Power-Down, the CS4330/31/33 adapt to these new operating conditions. It is recomended that the CS4330/31/33 not be powered up with the clocks (MCLK, LRCK, SCLK) going.

Power Supply Determination

The nominal power supply voltage for the CS4330/31/33 may be either +5 or +3 Volts. "SMART *Analog*" circuitry senses the power supply voltage during the initialization sequence or when exiting the Power-Down mode. +5V operation will be set with a 3.7 Vpp full scale output if VA+ is between 4.75 and 5.5 Volts. The CS4330/31/33 will be set for +3V operation with a 1.85 Vpp full scale output if VA+ is between 2.7 and 4.0 Volts. Supply voltages between 4.0 and 4.75 Volts should be avoided to prevent operation in the 5V mode. In this condition there is insufficient headroom to produce a 3.7 Vpp output.

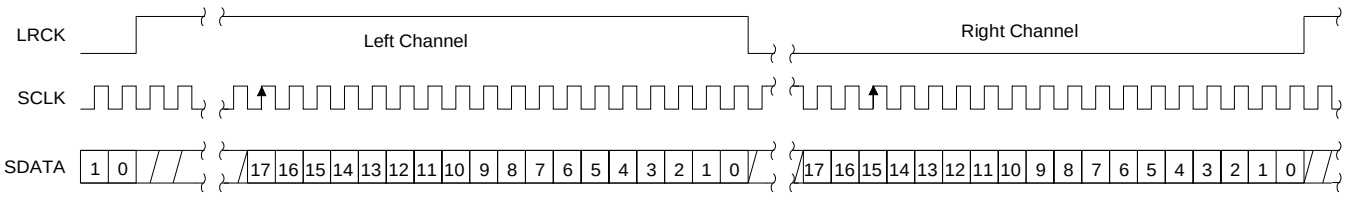
Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4330/31/33 require careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +3/+5V supply. Decoupling capacitors should be located as near to the CS4330/31/33 as possible.

Analog Output and Filtering

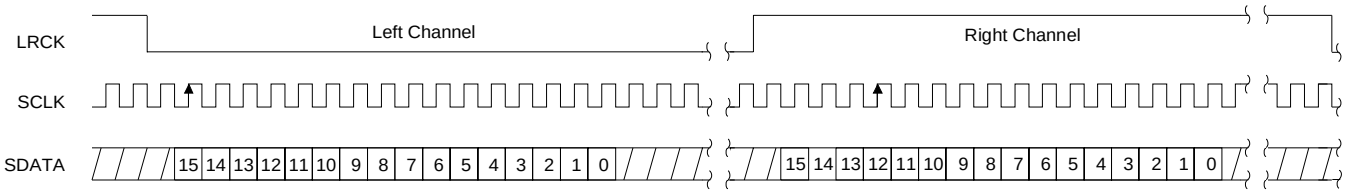
The CS4330/31/33 analog filter is a switched-capacitor filter. The switched-capacitor filter frequency response is clock dependent and will scale with sample rate.

The digital filter of the CS4330/31/33 is designed to compensate for the magnitude and phase response of a single-pole low-pass filter at twice the sample rate. Output filters consisting of a 2.4 kohm resistor and capacitor are recom-



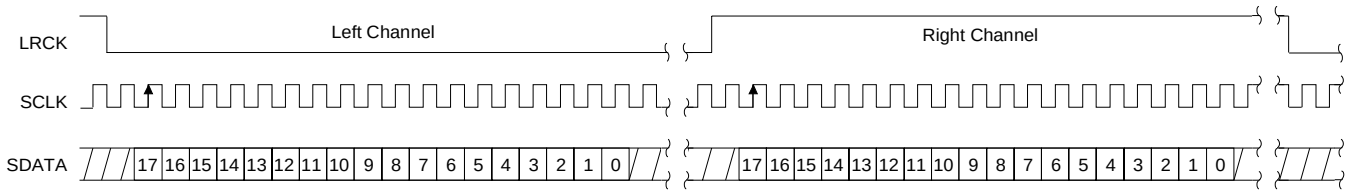
Internal SCLK Mode	External SCLK Mode
Right Justified, 18-Bit Data Data Valid on Rising Edge of SCLK INT SCLK = 64 Fs if MCLK/LRCK = 256 or 512 INT SCLK = 48 Fs if MCLK/LRCK = 384	Right Justified, 18-Bit Data Data Valid on Rising Edge of SCLK SCLK must have at least 36 cycles per LRCK

Figure 4. CS4330 Data Format



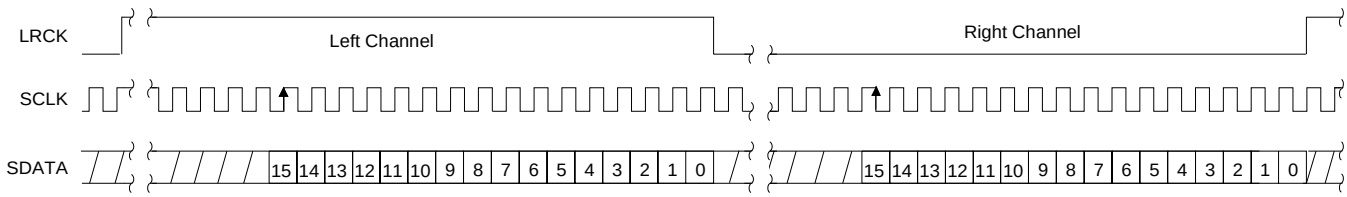
Internal SCLK Mode
I^2S, 16-Bit Data Data Valid on Rising Edge of SCLK INT SCLK = 32 Fs if MCLK/LRCK = 512 or 256 INT SCLK = 48 Fs if MCLK/LRCK = 384

Figure 5. CS4331 Internal SCLK Data Format (I^2S)



External SCLK Mode
I^2S, 18-Bit Data Data Valid on Rising Edge of SCLK SCLK must have at least 36 cycles per LRCK

Figure 6. CS4331 External SCLK Data Format (I^2S)



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK INT SCLK = 32 Fs if MCLK/LRCK = 512 or 256 INT SCLK = 48 Fs if MCLK/LRCK = 384	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK must have at least 32 cycles per LRCK

Figure 7. CS4333 SCLK Data Format

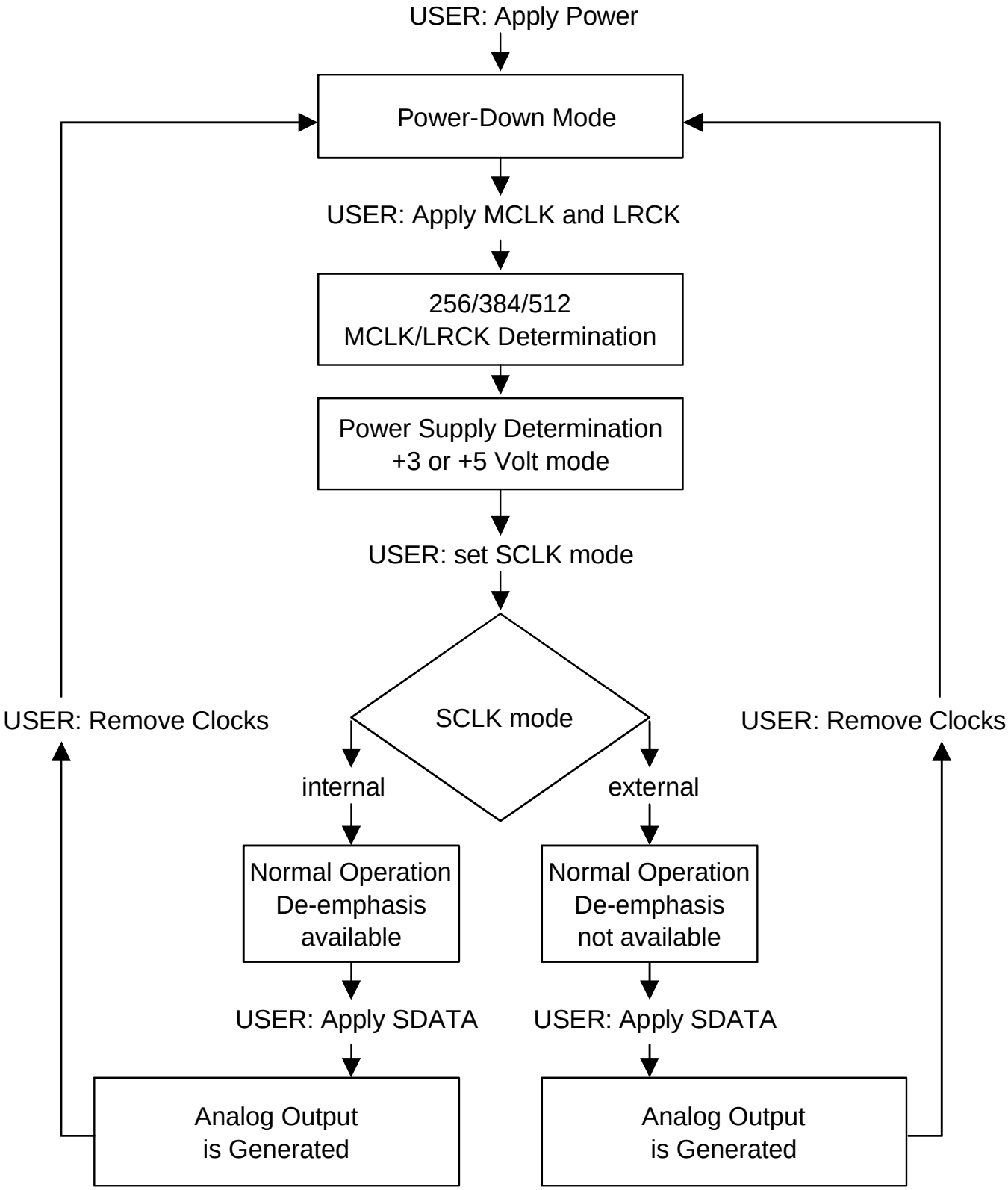


Figure 8. CS4330/31/33 Initialization and Power-Down Sequence

mended on the analog outputs. The required capacitor value is defined by:

$$C = \frac{1}{(2\pi)\,(Fs)\,(2400\ \Omega)\,(2)}$$

Example: Fs = 48 kHz
C = 690 pF

A value of 680 pF may be used with only 1.45% error which is negligible.

Combined Digital and Analog Filter Response

The frequency response of the combined analog switched-capacitor filter, digital filter, and off-chip single pole RC-filter at 2 Fs, is shown in Figures 9, 10, 11, and 12. The overall response is clock dependent and will scale with Fs. Note that the response plots have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

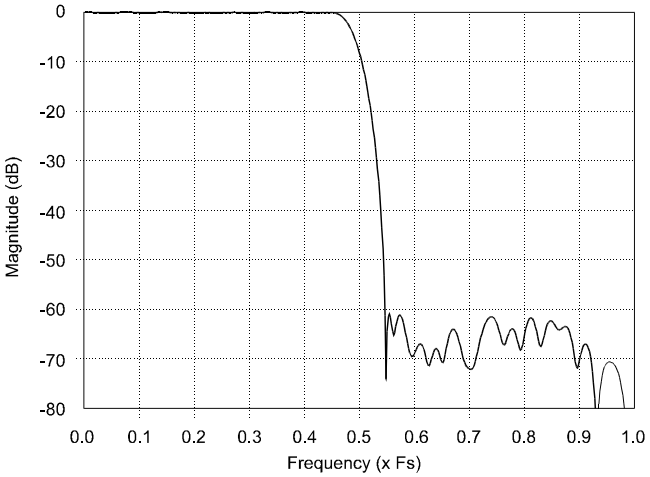


Figure 9. CS4330/31/33 Combined Digital and Analog Filter Stopband Rejection

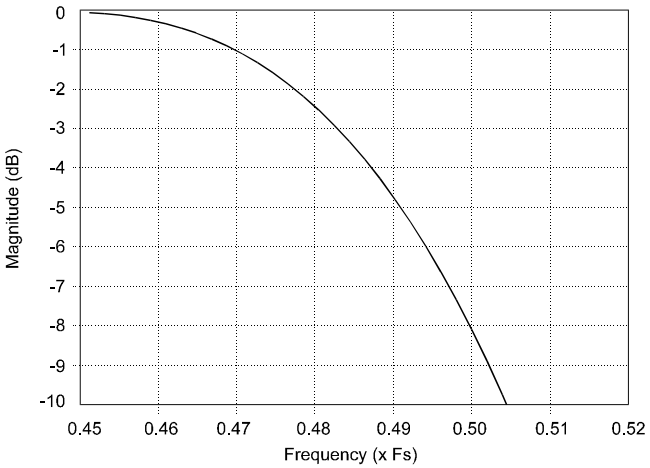


Figure 11. CS4330/31/33 Combined Digital and Analog Filter Transition Band

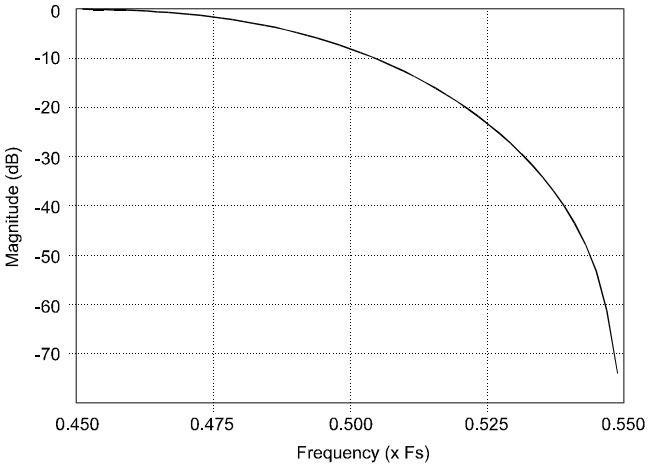


Figure 10. CS4330/31/33 Combined Digital and Analog Filter Transition Band

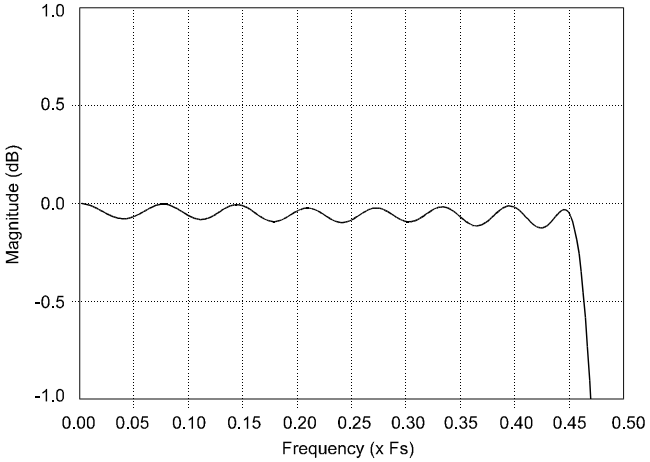


Figure 12. CS4330/31/33 Combined Digital and Analog Filter Passband Ripple

Performance Plots

The following CS4330/31/33 measurement plots were taken on the CDB4330/31/33 evaluation board with an Audio Precision Dual Domain System One. All plots are done in +5V mode at a 48 kHz sampling rate, and are shown in Figures 13-20.

Figure 13 shows the CS4330/31/33 frequency response. The response is flat to 20 kHz ± 0.1dB as specified.

Figure 14 shows THD+N versus signal amplitude for a 1 kHz 20-bit dithered input signal.

Figure 15 shows a 16k FFT of a 1 kHz full-scale input signal. The signal has been filtered by a notch filter within the System One to remove the fundamental component of the signal. This minimizes the distortion created in the analyzer analog-to-digital converter. This technique is discussed by Audio Precision in the 10th anniversary edition of AUDIO.TST.

Figure 16 shows a 16k FFT of a 1 kHz -3 dBFs input signal. The signal has been filtered by a notch filter within the System One to remove the fundamental component of the signal.

Figure 17 shows a 16k FFT of a 1 kHz -20 dBFs input signal. The signal has been filtered by a notch filter within the System One to remove the fundamental component of the signal.

Figure 18 shows a 16k FFT of a 1 kHz -60 dBFs input signal.

Figure 19 shows a 16k FFT of a 1 kHz -90 dBFs input signal.

Figure 20 shows the fade-to-noise linearity. The input signal is a dithered 18-bit 500 Hz sine

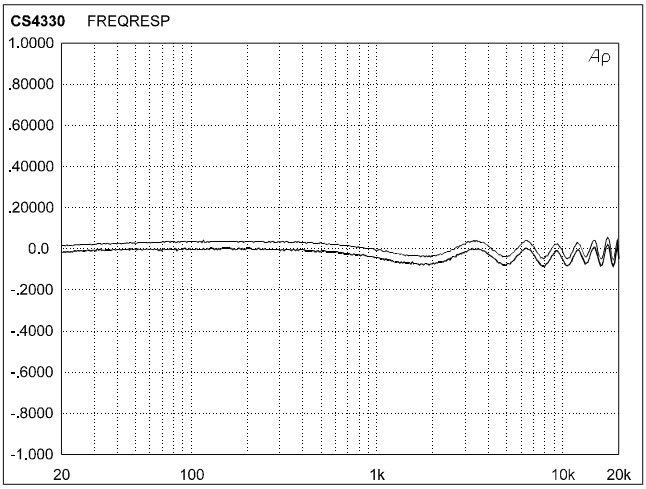


Figure 13. Frequency Response

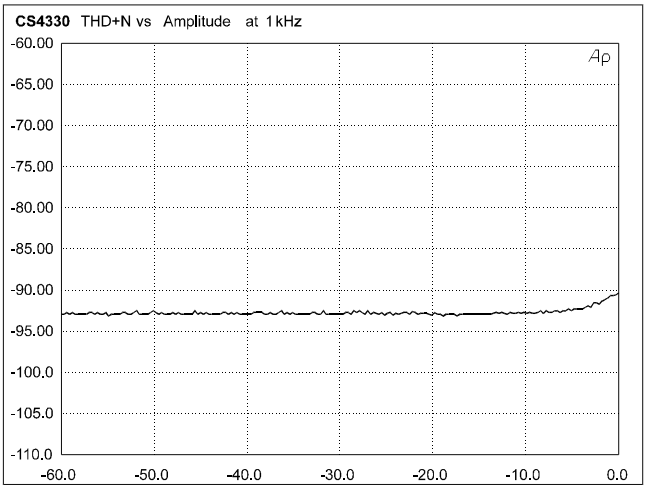


Figure 14. THD+N vs. Amplitude

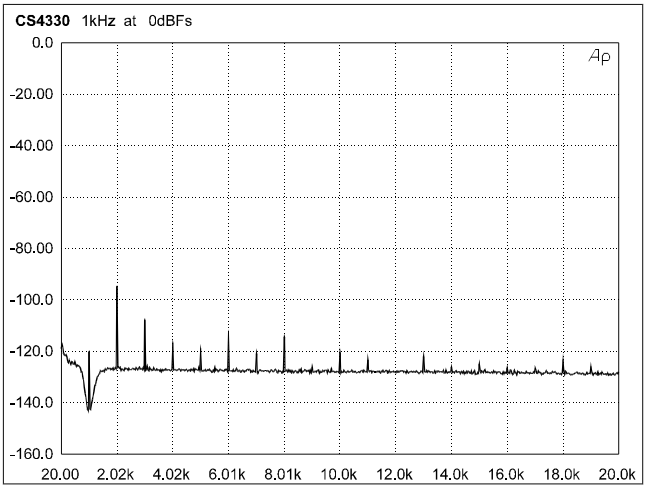


Figure 15. 0 dBFs FFT

wave which fades from -60 to -120 dBFs. During the fade, the output from the CS4330/31/33 is measured and compared to the ideal level. Notice the very close tracking of the output level to the ideal, even at low level inputs. This indicates very good low-level linearity, one of the key benefits of delta-sigma digital-to-analog conversion.

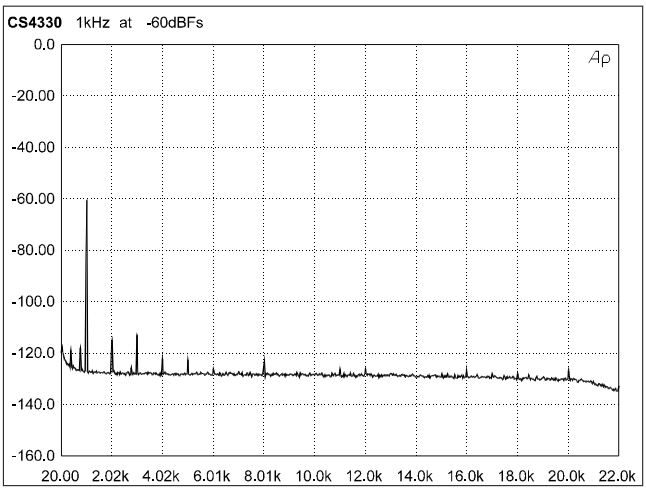


Figure 18. -60 dBFs FFT

Figure 16. -3 dBFs FFT

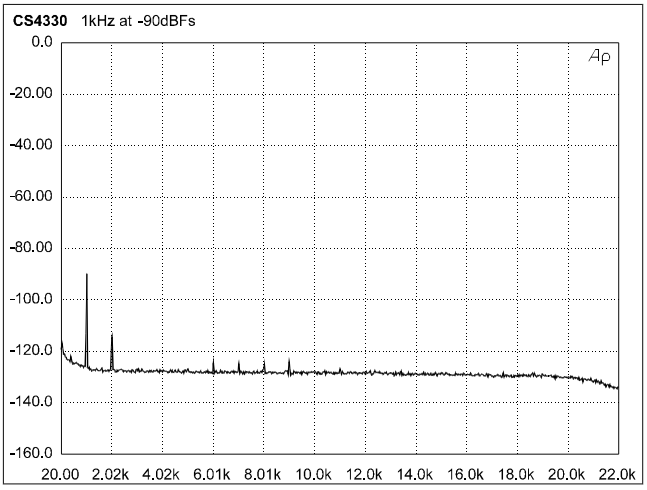


Figure 19. -90 dBFs FFT

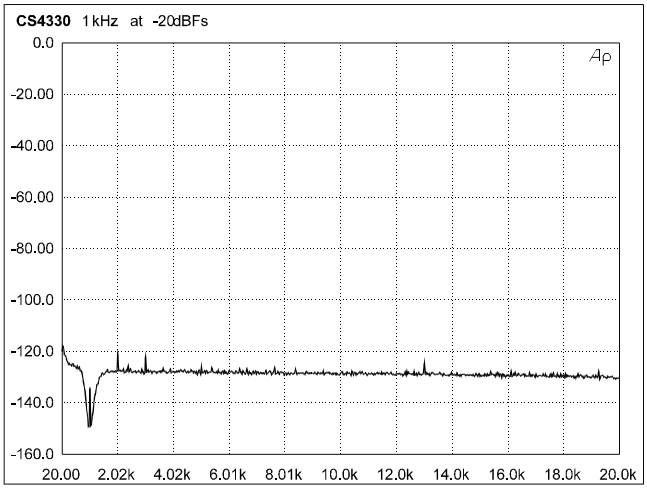


Figure 17. -20 dBFs FFT

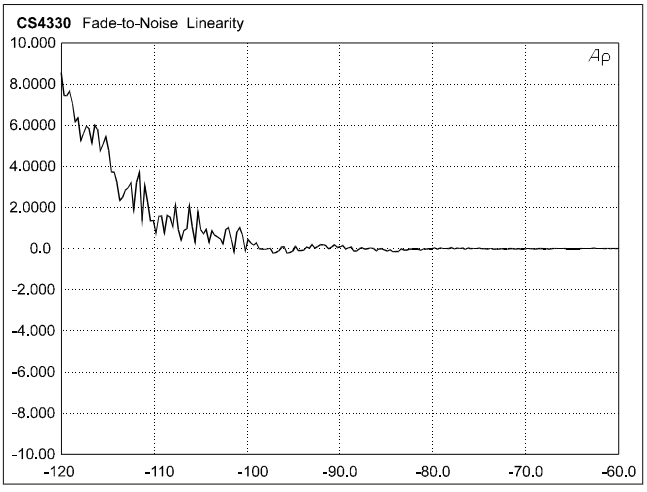


Figure 20. Fade-to-Noise Linearity

Configuration Register

The CS4330, CS4331, CS4333 support multiple 2's-complement data/clock formats. The required format is governed by the contents of the Configuration Register. The 5-bit register determines which serial data format is acceptable, the frequency of the Internal Serial Clock, on which edge of SCLK audio data must be valid, and the number of bits to be loaded into the input buffer. *On initial power-up, the register is loaded with the default settings, and it is not necessary to write to the register if this format is appropriate.* The default settings are shown in Figures 4-7. The 8-bit code includes a 3-bit preamble to prevent accidental access to the Configuration Register. Each bit of the code is read on the falling edge of LRCK as shown in the Figures 21 and 22. The code 01000000 is considered to be an error condition and is ignored. The configuration routine requires that the SDATA pin is held high, as shown in Figures 21 and 22, to prevent accidental writing to the register. The Configuration Register is only accessible prior to entering the External Serial Clock Mode. For I^2S mode, the user must set B6 to 0, and B7 to 1.

B1	B2	B3	B4	B5	B6	B7	B8

B1	**B2**	**B3**	Configuration Access Code
0	1	0	Access Allowed
All other Codes			Access Denied

B4	**B5**	Internal SCLK Mode only
Sets Internal SCLK/LRCK Ratio *		
0	0	SCLK/LRCK = 32
0	1	Reserved
1	0	SCLK/LRCK = 64
1	1	SCLK/LRCK = 128

* The Internal SCLK will be 48 Fs, if the MCLK/LRCK ratio is 384×.

B4	**B5**	External SCLK Mode only
Selects Data Sampling edge of SCLK		
1	0	Rising edge of SCLK
1	1	Falling edge of SCLK

B6	Left or Right Justified Data in relation to LRCK transition
0	Left Justified
1	Right Justified

B7	I^2S Data Format
0	Disabled
1	Enabled

B8	Sets the number of Bits
0	18 Bits
1	16 Bits

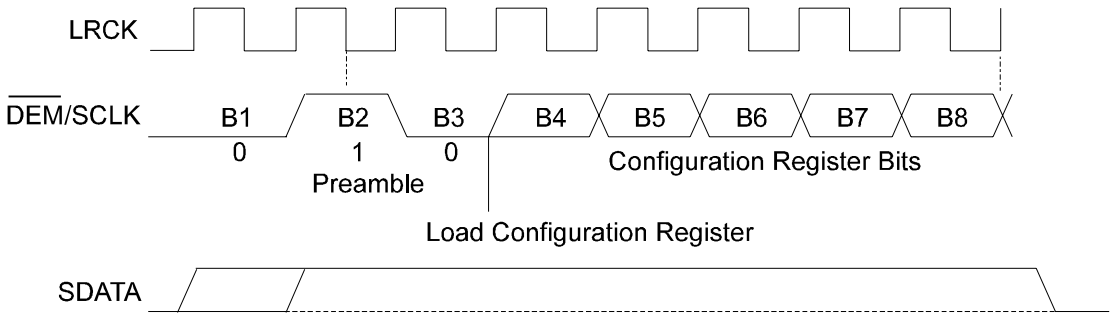


Figure 21. Configuration Operation

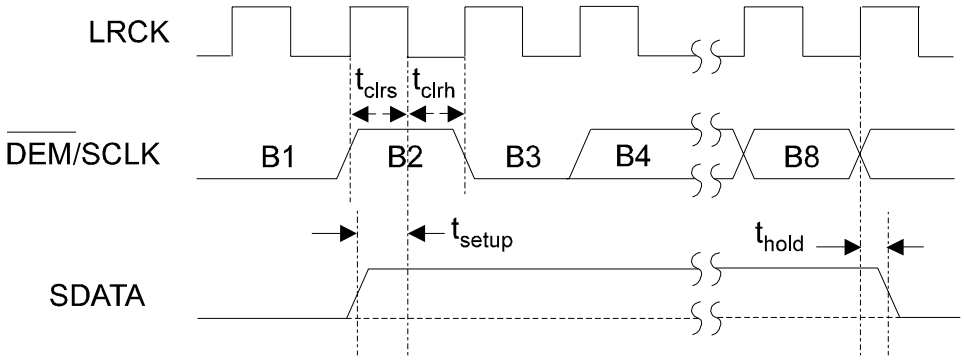


Figure 22. Configuration Timing

Parameter	Symbol	Min	Typ	Max	Units
DEM/SCLK TIMING					
DEM/SCLK valid to LRCK falling setup time	t_{clrs}	20	-	-	ns
LRCK falling to DEM/SCLK hold time	t_{clrh}	20	-	-	ns
SDATA setup time	t_{setup}	1	-	-	us
SDATA hold time	t_{hold}	1	-	-	us

Table 2. Configuration Timing Characteristics

REFERENCES

1)"An 18-Bit, 8-Pin Stereo Digital-to-Analog Converter" by J.J. Paulos, A.W. Krone, G.D Kamath, and S.T. Dupuie. Paper presented at the 97th Convention of the Audio Engineering Society, November 1994.

2)"How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

3)"Multiplier-Free Interpolation for Oversampled Digital-to-Analog Conversion" by Jeffrey W. Scott. Paper presented at the 92nd Convention of the Audio Engineering Society, March 1992.

4)"An 18-Bit Stereo D/A Converter With Integrated Digital and Analog Filters" by Nav S. Sooch, Jeffrey W. Scott. Paper presented at the 91st Convention of the Audio Engineering Society, November 1991.

5)CDB4330/31/33 Evaluation board Data Sheet; DS136DB2 MAR’96

PIN DESCRIPTIONS

SERIAL DATA INPUT	**SDATA**	1	8	**AOUTL**	ANALOG LEFT CHANNEL OUTPUT
DE-EMPHASIS / SCLK	**$\overline{\text{DEM}}$/SCLK**	2	7	**VA+**	ANALOG POWER
LEFT / RIGHT CLOCK	**LRCK**	3	6	**AGND**	ANALOG GROUND
MASTER CLOCK	**MCLK**	4	5	**AOUTR**	ANALOG RIGHT CHANNEL OUTPUT

Power Supply Connections

VA+ - Positive Analog Power, PIN 7.
Positive analog supply. Nominally +5V or +3V.

AGND - Analog Ground, PIN 6.
Analog ground reference.

Analog Outputs

AOUTL - Analog Left Channel Output, PIN 8.
Analog output for the left channel. Typically 3.7 Vpp for a full-scale input signal at VA+ = 5V and 1.85 Vpp at VA+ = 3V.

AOUTR - Analog Right Channel Output, PIN 5.
Analog output for the right channel. Typically 3.7 Vpp for a full-scale input signal at VA+ = 5V and 1.85 Vpp at VA+ = 3V.

Digital Inputs

MCLK - Master Clock Input, PIN 4.
The frequency must be 256×, 384× , or 512× the input sample rate (Fs).

LRCK - Left/Right Clock, PIN 3.
This input determines which channel is currently being input on the Audio Serial Data Input pin, SDATA.

SDATA - Audio Serial Data Input, PIN 1.
Two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4330, CS4331, and CS4333 via internal or external SCLK and the channel is determined by LRCK.

$\overline{\text{DEM}}$/SCLK - De-emphasis / External serial clock input , PIN 2.
A dual-purpose input used for de-emphasis filter control or external serial clock input.

PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)- The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range - The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFs signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

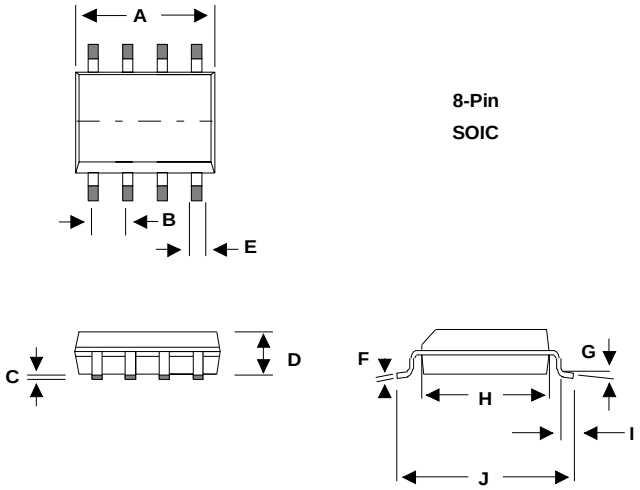
Gain Error - The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

ORDERING INFORMATION:

Model	Temperature	Package
CS4330-KS	-10 to +70°C	8-pin Plastic SOIC
CS4331-KS	-10 to +70°C	8-pin Plastic SOIC
CS4333-KS	-10 to +70°C	8-pin Plastic SOIC
CS4330-BS	-40 to +85°C	8-pin Plastic SOIC
CS4331-BS	-40 to +85°C	8-pin Plastic SOIC
CS4333-BS	-40 to +85°C	8-pin Plastic SOIC

PACKAGE DIMENSIONS



8-Pin SOIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.15	5.35	0.203	0.210
B	1.27	TYP	0.050	TYP
C	0	0.25	0	0.010
D	1.77	1.88	0.070	0.074
E	0.33	0.51	0.013	0.020
F	0.15	0.25	0.006	0.010
G	0°	8°	0°	8°
H	5.18	5.4	0.204	0.213
I	0.48	0.76	0.019	0.030
J	7.67	8.1	0.302	0.319

Note: The EIAJ package is not a standard JEDEC package size

• Notes •

A Cirrus Logic Company

CDB4330
CDB4331 CDB4333

Evaluation Board for CS4330 / CS4331 / CS4333

Features

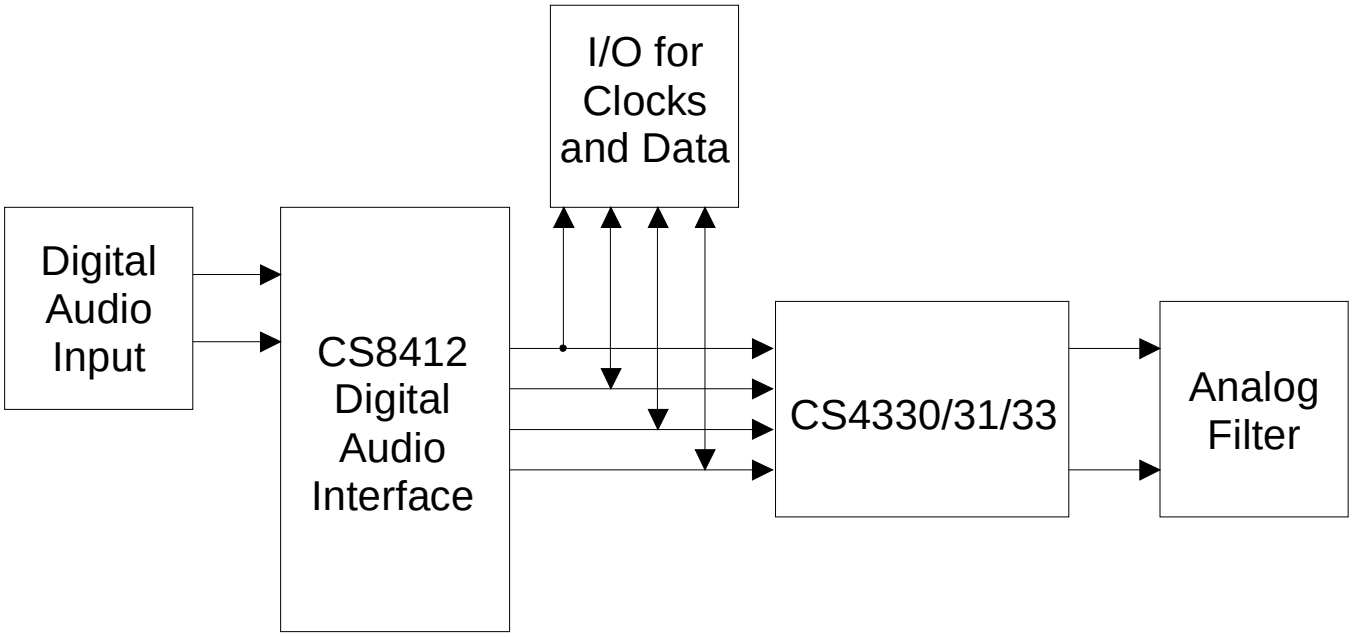
- Demonstrates recommended layout and grounding arrangements
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

General Description

The CDB4330/31/33 evaluation board is an excellent means for quickly evaluating the CS4330/31/33 18-bit, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source and a power supply. Analog outputs are provided via RCA connectors for both channels.

The CS8412 digital audio receiver I.C. provides the system timing necessary to operate the CS4330/31/33 and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION: CDB4330, CDB4331, CDB4333



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445 7581

CDB4330/31/33 System Overview

The CDB4330/31/33 evaluation board is an excellent means of quickly evaluating the CS4330/31/33. The CS8412 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4330/31/33 schematic has been partitioned into 5 schematics shown in Figures 2 through 7. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the the system diagram also includes the interconnections between the partitioned schematics.

CS4330/31/33 Digital to Analog Converter

A description of the CS4330/31/33 is included in the CS4330/31/33 data sheet.

CS8412 Digital Audio Receiver

The system receives and decodes the standard S/PDIF data format using a CS8412 Digital Audio Receiver, Figure 4. The outputs of the CS8412 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256Fs master clock. The operation of the CS8412 and a discussion of the digital audio interface are included in the 1994 *Crystal Semiconductor Audio Data Book.*

During normal operation, the CS8412 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper. This allows the CS8412 to decode and supply the de-emphasis bit from the digital audio interface for control of the CS4330/31/33 de-emphasis filter via pin 3, CC/F0, of the CS8412.

When the Error Information Switch is activated, the CS8412 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8412 data sheet. If the Error Information Switch is activated, and the CS4330/31/33 is in the internal serial clock mode, then it is likely that the de-emphasis control for the CS4330/31/33 will be erroneous and produce an incorrect audio output.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8412. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8412. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

The evaluation board has been designed such that the input can be either optical or coax, Figure 6. It is not necessary to select the active input. However, both inputs can not be driven simultaneously.

CS8412 Data Format

The CS8412 data format can be set with jumpers M0, M1, M2, and M3. These formats are shown in the CS8412 datasheet found in the 1994 *Crystal Semiconductor Audio Data Book*. The format selected must be compatible with the corresponding data format of the CS4330/31/33 shown in Figures 4-7 of the CS4330/31/33 datasheet. The default settings for M0-M3 on the evaluation board are given in Tables 2-4. The compatible data formats we have chosen for the CS8412 and CS4330/31/33 are:

CS8412 format 6;CS4330

CS8412 format 2;CS4331 (External SCLK only)

CS8412 format 5;CS4333 (External SCLK only)

Analog output filter

The recommended single pole filter required for the CS4330/31/33 has been combined with a unity gain output buffer (see Figure 2). The analog output filter uses a Motorola MC33202 single supply, dual op-amp. The low pass filter corner frequency is located at 2 Fs, or 88.2 kHz and is calculated by:

$$F = \frac{1}{(2\pi)\,(R_8 \,||\, R_9)\,(C_{29})}$$

$$F = \frac{1}{(2\pi)\,(15k\Omega \,||\, 6.65k\Omega)\,(390pF)} = 88.5\ \text{kHz}$$

Power Supply Circuitry

Power is supplied to the evaluation board by three binding posts (GND, +5V, +3V/+5V), See Figure 7. The +5V input supplies power to the +5 Volt digital circuitry (VD+5), while the +3V/+5V input supplies power to the Voltage Level Converter (VD+3/+5), and CS4330/31/33 (VA+3/+5) for evaluation in either +3 or +5 Volt mode. The op-amp is supplied from the analog supply (VA+) which can be derived from *either* the +5V post (VA+5) or the +3/+5V post (VA+3/+5) depending upon which Ferrite bead (L4 or L5) is installed. The evaluation board is configured with VA+ derived from VA+5 (L5 installed). To derive VA+ from the +3V/+5V post (VA+3/+5), remove the Ferrite bead at L5, and install it at L4.

Input/Output for Clocks and Data

The evaluation board has been designed to allow the interface to external systems via the 10-pin header, J1. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 5. The 74HC243 transceiver functions as an I/O buffer where the CLK SOURCE jumper determines if the transceiver operates as a transmitter or receiver.

The transceiver operates as a transmitter with the CLK SOURCE jumper in the 8412 position. LRCK, SDATA, and SCLK from the CS8412 will be available on J1. J22 must be in the 0 position and J23 must be in the 1 position for MCLK to be an output and to avoid bus contention on MCLK.

The transceiver operates as a receiver with the CLK SOURCE jumper in the EXTERNAL position. LRCK, SDATA and SCLK on J1 become inputs. The CS8412 must be removed from the evaluation board for operation in this mode.

There are 2 options for the source of MCLK in the External Clock Source mode. MCLK can be an input with J23 in the 1 position and J22 in the 0 position. However, the recommended mode of operation is to generate MCLK on the evaluation board. MCLK becomes an output with LRCK, SCLK and SDATA inputs. This technique insures that the CS4330/31/33 receives a jitter free clock to maximize performance. This can be accomplished by installing a crystal oscillator into U5, see Figure 4 (the socket for U5 is located within the footprint for the CS8412) and placing J22 in the 1 position and J23 in the 0 position.

Grounding and Power Supply Decoupling

The CS4330/31/33 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 shows the recommended power arrangements. The CS4330/31/33 is positioned over the analog ground plane near the digital/analog ground plane split. These ground planes are connected elsewhere on the board. This layout technique is used to minimizing digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the CS4330/31/33 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	input	(VD+5V) for CS8412 and digital section
	input	(VA+) for Analog output filter op-amp (configured for +5V)
+3/+5V	input	(VD+3/+5V) for Voltage Level Converter
	input	(VA+3/+5V) for CS4330/31/33
GND	input	ground connection from power supply
Digital Input	input	digital audio interface input via coax
Optical Input	input	digital audio interface input via optical
MCLK, SCLK, LRCK	input/output	I/O for master, serial, and left/right clocks
SDATA	input/output	I/O for serial data
AOUTL	output	left channel analog output
AOUTR	output	right channel analog output

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	selects channel for CS8412 channel status information	L R	See CS8412 data sheet for details
Clock Select	Selects source of system clocks and data	*8412 EXT	CS8412 clock/data source External clock/data source
J22 J23	Selects MCLK as Input or Output	*0 *1	See ***Input/Output for Clocks and Data*** section of text
M0 M1 M2 M3	CS8412 mode select	*Low *High *High *Low	See CS8412 data sheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8412	Selects source of de-emphasis control	*Low High	CS8412 de-emphasis De-emphasis input static high

* Default setting from factory

Table 2. CDB4330 Jumper Selectable Options

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	selects channel for CS8412 channel status information	L R	See CS8412 data sheet for details
Clock Select	Selects source of system clocks and data	*8412 EXT	CS8412 clock/data source External clock/data source
J22 J23	Selects MCLK as Input or Output	*0 *1	See ***Input/Output for Clocks and Data*** section of text
M0 M1 M2 M3	CS8412 mode select	*Low *High *Low *Low	See CS8412 data sheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode (Note 1) External SCLK Mode (Note 1)
DEM_8412	Selects source of de-emphasis control	*Low High	CS8412 de-emphasis De-emphasis input static high

* Default setting from factory

Note 1. The CS8412 output data format requires the CS4331 be in the External SCLK Mode

Table 3. CDB4331 Jumper Selectable Options

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	selects channel for CS8412 channel status information	L R	See CS8412 data sheet for details
Clock Select	Selects source of system clocks and data	*8412 EXT	CS8412 clock/data source External clock/data source
J22 J23	Selects MCLK as Input or Output	*0 *1	See ***Input/Output for Clocks and Data*** section of text
M0 M1 M2 M3	CS8412 mode select	*High *Low *High *Low	See CS8412 data sheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode (Note 1) External SCLK Mode (Note 1)
DEM_8412	Selects source of de-emphasis control	*Low High	CS8412 de-emphasis De-emphasis input static high

* Default setting from factory

Note 1. The CS8412 output data format requires the CS4333 be in the External SCLK Mode

Table 4. CDB4333 Jumper Selectable Options

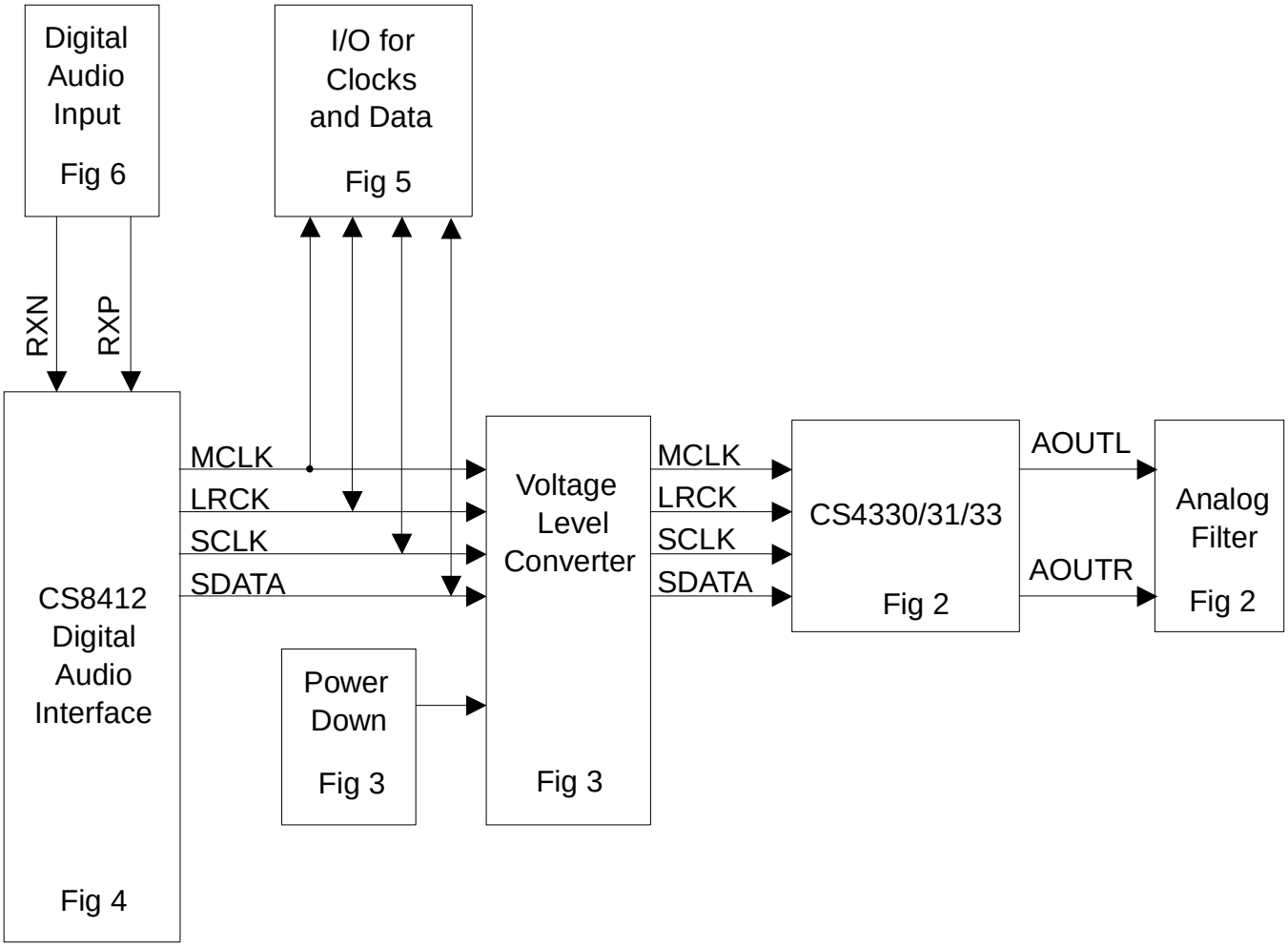


Figure 1. System Block Diagram and Signal Flow

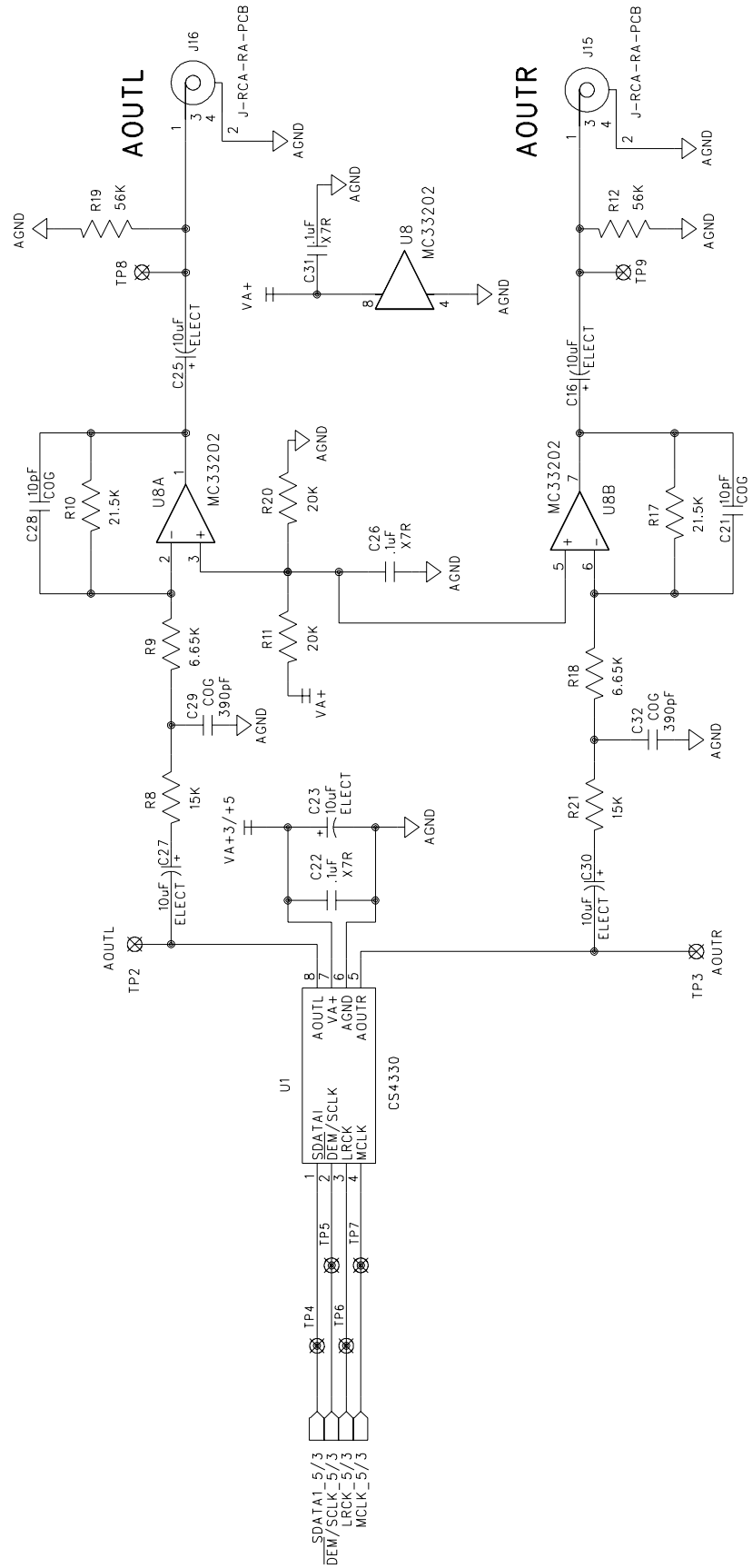


Figure 2. CS4330/31/33 and Connections

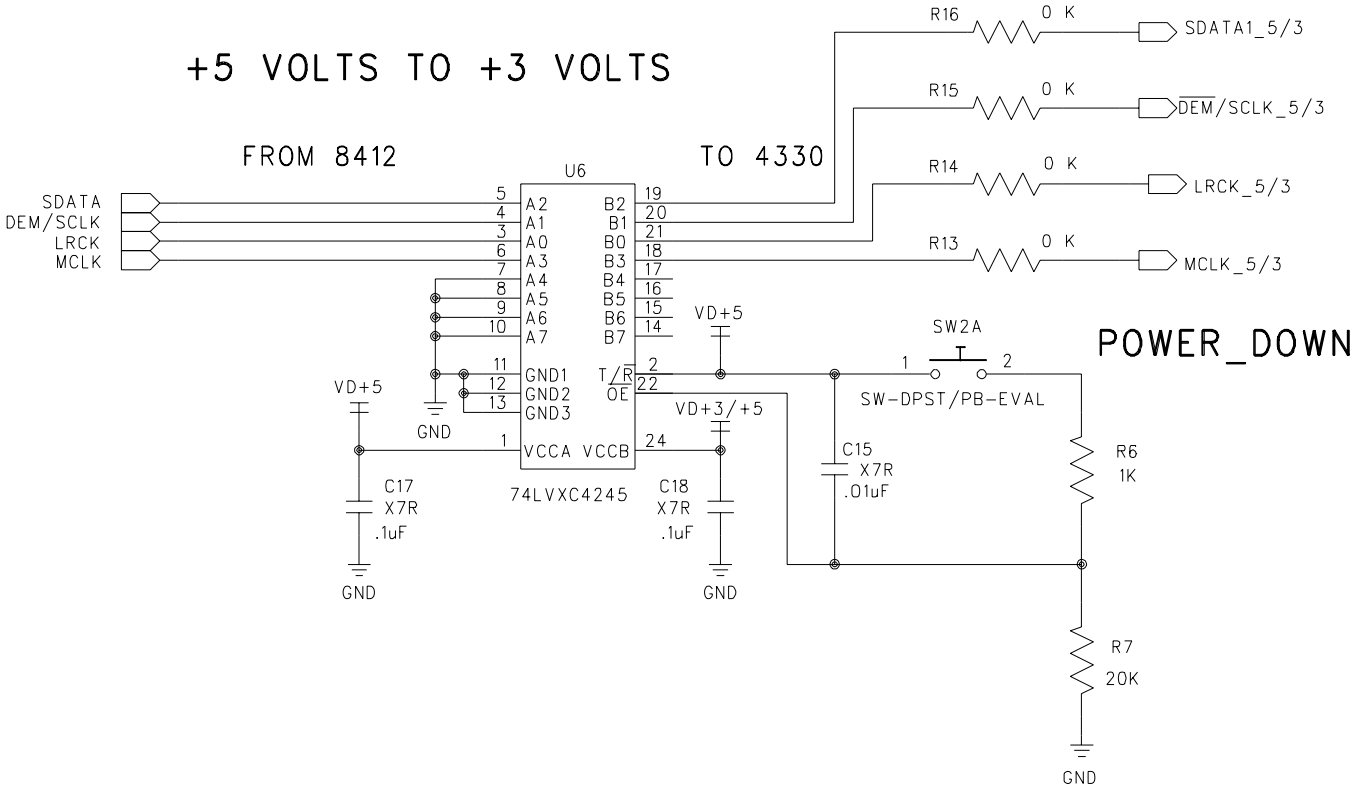
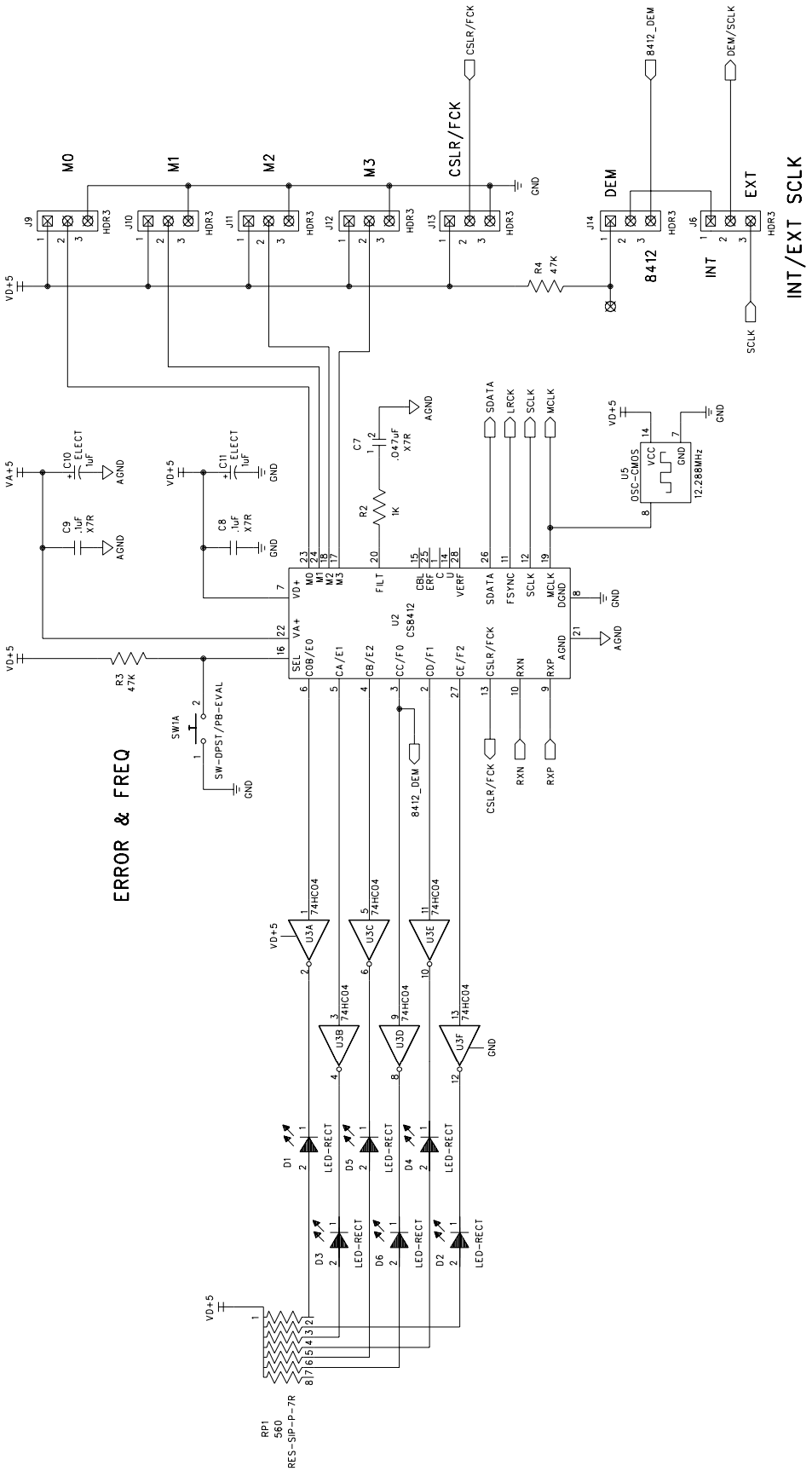


Figure 3. Voltage Level Conversion and Power Down Circuitry



NOTE: U2 and U5 cannot be installed simultaneously

Figure 4. CS8412 Digital Audio Receiver Connections

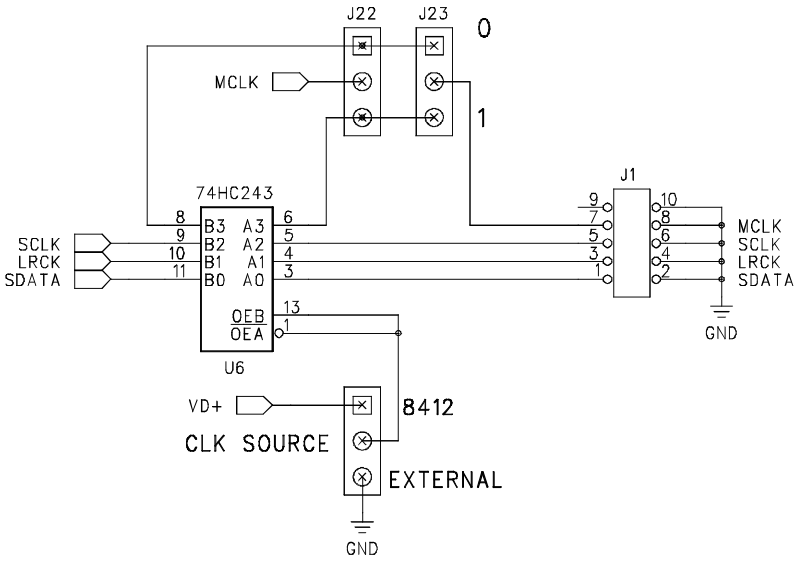


Figure 5. I/O Interface for Clocks and Data

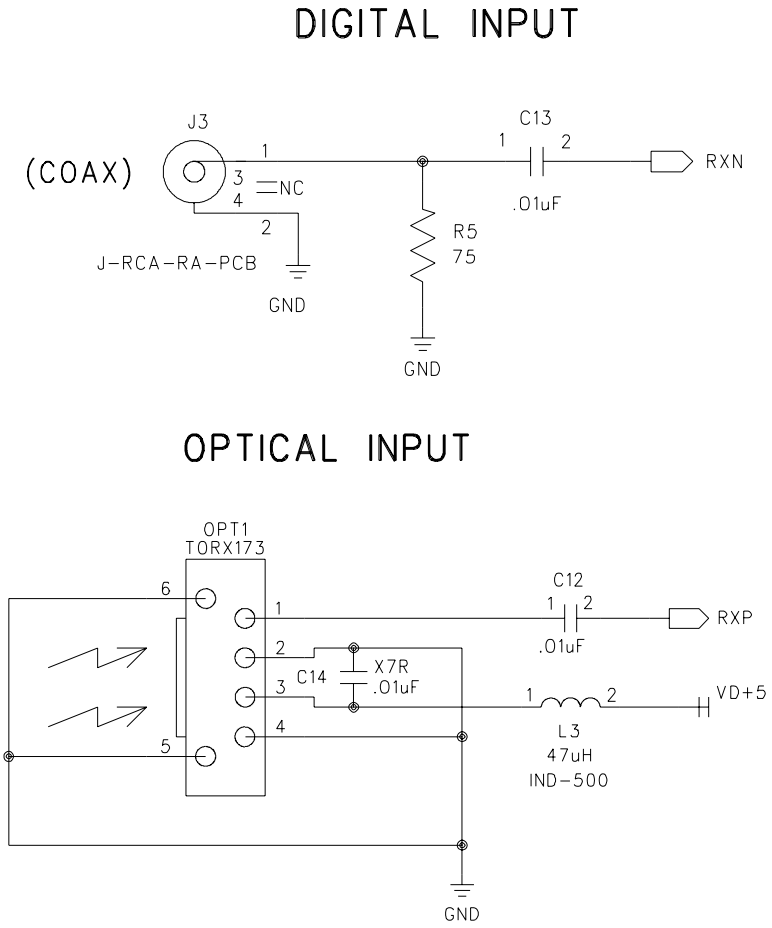


Figure 6. Digital Audio Input

Optical Toshiba part TORX173 available through Insight Electronics

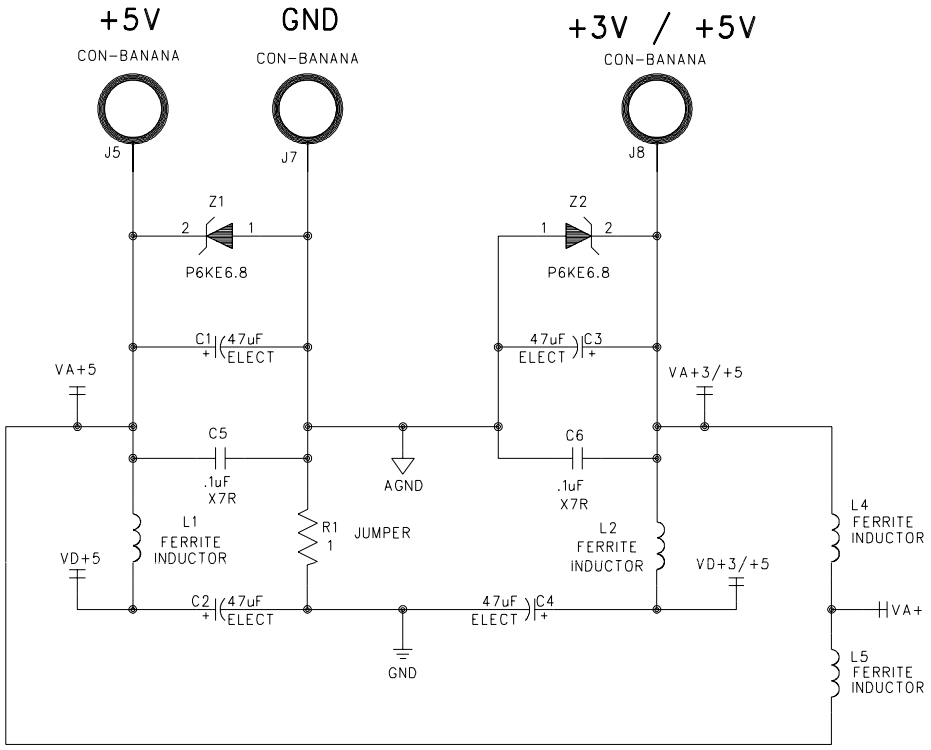


Figure 7. Power Supply

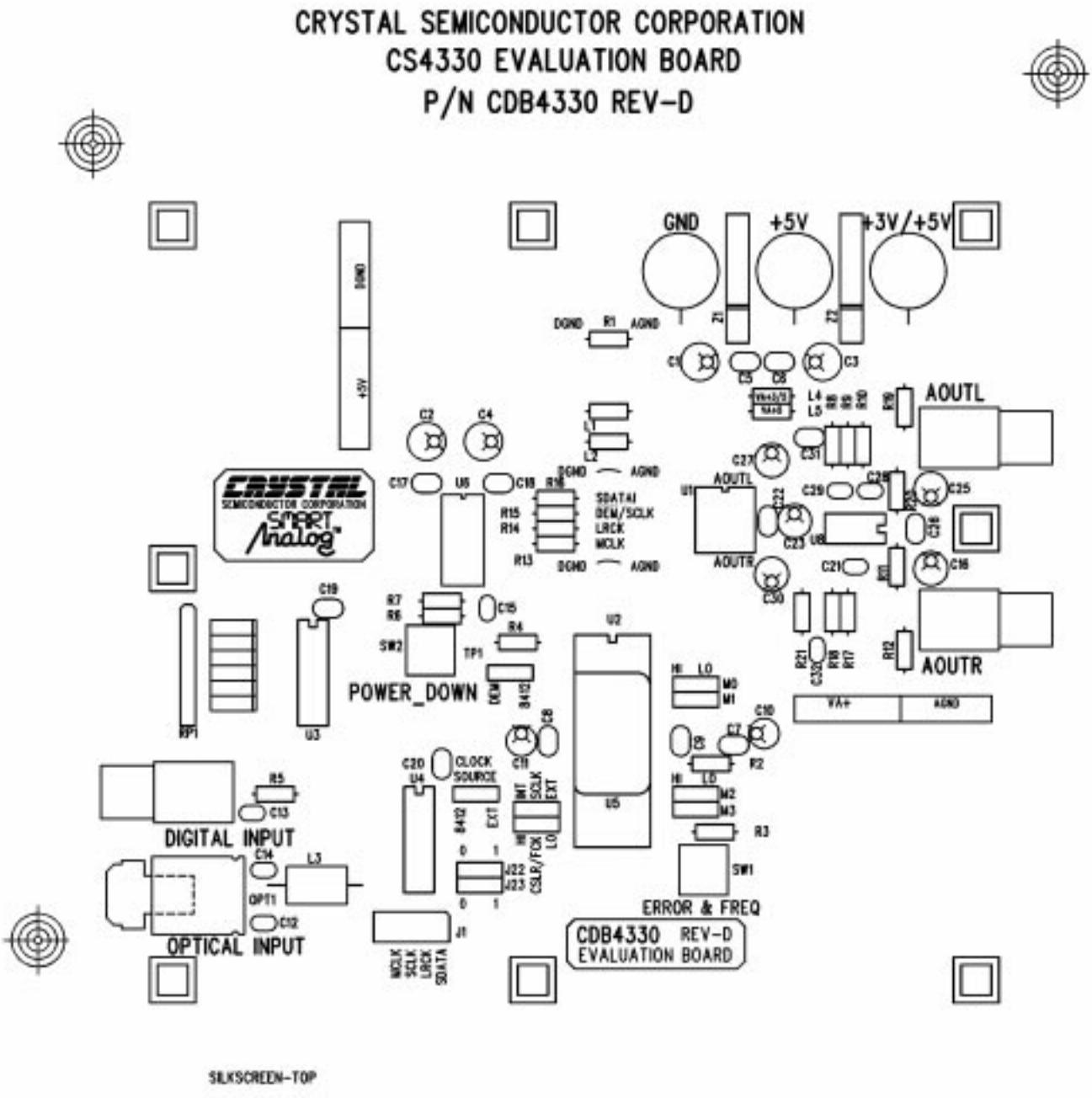


Figure 8. CDB4330/31/33 Component Side Silkscreen

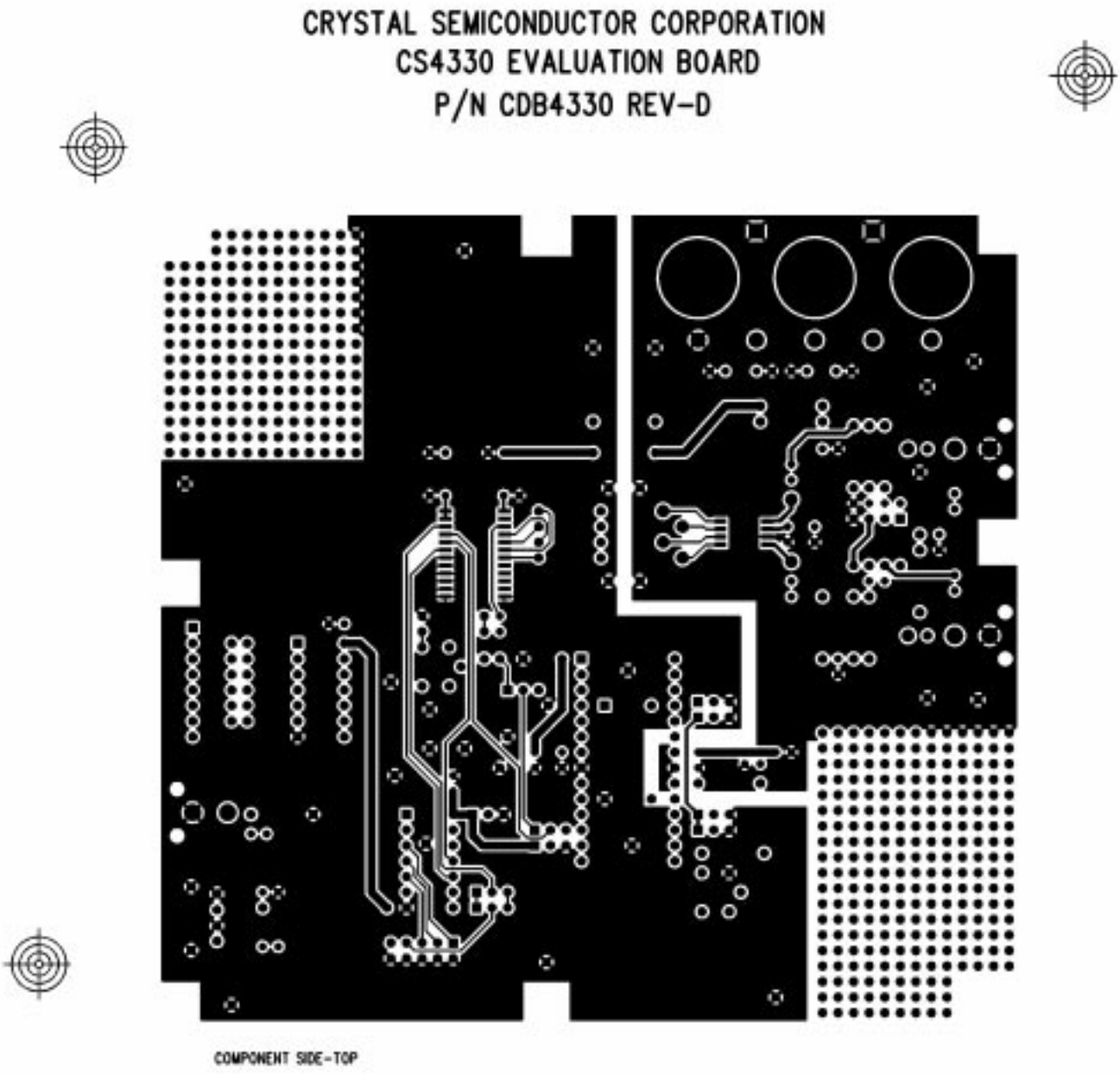


Figure 9. CDB4330/31/33 Component Side (top)

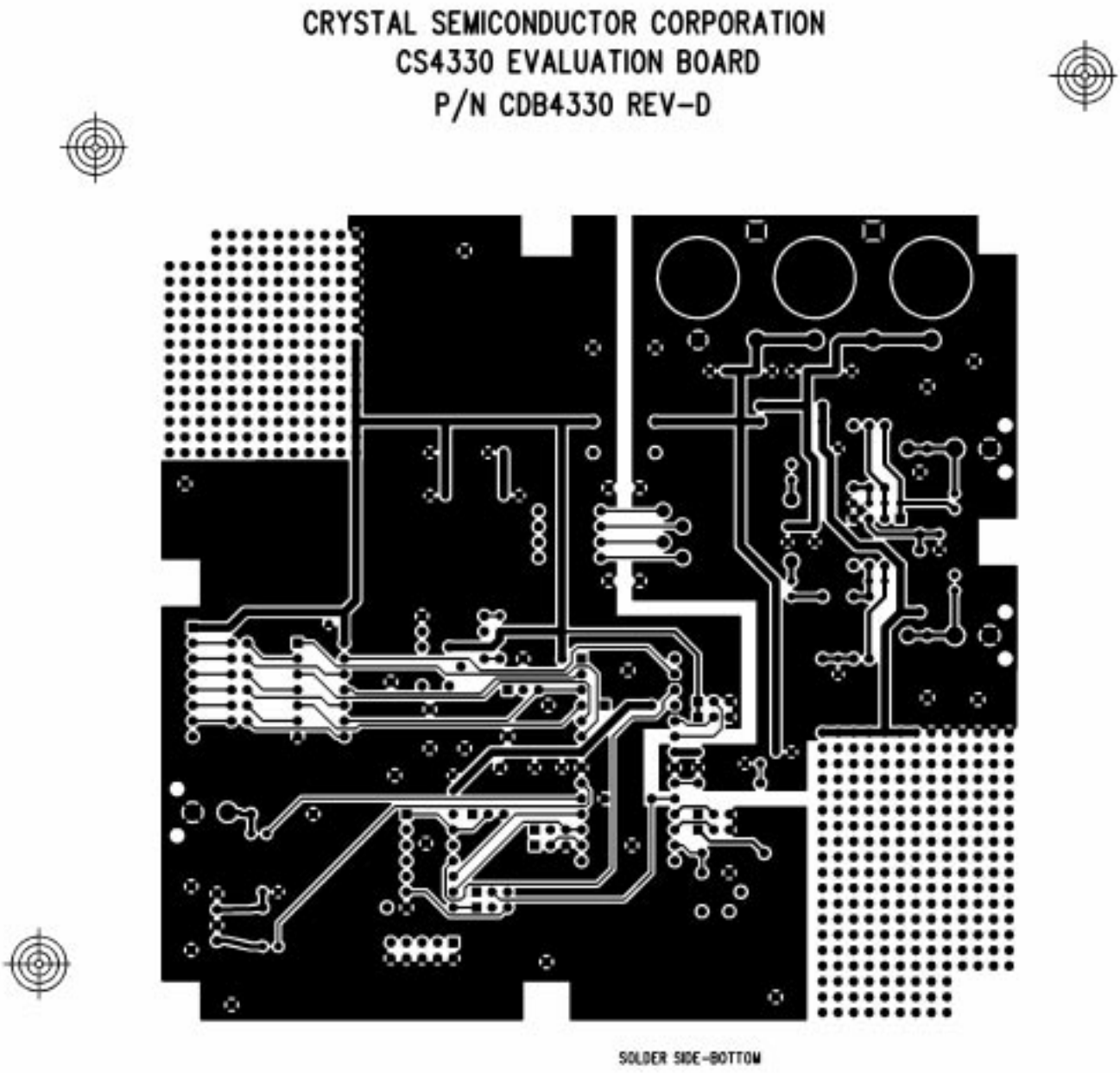


Figure 10. CDB4330/31/33 Solder Side (bottom)

• Notes •