

NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
 contact our Technical Support Center at
 1-888-INTERSIL or www.intersil.com/tsc

January 16, 2014

FN6154.6

39µA Micropower Precision Rail-to-Rail Input-Output (RRIO) Low Input Bias Current Op Amp

The ISL28156 is a micropower precision operational amplifier optimized for single supply operation at 5V and can be operated down to 2.4V.

This device features an Input Range Enhancement Circuit (IREC), which enables it to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.5V above a 5.0V supply (0.25V for a 2.5V supply) and to within 10mV from ground. The output operation is rail-to-rail.

The 1/f corner of the voltage noise spectrum is at 1kHz. This results in low frequency noise performance, which can only be found on devices with an order of magnitude higher than the supply current.

The ISL28156 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Ordering Information

PART NUMBER (Note 2)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL28156FHZ-T7 (Note 1)	GABV (Note3)	6 Ld SOT-23	P6.064A
ISL28156FBZ	28156 FBZ	8 Ld SOIC	M8.15E
ISL28156FBZ-T7 (Note 1)	28156 FBZ	8 Ld SOIC	M8.15E
ISL28156EVAL1Z	Evaluation Board		

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. The part marking is located on the bottom of the parts.

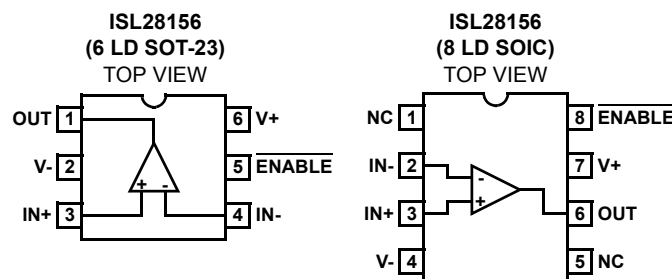
Features

- 39µA typical supply current
- 5nA max input bias current
- 250kHz gain bandwidth product ($A_V = 1$)
- 2.4V to 5.5V single supply voltage range
- Rail-to-rail input and output
- Enable pin
- Pb-free (RoHS compliant)

Applications

- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

Pinouts



Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

Supply Voltage	5.5V
Supply Turn On Voltage Slew Rate	1V/ μs
Differential Input Current	5mA
Differential Input Voltage	0.5V
Input Voltage	V- - 0.5V to V+ + 0.5V
ESD Rating	
Human Body Model	3kV
Machine Model	300V

Thermal Information

Thermal Resistance	θ_{JA} ($^\circ\text{C}/\text{W}$)
6 Ld SOT-23 Package (Note 4)	230
6 Ld SOIC Package	110
Output Short-Circuit Duration	Indefinite
Ambient Operating Temperature Range	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Operating Junction Temperature	+125 $^\circ\text{C}$
Pb-Free Reflow Profile	see link below

<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_+ = 5\text{V}$, $V_- = 0\text{V}$, $V_{CM} = 2.5\text{V}$, $T_A = +25^\circ\text{C}$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40 $^\circ\text{C}$ to +125 $^\circ\text{C}$.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V_{OS}	Input Offset Voltage	8 Ld SOIC	-120	-7	120	μV
			-200		250	
		6 Ld SOT-23	-400	-7	400	μV
			-450		450	
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drive vs Temperature			1.5		$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		-1.5	0.34	1.2	nA
			-5		2.5	
I_B	Input Bias Current		-2	1.14	5	nA
			-3.5		5	
E_N	Input Noise Voltage Density	$F_O = 1\text{kHz}$		46		$\text{nV}/\sqrt{\text{Hz}}$
I_N	Input Noise Current Density	$F_O = 1\text{kHz}$		0.14		$\text{pA}/\sqrt{\text{Hz}}$
CMIR	Input Common-Mode Voltage Range		0		5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0\text{V}$ to 5V	80	110		dB
			75			
PSRR	Power Supply Rejection Ratio	$V_S = 2.4\text{V}$ to 5V	90	104		dB
			75			
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.5\text{V}$ to 4.5V, $R_L = 100\text{k}\Omega$	200	412		V/mV
			175			
		$V_O = 0.5\text{V}$ to 4.5V, $R_L = 1\text{k}\Omega$	35	70		V/mV
			30			
V_{OUT}	Maximum Output Voltage Swing	Output low, $R_L = 100\text{k}\Omega$		3	6	mV
					8	
		Output low, $R_L = 1\text{k}\Omega$		130	150	mV
					200	
	Maximum Output Voltage Swing	Output high, $R_L = 100\text{k}\Omega$	4.992	4.985		V
			4.99			
		Output high, $R_L = 1\text{k}\Omega$	4.85	4.88		V
			4.8			

Electrical Specifications $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $T_A = +25^\circ C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+125^\circ C$.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
SR	Slew Rate			0.05		V/ μs
GBW	Gain Bandwidth Product	$A_V = 1$		250		kHz
$I_{S,ON}$	Supply Current, Enabled		29	39	47	μA
			18		56	
$I_{S,OFF}$	Supply Current, Disabled			10	14	μA
					16	
I_{O+}	Short-Circuit Output Current	$R_L = 10\Omega$	28	31		mA
			23			
I_{O-}	Short-Circuit Output Current	$R_L = 10\Omega$	24	26		mA
			18			
V_{SUPPLY}	Supply Operating Range	Guaranteed by PSRR test	2.4		5	V
V_{ENH}	Enable Pin High Level		2			V
V_{ENL}	Enable Pin Low Level				0.8	V
I_{ENH}	Enable Pin Input Current	$V_{EN} = 5V$		1	1.2	μA
					1.2	
I_{ENL}	Enable Pin Input Current	$V_{EN} = 0V$		16	25	nA
					30	
t_{EN}	Enable to Output On-state Delay Time	$V_{OUT} = 1V$ (enable state); $V_{EN} = \text{High-to-Low}$		10.8		μs
$t_{\overline{EN}}$	Enable to Output Off-state Delay Time	$V_{OUT} = 0V$ (disabled state); $V_{EN} = \text{Low-to-High}$		0.1		μs

NOTE:

5. Parts are 100% tested at $+25^\circ C$. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

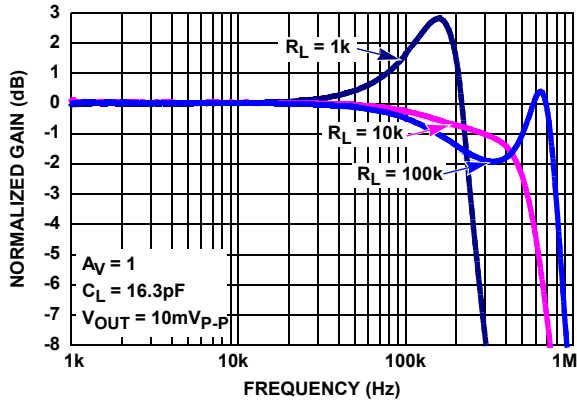
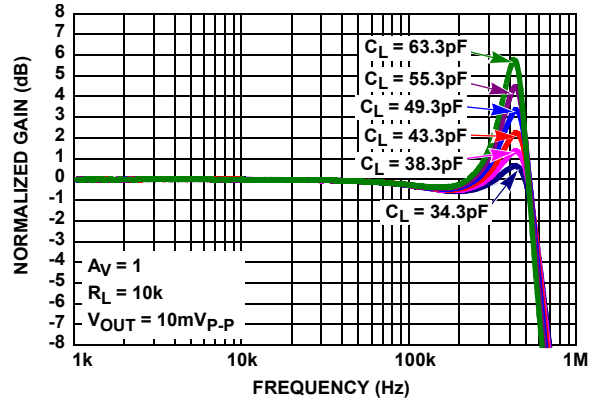
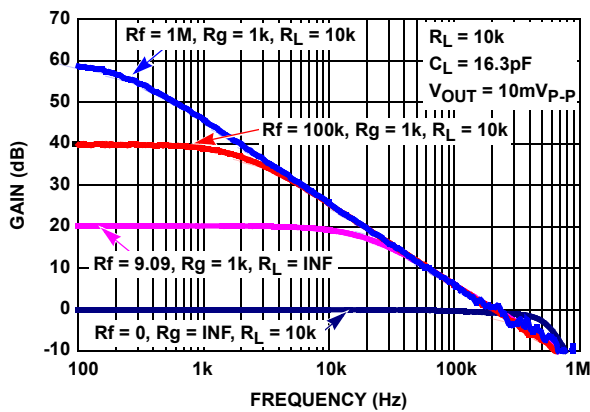
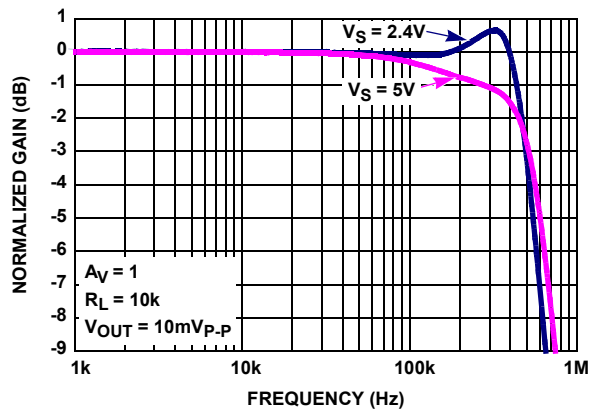
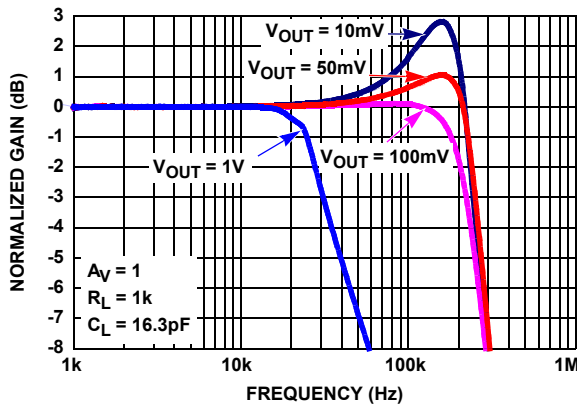
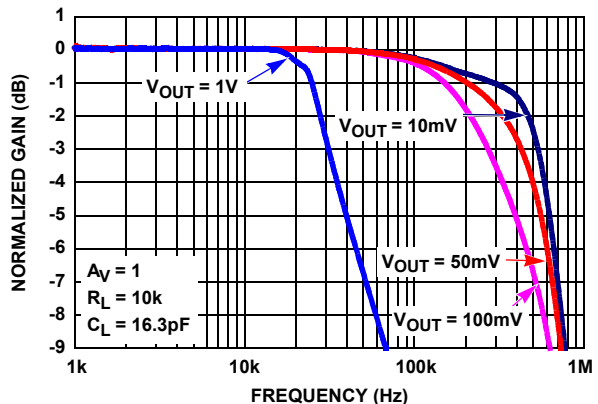
FIGURE 1. GAIN vs FREQUENCY vs R_L FIGURE 2. GAIN vs FREQUENCY vs C_L 

FIGURE 3. CLOSED LOOP GAIN vs FREQUENCY

FIGURE 4. GAIN vs FREQUENCY vs V_S FIGURE 5. GAIN vs FREQUENCY vs V_{OUT} FIGURE 6. GAIN vs FREQUENCY vs V_{OUT}

Typical Performance Curves (Continued)

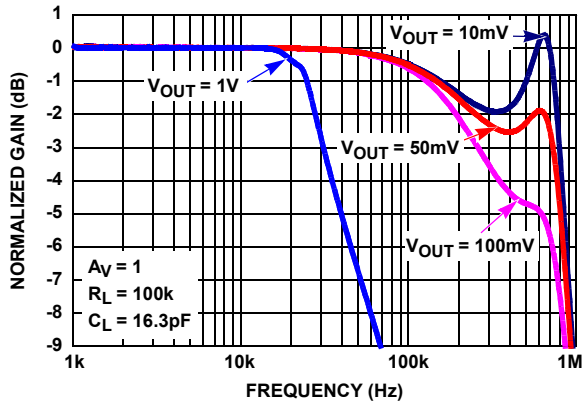
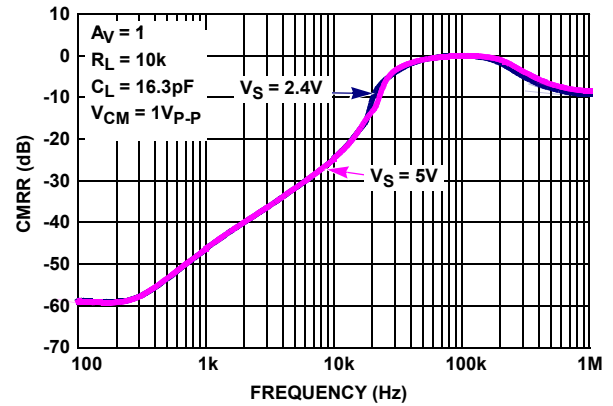
FIGURE 7. GAIN vs FREQUENCY vs V_{OUT} 

FIGURE 8. CMRR vs FREQUENCY

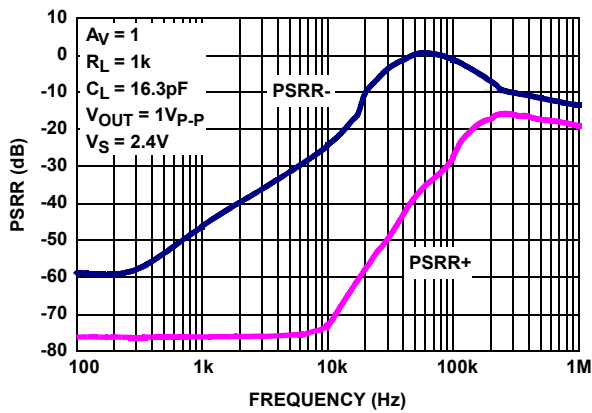
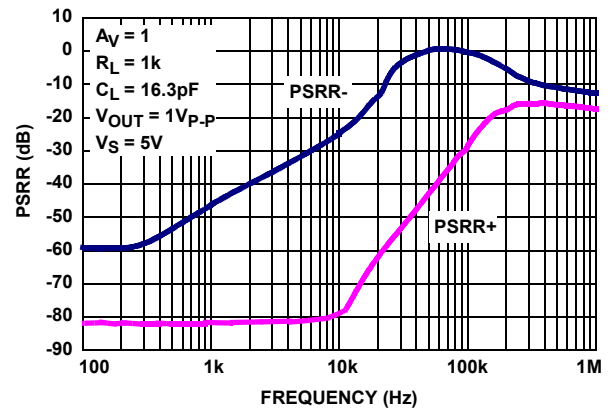
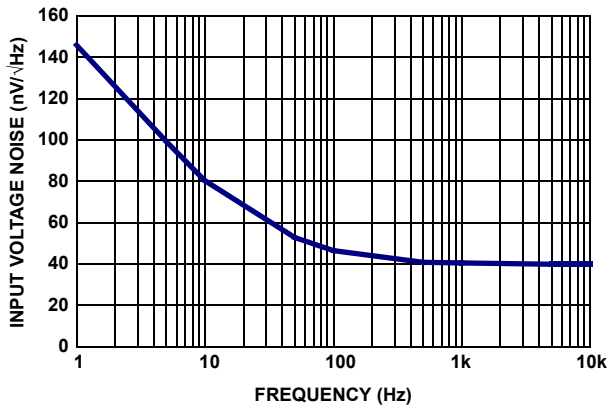
FIGURE 9. PSRR vs FREQUENCY, $V_S = 2.4V$ FIGURE 10. PSRR vs FREQUENCY, $V_S = 5V$ 

FIGURE 11. INPUT VOLTAGE NOISE vs FREQUENCY

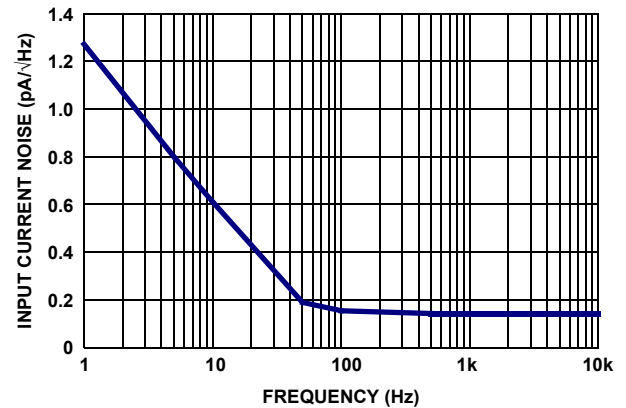


FIGURE 12. INPUT CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

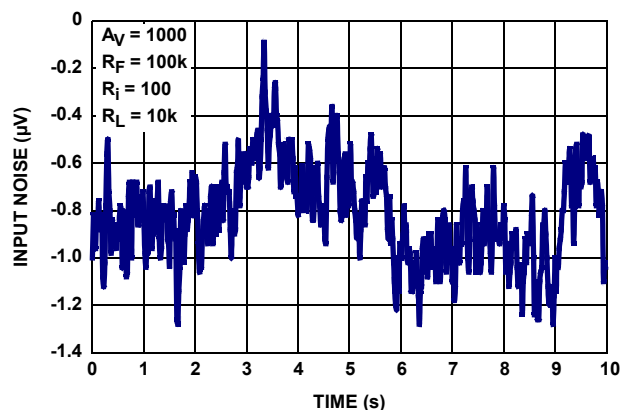


FIGURE 13. 1Hz TO 10Hz INPUT NOISE

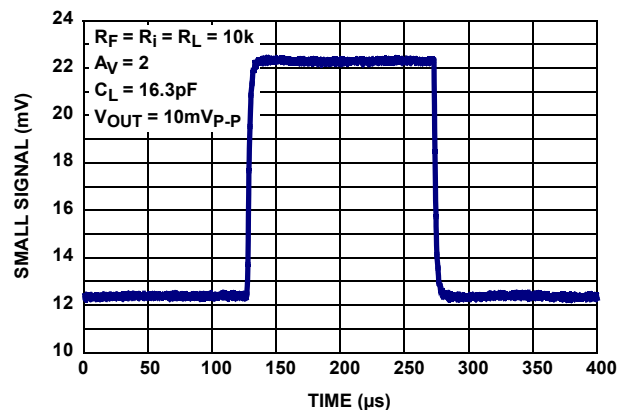


FIGURE 14. SMALL SIGNAL STEP RESPONSE

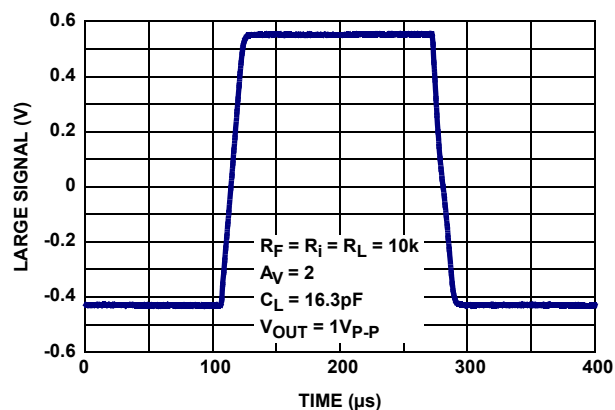


FIGURE 15. LARGE SIGNAL STEP RESPONSE

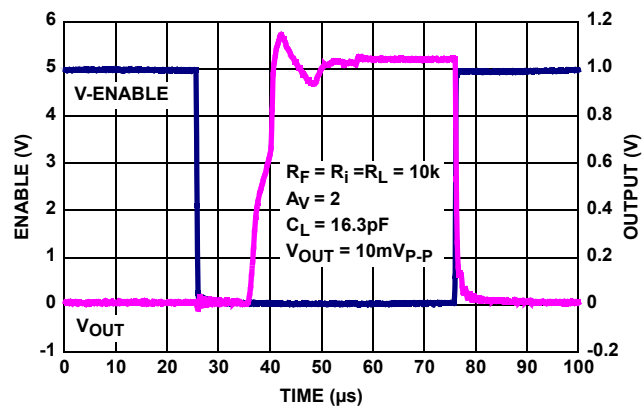
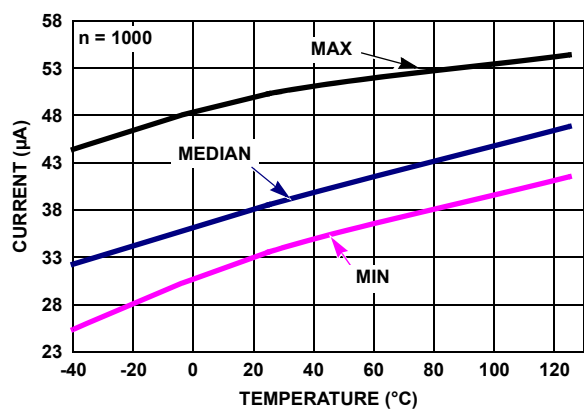
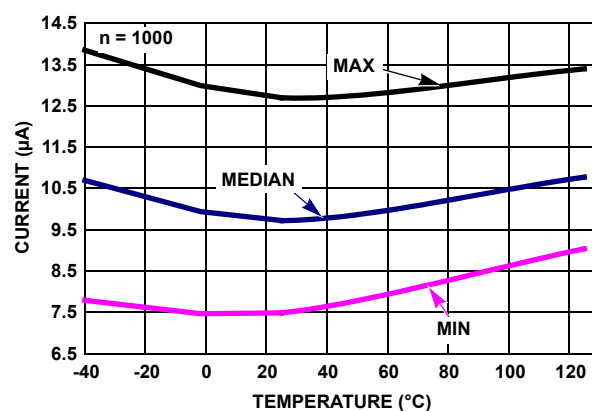
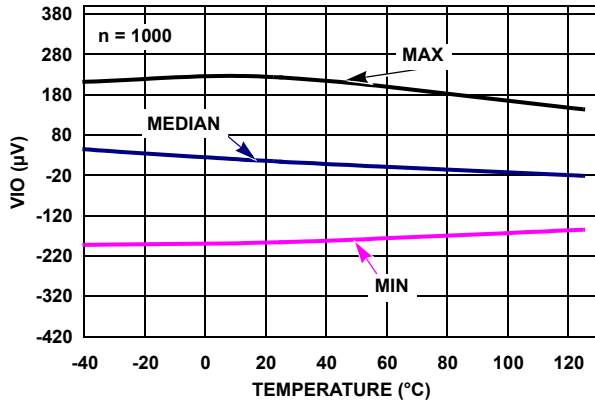
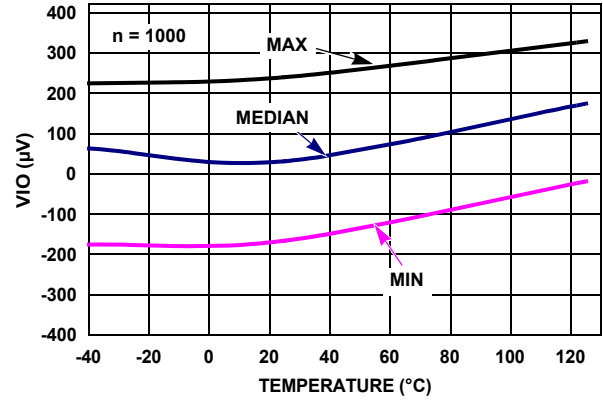
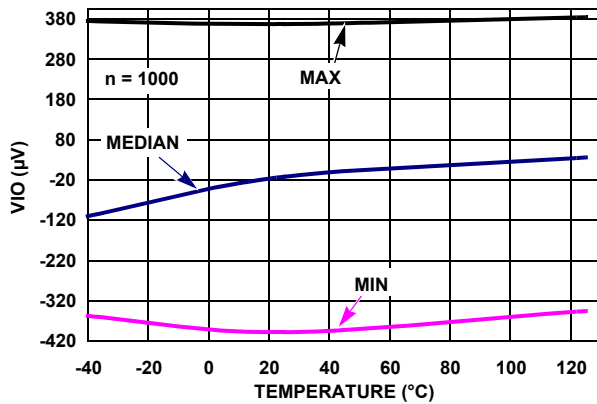
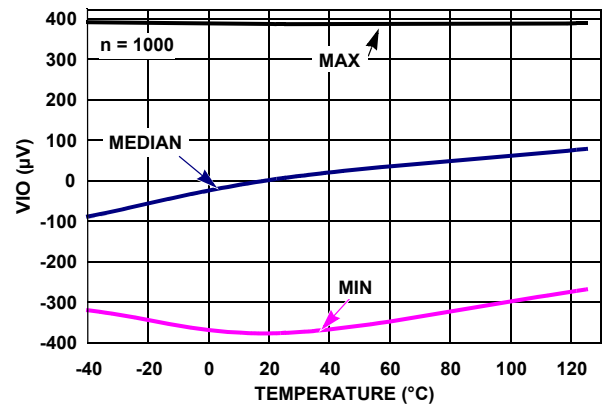
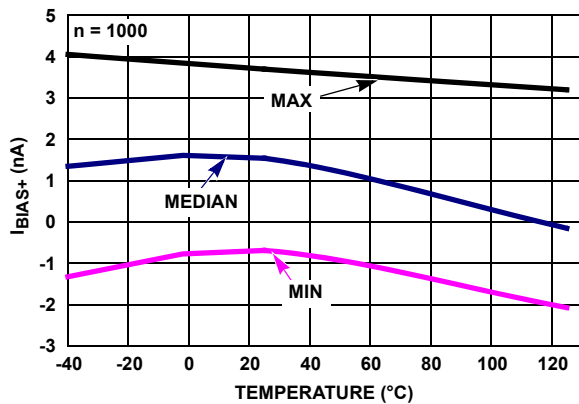
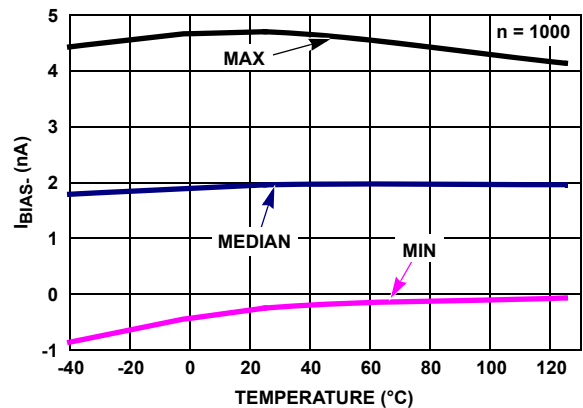


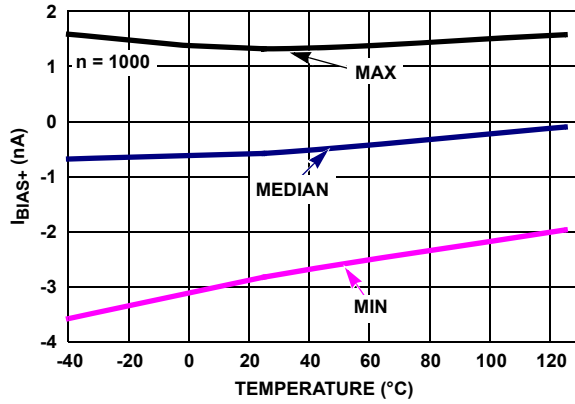
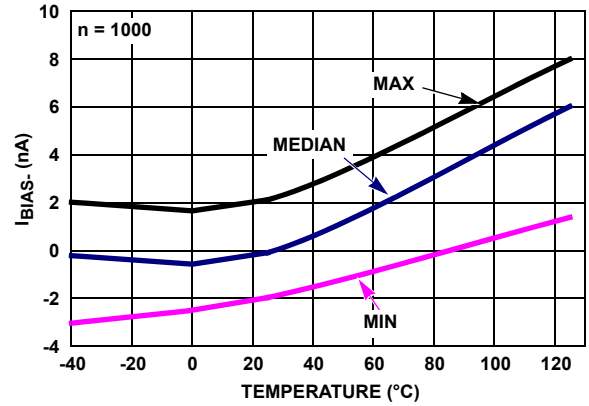
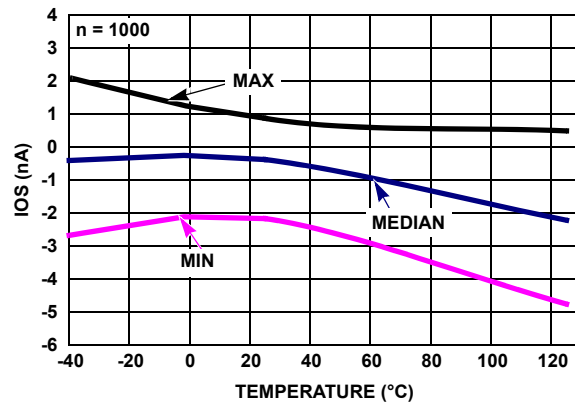
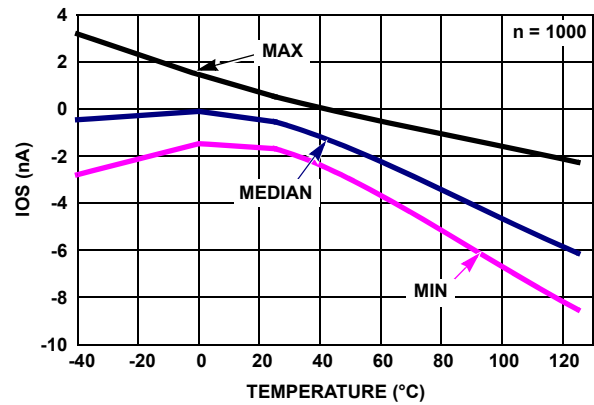
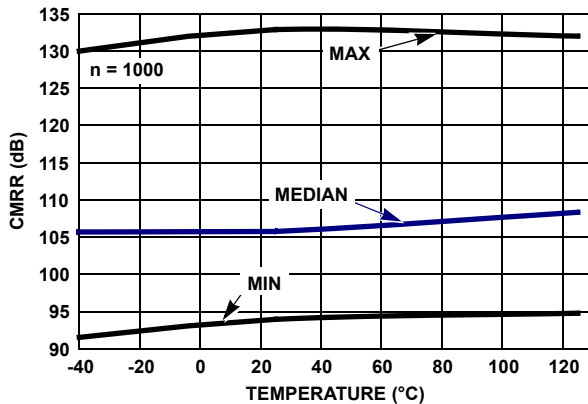
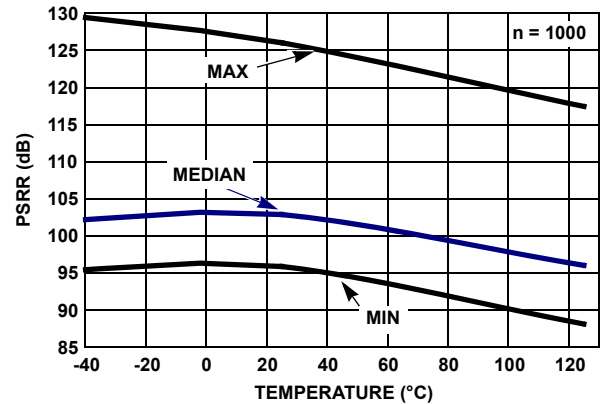
FIGURE 16. ENABLE TO OUTPUT DELAY

FIGURE 17. SUPPLY CURRENT ENABLED vs TEMPERATURE
 $V_S = \pm 2.5\text{V}$ FIGURE 18. SUPPLY CURRENT DISABLED vs TEMPERATURE
 $V_S = \pm 2.5\text{V}$

Typical Performance Curves (Continued)

FIGURE 19. VIO SO8 PACKAGE vs TEMPERATURE $V_S = \pm 2.5V$ FIGURE 20. VIO SO8 PACKAGE vs TEMPERATURE $V_S = \pm 1.2V$ FIGURE 21. VIO SOT-23 PACKAGE vs TEMPERATURE $V_S = \pm 2.5V$ FIGURE 22. VIO SOT-23 PACKAGE vs TEMPERATURE $V_S = \pm 1.2V$ FIGURE 23. I_{BIAS+} vs TEMPERATURE $V_S = \pm 2.5V$ FIGURE 24. I_{BIAS-} vs TEMPERATURE $V_S = \pm 2.5V$

Typical Performance Curves (Continued)

FIGURE 25. I_{BIAS+} vs TEMPERATURE $V_S = \pm 1.5V$ FIGURE 26. I_{BIAS-} vs TEMPERATURE $V_S = \pm 1.2V$ FIGURE 27. I_{OS} vs TEMPERATURE $V_S = \pm 2.5V$ FIGURE 28. I_{OS} vs TEMPERATURE $V_S = \pm 1.5V$ FIGURE 29. CMRR vs TEMPERATURE $V+ = \pm 2.5V, \pm 1.5V$ FIGURE 30. PSRR vs TEMPERATURE $\pm 1.2V$ to $\pm 2.5V$

Typical Performance Curves (Continued)

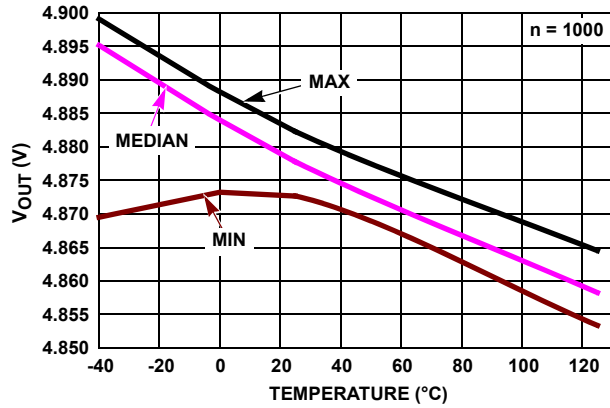


FIGURE 31. V_{OUT} HIGH vs TEMPERATURE $V_S = \pm 2.5V$, $R_L = 1k$

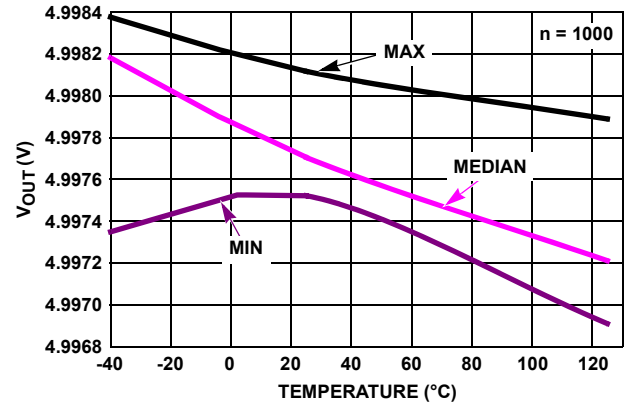


FIGURE 32. V_{OUT} HIGH $V_S = \pm 2.5V$, $R_L = 100k$

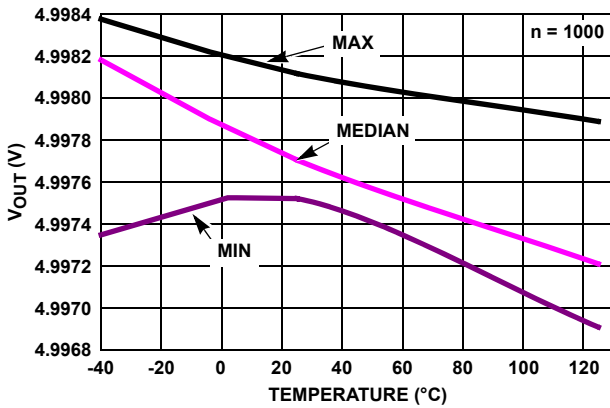


FIGURE 33. V_{OUT} LOW $V_S = \pm 2.5V$, $R_L = 1k$

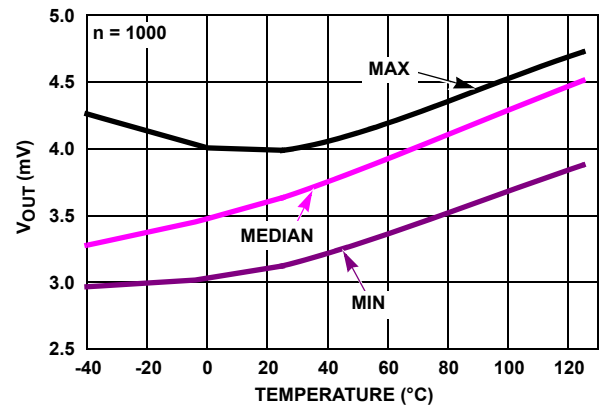
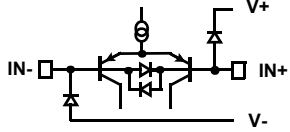
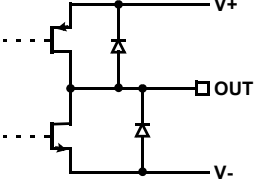
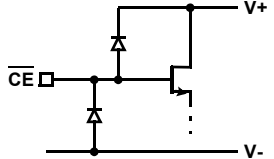


FIGURE 34. V_{OUT} LOW $V_S = \pm 2.5V$, $R_L = 100k$

Pin Descriptions

ISL28156 (6 Ld SOT-23)	ISL28156 (8 Ld SOIC)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
	1, 5	NC	Not connected	
4	2	IN-	Inverting input	 Circuit 1
3	3	IN+	Non-inverting input	(See Circuit 1)
2	4	V-	Negative supply	
1	6	OUT	Output	 Circuit 2
6	7	V+	Positive supply	
5	8	ENABLE	Chip enable	 Circuit 3

Applications Information

Introduction

The ISL28156 is a BiMOS rail-to-rail input, output (RRIO) operational amplifier with an enable feature. The device is designed to operate from single supply (2.4V to 5.0V) or dual supplies ($\pm 1.2V$ to $\pm 2.5V$) while drawing only 39 μA of supply current. This combination of low power and precision performance makes this device suitable for a variety of low power applications including battery powered systems.

Rail-to-Rail Input/Output

This device features bi-polar inputs, which have an input common mode range that extends up to 0.5V beyond the V+ rail, and to within 10mV of the V- rail. The CMOS outputs typically swing to within about 4mV of the supply rails with a 100k Ω load. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA (Figure 35).

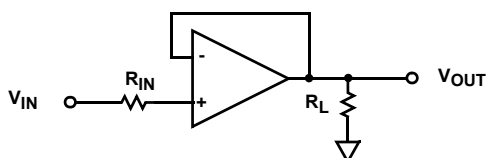


FIGURE 35. INPUT CURRENT LIMITING

Enable/Disable Feature

The ISL28156 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10 μA . By disabling the part, multiple ISL28156 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together.

Current Limiting

This device has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \quad (EQ. 1)$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})

PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad (EQ. 2)$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9001 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

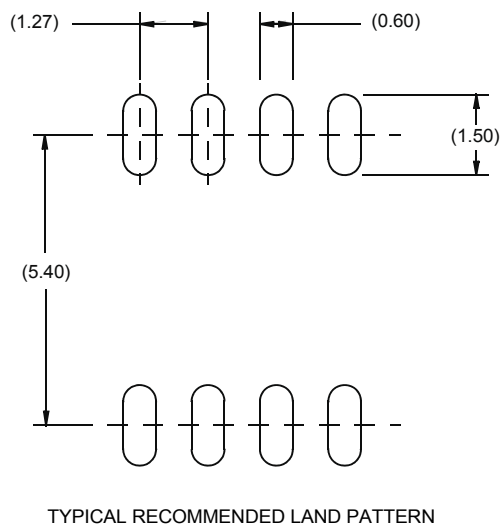
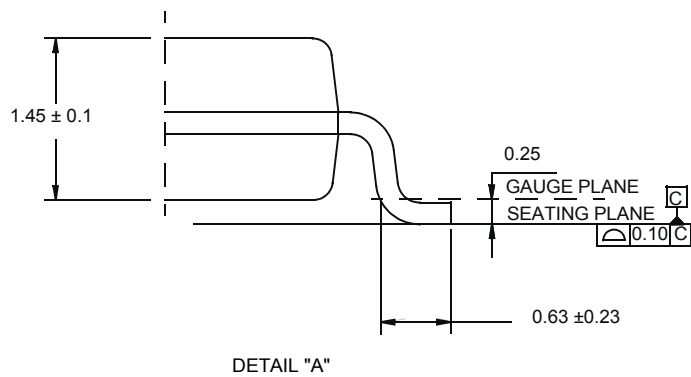
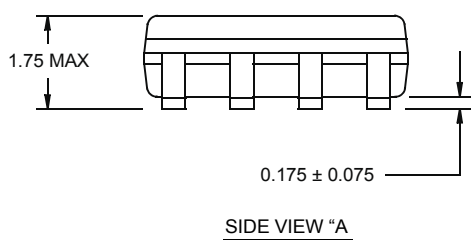
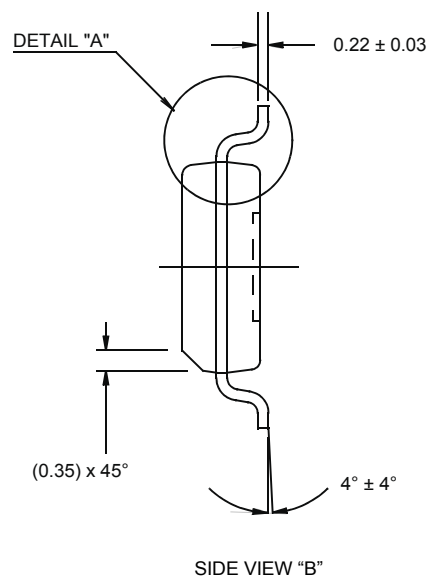
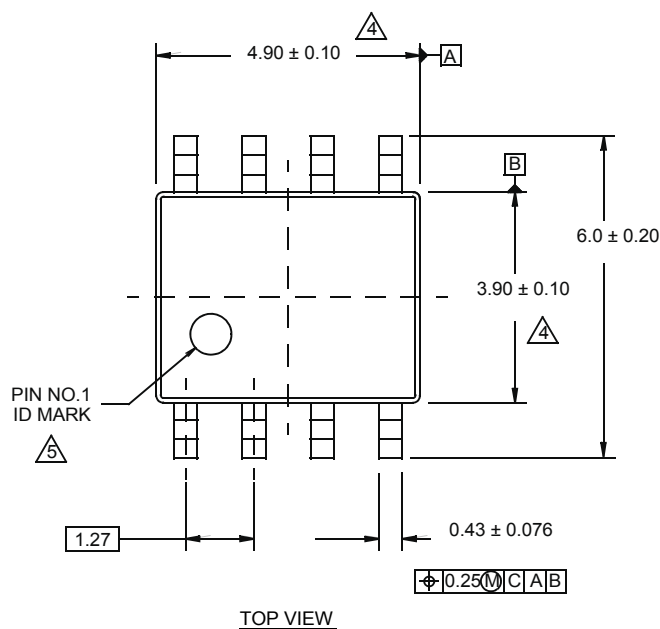
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 0, 08/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.