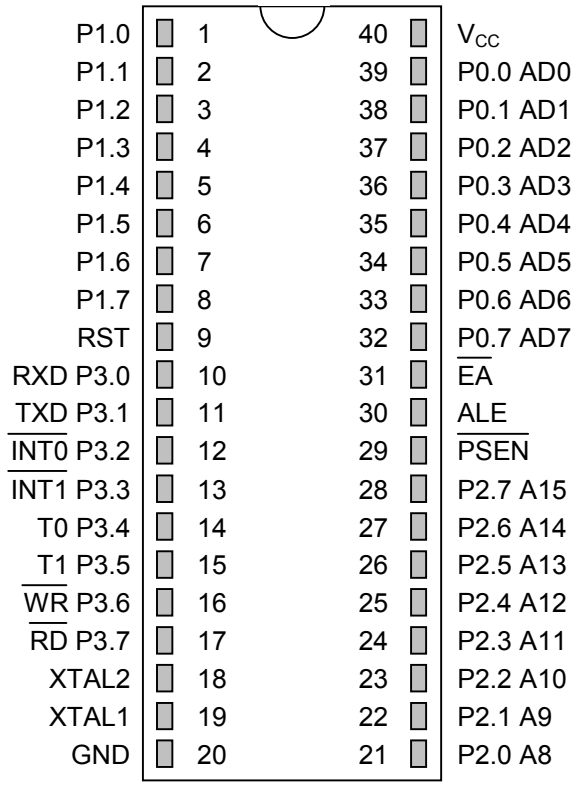
DS5000T
Soft Microcontroller Module

www.maxim-ic.com

FEATURES

- 8-bit 8051-compatible microcontroller adapts to task at hand:
  - 8 or 32 kbytes of nonvolatile RAM for program and/or data memory storage
  - Initial downloading of software in end system via on-chip serial port
  - Capable of modifying its own program and/or data memory in end use
- Crashproof operation:
  - Maintains all nonvolatile resources for 10 years in the absence of V_{CC}
  - Power-Fail Reset
  - Early Warning Power-Fail Interrupt
  - Watchdog Timer
- Software security feature:
  - Executes encrypted software to prevent unauthorized disclosure
- On-chip, full-duplex serial I/O ports
- Two on-chip timer/event counters
- 32 parallel I/O lines
- Compatible with industry standard 8051 instruction set and pinout
- Optional permanently powered real time clock (DS5000T)

PIN ASSIGNMENT



40-Pin Encapsulated Package

DESCRIPTION

The DS5000(T) Soft Microcontroller Module is a fully 8051-compatible 8-bit CMOS microcontroller that offers "softness" in all aspects of its application. This is accomplished through the comprehensive use of nonvolatile technology to preserve all information in the absence of system V_{CC}. The internal program/data memory space is implemented using either 8 or 32 kbytes of nonvolatile CMOS SRAM. Furthermore, internal data registers and key configuration registers are also nonvolatile. An optional real time clock gives permanently powered timekeeping. The clock keeps time to a hundredth of a second using an onboard crystal.

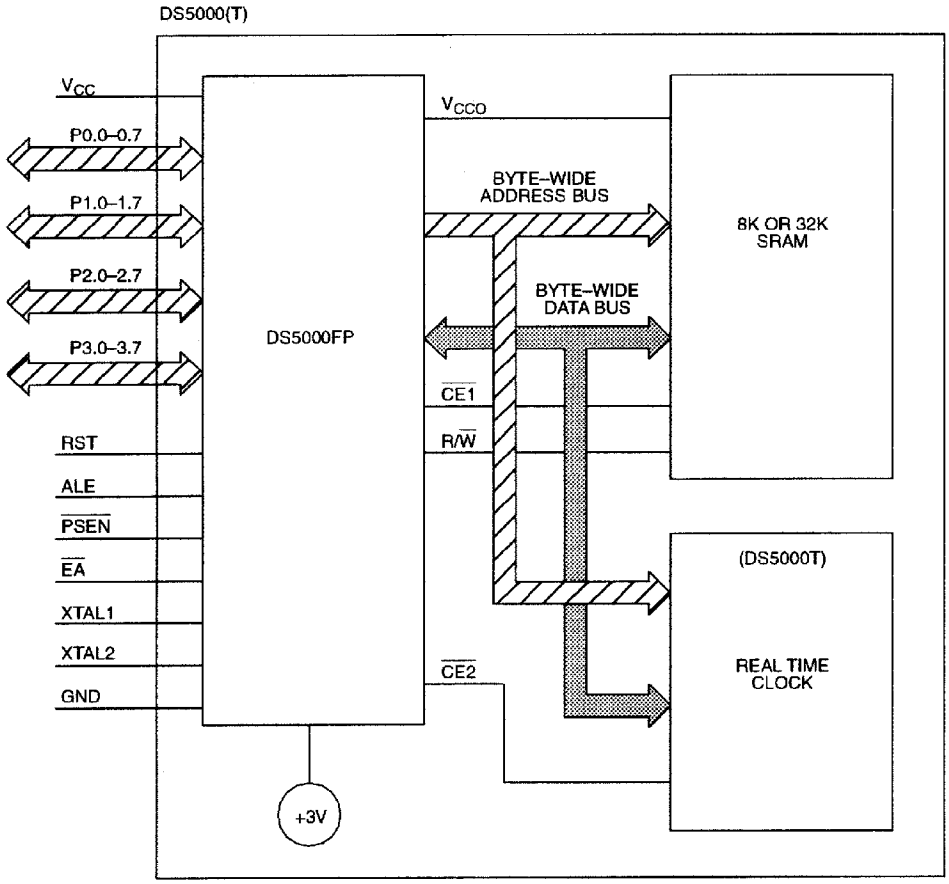
Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://dbserv.maxim-ic.com/errata.cfm.

ORDERING INFORMATION

PART NUMBER	RAM SIZE	MAX CRYSTAL SPEED	TIMEKEEPING?
DS5000-8-16	8 kbytes	16 MHz	No
DS5000-32-16	32 kbytes	16 MHz	No
DS5000-8-16	8 kbytes	16 MHz	Yes
DS5000T-32-16	32 kbytes	16 MHz	Yes

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

DS5000(T) BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	DESCRIPTION
1-8	**P1.0 - P1.7.** General purpose I/O Port 1.
9	**RST -** Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used.
10	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should not be connected directly to a PC COM port.
11	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should not be connected directly to a PC COM port.
12	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
13	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
14	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
15	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
16	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
17	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
18, 19	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
20	**GND.** Logic ground.
21-28	**P2.0-P2.7.** General purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
29	**$\overline{\text{PSEN}}$ -** Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ also is used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS5000(T) is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
30	**ALE -** Address Latch Enable. Used to de-multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch. When using a parallel programmer, this pin also assumes the $\overline{\text{PROG}}$ function for programming pulses.
31	**$\overline{\text{EA}}$ -** External Access. This pin forces the DS5000(T) to behave like an 8031. No internal memory (or clock) will be available when this pin is at a logic low. Since this pin is pulled down internally, it should be connected to +5V to use NV RAM. In a parallel programmer, this pin also serves as V_{PP} for super voltage pulses.
32-39	**P0.7-P0.0.** General purpose I/O Port 0. This port is open-drain and cannot drive a logic 1. It requires external pullups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pullups.
40	**V_{CC} - +5 volts.**

INSTRUCTION SET

The DS5000(T) executes an instruction set which is object code-compatible with the industry standard 8051 microcontroller. As a result, software development packages which have been written for the 8051 are compatible with the DS5000(T), including cross-assemblers, high-level language compilers, and debugging tools.

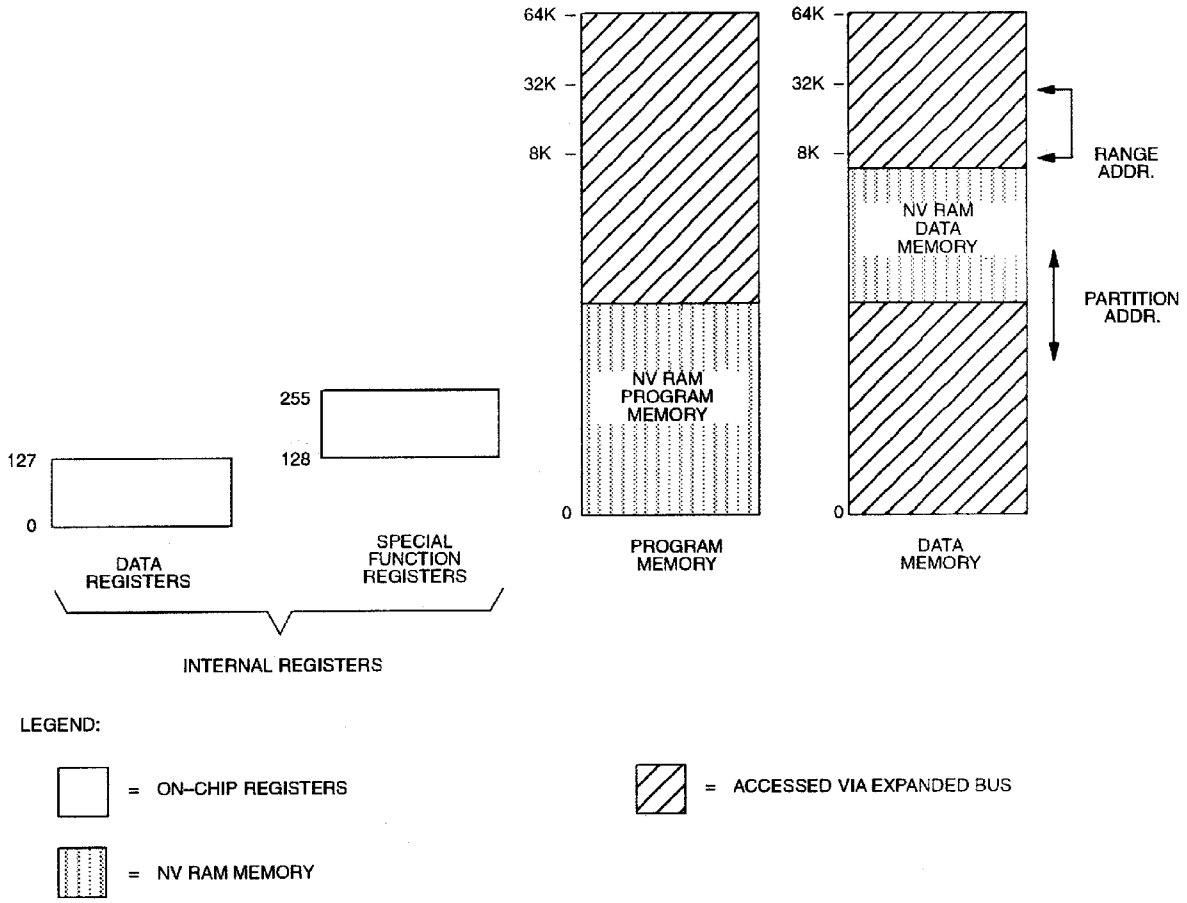
A complete description for the DS5000(T) instruction set is available in the User's Guide section of the Secure Microcontroller Data Book.

MEMORY ORGANIZATION

Figure 2 illustrates the address spaces which are accessed by the DS5000(T). As illustrated in the figure, separate address spaces exist for program and data memory. Since the basic addressing capability of the machine is 16 bits, a maximum of 64 kbytes of program memory and 64 kbytes of data memory can be accessed by the DS5000(T) CPU. The 8- or 32-kbyte RAM area inside of the DS5000(T) can be used to contain both program and data memory.

The Real time Clock (RTC) in the DS5000T is reached in the memory map by setting a SFR bit. The MCON.2 bit (ECE2) is used to select an alternate data memory map. While ECE2=1, all MOVXs will be routed to this alternate memory map. The real time clock is a serial device that resides in this area. A full description of the RTC access and example software is given in the User's Guide section of the Secure Microcontroller Data Book. If the ECE2 bit is set on a DS5000 without a timekeeper, the MOVXs will simply go to a nonexistent memory. Software execution would not be affected otherwise.

DS5000(T) LOGICAL ADDRESS SPACES Figure 2



PROGRAM LOADING

The Program Load Modes allow initialization of the NV RAM Program/Data Memory. This initialization may be performed in one of two ways:

1. Serial Program Loading which is capable of performing Bootstrap Loading of the DS5000(T). This feature allows the loading of the application program to be delayed until the DS5000(T) is installed in the end system. Dallas Semiconductor strongly recommends the use of serial program loading because of its versatility and ease of use.
2. Parallel Program Load cycles which perform the initial loading from parallel address/data information presented on the I/O port pins. This mode is timing set-compatible with the 8751H microcontroller programming mode.

The DS5000(T) is placed in its Program Load configuration by simultaneously applying a logic 1 to the RST pin and forcing the $\overline{\text{PSEN}}$ line to a logic 0 level. Immediately following this action, the DS5000(T) will look for a parallel Program Load pulse, or a serial ASCII carriage return (0DH) character received at 9600, 2400, 1200, or 300 bps over the serial port.

The hardware configurations used to select these modes of operation are illustrated in Figure 3.

PROGRAM LOADING CONFIGURATIONS Figure 3

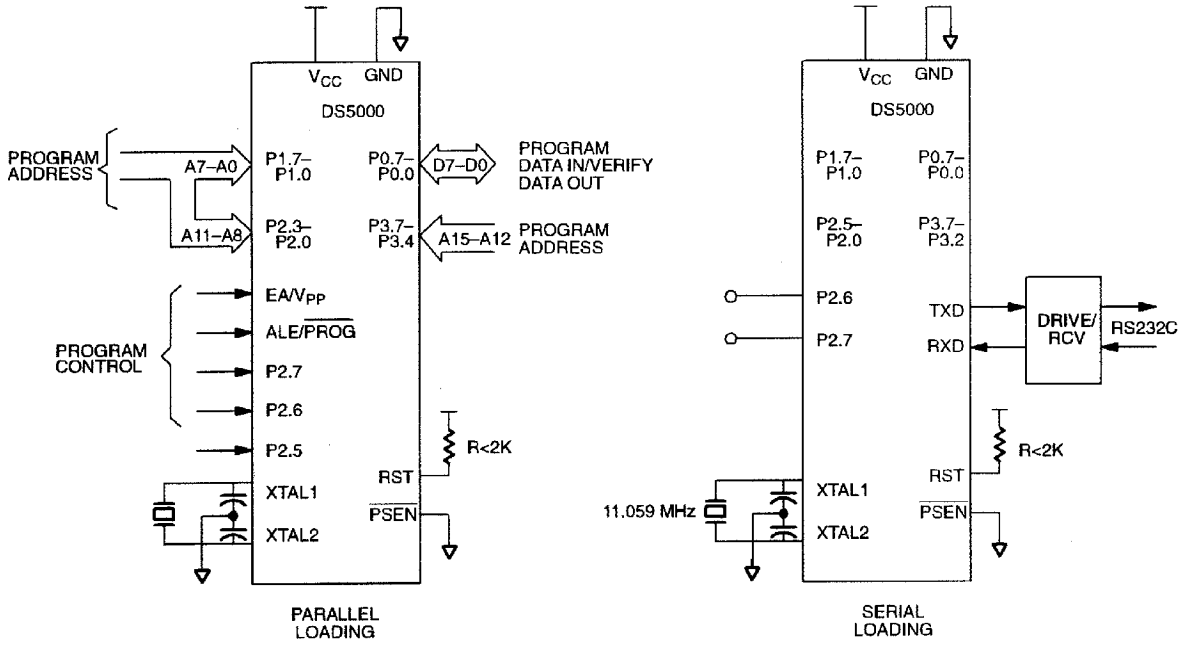


Table 1 summarizes the selection of the available Parallel Program Load cycles. The timing associated with these cycles is illustrated in the electrical specs.

SERIAL BOOTSTRAP LOADER

The Serial Program Load Mode is the easiest, fastest, most reliable, and most complete method of initially loading application software into the DS5000(T) nonvolatile RAM. Communication can be performed over a standard asynchronous serial communications port. A typical application would use a simple RS232C serial interface to program the DS5000(T) as a final production procedure. The hardware configuration which is required for the Serial Program Load mode is illustrated in Figure 3. Port pins 2.7 and 2.6 must be either open or pulled high to avoid placing the DS5000(T) in a parallel load cycle. Although an 11.0592 MHz crystal is shown in Figure 3, a variety of crystal frequencies and loader baud rates are supported, shown in Table 2. The serial loader is designed to operate across a 3-wire interface from a standard UART. The receive, transmit, and ground wires are all that are necessary to establish communication with the DS5000(T).

The Serial Bootstrap Loader implements an easy-to-use command line interface which allows an application program in an Intel hex representation to be loaded into and read back from the device. Intel hex is the typical format which existing 8051 cross-assemblers output. The serial loader responds to single character commands which are summarized below:

COMMAND	FUNCTION
C	Return CRC-16 checksum of embedded RAM
D	Dump Intel hex file
F	Fill embedded RAM block with constant
K	Load 40-bit encryption key
L	Load Intel hex file
R	Read MCON register
T	Trace (echo) incoming Intel hex data
U	Clear security lock
V	Verify embedded RAM with incoming Intel hex
W	Write MCON register
Z	Set security lock
P	Put a value to a port
G	Get a value from a port

PARALLEL PROGRAM LOAD CYCLES Table 1

MODE	RST	$\overline{\text{PSEN}}$	$\overline{\text{PROG}}$	$\overline{\text{EA}}$	P2.7	P2.6	P2.5
Program	1	0	0	V_{PP}	1	0	X
Security Set	1	0	0	V_{PP}	1	1	X
Verify	1	X	X	1	0	0	X
Prog Expanded	1	0	0	V_{PP}	0	1	0
Verify Expanded	1	0	1	1	0	1	0
Prog MCON or Key registers	1	0	0	V_{PP}	0	1	1
Verify MCON registers	1	0	1	1	0	1	1

The Parallel Program Cycle is used to load a byte of data into a register or memory location within the DS5000(T). The Verify Cycle is used to read this byte back for comparison with the originally loaded value to verify proper loading. The Security Set Cycle may be used to enable and the Software Security feature of the DS5000(T). One may also enter bytes for the MCON register or for the five encryption registers using the Program MCON cycle. When using this cycle, the absolute register address must be presented at Ports 1 and 2 as in the normal program cycle (Port 2 should be 00H). The MCON contents can likewise be verified using the Verify MCON cycle.

When the DS5000(T) first detects a Parallel Program Strobe pulse or a Security Set Strobe pulse while in the Program Load Mode following a Power-On Reset, the internal hardware of the DS5000(T) is initialized so that an existing 4-kbyte program can be programmed into a DS5000(T) with little or no modification. This initialization automatically sets the Range Address for 8 kbytes and maps the lowest 4-kbyte bank of Embedded RAM as program memory. The next 4 kbytes of Embedded RAM are mapped as Data Memory.

In order to program more than 4 kbytes of program code, the Program/Verify Expanded cycles can be used. Up to 32 kbytes of program code can be entered and verified. Note that the expanded 32-kbyte Program/ Verify cycles take much longer than the normal 4-kbyte Program/Verify cycles.

A typical parallel loading session would follow this procedure. First, set the contents of the MCON register with the correct range and partition only if using expanded programming cycles. Next, the encryption registers can be loaded to enable encryption of the program/data memory (not required). Then,

program the DS5000(T) using either normal or expanded program cycles and check the memory contents using Verify cycles. The last operation would be to turn on the security lock feature by either a Security Set cycle or by explicitly writing to the MCON register and setting MCON.0 to a 1.

SERIAL LOADER BAUD RATES FOR DIFFERENT CRYSTAL FREQUENCIES Table 2

CRYSTAL FREQ (MHz)	BAUD RATE					
	300	1200	2400	9600	19200	57600
14.7456		Y	Y	Y	Y	
11.0592	Y	Y	Y	Y	Y	Y
9.21600	Y	Y	Y	Y		
7.37280	Y	Y	Y	Y		
5.52960	Y	Y	Y	Y		
1.84320	Y	Y	Y	Y		

ADDITIONAL INFORMATION

A complete description for all operational aspects of the DS5000(T), is provided in the User's Guide section of the Secure Microcontroller Data Book.

DEVELOPMENT SUPPORT

Dallas Semiconductor offers a kit package for developing and testing user code. The DS5000TK Evaluation Kit allows the user to download Intel hex formatted code directly to the DS5000(T) from a PC-XT/AT or compatible computer. The kit consists of a DS5000T-32, an interface pod, demo software, and an RS232 connector that attaches to the COM1 or COM2 serial port of a PC. See the Development Tools section of the Secure Microcontroller Data Book for further details.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A=0°C to 70°C; V_{CC}=5V ± 5%)

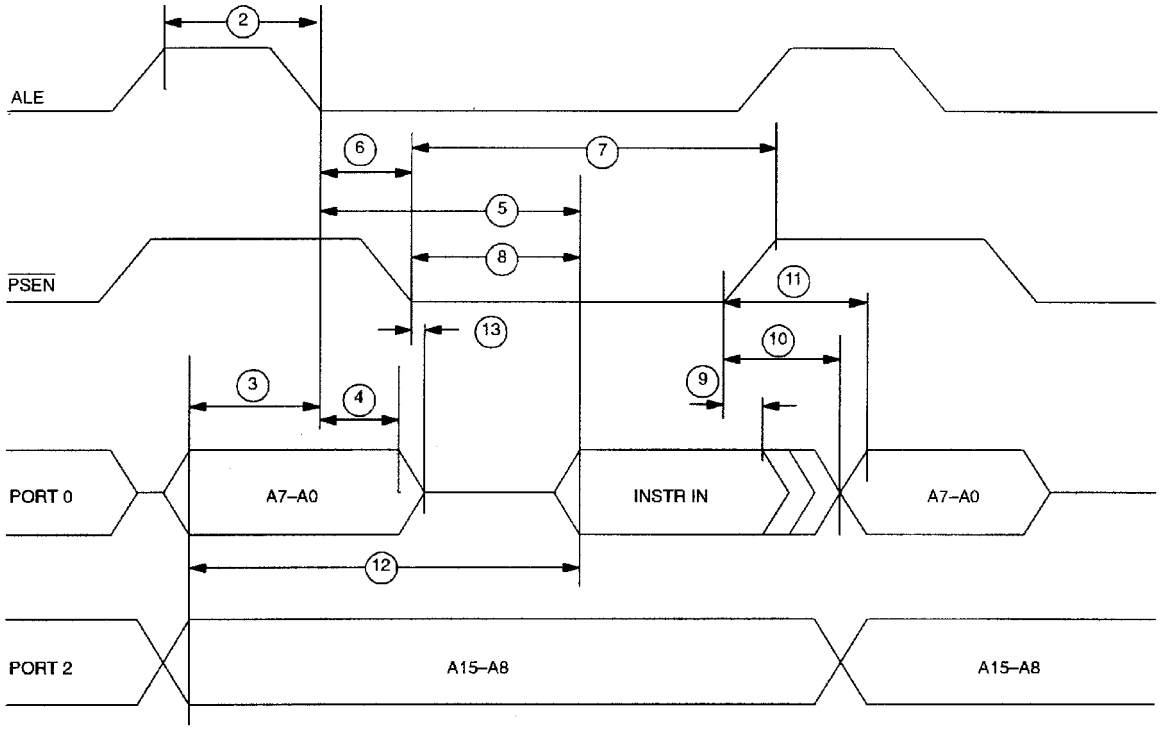
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	-0.3		0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage RST, XTAL1	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Ports 0, ALE, $\overline{PSEN}$)	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=-80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=-400 µA (Ports 0, ALE, $\overline{PSEN}$)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			-50	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3)	I_{TL}			-500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_L			±10	µA	
RST, $\overline{EA}$ Pulldown Resistor	R_{RE}	40		125	kΩ	
Stop Mode Current	I_{SM}			80	µA	4
Power-Fail Warning Voltage	V_{PFW}	4.15	4.6	4.75	V	1
Minimum Operating Voltage	V_{CCmin}	4.05	4.5	4.65	V	1
Programming Supply Voltage (Parallel Program Mode)	V_{PP}	12.5		13	V	1
Program Supply Current	I_{PP}		15	20	mA	
Operating Current DS5000-8k @ 8MHz DS5000-32k @ 12 MHz DS5000(T)-32-16 @ 16 MHz	I_{CC}		25.2 35.7 45.6	43 48 54	mA	2
Idle Mode Current @ 12 MHz	I_{CC}		4.5	6.2	mA	3

AC CHARACTERISTICS: EXPANDED BUS MODE TIMING SPECIFICATIONS

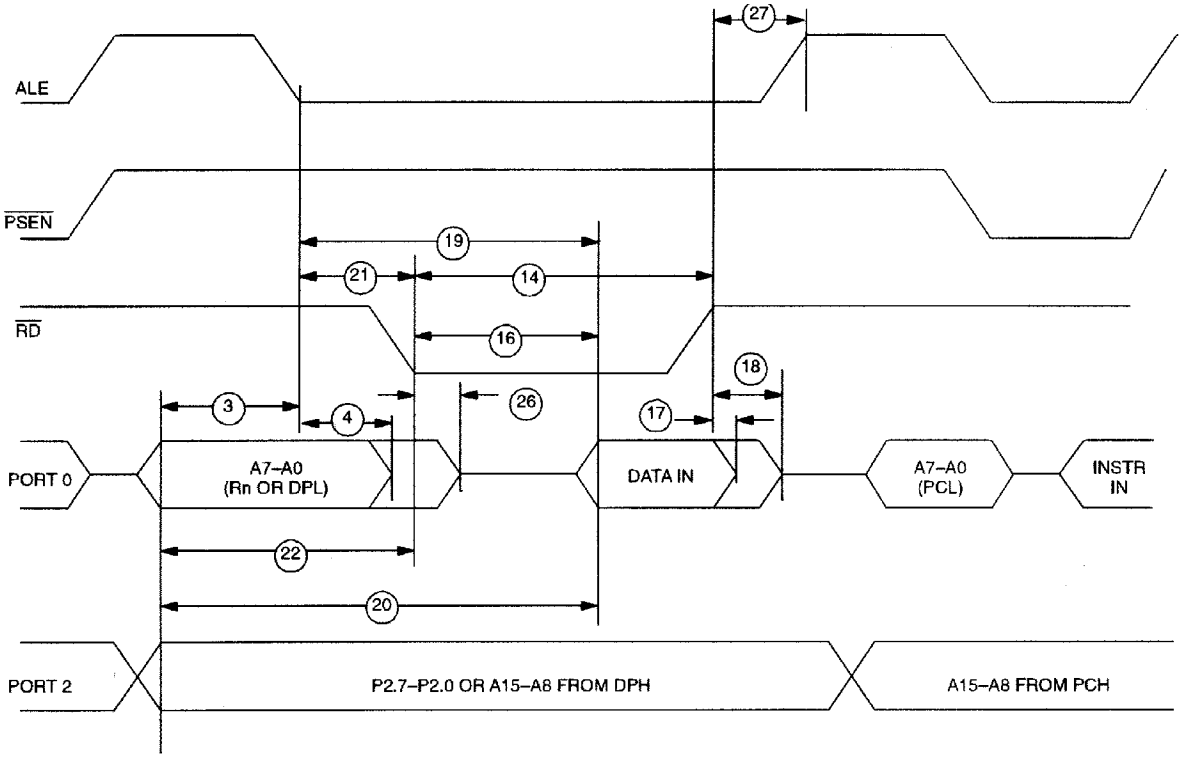
(t_A=0°C to 70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$ -40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK} -40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK} -35		ns
5	ALE Low to Valid Instr. In @ 12 MHz @ 16 MHz	t_{ALLVI}		$4t_{CLK}$ -150 $4t_{CLK}$ -90	ns ns
6	ALE Low to $\overline{\text{PSEN}}$ Low	t_{ALLPSL}	t_{CLK} -25		ns
7	$\overline{\text{PSEN}}$ Pulse Width	t_{PSPW}	$3t_{CLK}$ -35		ns
8	$\overline{\text{PSEN}}$ Low to Valid Instr. In @ 12 MHz @ 16 MHz	t_{PSLVI}		$3t_{CLK}$ -150 $3t_{CLK}$ -90	ns ns
9	Input Instr. Hold after $\overline{\text{PSEN}}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{\text{PSEN}}$ Going High	t_{PSIX}		t_{CLK} -20	ns
11	Address Hold after $\overline{\text{PSEN}}$ Going High	t_{PSAV}	t_{CLK} -8		ns
12	Address Valid to Valid Instr. In @ 12 MHz @ 16 MHz	t_{AVVI}		$5t_{CLK}$ -150 $5t_{CLK}$ -90	ns ns
13	$\overline{\text{PSEN}}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{\text{RD}}$ Pulse Width	t_{RDPW}	$6t_{CLK}$ -100		ns
15	$\overline{\text{WR}}$ Pulse Width	t_{WRPW}	$6t_{CLK}$ -100		ns
16	$\overline{\text{RD}}$ Low to Valid Data In @ 12 MHz @ 16 MHz	t_{RDLDV}		$5t_{CLK}$ -165 $5t_{CLK}$ -105	ns ns
17	Data Hold after $\overline{\text{RD}}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{\text{RD}}$ High	t_{RDHDZ}		$2t_{CLK}$ -70	ns
19	ALE Low to Valid Data In @ 12 MHz @ 16 MHz	t_{ALLVD}		8_{CLK} -150 $8t_{CLK}$ -90	ns ns
20	Valid Addr. to Valid Data In @ 12 MHz @ 16 MHz	t_{AVDV}		$9t_{CLK}$ -165 $9t_{CLK}$ -105	ns ns
21	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	t_{ALLRDL}	$3t_{CLK}$ -50	$3t_{CLK}$ +50	ns
22	Address Valid to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	t_{AVRDL}	$4t_{CLK}$ -130		ns
23	Data Valid to $\overline{\text{WR}}$ Going Low	t_{DVWRL}	t_{CLK} -60		ns
24	Data Valid to $\overline{\text{WR}}$ High @ 12 MHz @ 16 MHz	t_{DVWRH}	$7t_{CLK}$ -150 $7t_{CLK}$ -90		ns ns
25	Data Valid after $\overline{\text{WR}}$ High	t_{WRHDV}	t_{CLK} -50		ns
26	$\overline{\text{RD}}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	t_{RDHALH}	t_{CLK} -40	t_{CLK} +50	ns

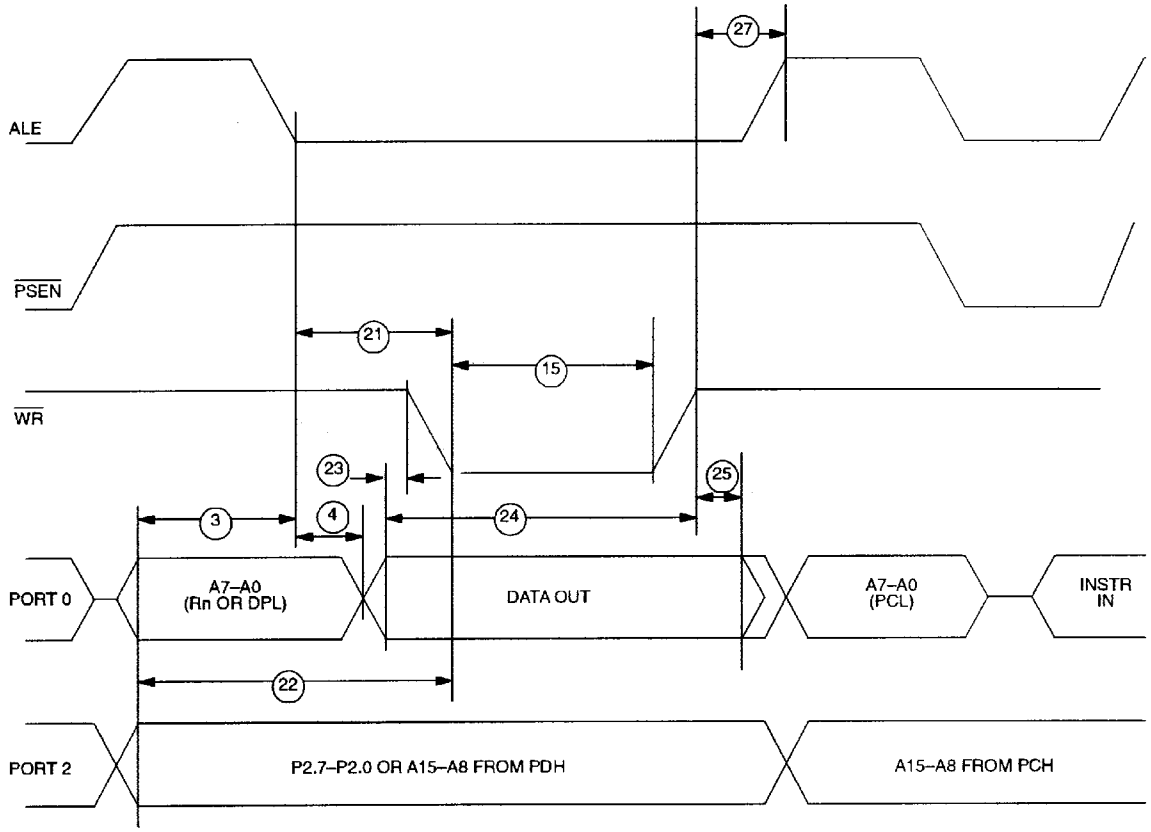
EXPANDED PROGRAM MEMORY READ CYCLE



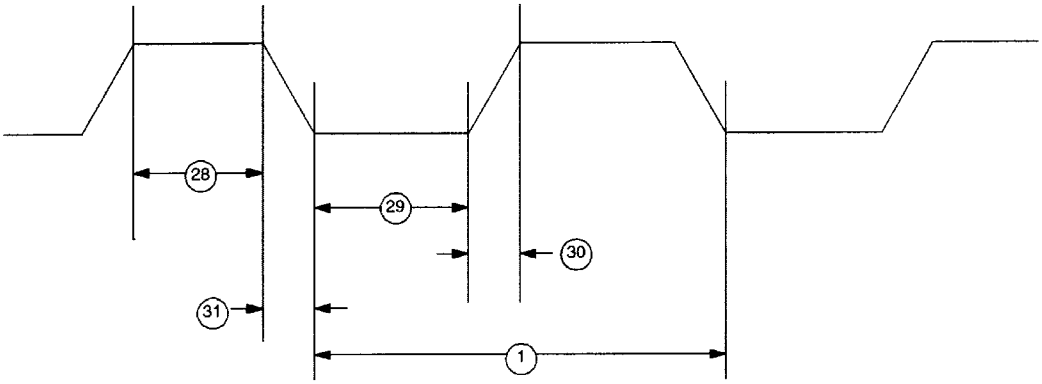
EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK TIMING



AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE

(t_A=0°C to 70°C; V_{CC}=5V ± 5%)

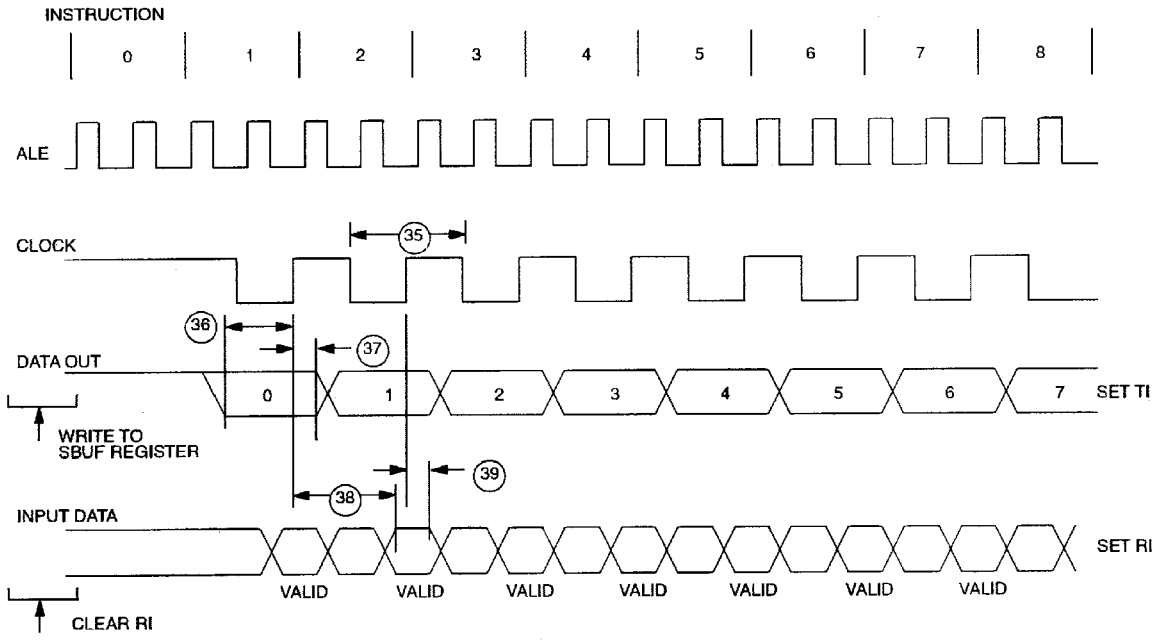
#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@ 12 MHz @ 16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@ 12 MHz @ 16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@ 12 MHz @ 16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@ 12 MHz @ 16 MHz	t_{CLKF}		20 15	ns ns

AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING - MODE 0

(t_A=0°C to 70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$ -133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$ -117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$ -133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING - MODE 0



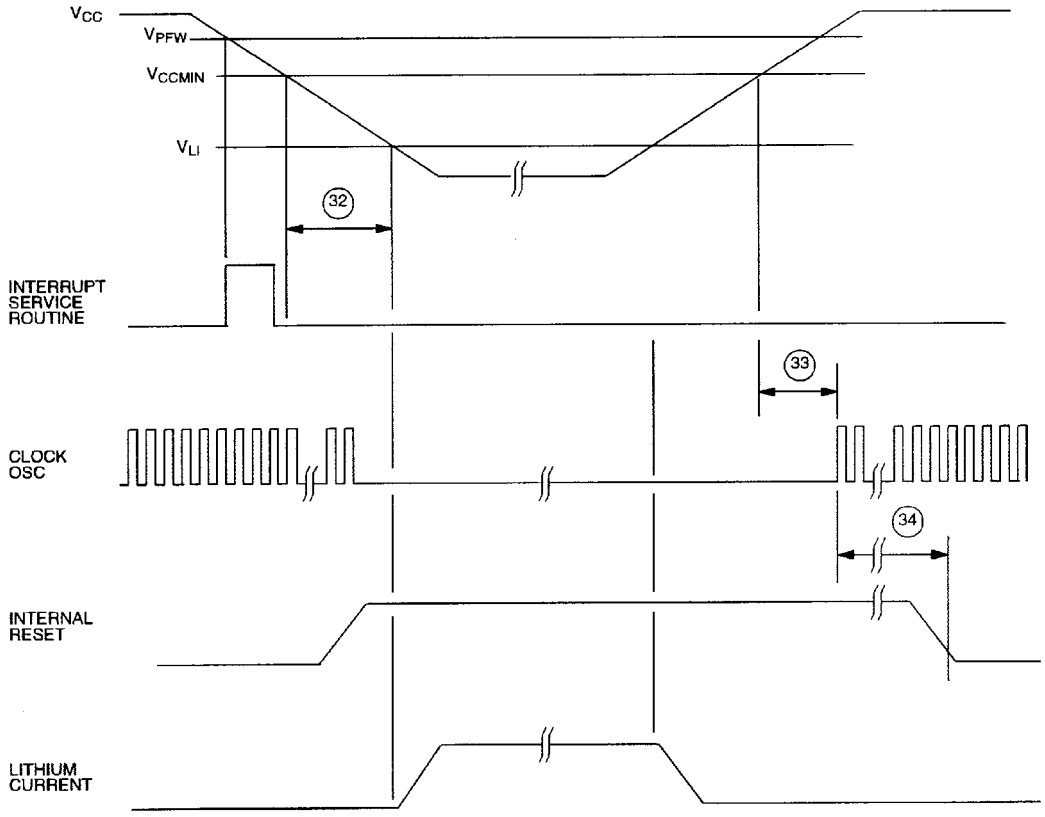
AC CHARACTERISTICS (cont'd)

POWER CYCLING TIMING

(t_A=0°C to 70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to 3.3V	t_F	40		µs
33	Crystal Start-up Time	t_{CSU}		(note 5)	
34	Power-on Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING



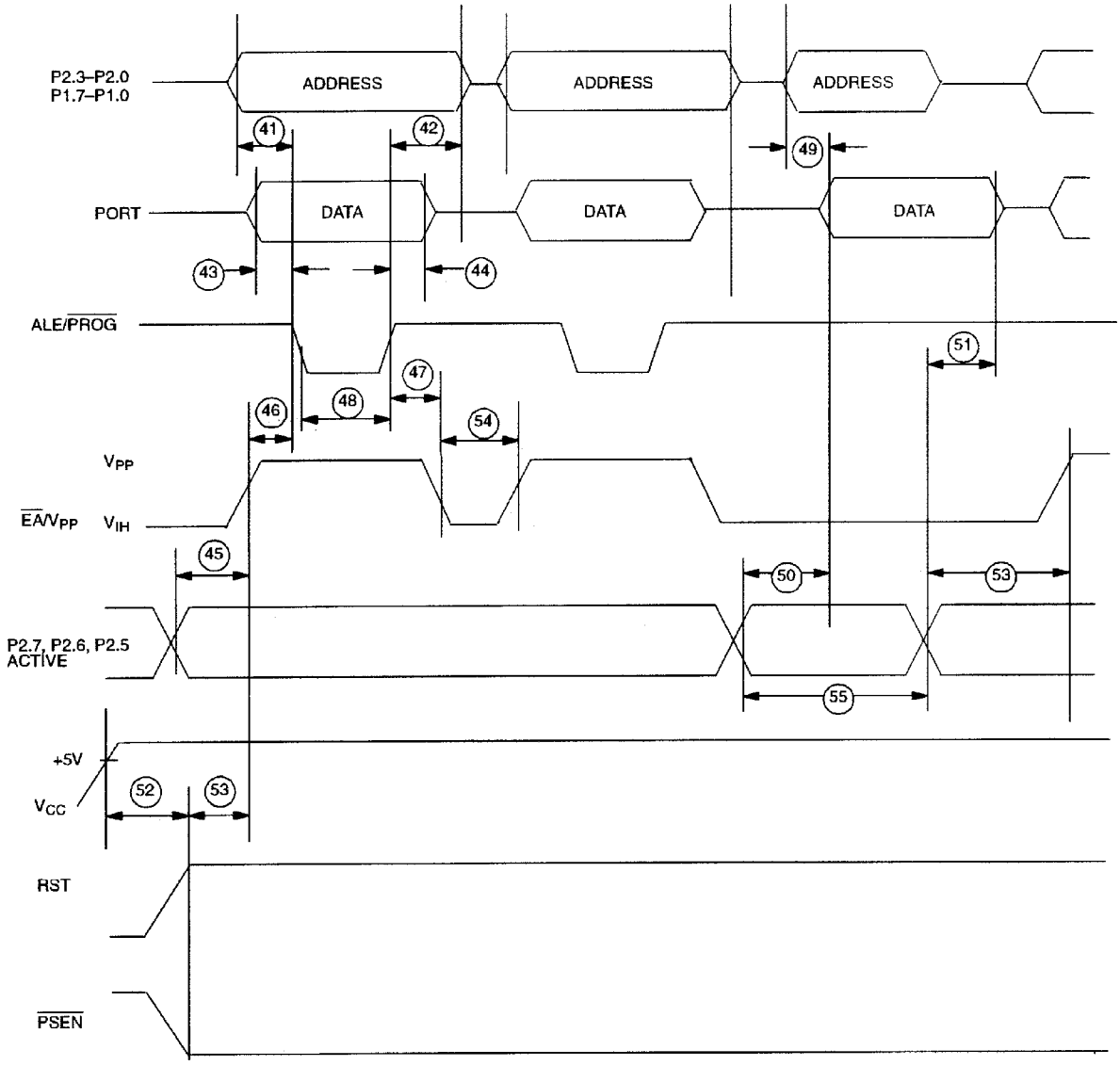
AC CHARACTERISTICS (cont'd)

PARALLEL PROGRAM LOAD TIMING (t_A=0°C to 70°C; V_{CC}=5V ± 5%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Oscillator Frequency	$1/t_{CLK}$	1.0	12.0	MHz
41	Address Setup to $\overline{PROG}$ Low	t_{AVPRL}	0		
42	Address Hold after $\overline{PROG}$ High	t_{PRHAV}	0		
43	Data Setup to $\overline{PROG}$ Low	t_{DVPRL}	0		
44	Data Hold after $\overline{PROG}$ High	t_{PRHDV}	0		
45	P2.7, 2.6, 2.5 Setup to V_{PP}	t_{P27HVP}	0		
46	V_{PP} Setup to $\overline{PROG}$ Low	t_{VPHPRL}	0		
47	V_{PP} Hold after $\overline{PROG}$ Low	t_{PRHVPL}	0		
48	$\overline{PROG}$ Width Low	t_{PRW}	2400		t_{CLK}
49	Data Output from Address Valid	t_{AVDV}		48 1800*	t_{CLK}
50	Data Output from P2.7 Low	t_{DVP27L}		48 1800*	t_{CLK}
51	Data Float after P2.7 High	t_{P27HDZ}	0	48 1800*	t_{CLK}
52	Delay to Reset/$\overline{PSEN}$ Active after Power On	t_{PORPV}	21504		t_{CLK}
53	Reset/$\overline{PSEN}$ Active (or Verify Inactive) to V_{PP} High	t_{RAVPH}	1200		t_{CLK}
54	V_{PP} Inactive (Between Program Cycles)	t_{VPPPC}	1200		t_{CLK}
55	Verify Active Time	t_{VFT}	48 2400*		t_{CLK}

* Second set of numbers refers to expanded memory programming up to 32k bytes.

PARALLEL PROGRAM LOAD TIMING

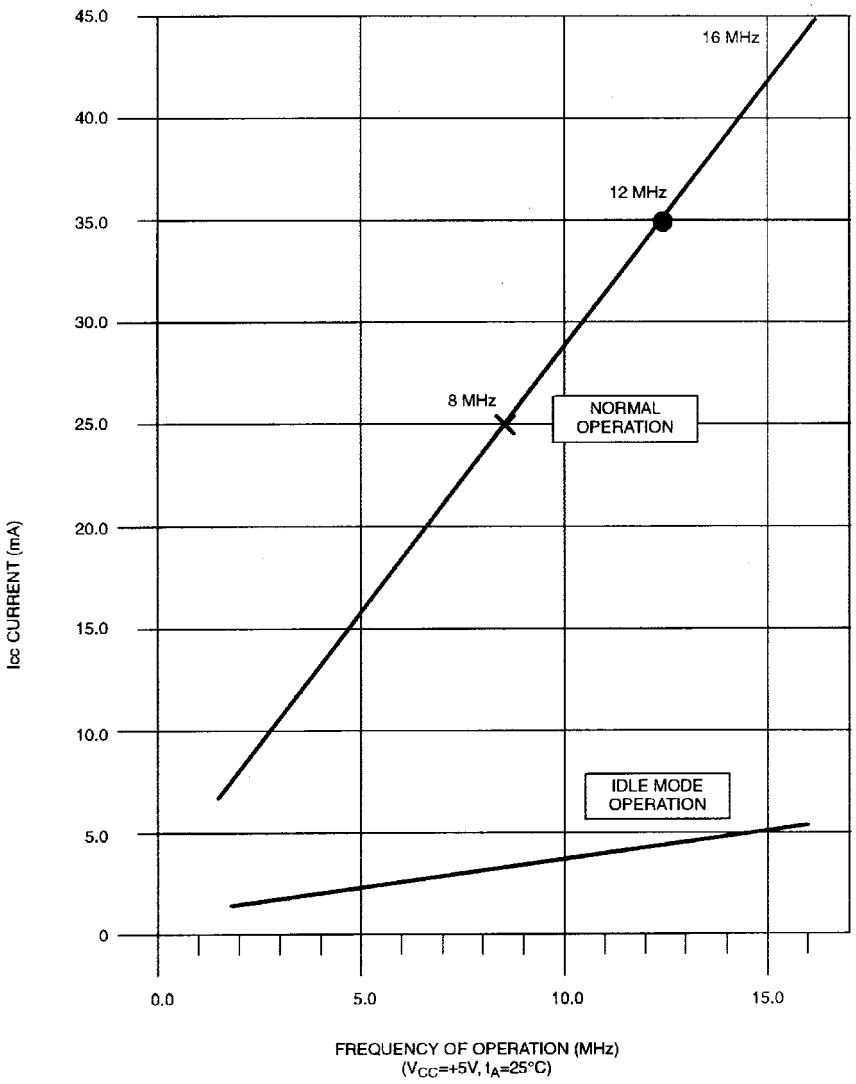


CAPACITANCE

(test frequency=1MHz; t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Capacitance	C_O			10	pF	
Input Capacitance	C_I			10	pF	

DS5000(T) TYPICAL I_{CC} VS. FREQUENCY



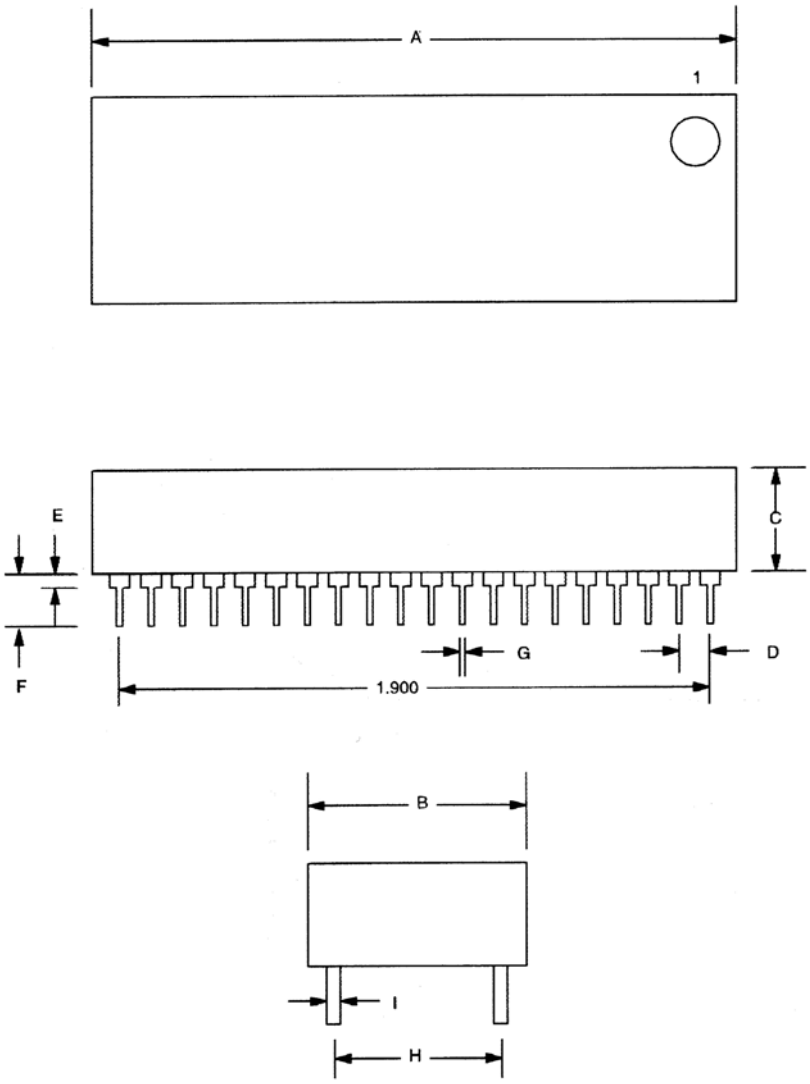
Normal operation is measured using:
1) External crystals on XTAL1 and 2
2) All port pins disconnected
3) RST=0 volts and EA=V_{CC}
4) Part performing endless loop writing to internal memory

Idle mode operation is measured using:
1) External clock source at XTAL1; XTAL2 floating
2) All port pins disconnected
3) RST=0 volts and EA=V_{CC}
4) Part set in IDLE mode by software

NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = RST = PORT0 = V_{CC}.
3. Idle mode I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; $\overline{EA}$ = PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = PORT0 = V_{CC}; XTAL2 not connected; RST = V_{SS}.
5. Crystal start-up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for the worst case spec on this time.

PACKAGE DRAWING



DIM	INCHES	
	MIN	MAX
A IN.	2.080	2.100
B IN.	0.680	0.700
C IN.	0.290	0.325
D IN.	0.090	0.110
E IN.	0.030	0.060
F IN.	0.145	0.185
G IN.	0.016	0.020
H IN.	0.590	0.610
I IN.	0.009	0.015

DATA SHEET REVISION SUMMARY

The following represent the key differences between the dates 07/20/95 to 07/24/96 of the DS5000(T) data sheet. Please review this summary carefully.

1. Correct Figure 3 to show RST active high.
2. Add Data Sheet Revision Summary.