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DS481

Low Power RS-485/RS-422 Multipoint Transceiver with Sleep Mode

General Description

The DS481 is a low-power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The drivers slew rate allows for operation up to 2.0 Mbps (see Applications Information section).

The transceiver draws 200 μ A of supply current when unloaded or 0.2 μ A when in the automatic sleep mode. Sleep mode is activated by inactivity on the enables (DE and RE (Note 1)). Holding DE =L and RE (Note 1)=H for greater than 600 ns will enable the sleep mode. The DS481 operates from a single +5V supply.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE® (High Impedance state) under fault conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

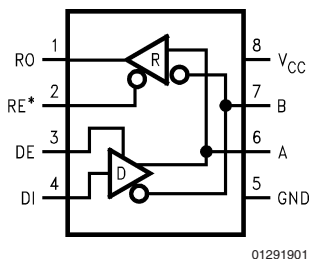
The receiver has a failsafe feature that guarantees a logic-high output if the input is open circuit.

The DS481 is available in a surface mount package and is characterized for Industrial temperature range operation.

Features

- Meets TIA/EIA RS-485 multipoint standard
- Sleep mode reduces I_{CC} to 0.2 μ A
- Guaranteed full load output voltage (V_{OD3})
- Low quiescent current: 200 μ A typ
- -7V to +12V common-mode input voltage range
- TRI-STATE outputs on driver and receiver
- AC performance:
 - Driver transition time: 25 ns typ
 - Driver propagation delay: 40 ns typ
 - Driver skew: 1 ns typ
 - Receiver propagation delay: 200 ns typ
 - Receiver skew: 20 ns typ
- Half-duplex flow through pinout
- Operates from a single 5V supply
- Allows up to 64 transceivers on the bus
- Current-limiting and thermal shutdown for driver overload protection
- Industrial temperature range operation
- Pin and functional compatible with MAX481C and MAX481E

Connection and Logic Diagram



*Note: Non Terminated, Open Input only

Order Number	Temp. Range	Package/###
DS481TM	-40°C to +85°C	SOP/M08A

Truth Table

DRIVER SECTION				
RE (Note 1)	DE	DI	A	B
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z (Note 2)
RECEIVER SECTION				
RE (Note 1)	DE	A-B		RO
L	L	≥+0.2V		H
L	L	≤−0.2V		L
H	X	X		Z (Note 2)
L	L	OPEN (Note 1)		H

X = indeterminate
Z = TRI-STATE

Note 1: Non Terminated, Open Input only

Note 2: Device enters sleep mode if enable conditions are held > 600 ns, DE = L and RE (Note 1) = H.

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+12V
Enable Input Voltage (RE (Note 1), DE)	-0.5V to ($V_{CC} + 0.5V$)
Driver Input Voltage (DI)	-0.5V to ($V_{CC} + 0.5V$)
Driver Output Voltage (A, B)	-14V to +14V
Receiver Input Voltage (A, B)	-14V to +14V
Receiver Output Voltage (RO)	-0.5V to ($V_{CC} + 0.5V$)
Maximum Package Power Dissipation @ +25°C	
M Package	1.19W
Derate M Package 9.5 mW/°C above +25°C	

M Package

0.76W

Storage Temperature Range

-65°C to +150°C

Lead Temperature Range

(Soldering, 4 sec.)

+260°C

ESD (HBM)

≥2 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Operating Free Air Temperature (T_A)				
DS481T	-40	+25	+85	°C
Bus Common Mode Voltage	-7		+12	V

Maximum Package Power Dissipation @ +70°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 4, 5)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage	(No Load)	A, B	1.5		5	V
V_{OD2}	Differential Driver Output Voltage with Load	$R_L = 50\Omega$, (RS422), Figure 1		2	2.8		V
		$R_L = 27\Omega$, (RS485), Figure 1		1.5	2.3	5	V
ΔV_{OD}	Change in Magnitude of Output Differential Voltage	$R_L = 27\Omega$ or 50Ω (Note 6)				0.2	V
V_{OD3}	Differential Driver Output Voltage — Full Load with Max V_{CM}	$R_1 = 54\Omega$, $R_2 = 375\Omega$ $V_{TEST} = -7V$ to +12V, Figure 2		1.5	2.0	5	V
V_{OC}	Driver Common-Mode Output Voltage	$R_L = 27\Omega$ or 50Ω , Figure 1		0		3	V
ΔV_{OC}	Change in Magnitude of Common-Mode Output Voltage	$R_L = 27\Omega$ or 50Ω , Figure 1 (Note 6)				0.2	V
V_{IH}	Input High Voltage		DI, DE, RE (Note 1)	2.0			V
V_{IL}	Input Low Voltage					0.8	V
I_{IN1}	Input Current	$V_{IN} = 0V$ or V_{CC}				±2	μA
I_{IN2}	Input Current (Note 7) DE = 0V, $V_{CC} = 0V$ or 5.25V	$V_{IN} = +12V$	DS481T	0	190	500	μA
		$V_{IN} = -7V$		0	-100	-400	μA
V_{TH}	Receiver Differential Threshold Voltage	$-7V \leq V_{CM} \leq +12V$		-0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4$ mA, $V_{ID} = 0.2V$	RO	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4$ mA, $V_{ID} = -0.2V$				0.5	V
I_{OZR}	TRI-STATE Output Current at Receiver	$0.4V \leq V_O \leq 2.4V$				±1	μA
R_{IN}	Receiver Input Resistance	$-7V \leq V_{IN} \leq +12V$	DS481T	24			kΩ
I_{CC}	No-Load Supply Current (Note 8)	DE = V_{CC} , RE (Note 1) = 0V or V_{CC}	V_{CC}		200	500	μA
		DE = 0V, RE (Note 1) = 0V or V_{CC}			200	500	μA
I_{CCX}	Sleep Mode Supply Current	DE = GND RE (Note 1) = V_{CC} (Figure 14)	V_{CC}		0.2	10	μA
I_{OSD1}	Driver Short Circuit Current, $V_O = HIGH$	$-7V \leq V_O \leq +12V$	A, B			250	mA
I_{OSD2}	Driver Short Circuit Current, $V_O = LOW$	$-7V \leq V_O \leq +12V$				-250	mA
I_{OSR}	Receiver Short Circuit Current	$V_O = GND$	RO	7		85	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 5, 9, 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLHD}	Driver Differential Propagation Delay—Low to High	$R_L = 54\Omega$, $C_L = 100\text{ pF}$	10	40	80	ns
t_{PHLD}	Driver Differential Propagation Delay—High to Low		10	39	80	ns
t_{SKEW}	Differential Skew $ t_{PHLD} - t_{PLHD} $		0	1	10	ns
t_r	Driver Rise Time		3	25	50	ns
t_f	Driver Fall Time		3	25	50	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100\text{ pF}$		50	200	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100\text{ pF}$		65	200	ns
t_{LZ}	Driver Disable from Output Low	$C_L = 15\text{ pF}$		80	200	ns
t_{HZ}	Driver Disable from Output High	$C_L = 15\text{ pF}$		80	200	ns
t_{PSH}	Driver Enable from Sleep Mode to Output High	$C_L = 100\text{ pF}$ (Note 12) (Figures 5, 6)	70	98	250	ns
t_{PSL}	Driver Enable from Sleep Mode to Output Low	$C_L = 100\text{ pF}$ (Note 12) (Figures 7, 8)	70	98	250	ns
t_{PLHD}	Receiver Differential Propagation Delay—Low to High	$C_L = 15\text{ pF}$ (RO)	30	190	400	ns
t_{PHLD}	Receiver Differential Propagation Delay—High to Low		30	210	400	ns
t_{SKEW}	Differential Skew $ t_{PHLD} - t_{PLHD} $		0	20	50	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15\text{ pF}$		45	150	ns
t_{ZL}	Receiver Enable to Output Low			40	150	ns
t_{LZ}	Receiver Disable from Output Low			50	150	ns
t_{HZ}	Receiver Disable from Output High			55	150	ns
t_{PSH}	Receiver Enable from Sleep Mode to Output High	$C_L = 15\text{ pF}$ (Note 12) (Figures 11, 13)	70	97	250	ns
t_{PSL}	Receiver Enable from Sleep Mode to Output Low	$C_L = 15\text{ pF}$ (Note 12) (Figures 11, 12)	70	95	250	ns
t_{SLEEP}	Time to Sleep (Device)	DE = L and RE (Note 1) = H (Figure 14)	50		600	ns
f_{max}	Maximum Data Rate	(Note 11)	2.0			Mbps

Note 3: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Note 4: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{OD1/2/3}$ and V_{ID} .

Note 5: All typicals are given for: $V_{CC} = +5.0V$, $T_A = +25^\circ C$.

Note 6: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input changes state.

Note 7: I_{IN2} includes the receiver input current and driver TRI-STATE leakage current.

Note 8: Supply current specification is valid for loaded transmitters when DE = 0V or enabled (DE = H) with no load.

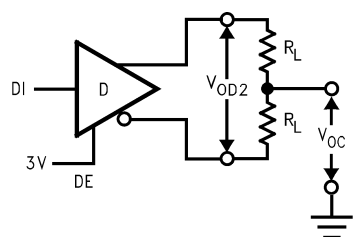
Note 9: $f = 1\text{ MHz}$, t_r and $t_f \leq 6\text{ ns}$, $Z_O = 50\Omega$.

Note 10: C_L includes jig and probe capacitance.

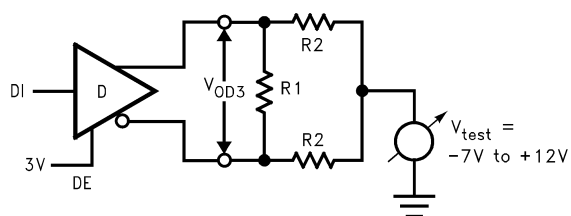
Note 11: f_{max} is the guaranteed data rate for 50 ft of twisted pair cable. f_{max} may be conservatively determined from the ratio of driver transition time (t_r) to the data rate unit interval ($1/f_{max}$). Using a 10% ratio yields $f_{max} = (0.1)/50\text{ ns} = 2.0\text{ Mb/s}$. Higher data rates may be supported by allowing larger ratios.

Note 12: For enable from sleep mode delays DE = L and RE (Note 1) = H for greater than 600 ns prior to test (device is in sleep mode).

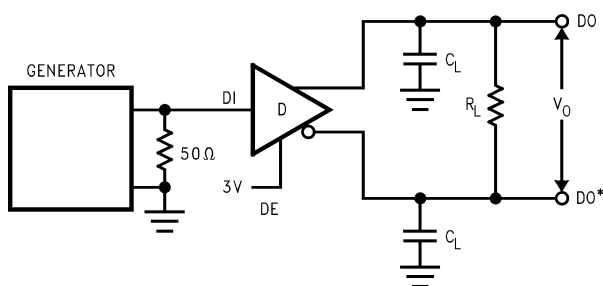
Parameter Measurement Information



01291902

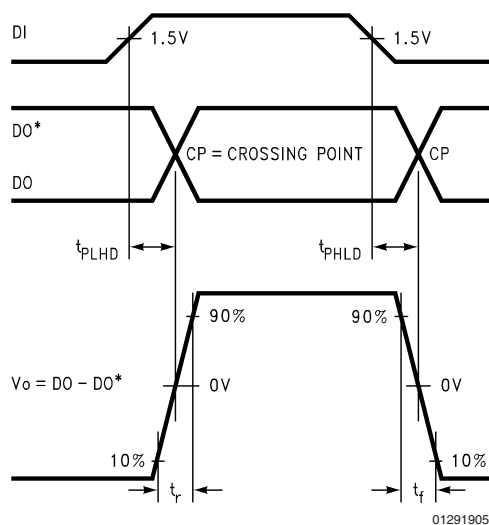
FIGURE 1. V_{OD} 

01291903

FIGURE 2. V_{OD3} 

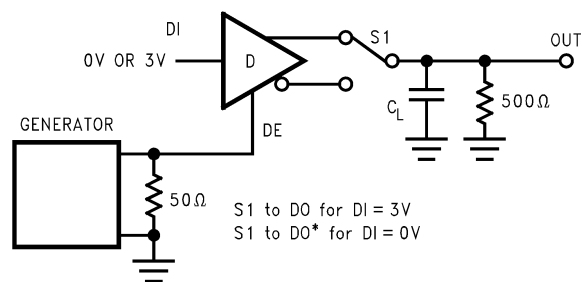
01291904

FIGURE 3.



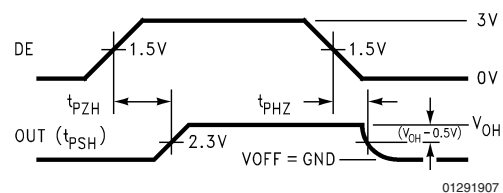
01291905

FIGURE 4.



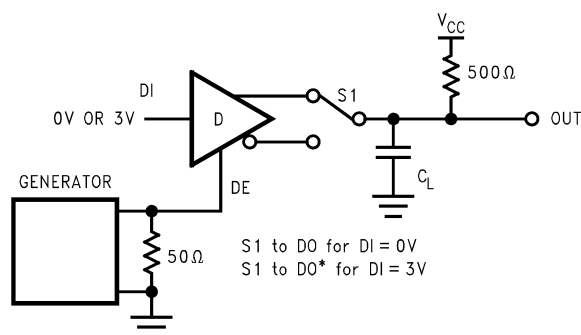
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FIGURE 5.



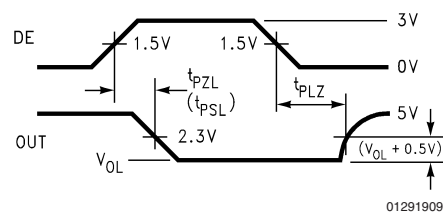
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FIGURE 6.



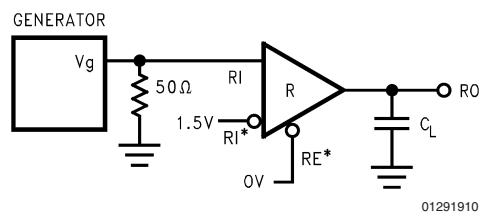
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FIGURE 7.



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FIGURE 8.



01291910

FIGURE 9.

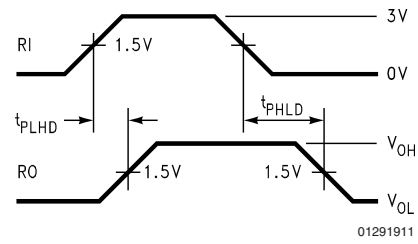


FIGURE 10.

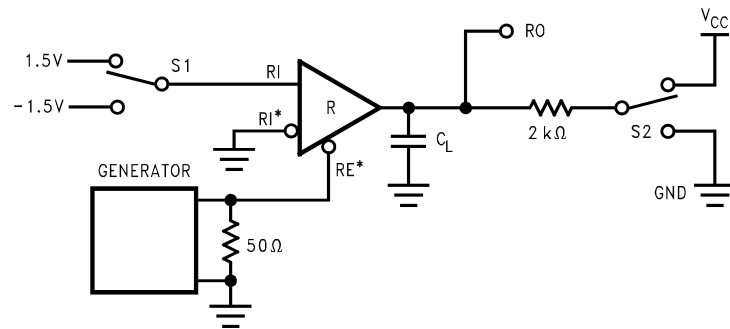


FIGURE 11.

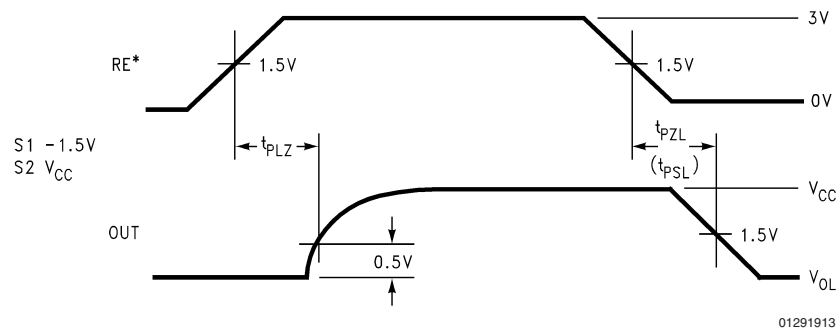


FIGURE 12.

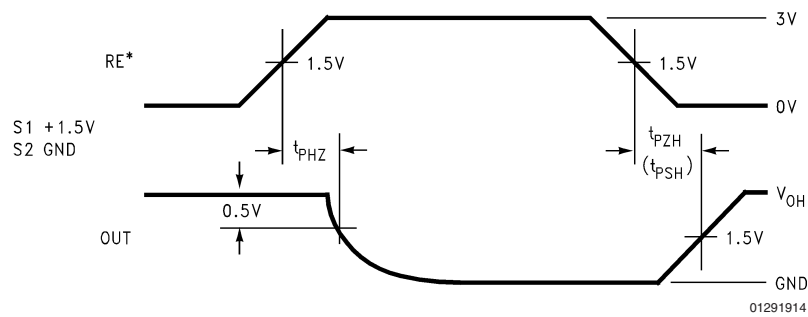
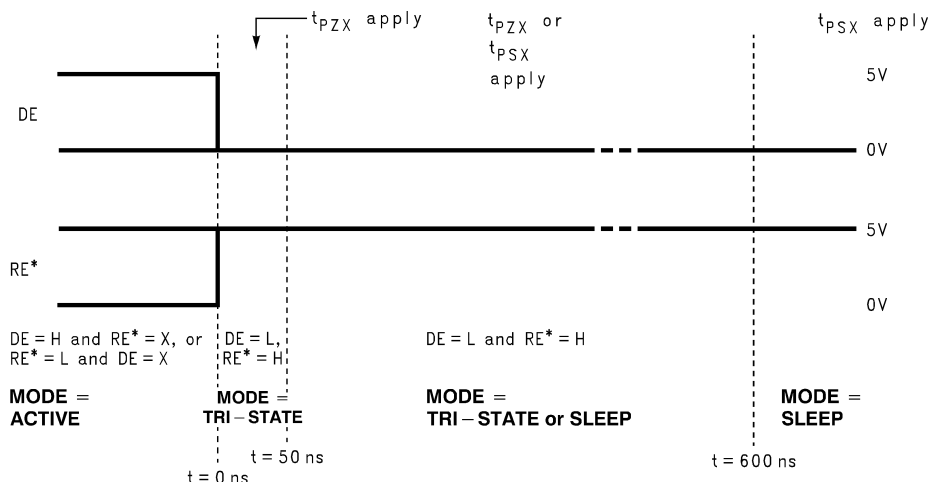


FIGURE 13.

Parameter Measurement Information (Continued)



01291915

*Note: Non Terminated, Open Input only

FIGURE 14. Entering Sleep Mode Conditions (modes and exit parameters shown)

TABLE 1. Device Pin Descriptions

Pin No.	Name	Description
1	RO	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if $DO/RI \geq DO$ (Note 1)/RI (Note 1) by 200 mV, RO will be HIGH. If $DO/RI \leq DO$ (Note 1)/RI (Note 1) by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
2	RE (Note 1)	Receiver Output Enable: When RE (Note 1) is LOW the receiver output is enabled. When RE (Note 1) is HIGH, the receiver output is in TRI-STATE (OFF). When RE (Note 1) is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
3	DE	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). When RE (Note 1) is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
4	DI	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO (Note 1)/RI (Note 1) will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO (Note 1)/RI (Note 1) is LOW.
5	GND	Ground Connection.
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO (Note 1) /RI (Note 1)	Driver Output/Receiver Input, 485 Bus Pin.
8	V _{CC}	Positive Power Supply Connection: Recommended operating range for V _{CC} is +4.75V to +5.25V.

Unit Load

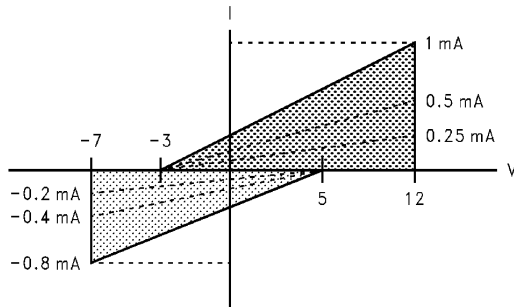
A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from -7V to +12V. The top border extending from -3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to -7V at -0.8 mA is also defined as one unit load (see Figure 15). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes.

The DS481 has ½ unit load and will allow up to 64 nodes guaranteed over temperature.

For a ½ UL device the top and bottom borders shown in Figure 15 are scaled. Both 0 mA reference points at +5V and -3V stay the same. The other reference points are +12V at +0.5 mA for the top border and -7V at -0.4 mA for the bottom border (see Figure 15). Again, both 0 mA reference points at +5V and -3V stay the same. The other reference points are +12V at +0.25 mA for the top border and -7V at -0.2 mA for the bottom border (see Figure 15).

Unit Load (Continued)

The advantage of the $\frac{1}{2}$ UL device is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS481 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.



01291916

FIGURE 15. Input Current vs Input Voltage Operating Range

the sleep mode is automatic, no external components are required. It may be used as little or as much as the application requires. The more the feature is utilized, the more power it saves.

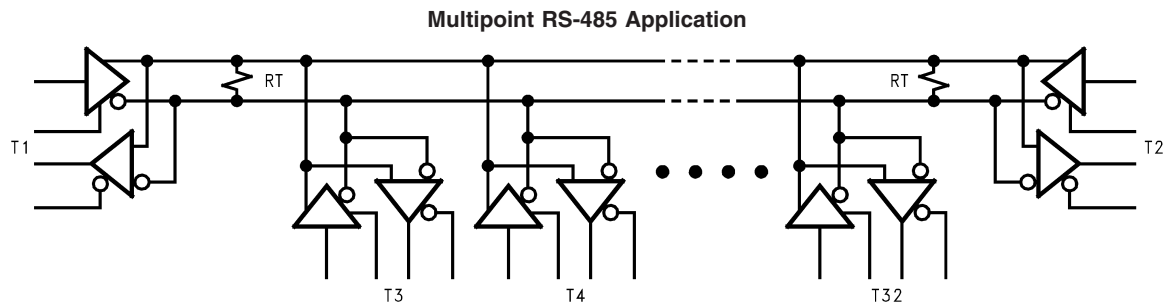
The sleep mode is automatically entered when both the driver and receiver are disabled. This occurs when both the DE pin is asserted to a logic low and the RE (Note 1) pin is asserted to a logic high. Once both pins are asserted the device will enter sleep mode after 50 ns. The DS481 is guaranteed to go into sleep mode within 600 ns after both pins are asserted. The device wakes up (comes out of sleep mode) when either the DE pin is asserted to a logic high and/or the RE (Note 1) pin is asserted to a logic low. After the device enters sleep mode it will take longer for the device to wake up than it does for the device to enable from TRI-STATE. Refer to datasheet specifications t_{PSL} and t_{PSH} and compare with t_{PZL} and t_{PZH} for timing differences.

The benefit of the DS481 is definitely its power savings. When active the device has a maximum I_{CC} of 500 μ A. When in sleep mode the device has a maximum I_{CC} of only 10 μ A, which is 50 times less power than when active. The I_{CC} when the device is active is already very low but when in sleep mode the I_{CC} is ultra low.

Applications Information

Sleep Mode

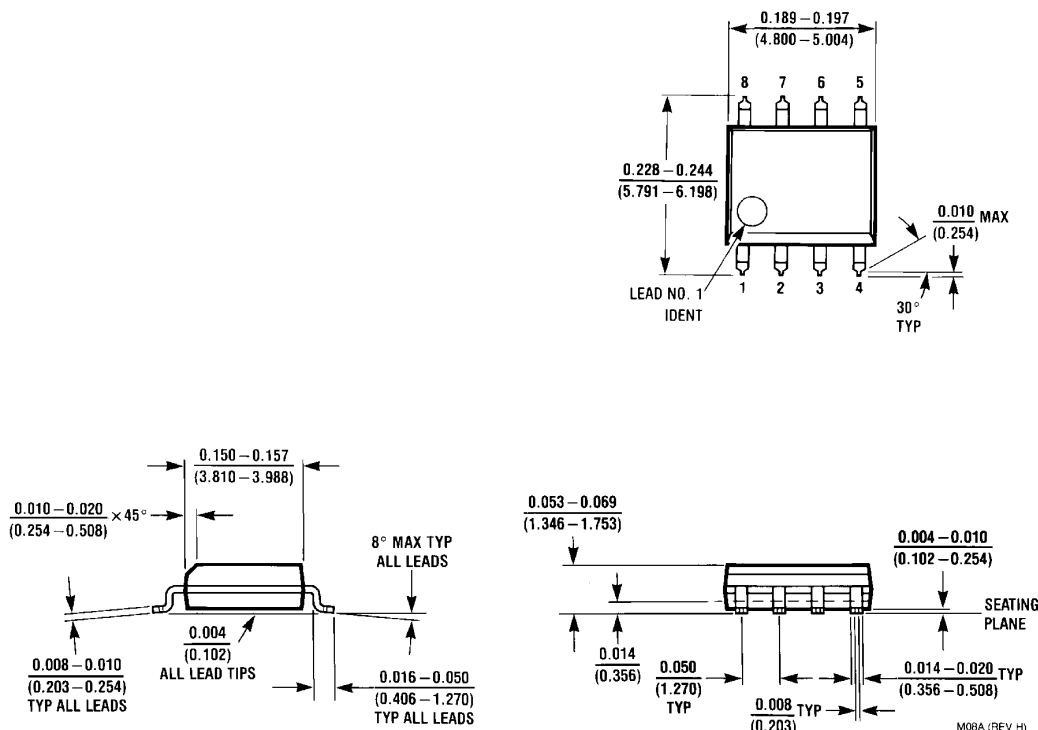
The DS481 features an automatic sleep mode that allows the device to save power when not transmitting data. Since



01291917

Physical Dimensions inches (millimeters)

unless otherwise noted



Order Number DS481TM
NS Package Number M08A

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