

SN74ALVCH16901

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

SCES010E – JULY 1995 – REVISED FEBRUARY 1999

- Member of the Texas Instruments *Widebus+*™ Family
- *EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Simultaneously Generates and Checks Parity
- Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Shrink Small-Outline Package

description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The SN74ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (\overline{LEAB} or LEBA), and dual 9-bit clock-enable (CLKENAB or CLKENBA) inputs. It also provides parity-enable (SEL) and parity-select (ODD/EVEN) inputs and separate error-signal (\overline{ERRA} or ERRB) outputs for checking parity. The direction of data flow is controlled by \overline{OEAB} and OEBA. When SEL is low, the parity functions are enabled. When SEL is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16901 is characterized for operation from -40°C to 85°C .

DGG PACKAGE
(TOP VIEW)

| | | | | |
|-----------------------|----|--|----|-----------------------|
| $\overline{1CLKENAB}$ | 1 | | 64 | $\overline{1CLKENBA}$ |
| LEAB | 2 | | 63 | LEBA |
| CLKAB | 3 | | 62 | CLKBA |
| $\overline{1ERRA}$ | 4 | | 61 | $\overline{1ERRB}$ |
| $\overline{1APAR}$ | 5 | | 60 | $\overline{1BPAR}$ |
| GND | 6 | | 59 | GND |
| 1A1 | 7 | | 58 | 1B1 |
| 1A2 | 8 | | 57 | 1B2 |
| 1A3 | 9 | | 56 | 1B3 |
| V_{CC} | 10 | | 55 | V_{CC} |
| 1A4 | 11 | | 54 | 1B4 |
| 1A5 | 12 | | 53 | 1B5 |
| 1A6 | 13 | | 52 | 1B6 |
| GND | 14 | | 51 | GND |
| 1A7 | 15 | | 50 | 1B7 |
| 1A8 | 16 | | 49 | 1B8 |
| 2A1 | 17 | | 48 | 2B1 |
| 2A2 | 18 | | 47 | 2B2 |
| GND | 19 | | 46 | GND |
| 2A3 | 20 | | 45 | 2B3 |
| 2A4 | 21 | | 44 | 2B4 |
| 2A5 | 22 | | 43 | 2B5 |
| V_{CC} | 23 | | 42 | V_{CC} |
| 2A6 | 24 | | 41 | 2B6 |
| 2A7 | 25 | | 40 | 2B7 |
| 2A8 | 26 | | 39 | 2B8 |
| GND | 27 | | 38 | GND |
| $\overline{2APAR}$ | 28 | | 37 | $\overline{2BPAR}$ |
| $\overline{2ERRA}$ | 29 | | 36 | $\overline{2ERRB}$ |
| \overline{OEAB} | 30 | | 35 | OEBA |
| SEL | 31 | | 34 | ODD/EVEN |
| $\overline{2CLKENAB}$ | 32 | | 33 | $\overline{2CLKENBA}$ |

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WITH PARITY GENERATORS/CHECKERS

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Function Tables

FUNCTION†

| INPUTS | | | | | OUTPUT B |
|---------|------|------|-------|---|------------------|
| CLKENAB | OEAB | LEAB | CLKAB | A | |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | B ₀ ‡ |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | B ₀ ‡ |
| L | L | L | H | X | B ₀ § |

† A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY ENABLE

| INPUTS | | | OPERATION OR FUNCTION | |
|--------|------|------|-----------------------------------------------------------------------------------------|----------------------------------------------------|
| SEL | OEBA | OEAB | | |
| L | H | L | Parity is checked on port A and is generated on port B. | |
| L | L | H | Parity is checked on port B and is generated on port A. | |
| L | H | H | Parity is checked on port B and port A. | |
| L | L | L | Parity is generated on port A and B if device is in FF mode. | |
| H | L | L | Parity functions are disabled; device acts as a standard 18-bit registered transceiver. | |
| H | L | H | | Q _A data to B, Q _B data to A |
| H | H | L | | Q _B data to A |
| H | H | H | | Q _A data to B Isolation |

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Function Tables (Continued)

| PARITY | | | | | | | | | | | |
|--------|------|------|----------|---------------------------------|---------------------------------|------|------|---------|------|------|------|
| INPUTS | | | | | | | | OUTPUTS | | | |
| SEL | OEBA | OEAB | ODD/EVEN | Σ OF INPUTS A1–A8 = H | Σ OF INPUTS B1–B8 = H | APAR | BPAR | APAR | ERRA | BPAR | ERRB |
| L | H | L | L | 0, 2, 4, 6, 8 | N/A | L | N/A | N/A | H | L | Z |
| L | H | L | L | 1, 3, 5, 7 | N/A | L | N/A | N/A | L | H | Z |
| L | H | L | L | 0, 2, 4, 6, 8 | N/A | H | N/A | N/A | L | L | Z |
| L | H | L | L | 1, 3, 5, 7 | N/A | H | N/A | N/A | H | H | Z |
| L | L | H | L | N/A | 0, 2, 4, 6, 8 | N/A | L | L | Z | N/A | H |
| L | L | H | L | N/A | 1, 3, 5, 7 | N/A | L | L | H | Z | N/A |
| L | L | H | L | N/A | 0, 2, 4, 6, 8 | N/A | H | L | Z | N/A | L |
| L | L | H | L | N/A | 1, 3, 5, 7 | N/A | H | L | H | Z | N/A |
| L | H | L | H | 0, 2, 4, 6, 8 | N/A | L | N/A | N/A | L | H | Z |
| L | H | L | H | 1, 3, 5, 7 | N/A | L | N/A | N/A | H | L | Z |
| L | H | L | H | 0, 2, 4, 6, 8 | N/A | H | N/A | N/A | H | H | Z |
| L | H | L | H | 1, 3, 5, 7 | N/A | H | N/A | N/A | L | L | Z |
| L | L | H | H | N/A | 0, 2, 4, 6, 8 | N/A | L | L | H | Z | N/A |
| L | L | H | H | N/A | 1, 3, 5, 7 | N/A | L | L | L | Z | N/A |
| L | L | H | H | N/A | 0, 2, 4, 6, 8 | N/A | H | L | H | Z | N/A |
| L | L | H | H | N/A | 1, 3, 5, 7 | N/A | H | L | L | Z | N/A |
| L | H | H | L | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | L | L | Z | H | Z | H |
| L | H | H | L | 1, 3, 5, 7 | 1, 3, 5, 7 | L | L | Z | L | Z | L |
| L | H | H | L | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | H | H | Z | L | Z | L |
| L | H | H | L | 1, 3, 5, 7 | 1, 3, 5, 7 | H | H | Z | H | Z | H |
| L | H | H | L | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | L | L | Z | L | Z | L |
| L | H | H | L | 1, 3, 5, 7 | 1, 3, 5, 7 | L | L | Z | H | Z | H |
| L | H | H | L | 0, 2, 4, 6, 8 | 0, 2, 4, 6, 8 | H | H | Z | H | Z | H |
| L | H | H | L | 1, 3, 5, 7 | 1, 3, 5, 7 | H | H | Z | L | Z | L |
| L | L | L | L | N/A | N/A | N/A | N/A | PE† | Z | PE† | Z |
| L | L | L | H | N/A | N/A | N/A | N/A | PO‡ | Z | PO‡ | Z |

† Parity output is set to the level so that the specific bus side is set to even parity.

‡ Parity output is set to the level so that the specific bus side is set to odd parity.

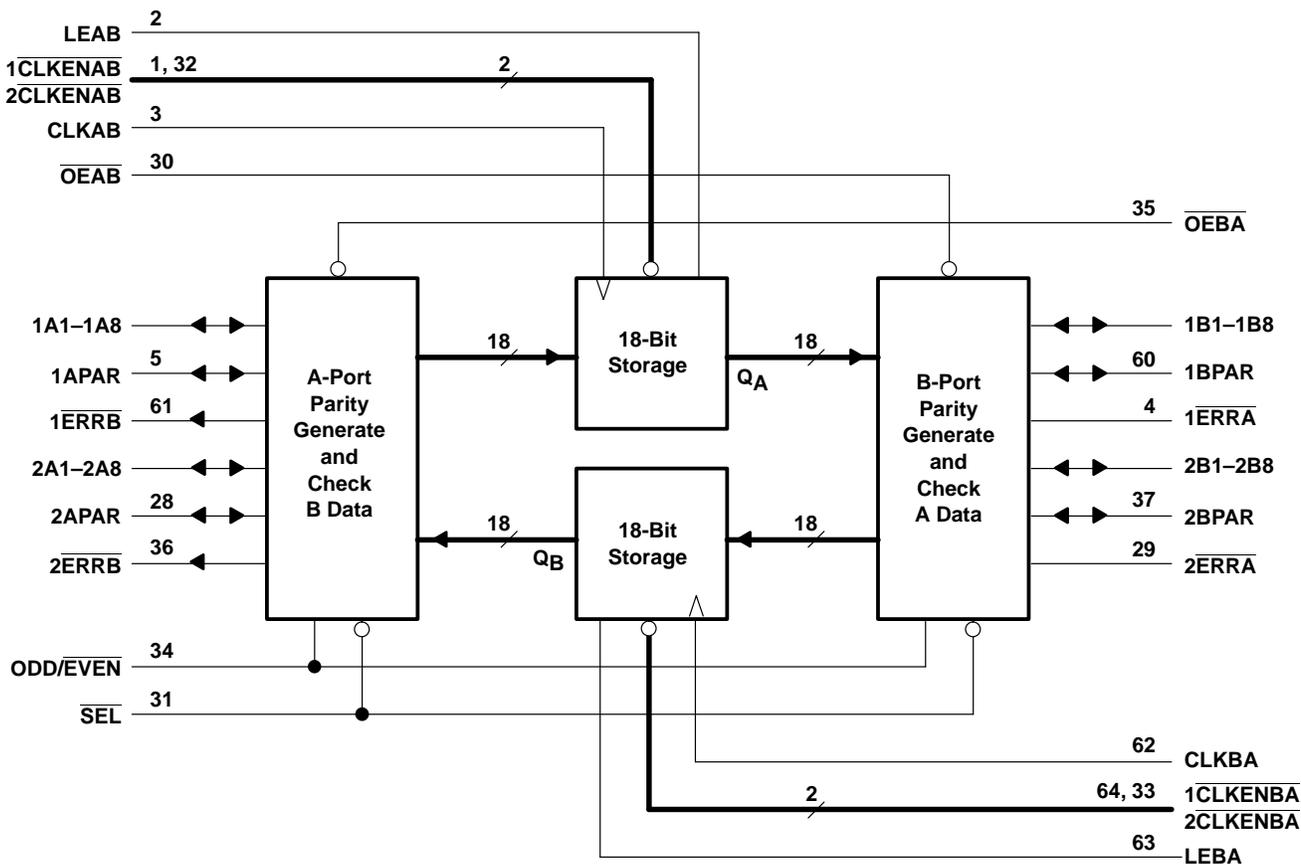


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functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|------------------------------------------------------------------|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Input voltage range, V_I : Except I/O ports (see Note 1) | -0.5 V to 4.6 V |
| I/O ports (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Continuous output current, I_O | ± 50 mA |
| Continuous current through each V_{CC} or GND | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 3) | 73°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|------------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 1.65 | 3.6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | |
| V _I | Input voltage | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | –4 | mA |
| | | V _{CC} = 2.3 V | –12 | |
| | | V _{CC} = 2.7 V | –12 | |
| | | V _{CC} = 3 V | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | mA |
| | | V _{CC} = 2.3 V | 12 | |
| | | V _{CC} = 2.7 V | 12 | |
| | | V _{CC} = 3 V | 24 | |
| Δt/Δv | Input transition rise or fall rate | | 10 | ns/V |
| T _A | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP† | MAX | UNIT |
|--------------------------|------------------------------------------------------------------------------|-----------------------------------------|----------------------|------|------|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} -0.2 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -6 mA | 2.3 V | 2 | | | |
| | I _{OH} = -12 mA | 2.3 V | 1.7 | | | |
| | | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| I _{OH} = -24 mA | 3 V | 2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 6 mA | 2.3 V | | | 0.4 | |
| | I _{OL} = 12 mA | 2.3 V | | | 0.7 | |
| | | 2.7 V | | | 0.4 | |
| I _{OL} = 24 mA | 3 V | | | 0.55 | | |
| I _I | V _I = V _{CC} or GND | 3.6 V | | | ±5 | μA |
| I _I (hold) | V _I = 0.58 V | 1.65 V | 25 | | | μA |
| | V _I = 1.07 V | 1.65 V | -25 | | | |
| | V _I = 0.7 V | 2.3 V | 45 | | | |
| | V _I = 1.7 V | 2.3 V | -45 | | | |
| | V _I = 0.8 V | 3 V | 75 | | | |
| | V _I = 2 V | 3 V | -75 | | | |
| | V _I = 0 to 3.6 V‡ | 3.6 V | | | ±500 | |
| I _{OZ} § | V _O = V _{CC} or GND | 3.6 V | | | ±10 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | | | 40 | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 3.6 V | | | 750 | μA |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | 3 | | pF |
| C _{io} | A or B ports | V _O = V _{CC} or GND | 3.3 V | 7.5 | | pF |
| C _o | ERR ports | V _O = V _{CC} or GND | 3.3 V | 6 | | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| | | | V _{CC} = 1.8 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|--------------------|-----------------|--------------------------------|-------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | † | | 125 | | 125 | | 125 | | MHz |
| t _w | Pulse duration | CLK↑ | † | | 3 | | 3 | | 3 | | ns |
| | | LE high | † | | 3 | | 3 | | 3 | | |
| t _{su} | Setup time | A, APAR or B, BPAR before CLK↑ | † | | 1.9 | | 2 | | 1.7 | | ns |
| | | CLKEN̄ before CLK↑ | † | | 2.1 | | 2.1 | | 1.7 | | |
| | | A, APAR or B, BPAR before LE↓ | † | | 1.4 | | 1.3 | | 1.2 | | |
| t _h | Hold time | A, APAR or B, BPAR after CLK↑ | † | | 0.4 | | 0.4 | | 0.5 | | ns |
| | | CLKEN̄ after CLK↑ | † | | 0.5 | | 0.5 | | 0.7 | | |
| | | A, APAR or B, BPAR after LE↓ | † | | 0.9 | | 1.1 | | 0.9 | | |

† This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|------------------|-----------------|---------------------------------|-------------------------|-----|---------------------------------|------|-------------------------|-----|---------------------------------|-----|------|
| | | | MIN | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | † | | 125 | | 125 | | 125 | | MHz |
| t _{pd} | A or B | B or A | | † | 1 | 5.2 | | 4.8 | 1 | 4.4 | ns |
| | | BPAR or APAR | | † | 2 | 8.9 | | 7.6 | 2 | 6.7 | |
| | APAR or BPAR | BPAR or APAR | | † | 1 | 5.7 | | 5.2 | 1 | 4.7 | |
| | | ERRA or ERRA | | † | 2 | 9.7 | | 8.7 | 2 | 7.5 | |
| | ODD/EVEN | ERRA or ERRA | | † | 1.5 | 8.7 | | 7.9 | 1.5 | 6.8 | |
| | | BPAR or APAR | | † | 1.5 | 8.3 | | 7.6 | 1.5 | 6.5 | |
| | SEL | BPAR or APAR | | † | 1 | 6.1 | | 5.9 | 1 | 5.1 | |
| | CLKAB or CLKBA | A or B | | † | 1 | 6.4 | | 5.8 | 1 | 5.1 | |
| | | BPAR or APAR parity feedthrough | | † | 1.5 | 7.1 | | 6.3 | 1.5 | 5.6 | |
| | | BPAR or APAR parity generated | | † | 2.5 | 10.2 | | 8.7 | 2 | 7.7 | |
| | | ERRA or ERRA | | † | 2.5 | 10.5 | | 8.9 | 2 | 7.9 | |
| | LEAB or LEBA | A or B | | † | 1 | 6 | | 5.5 | 1 | 4.8 | |
| | | BPAR or APAR parity feedthrough | | † | 1.5 | 6.7 | | 6 | 1.5 | 5.3 | |
| | | BPAR or APAR parity generated | | † | 2.5 | 9.8 | | 8.3 | 2 | 7.4 | |
| | | ERRA or ERRA | | † | 2.5 | 9.9 | | 8.5 | 2 | 7.5 | |
| | t _{en} | OEAB or OEBA | B, BPAR or A, APAR | | † | 1.4 | 6.3 | | 6.1 | 1 | |
| t _{dis} | OEAB or OEBA | B, BPAR or A, APAR | | † | 1.3 | 6.1 | | 5.2 | 1.5 | 4.9 | ns |
| t _{en} | OEAB or OEBA | ERRA or ERRA | | † | 1.4 | 6.2 | | 5.5 | 1 | 4.9 | ns |
| t _{dis} | OEAB or OEBA | ERRA or ERRA | | † | 1.3 | 7.3 | | 6.5 | 1 | 5.7 | ns |
| t _{en} | SEL | ERRA or ERRA | | † | 1.4 | 6.7 | | 6.5 | 1 | 5.5 | ns |
| t _{dis} | SEL | ERRA or ERRA | | † | 1.3 | 6.4 | | 5.4 | 1.5 | 4.9 | ns |

† This information was not available at the time of publication.

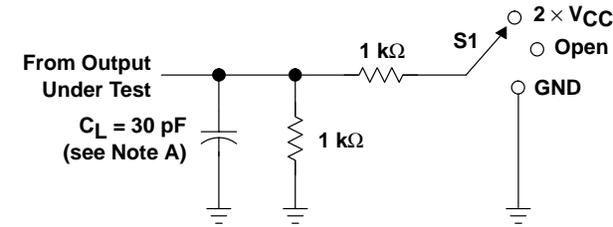
operating characteristics, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT | |
|-----------------|-------------------------------|-------------------------------------|------------------------------------|-------------------------|-------------------------|------|----|
| | | | TYP | TYP | TYP | | |
| C _{pd} | Power dissipation capacitance | Outputs enabled Outputs disabled | C _L = 50 pF, f = 10 MHz | † | 22 | 27 | pF |
| | | | | † | 5 | 8 | |

† This information was not available at the time of publication.

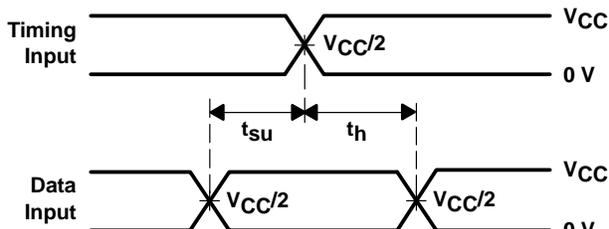


PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 1.8\text{ V}$

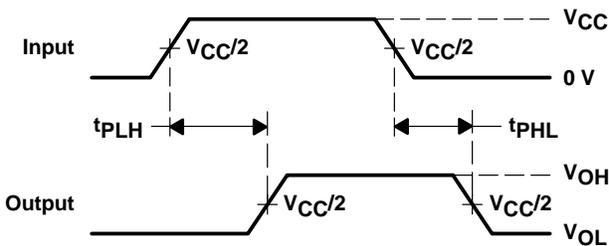


LOAD CIRCUIT

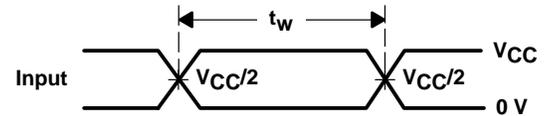
| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



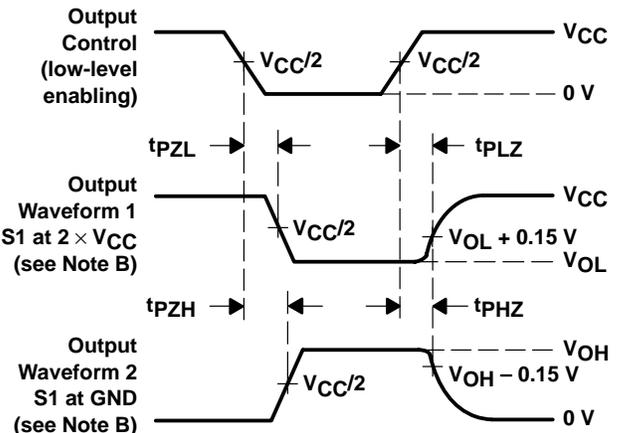
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

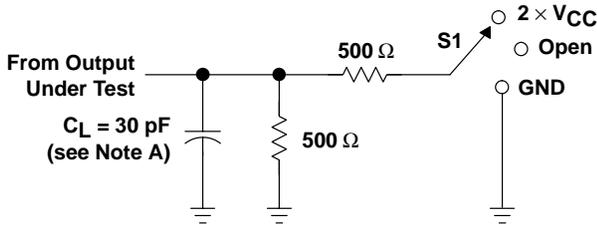
Figure 1. Load Circuit and Voltage Waveforms

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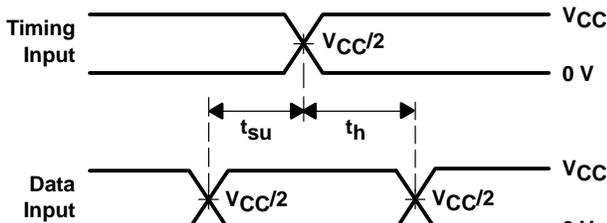
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

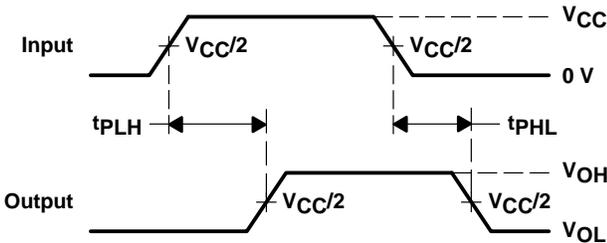


LOAD CIRCUIT

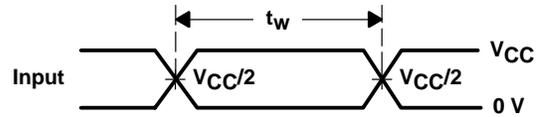
| TEST | S1 |
|-------------------|-------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |



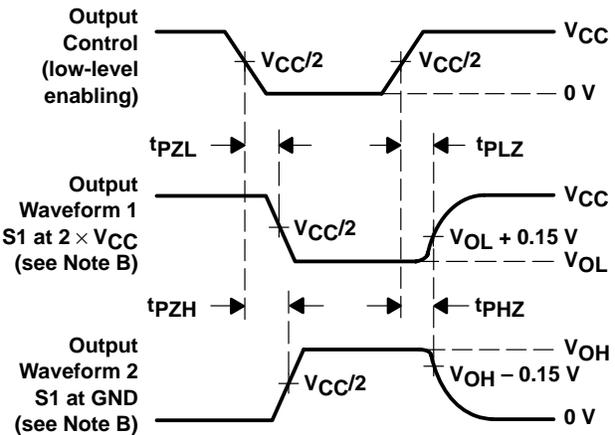
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



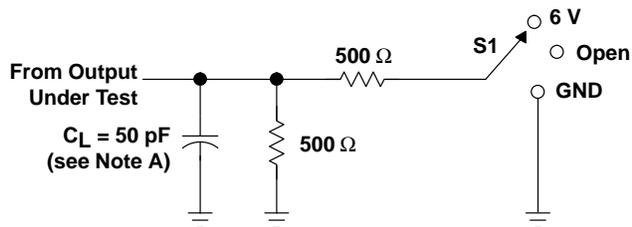
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

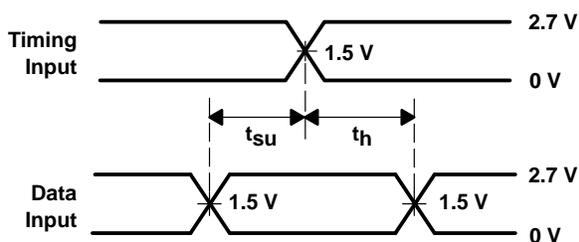
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

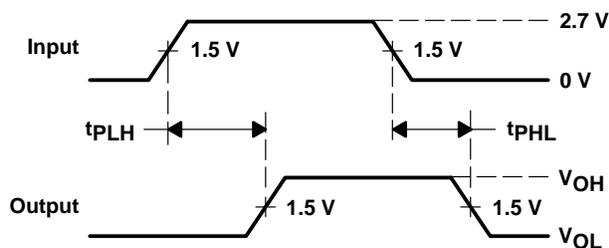


LOAD CIRCUIT

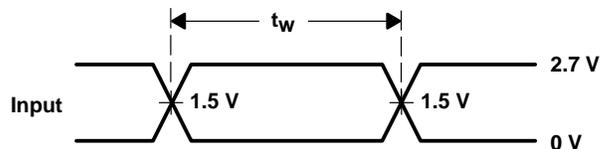
| TEST | S1 |
|-------------------|------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



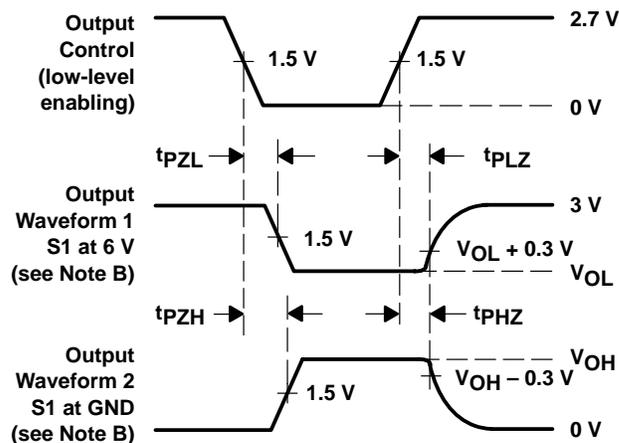
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms