

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

### 5.1 Electrical Characteristics

#### 5.1.1 Absolute maximum ratings

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~7.0	V
V <sub>I</sub>	Input voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , V <sub>REF</sub>	All voltages measured with reference to the V <sub>SS</sub> pin, output transistors isolated.	-0.3~V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage RESET, X <sub>IN</sub>		-0.3~V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage CNV <sub>SS</sub>		-0.3~13	V
V <sub>O</sub>	Output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , X <sub>OUT</sub>		-0.3~V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	500	mW
T <sub>opr</sub>	Operating temperature		-20~85	°C
T <sub>stg</sub>	Storage temperature		-40~125	°C

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

### 5.1.2 Recommended operating conditions

Recommended Operating Conditions ( $V_{CC} = 4.0$  to  $5.5V$ ,  $T_a = -20$  to  $85^{\circ}C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$V_{CC}$	Power supply voltage	4.0	5.0	5.5	V
$V_{SS}$	Power supply voltage		0		V
$V_{REF}$	Analog reference voltage (when A-D converter is used)	2.0		$V_{CC}$	V
	Analog reference voltage (when D-A converter is used)	4.0		$V_{CC}$	V
$AV_{SS}$	Analog power supply voltage		0		V
$V_{IA}$	Analog input voltage	$AN_0 \sim AN_7$	$AV_{SS}$	$V_{CC}$	V
$V_{IH}$	"H" input voltage	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7,$ $P6_0 \sim P6_7, P7_0 \sim P7_7, P8_0 \sim P8_7$	$0.8V_{CC}$	$V_{CC}$	V
$V_{IH}$	"H" input voltage	RESET, $X_{IN}, CNV_{SS}$	$0.8V_{CC}$	$V_{CC}$	V
$V_{IL}$	"L" input voltage	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7,$ $P6_0 \sim P6_7, P7_0 \sim P7_7, P8_0 \sim P8_7$	0	$0.2V_{CC}$	V
$V_{IL}$	"L" input voltage	RESET	0	$0.2V_{CC}$	V
$V_{IL}$	"L" input voltage	$X_{IN}$	0	$0.16V_{CC}$	V
$V_{IL}$	"L" input voltage	$CNV_{SS}$	0	$0.2V_{CC}$	V
$\Sigma I_{OH1}(\text{peak})$	"H" peak output total current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P8_0 \sim P8_7$		-80	mA
$\Sigma I_{OH2}(\text{peak})$	"H" peak output total current	$P4_0 \sim P4_7, P5_0 \sim P5_7, P6_0 \sim P6_7$		-80	mA
$\Sigma I_{OL1}(\text{peak})$	"L" peak output total current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P8_0 \sim P8_7$		80	mA
$\Sigma I_{OL2}(\text{peak})$	"L" peak output total current	$P4_0 \sim P4_7, P5_0 \sim P5_7, P6_0 \sim P6_7,$ $P7_0 \sim P7_7$		80	mA
$\Sigma I_{OH1}(\text{avg})$	"H" average output total current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P8_0 \sim P8_7$ (Note 1)		-40	mA
$\Sigma I_{OH2}(\text{avg})$	"H" average output total current	$P4_0 \sim P4_7, P5_0 \sim P5_7, P6_0 \sim P6_7$ (Note 1)		-40	mA
$\Sigma I_{OL1}(\text{avg})$	"L" average output total current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P8_0 \sim P8_7$ (Note 1)		40	mA
$\Sigma I_{OL2}(\text{avg})$	"L" average output total current	$P4_0 \sim P4_7, P5_0 \sim P5_7, P6_0 \sim P6_7,$ $P7_0 \sim P7_7$ (Note 1)		40	mA
$I_{OH}(\text{peak})$	"H" peak output current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7,$ $P6_0 \sim P6_7, P7_0 \sim P7_7, P8_0 \sim P8_7$		-10	mA
$I_{OL}(\text{peak})$	"L" peak output current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7,$ $P6_0 \sim P6_7, P7_0 \sim P7_7, P8_0 \sim P8_7$		10	mA
$I_{OH}(\text{avg})$	"H" average output current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7,$ $P6_0 \sim P6_7, P7_0 \sim P7_7, P8_0 \sim P8_7$ (Note 1)		-5	mA
$I_{OL}(\text{avg})$	"L" average output current	$P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7,$ $P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7,$ $P6_0 \sim P6_7, P7_0 \sim P7_7, P8_0 \sim P8_7$ (Note 1)		5	mA
$f(X_{IN})$	Internal clock oscillation frequency			5	MHz

Note 1 : The average output currents are average values measured over 100ms.

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

### 5.1.3 Electrical characteristics

Electrical Characteristics ( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{OH}$	"H" output voltage	P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> (Note 2)	$I_{OH} = -10mA$	$V_{CC} - 2.0$		V
$V_{OL}$	"L" output voltage	P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>	$I_{OL} = 10mA$		2.0	V
$V_{T+} - V_{T-}$	Hysteresis	CNTR <sub>0</sub> , CNTR <sub>1</sub> , INT <sub>0</sub> ~INT <sub>4</sub>			0.4	V
$V_{T+} - V_{T-}$	Hysteresis	RxD, SCLK			0.5	V
$V_{T+} - V_{T-}$	Hysteresis	RESET			0.5	V
$I_{IH}$	"H" input current	P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>	$V_i = V_{CC}$			5.0 $\mu A$
$I_{IH}$	"H" input current	RESET, CNV <sub>SS</sub>	$V_i = V_{CC}$			5.0 $\mu A$
$I_{IH}$	"H" input current	X <sub>IN</sub>	$V_i = V_{CC}$		4	$\mu A$
$I_{IL}$	"L" input current	P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>	$V_i = V_{SS}$			-5.0 $\mu A$
$I_{IL}$	"L" input current	RESET, CNV <sub>SS</sub>	$V_i = V_{SS}$			-5.0 $\mu A$
$I_{IL}$	"L" input current	X <sub>IN</sub>	$V_i = V_{SS}$		-4	$\mu A$
$V_{RAM}$	RAM retention voltage		Clock is stopped	2.0		5.5 V
$I_{CC}$	Power supply current (Note 3)	$I(X_{IN}) = 5MHz$			4	8 mA
		$I(X_{IN}) = 5MHz$ (wait mode)			1	mA
		With all oscillation stopped (stop mode)	$T_a = 25^\circ C$	0.1	1	$\mu A$
			$T_a = 85^\circ C$		10	$\mu A$

Note 2 : P4<sub>s</sub> is measured when the P4<sub>5</sub>/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B<sub>16</sub>) is "0".

Note 3 : Not including the current flowing through the V<sub>REF</sub> pin. The A-D converter has completed conversion. Output transistors isolated.

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

### 5.1.4 A-D converter characteristics

A-D Converter Characteristics ( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $V_{REF} = 2.0V$  to  $V_{CC}$ ,  $T_a = -20$  to  $85^\circ C$ ,  $f(X_{IN}) = 5MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limit			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute accuracy (disregarding quantization error)			$\pm 1$	$\pm 2.5$	LSB
$t_{CONV}$	Conversion time				50	$t_c(\phi)$
$R_{LADDER}$	Ladder resistor			35		$k\Omega$
$I_{VREF}$	Reference power supply input current	(Note 4)	50	150	200	$\mu A$
$I(AD)$	A-D port input current			0.5		$\mu A$

Note 4 : When D-A conversion registers (addresses 0036<sub>16</sub> and 0037<sub>16</sub>) are at "00<sub>16</sub>".

### 5.1.5 D-A converter characteristics

D-A Converter Characteristics ( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $V_{REF} = 4.0V$  to  $V_{CC}$ ,  $T_a = -20$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
$t_{SU}$	Setting time				3	$\mu s$
$R_o$	Output resistor		1	2.5	4	$k\Omega$
$I_{VREF}$	Reference power supply input current	(Note 5)			3.2	$mA$

Note 5 : Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00<sub>16</sub>", and not including the ladder resistor of A-D converter.

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

### 5.1.6 Timing requirements and switching characteristics

#### Timing Requirements

( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			$\mu s$
$t_c(X_{IN})$	External clock input cycle time	200			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	50			ns
$t_c(\text{CNTR})$	CNTR <sub>0</sub> , CNTR <sub>1</sub> input cycle time	200			ns
$t_{WH}(\text{CNTR})$	CNTR <sub>0</sub> , CNTR <sub>1</sub> , INT <sub>0</sub> to INT <sub>4</sub> input "H" pulse width	80			ns
$t_{WL}(\text{CNTR})$	CNTR <sub>0</sub> , CNTR <sub>1</sub> , INT <sub>0</sub> to INT <sub>4</sub> input "L" pulse width	80			ns
$t_c(\text{SCLK}_1)$	Serial clock input 1 cycle time	800			ns
$t_c(\text{SCLK}_2)$	Serial clock input 2 cycle time	1000			ns
$t_{WH}(\text{SCLK}_1)$	Serial clock input 1 "H" pulse width (Note 6)	370			ns
$t_{WH}(\text{SCLK}_2)$	Serial clock input 2 "H" pulse width	400			ns
$t_{WL}(\text{SCLK}_1)$	Serial clock input 1 "L" pulse width (Note 6)	370			ns
$t_{WL}(\text{SCLK}_2)$	Serial clock input 2 "L" pulse width	400			ns
$t_{su}(\text{Rx}D\text{-SCLK}_1)$	Serial input 1 setup time	220			ns
$t_{su}(\text{SIN}_2\text{-SCLK}_2)$	Serial input 2 setup time	200			ns
$t_h(\text{SCLK}_1\text{-Rx}D)$	Serial input 1 hold time	100			ns
$t_h(\text{SCLK}_2\text{-SIN}_2)$	Serial input 2 hold time	200			ns

Note 6 : When  $f(X_{IN}) = 5\text{MHz}$  and bit 6 of address 001A<sub>16</sub> is "1". The minimum time is quarter of the value when  $f(X_{IN}) = 5\text{MHz}$  and bit 6 of address 001A<sub>16</sub> is "0".

#### Switching Characteristics

( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(\text{SCLK}_1)$	Serial clock output 1 "H" pulse width	$t_c(\text{SCLK}_1)/2\text{-}30$			ns
$t_{WL}(\text{SCLK}_1)$	Serial clock output 1 "L" pulse width	$t_c(\text{SCLK}_1)/2\text{-}30$			ns
$t_{WH}(\text{SCLK}_2)$	Serial clock output 2 "H" pulse width	$t_c(\text{SCLK}_2)/2\text{-}160$			ns
$t_{WL}(\text{SCLK}_2)$	Serial clock output 2 "L" pulse width	$t_c(\text{SCLK}_2)/2\text{-}160$			ns
$t_d(\text{SCLK}_1\text{-Tx}D)$	Serial output delay time (Note 7)			140	ns
$t_d(\text{SCLK}_2\text{-SOUT}_2)$	Serial output delay time			0.2 $t_c$	
$t_v(\text{SCLK}_1\text{-Tx}D)$	Serial output hold time (Note 7)	-30			ns
$t_v(\text{SCLK}_2\text{-SOUT}_2)$	Serial output hold time	0			
$t_r$	Total CMOS pin rise time (Note 8)		10	30	ns
$t_f$	Total CMOS pin fall time (Note 8)		10	30	ns

Note 7 : When the P4<sub>5</sub>/Tx<sub>D</sub> P-channel output disable bit of the UART control register (bit 4 of address 001B<sub>16</sub>) is at "0".

Note 8 : X<sub>OUT</sub> pin excluded.

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

Memory Expansion Mode and Microprocessor Mode Timing Requirements  
 ( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su}(\overline{ONW} - \phi)$	$\overline{ONW}$ input setup time	-20			ns
$t_{h}(\phi - \overline{ONW})$	$\overline{ONW}$ input hold time	-20			ns
$t_{su}(DB - \phi)$	Data bus setup time	60			ns
$t_{h}(\phi - DB)$	Data bus hold time	0			ns

Memory Expansion Mode and Microprocessor mode Switching Characteristics  
 ( $V_{CC} = 4.0$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -20$  to  $85^\circ C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_c(\phi)$	$\phi$ clock cycle time		$2 \times t_c(X_N)$		ns
$t_{WH}(\phi)$	$\phi$ clock "H" pulse width	$t_c(X_{IN}) - 10$			ns
$t_{WL}(\phi)$	$\phi$ clock "L" pulse width	$t_c(X_{IN}) - 10$			ns
$t_d(\phi - AH)$	$AD_{15}$ to $AD_8$ delay time		20	40	ns
$t_v(\phi - AH)$	$AD_{15}$ to $AD_8$ valid time	6	10		ns
$t_d(\phi - AL)$	$AD_7$ to $AD_0$ delay time		25	45	ns
$t_v(\phi - AL)$	$AD_7$ to $AD_0$ valid time	6	10		ns
$t_d(\phi - SYNC)$	SYNC delay time		20		ns
$t_v(\phi - SYNC)$	SYNC valid time		10		ns
$t_d(\phi - WR)$	$\overline{RD}$ and $\overline{WR}$ delay time		10	20	ns
$t_v(\phi - WR)$	$\overline{RD}$ and $\overline{WR}$ valid time	3	5	10	ns
$t_d(\phi - DB)$	Data bus delay time		20	70	ns
$t_v(\phi - DB)$	Data bus valid time	15			ns
$t_d(\overline{RESET} - \overline{RESET}_{OUT})$	$\overline{RESET}_{OUT}$ output delay time (Note 9)			200	ns
$t_v(\phi - \overline{RESET})$	$\overline{RESET}_{OUT}$ output valid time (Note 9,10)	0		200	ns

Note 9 : This is valid only in microprocessor mode.

Note 10 : The  $\overline{RESET}_{OUT}$  output goes "H" with the rise of the  $\phi$  clock, between 1 cycle and 19 cycles after the  $\overline{RESET}$  input goes "H".

### 5.1.7 Test conditions

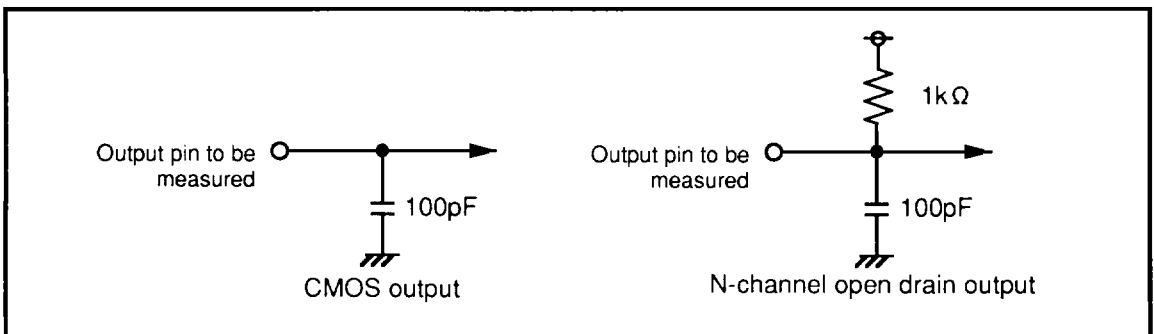
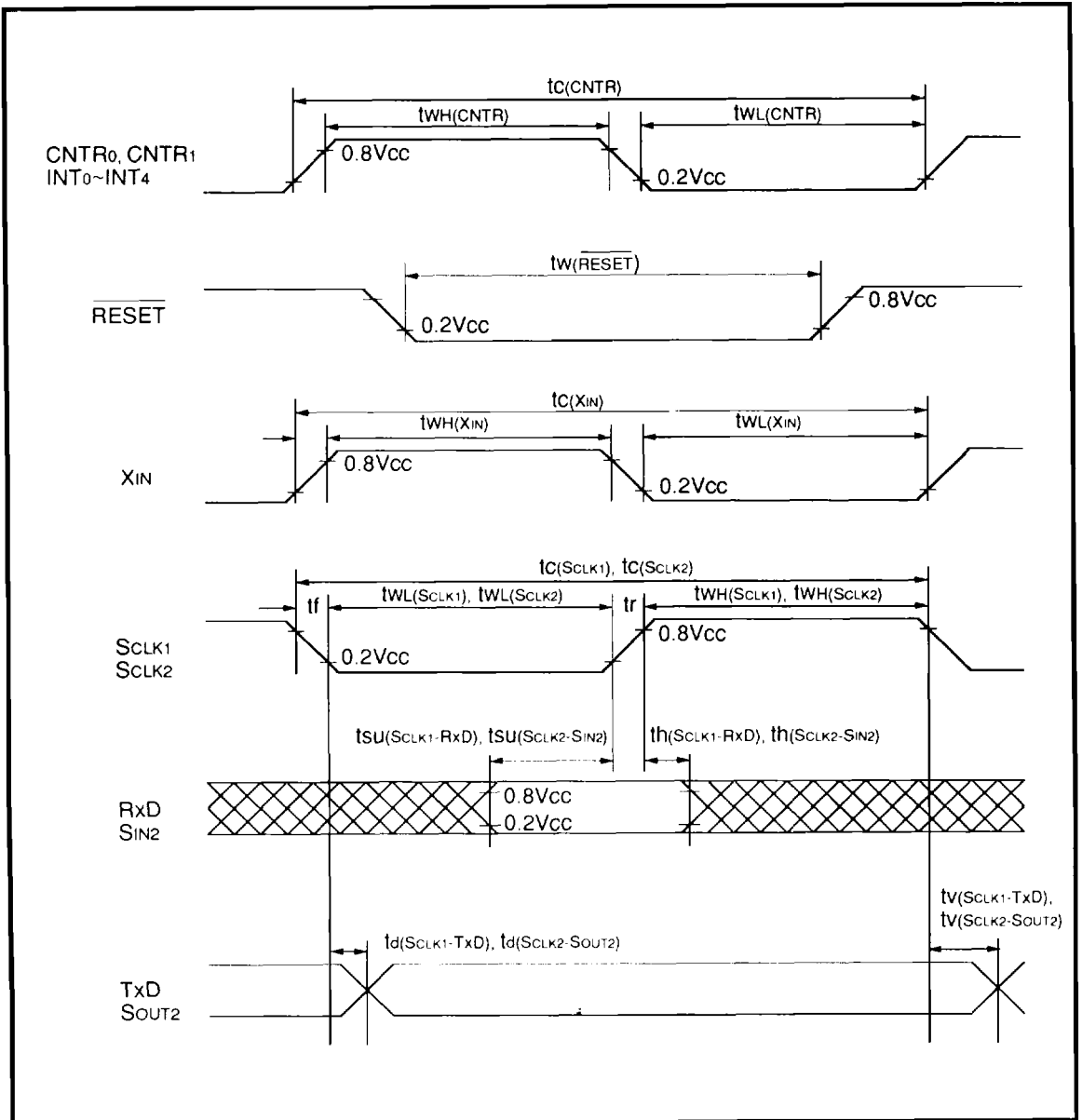


Fig. 5.1.1 Circuit for Measuring Output Switching Characteristics

# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

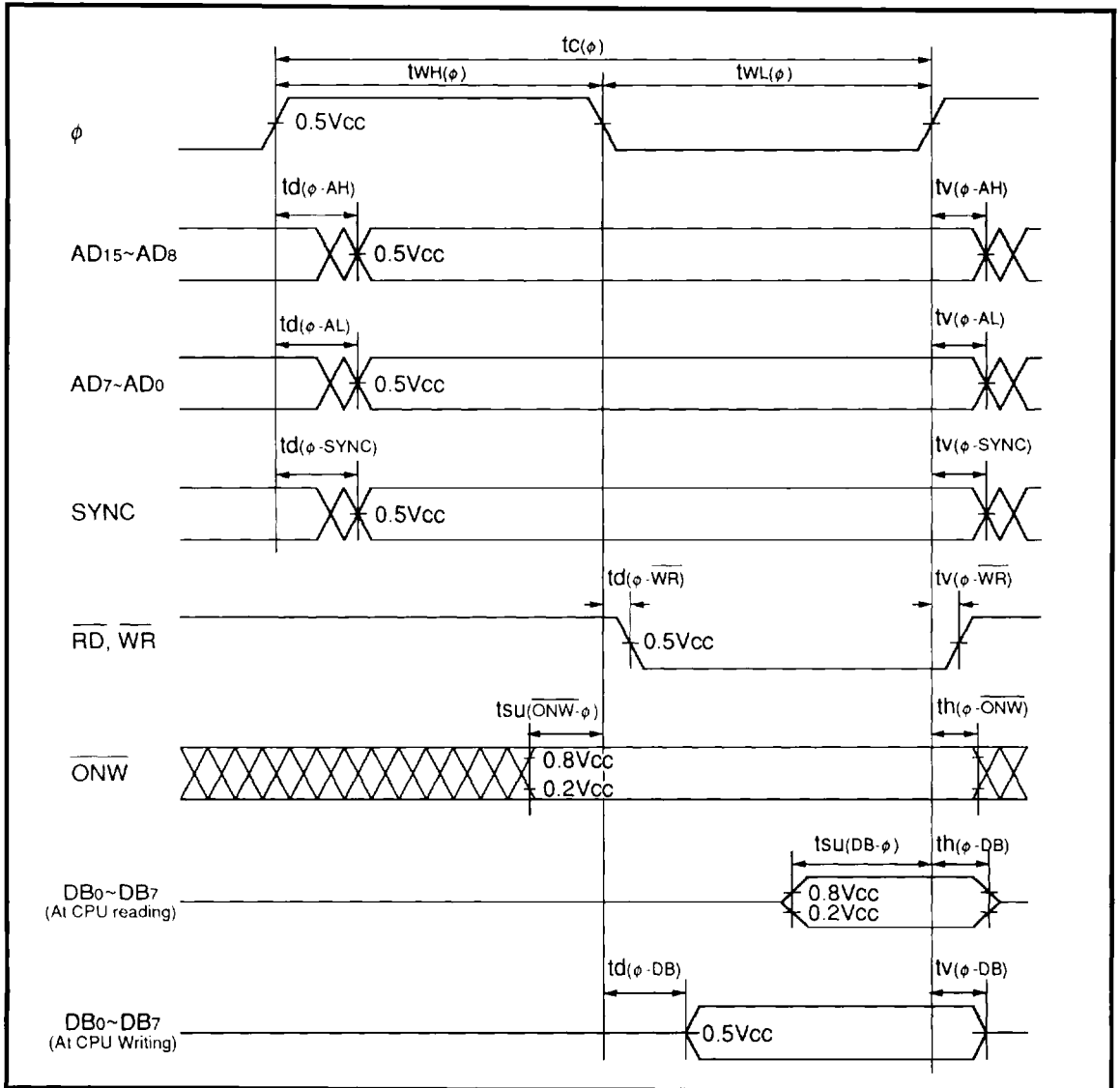
### 5.1.8 Timing diagram (1) Timing diagram



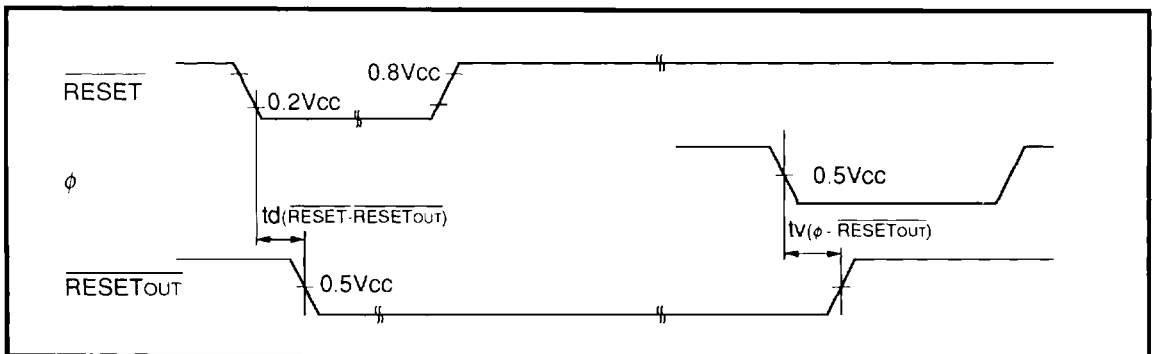
# ELECTRICAL CHARACTERISTICS

## 5.1 Electrical Characteristics

(2) Memory expansion mode, microprocessor mode



(3) Microprocessor mode





# ELECTRICAL CHARACTERISTICS

## 5.2 Typical Characteristics

### 5.2 Typical Characteristics

#### 5.2.1 Typical current consumption

The typical current consumption of the M38063M6-XXXFP/GP is as shown in Figure 5.2.1.

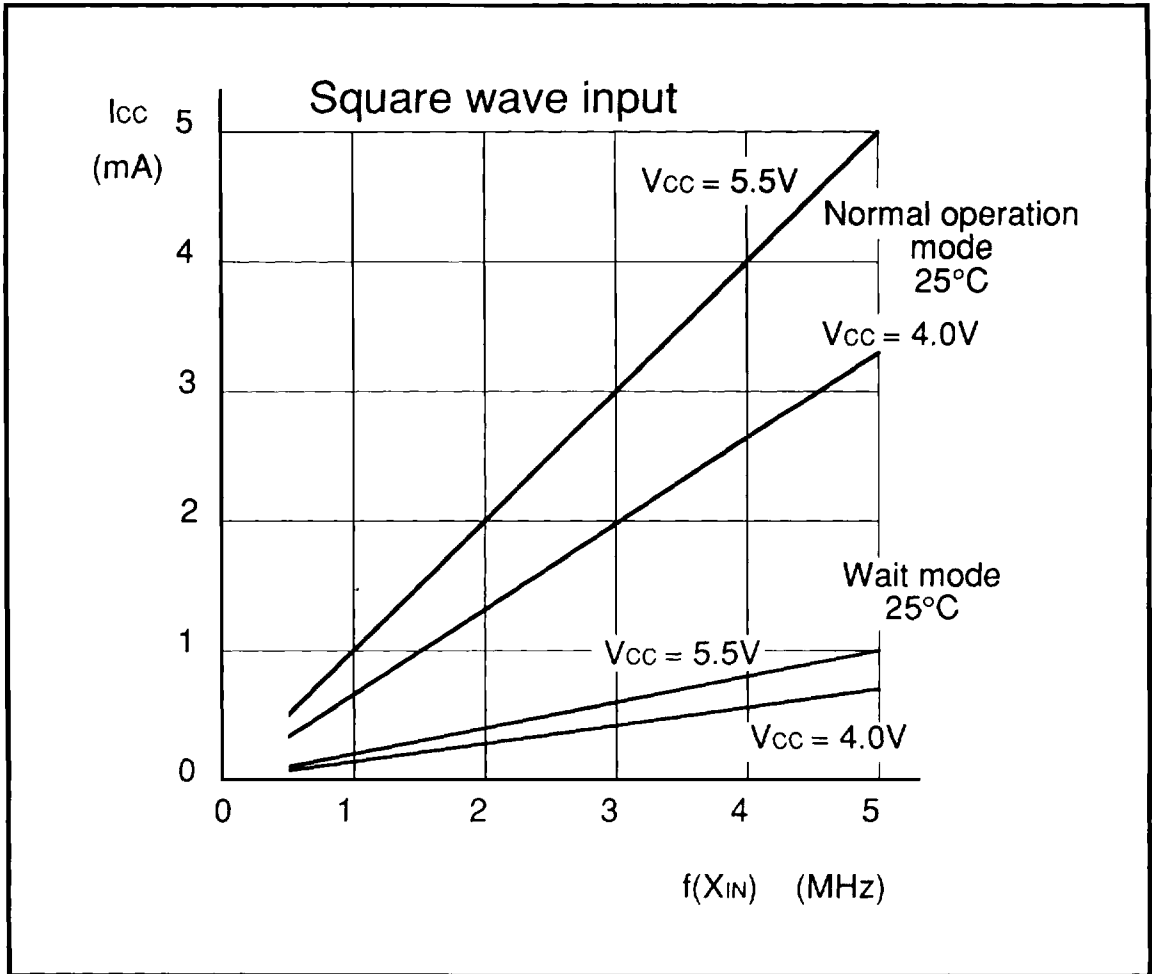


Fig. 5.2.1 Typical Current Consumption

# ELECTRICAL CHARACTERISTICS

## 5.2 Typical Characteristics

### 5.2.2 Typical port characteristics

Typical port characteristics of the M38063M6-XXXFP/GP are shown in Figures 5.2.2 and 5.2.3

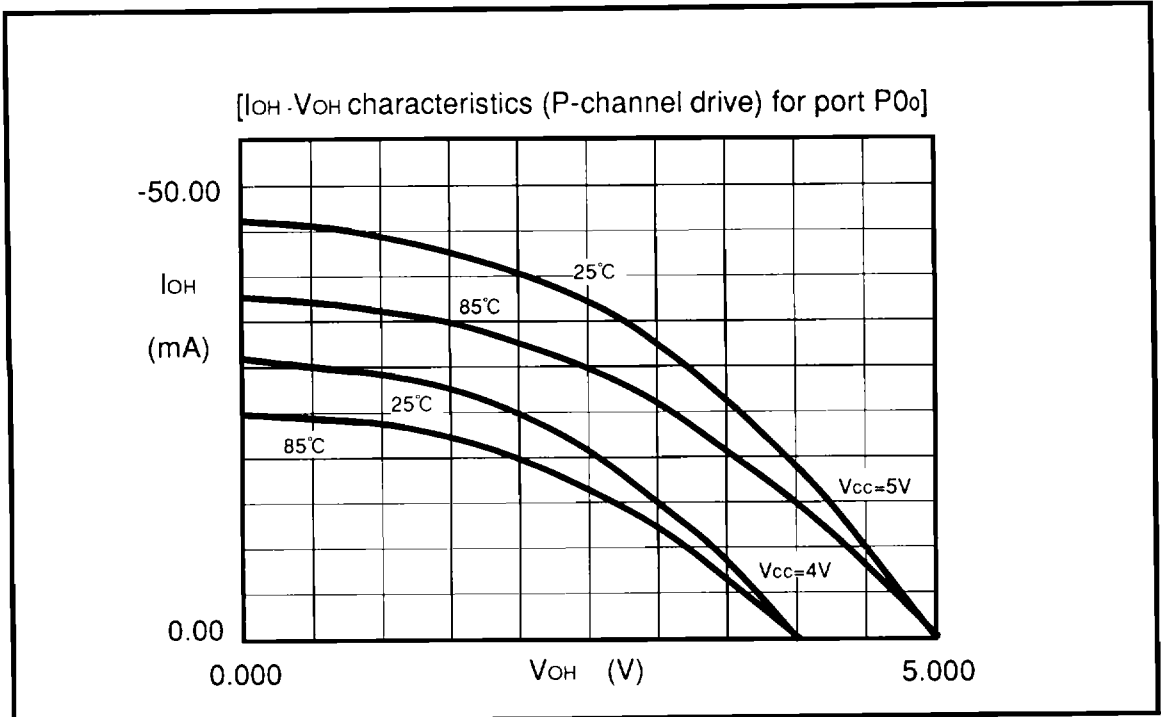


Fig. 5.2.2 Typical Characteristics of Port P0 P-Channel Output Transistor

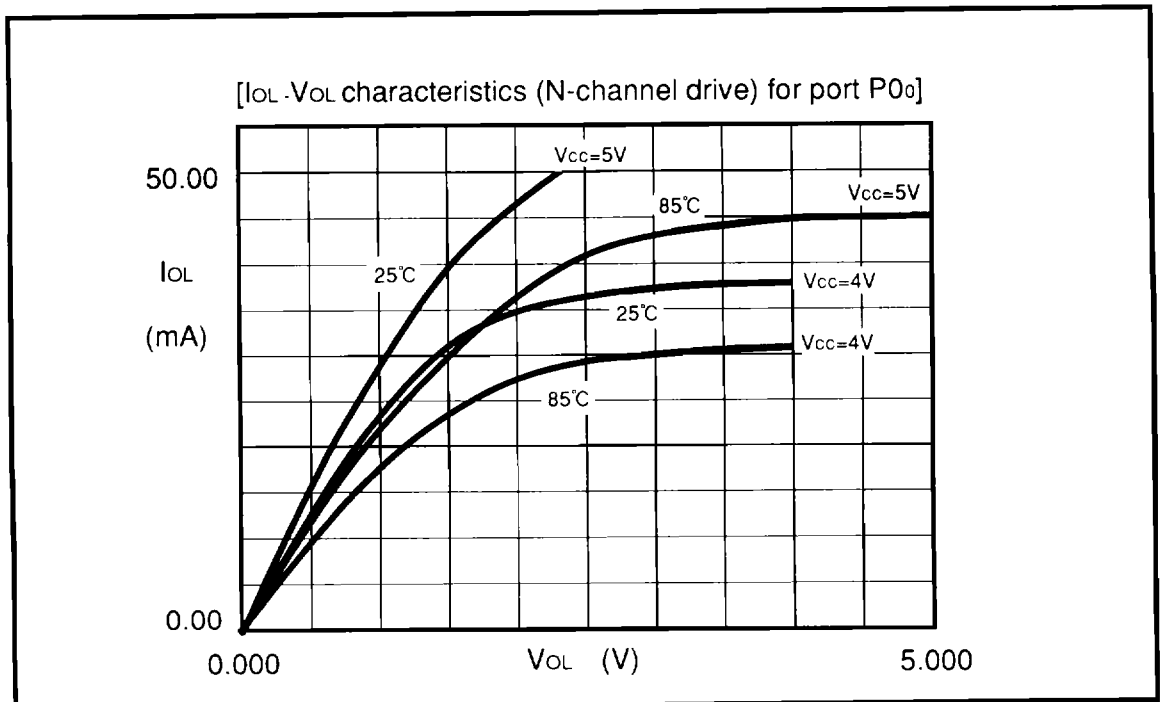


Fig. 5.2.3 Typical Characteristics of Port P0 N-Channel Output Transistor

# ELECTRICAL CHARACTERISTICS

## 5.2 Typical Characteristics

### 5.2.3 Typical A-D conversion characteristics

Typical A-D conversion characteristics of the M38063M6-XXXFP/GP are shown in Figure 5.2.4. The line in the lower part of the graph shows the absolute accuracy error. This indicates the deviation from the ideal value at the point that the A-D output changes. For example, the change in the A-D output from  $00_{16}$  to  $01_{16}$  should ideally occur at the point that  $AN_1 = 10\text{mV}$ , but since it changes at  $0\text{mV}$ , the error is:  $10 - 0 = 10\text{mV}$ .

The line in the upper part of the graph shows the step width of the input voltage at any given A-D output value. For example, the measured step width of the input voltage is  $22\text{mV}$  when the A-D code is  $0D_{16}$ , and the non-linearity error is  $22 - 20 = 2\text{mV}$  (0.3 LSB).

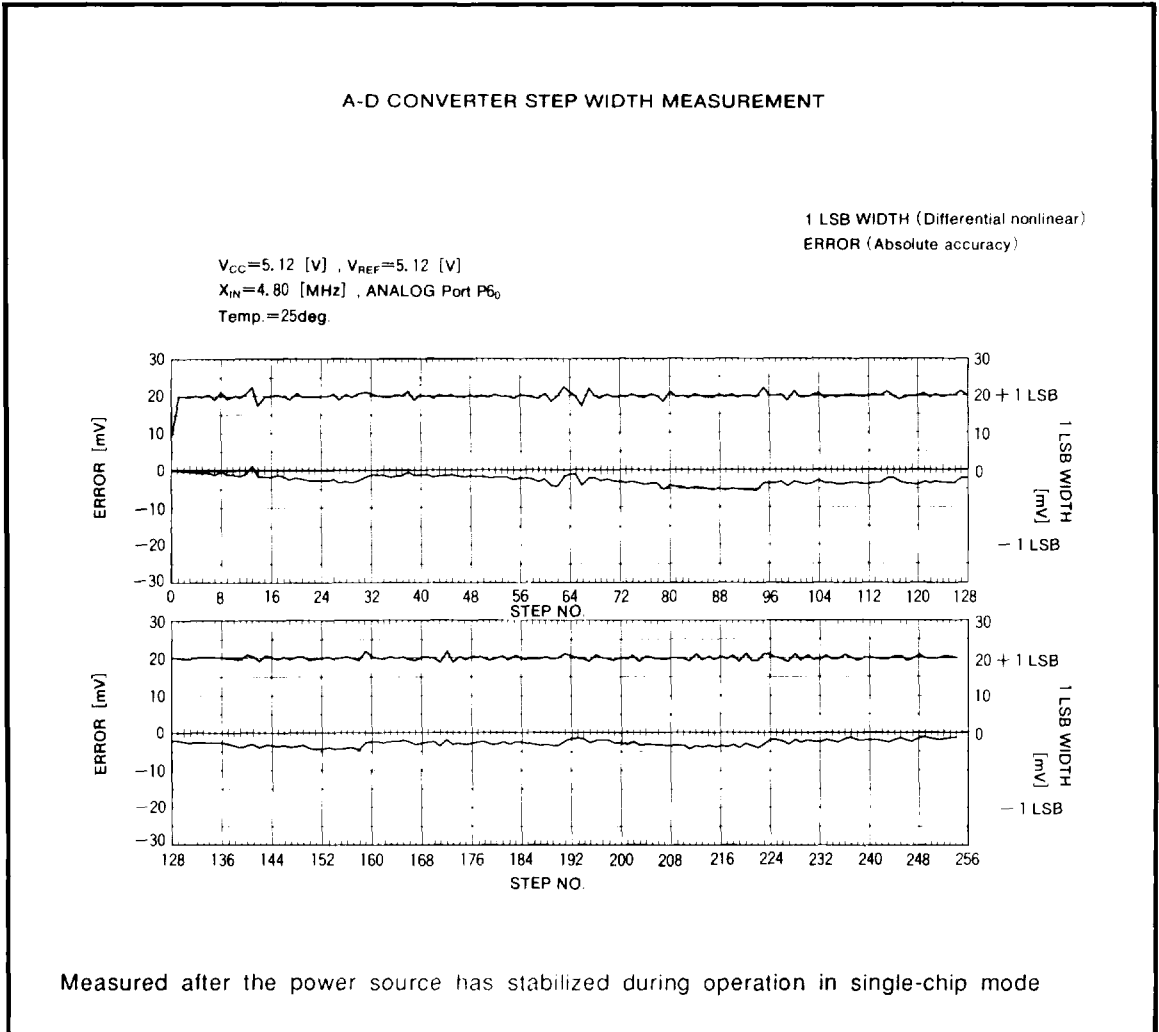


Fig. 5.2.4 Typical A-D Conversion Characteristics

# ELECTRICAL CHARACTERISTICS

## 5.2 Typical Characteristics

### 5.2.4 Typical D-A conversion characteristics

Typical D-A conversion characteristics of the M38063M6-XXXFP/GP are shown in Figure 5.2.5. The line in the lower part of the graph shows absolute accuracy error. This indicates the difference between the ideal analog output and the measured output value. The line in the upper part of the graph shows the step width of the output analog value for a one-bit change in the value input to the D-A converter.

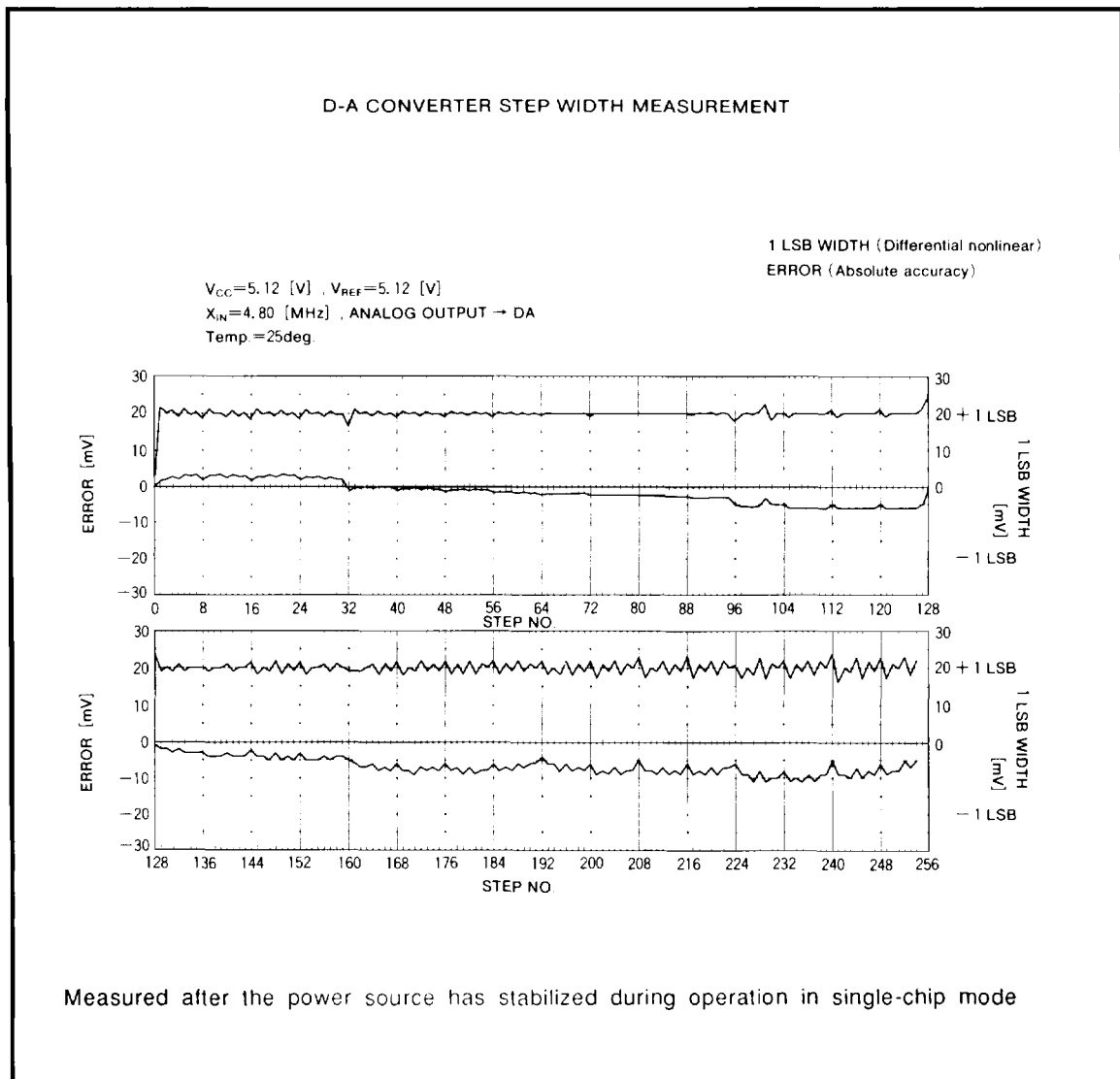


Fig. 5.2.5 Typical D-A Conversion Characteristics