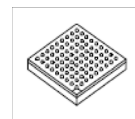


P5020/P5010

QorIQ P5020/P5010 Data Sheet



FC-PBGA-1295
37.5 mm × 37.5 mm

The P5020 and P5010 QorIQ integrated communication processor combines Power Architecture® processor cores with high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices while also greatly simplifying board design.

NOTE

Unless otherwise stated, all parameters within this document apply to both the P5020 and the P5010.

The chip includes the following function and features:

- Two e5500 Power Architecture cores (one on the P5010)
 - Each core has a backside 512-Kbyte L2 Cache with ECC
 - Three levels of instructions: User, Supervisor, and Hypervisor
 - Independent boot and reset
 - Secure boot capability
- CoreNet fabric supporting coherent and non-coherent transactions amongst CoreNet endpoints
- 2-Mbyte CoreNet platform cache with ECC (one on the P5010)
- One 10-Gigabit Ethernet (XAUI) controller
- Five 1-Gigabit Ethernet controllers
 - 1 Gb/s SGMII, 2.5 Gb/s SGMII and RGMII interfaces
- Two 64-bit DDR3/3L SDRAM memory controllers with ECC (one on the P5010)
- Multicore programmable interrupt controller (MPIC)
- Four I²C controllers
- Four 2-pin UARTs or two 4-pin UARTs

- Two 4-channel DMA engines
- Enhanced local bus controller (eLBC)
- Four PCI Express 2.0 controllers/ports
- Two Serial RapidIO® controllers/ports (sRIO port) v1.3-compliant with features of v2.1
- Two serial ATA (SATA) 2.0 controllers
- Enhanced secure digital host controller (SD/MMC)
- Enhanced serial peripheral interfaces (eSPI)
- 2× full-speed USB 2.0 controllers with integrated PHYs
- RAID 5 and 6 storage accelerator with support for end-to-end data protection information

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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This figure shows the major functional units within the P5020.

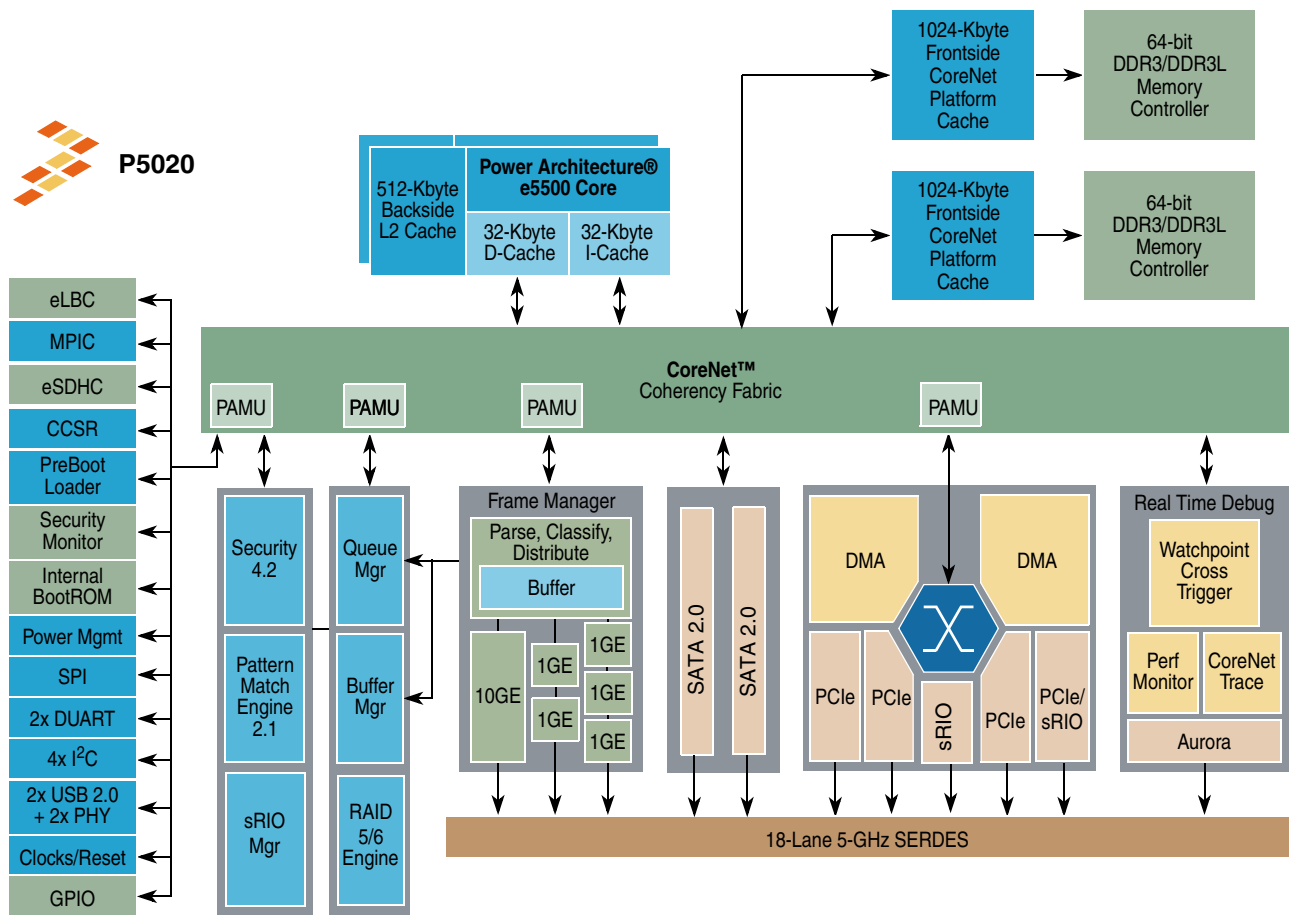


Figure 1. Preliminary P5020 block diagram

Pin assignments and reset states

This figure shows the major functional units within the P5010.

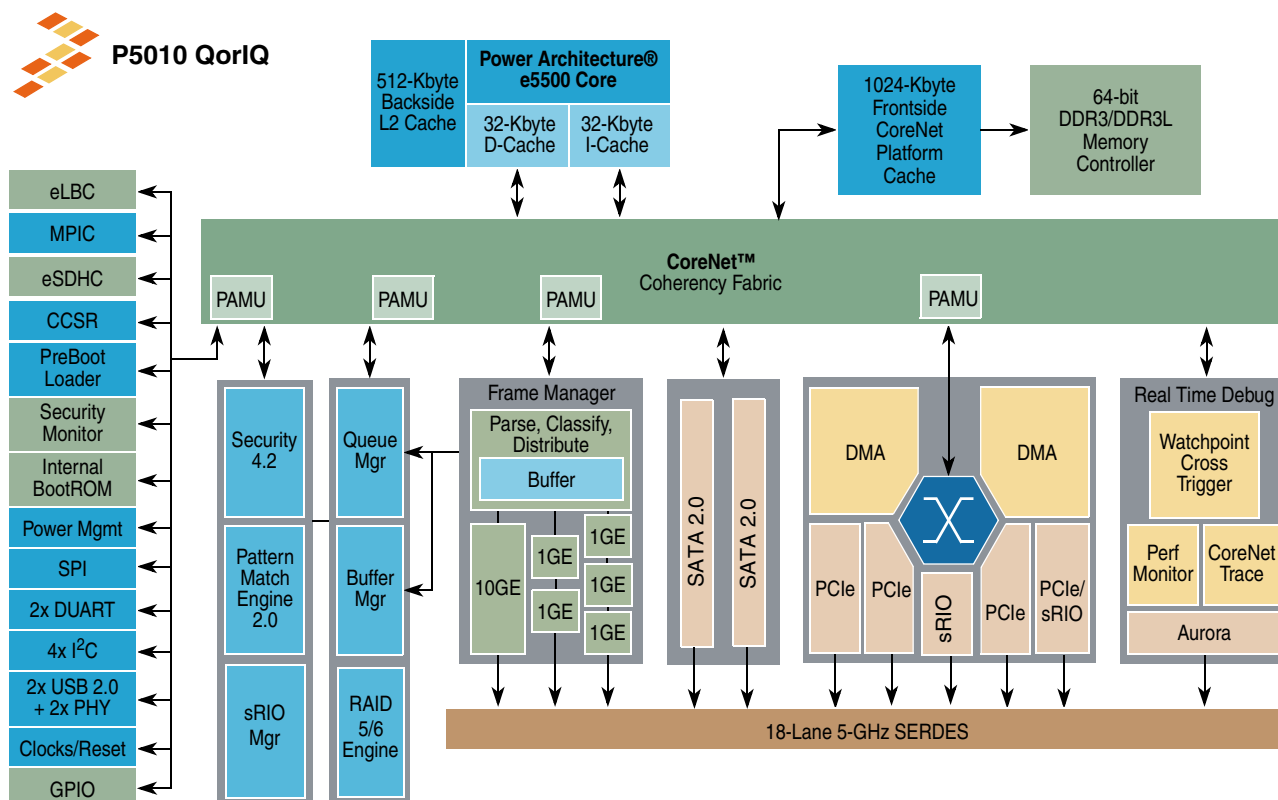


Figure 2. Preliminary P5010 block diagram

1 Pin assignments and reset states

1.1 1295 FC-PBGA ball layout diagrams

These figures show the FC-PBGA ball map diagrams.

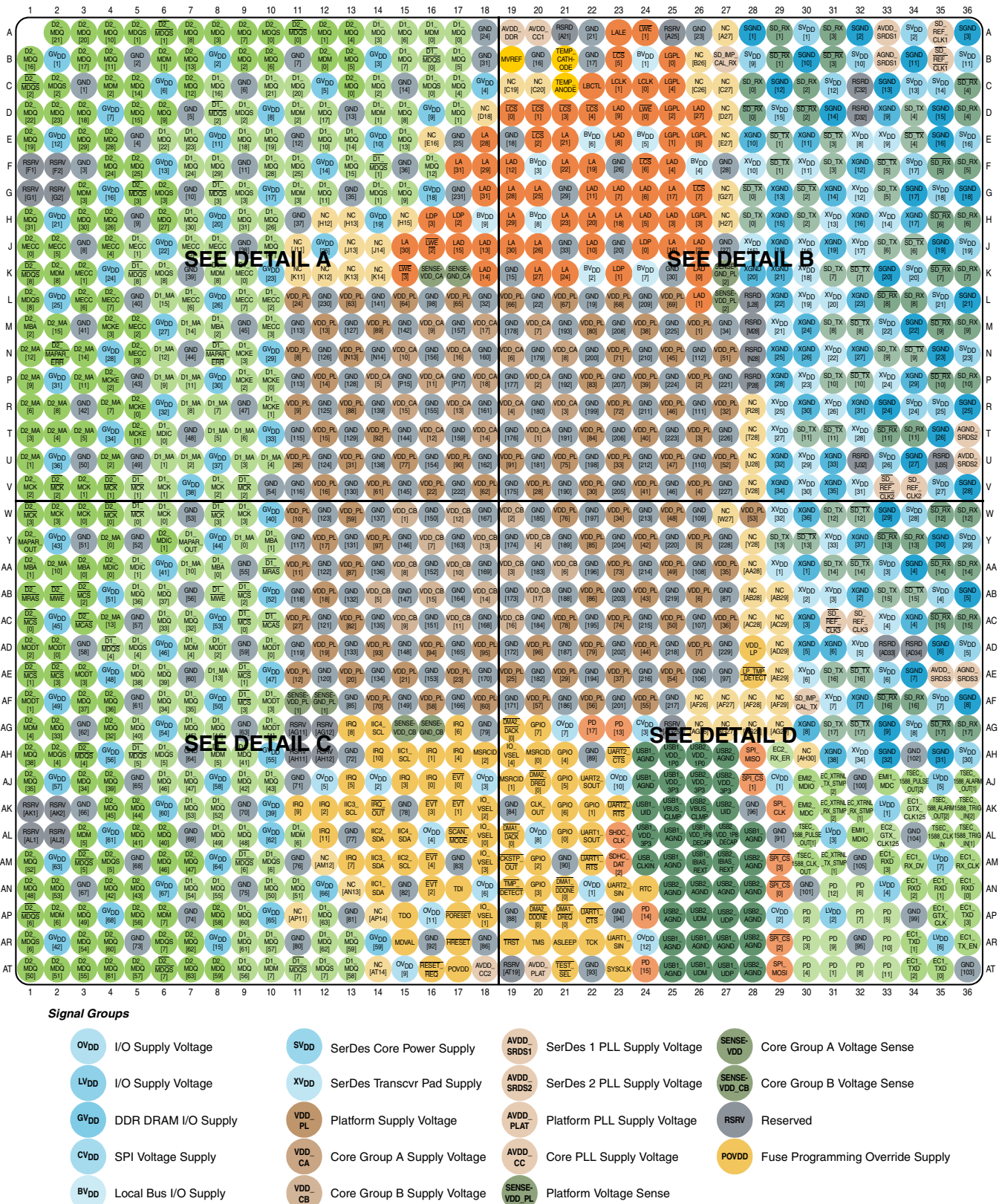


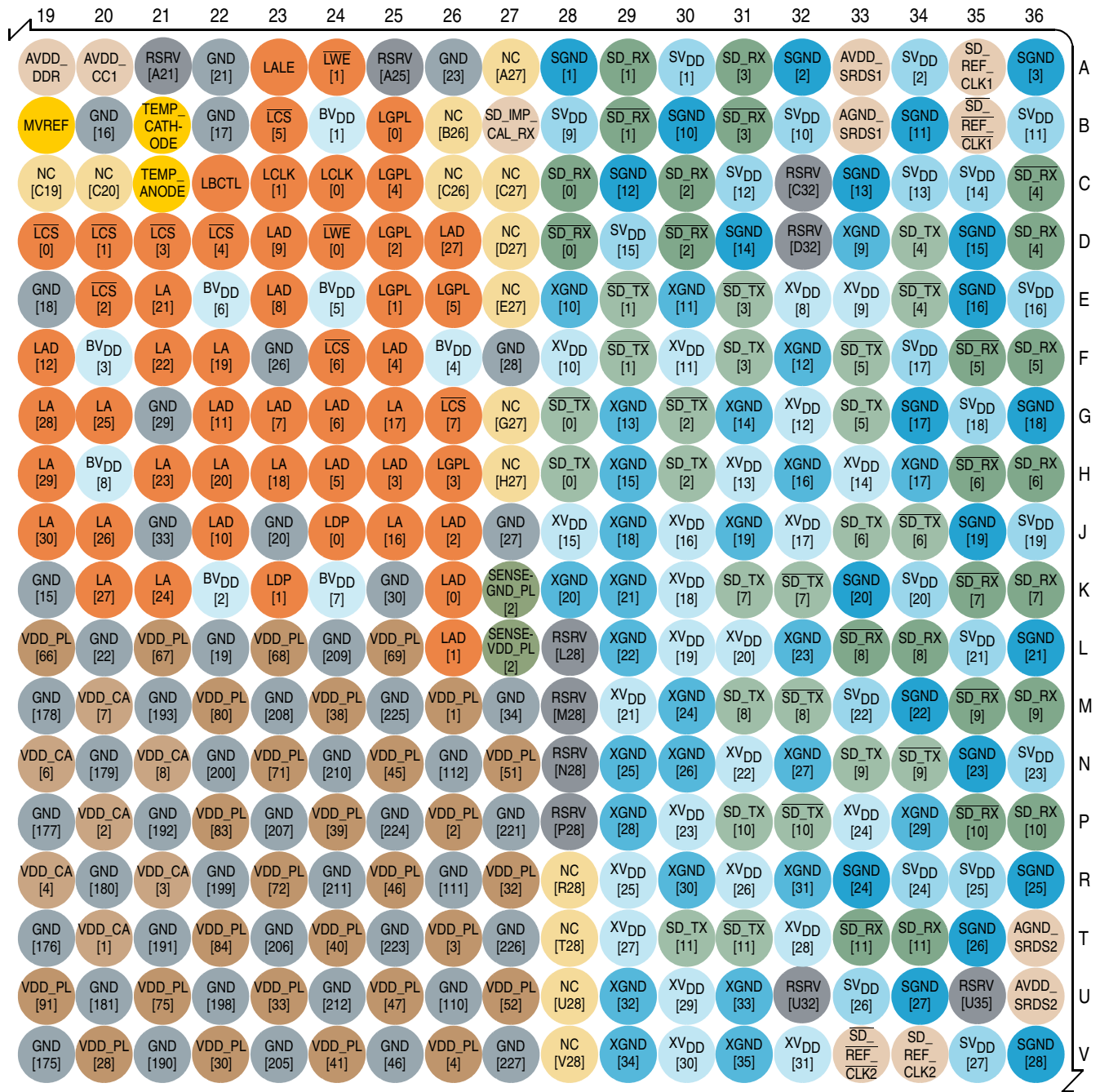
Figure 3. P5020—1295 BGA ball map diagram (top view)

Pin assignments and reset states

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		D2_MDQ [21]	D2_MDQ [20]	D2_MDQ [10]	D2_MDQS [1]	D2_MDQS [1]	D2_MDQ [8]	D2_MDQ [3]	D2_MDQ [7]	D2_MDQS [0]	D2_MDQS [0]	D2_MDQ [1]	D2_MDQ [4]	D1_MDQ [3]	D1_MDM [0]	D1_MDM [0]	D1_MDM [0]	GND [24]
B	D2_MDQ [16]	GVDD [1]	D2_MDQ [17]	D2_MDQ [11]	GND [2]	D2_MDM [1]	D2_MDQ [13]	GVDD [2]	D2_MDQ [2]	D2_MDQ [6]	GND [7]	D2_MDM [0]	D2_MDQ [5]	GVDD [3]	D1_MDQ [7]	D1_MDQS [0]	D1_MDM [5]	GND [31]
C	D2_MDQS [2]	D2_MDQS [2]	GND [1]	D2_MDM [2]	D2_MDQ [14]	GVDD [6]	D2_MDQ [12]	D1_MDQ [16]	GND [6]	D1_MDQ [21]	D1_MDQ [20]	GVDD [5]	D2_MDQ [0]	D1_MDQ [2]	GND [14]	D1_MDQS [0]	D1_MDM [4]	GVDD [4]
D	D2_MDQ [22]	D2_MDQ [23]	D2_MDQ [18]	GVDD [7]	D2_MDQ [15]	GND [5]	D1_MDQS [2]	D1_MDQS [2]	GVDD [8]	D1_MDM [2]	D1_MDM [17]	GND [13]	D1_MDM [1]	D1_MDM [8]	GVDD [9]	D1_MDM [1]	NC [D18]	
E	D2_MDQ [19]	GVDD [12]	D2_MDQ [29]	D2_MDQ [28]	GND [4]	D1_MDQ [22]	D1_MDQ [23]	GVDD [11]	D1_MDQ [18]	D1_MDQ [19]	GND [12]	D1_MDQ [10]	D1_MDM [14]	GVDD [10]	D1_MDM [13]	NC [E16]	GND [25]	LAD [28]
F	RSRV [F1]	RSRV [F2]	GND [3]	D2_MDQ [24]	D2_MDQS [25]	GVDD [13]	D1_MDQ [24]	D1_MDQS [29]	GND [11]	D1_MDM [28]	D1_MDM [25]	GVDD [14]	D1_MDQS [15]	D1_MDQS [1]	GND [36]	D1_MDM [12]	LAD [31]	LAD [29]
G	RSRV [G1]	RSRV [G2]	D2_MDM [3]	GVDD [16]	D2_MDQS [3]	D2_MDQS [3]	GND [10]	D1_MDQS [3]	D1_MDQS [3]	GVDD [17]	D1_MDM [3]	D1_MDM [11]	GND [35]	D1_MDQS [1]	D1_MDM [9]	GVDD [18]	GND [231]	LA [31]
H	D2_MDQ [31]	GVDD [21]	D2_MDQ [30]	D2_MDM [26]	GND [9]	D2_MDM [27]	D1_MDM [30]	GVDD [20]	D1_MDM [31]	D1_MDM [26]	GND [37]	NC [H12]	NC [H13]	GVDD [19]	NC [H15]	LDP [3]	LDP [2]	BVDD [9]
J	D2_MECC [0]	D2_MECC [5]	GND [8]	D2_MECC [4]	D1_MECC [1]	GVDD [22]	D1_MECC [5]	D1_MECC [4]	GND [38]	D1_MDM [27]	NC [J11]	GVDD [35]	NC [J13]	NC [J14]	LAD [30]	LWE [2]	LAD [15]	LAD [13]
K	D2_MDQS [8]	D2_MDM [8]	D2_MECC [1]	GVDD [24]	D1_MDQS [8]	D1_MDQS [8]	GND [39]	D1_MDM [8]	D1_MECC [0]	GVDD [23]	NC [K11]	NC [K12]	NC [K13]	NC [K14]	LWE [3]	SENSE-VDD_CA	SENSE-GND_CA	LAD [14]
L	D2_MDQS [8]	GVDD [25]	D2_MECC [6]	D2_MECC [7]	GND [40]	D1_MA [15]	D1_MECC [6]	GVDD [26]	D1_MECC [7]	D1_MECC [2]	VDD_PL [24]	GND [230]	VDD_PL [63]	GND [141]	VDD_PL [64]	GND [98]	VDD_PL [65]	GND [32]
M	D2_MBA [2]	D2_MA [15]	GND [41]	D2_MCKE [3]	D2_MECC [2]	GVDD [27]	D1_MA [14]	D1_MBA [2]	GND [45]	D1_MECC [3]	GND [113]	VDD_PL [13]	GND [127]	VDD_PL [89]	GND [142]	VDD_CA [9]	GND [157]	VDD_CA [17]
N	D2_MA [12]	D2_MAPAR_ERR	D2_MA [14]	GVDD [28]	D2_MECC [3]	D1_MA [12]	GND [44]	D1_MAPAR_ERR	D1_MCKE [3]	GVDD [29]	VDD_PL [8]	GND [126]	VDD_PL [81]	GND [140]	VDD_CA [10]	GND [156]	VDD_CA [16]	GND [160]
P	D2_MA [9]	GVDD [31]	D2_MA [11]	D2_MCKE [2]	GND [43]	D1_MA [9]	D1_MA [11]	GVDD [30]	D1_MCKE [2]	D1_MCKE [0]	GND [114]	VDD_PL [14]	GND [128]	VDD_CA [5]	GND [143]	VDD_CA [11]	GND [158]	VDD_CA [18]
R	D2_MA [6]	D2_MA [8]	GND [42]	D2_MA [7]	D2_MCKE [0]	GVDD [32]	D1_MA [8]	D1_MA [7]	GND [47]	D1_MCKE [1]	VDD_PL [9]	GND [125]	VDD_PL [88]	GND [139]	VDD_CA [15]	GND [155]	VDD_CA [13]	GND [161]
T	D2_MA [3]	D2_MA [4]	D2_MA [5]	GVDD [34]	D2_MCKE [1]	D1_MDIC [0]	GND [48]	D1_MA [5]	D1_MA [6]	GVDD [33]	GND [115]	VDD_PL [15]	GND [129]	VDD_PL [92]	GND [144]	VDD_CA [12]	GND [159]	VDD_CA [14]
U	D2_MA [1]	GVDD [36]	GND [50]	D2_MA [2]	GND [49]	D1_MA [1]	D1_MA [2]	GVDD [37]	D1_MA [3]	D1_MA [4]	VDD_PL [26]	GND [124]	VDD_PL [31]	GND [138]	VDD_PL [77]	GND [154]	VDD_PL [90]	GND [162]
V	D2_MCK [2]	D2_MCK [2]	D2_MCK [1]	D2_MCK [1]	D1_MCK [1]	D1_MCK [1]	GVDD [38]	D1_MCK [2]	D1_MCK [2]	GND [54]	GND [116]	VDD_PL [16]	GND [130]	VDD_PL [61]	GND [145]	VDD_PL [22]	GND [222]	VDD_PL [62]

DETAIL A

Figure 4. P5020—1295 BGA ball map diagram (detail view A)



DETAIL B

Figure 5. P5020—1295 BGA ball map diagram (detail view B)

DETAIL C

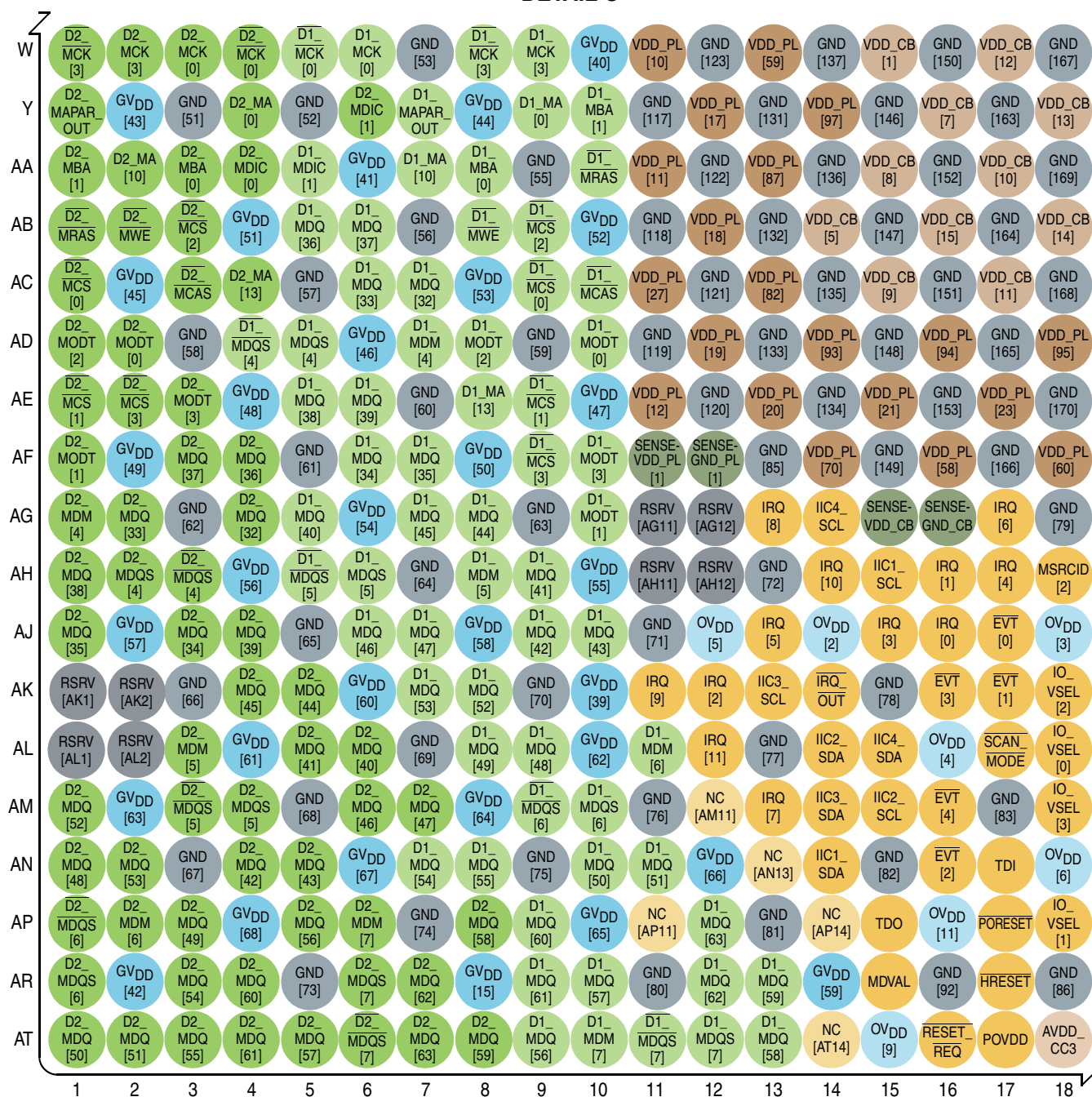


Figure 6. P5020—1295 BGA ball map diagram (detail view C)

DETAIL D

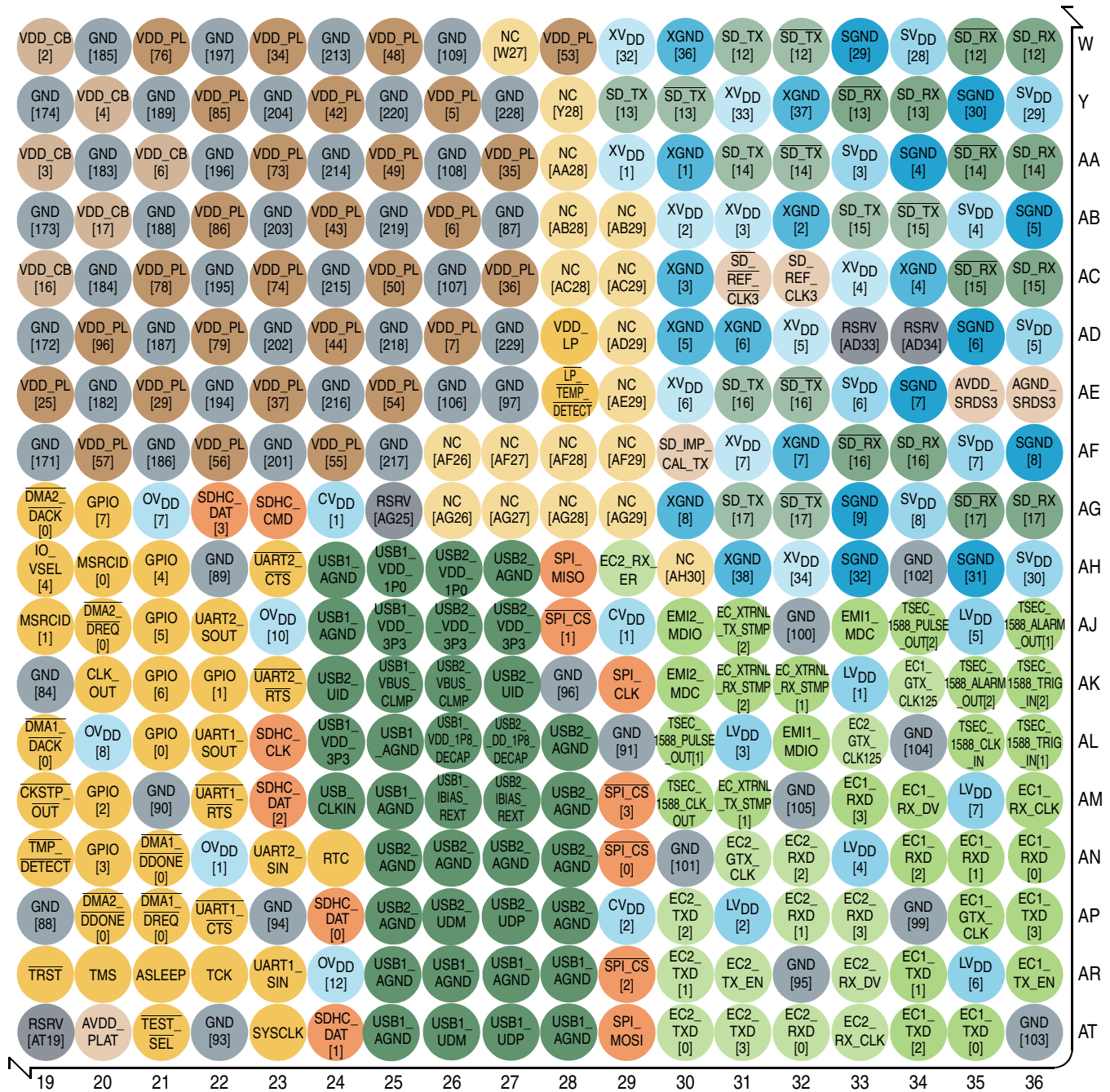


Figure 7. P5020—1295 BGA ball map diagram (detail view D)

1.2 Pinout list

This table provides the pinout listing for the 1295 FC-PBGA package by bus.

Table 1. Pins listed by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM memory interface 1					
D1_MDQ00	Data	A17	I/O	GV _{DD}	—
D1_MDQ01	Data	D17	I/O	GV _{DD}	—
D1_MDQ02	Data	C14	I/O	GV _{DD}	—
D1_MDQ03	Data	A14	I/O	GV _{DD}	—
D1_MDQ04	Data	C17	I/O	GV _{DD}	—
D1_MDQ05	Data	B17	I/O	GV _{DD}	—
D1_MDQ06	Data	A15	I/O	GV _{DD}	—
D1_MDQ07	Data	B15	I/O	GV _{DD}	—
D1_MDQ08	Data	D15	I/O	GV _{DD}	—
D1_MDQ09	Data	G15	I/O	GV _{DD}	—
D1_MDQ10	Data	E12	I/O	GV _{DD}	—
D1_MDQ11	Data	G12	I/O	GV _{DD}	—
D1_MDQ12	Data	F16	I/O	GV _{DD}	—
D1_MDQ13	Data	E15	I/O	GV _{DD}	—
D1_MDQ14	Data	E13	I/O	GV _{DD}	—
D1_MDQ15	Data	F13	I/O	GV _{DD}	—
D1_MDQ16	Data	C8	I/O	GV _{DD}	—
D1_MDQ17	Data	D12	I/O	GV _{DD}	—
D1_MDQ18	Data	E9	I/O	GV _{DD}	—
D1_MDQ19	Data	E10	I/O	GV _{DD}	—
D1_MDQ20	Data	C11	I/O	GV _{DD}	—
D1_MDQ21	Data	C10	I/O	GV _{DD}	—
D1_MDQ22	Data	E6	I/O	GV _{DD}	—
D1_MDQ23	Data	E7	I/O	GV _{DD}	—
D1_MDQ24	Data	F7	I/O	GV _{DD}	—
D1_MDQ25	Data	F11	I/O	GV _{DD}	—
D1_MDQ26	Data	H10	I/O	GV _{DD}	—
D1_MDQ27	Data	J10	I/O	GV _{DD}	—
D1_MDQ28	Data	F10	I/O	GV _{DD}	—
D1_MDQ29	Data	F8	I/O	GV _{DD}	—
D1_MDQ30	Data	H7	I/O	GV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ31	Data	H9	I/O	GV _{DD}	—
D1_MDQ32	Data	AC7	I/O	GV _{DD}	—
D1_MDQ33	Data	AC6	I/O	GV _{DD}	—
D1_MDQ34	Data	AF6	I/O	GV _{DD}	—
D1_MDQ35	Data	AF7	I/O	GV _{DD}	—
D1_MDQ36	Data	AB5	I/O	GV _{DD}	—
D1_MDQ37	Data	AB6	I/O	GV _{DD}	—
D1_MDQ38	Data	AE5	I/O	GV _{DD}	—
D1_MDQ39	Data	AE6	I/O	GV _{DD}	—
D1_MDQ40	Data	AG5	I/O	GV _{DD}	—
D1_MDQ41	Data	AH9	I/O	GV _{DD}	—
D1_MDQ42	Data	AJ9	I/O	GV _{DD}	—
D1_MDQ43	Data	AJ10	I/O	GV _{DD}	—
D1_MDQ44	Data	AG8	I/O	GV _{DD}	—
D1_MDQ45	Data	AG7	I/O	GV _{DD}	—
D1_MDQ46	Data	AJ6	I/O	GV _{DD}	—
D1_MDQ47	Data	AJ7	I/O	GV _{DD}	—
D1_MDQ48	Data	AL9	I/O	GV _{DD}	—
D1_MDQ49	Data	AL8	I/O	GV _{DD}	—
D1_MDQ50	Data	AN10	I/O	GV _{DD}	—
D1_MDQ51	Data	AN11	I/O	GV _{DD}	—
D1_MDQ52	Data	AK8	I/O	GV _{DD}	—
D1_MDQ53	Data	AK7	I/O	GV _{DD}	—
D1_MDQ54	Data	AN7	I/O	GV _{DD}	—
D1_MDQ55	Data	AN8	I/O	GV _{DD}	—
D1_MDQ56	Data	AT9	I/O	GV _{DD}	—
D1_MDQ57	Data	AR10	I/O	GV _{DD}	—
D1_MDQ58	Data	AT13	I/O	GV _{DD}	—
D1_MDQ59	Data	AR13	I/O	GV _{DD}	—
D1_MDQ60	Data	AP9	I/O	GV _{DD}	—
D1_MDQ61	Data	AR9	I/O	GV _{DD}	—
D1_MDQ62	Data	AR12	I/O	GV _{DD}	—
D1_MDQ63	Data	AP12	I/O	GV _{DD}	—
D1_MECC0	Error Correcting Code	K9	I/O	GV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MECC1	Error Correcting Code	J5	I/O	GV _{DD}	—
D1_MECC2	Error Correcting Code	L10	I/O	GV _{DD}	—
D1_MECC3	Error Correcting Code	M10	I/O	GV _{DD}	—
D1_MECC4	Error Correcting Code	J8	I/O	GV _{DD}	—
D1_MECC5	Error Correcting Code	J7	I/O	GV _{DD}	—
D1_MECC6	Error Correcting Code	L7	I/O	GV _{DD}	—
D1_MECC7	Error Correcting Code	L9	I/O	GV _{DD}	—
D1_MAPAR_ERR	Address Parity Error	N8	I	GV _{DD}	40
D1_MAPAR_OUT	Address Parity Out	Y7	O	GV _{DD}	—
D1_MDM0	Data Mask	A16	O	GV _{DD}	—
D1_MDM1	Data Mask	D14	O	GV _{DD}	—
D1_MDM2	Data Mask	D11	O	GV _{DD}	—
D1_MDM3	Data Mask	G11	O	GV _{DD}	—
D1_MDM4	Data Mask	AD7	O	GV _{DD}	—
D1_MDM5	Data Mask	AH8	O	GV _{DD}	—
D1_MDM6	Data Mask	AL11	O	GV _{DD}	—
D1_MDM7	Data Mask	AT10	O	GV _{DD}	—
D1_MDM8	Data Mask	K8	O	GV _{DD}	—
D1_MDQS0	Data Strobe	C16	I/O	GV _{DD}	—
D1_MDQS1	Data Strobe	G14	I/O	GV _{DD}	—
D1_MDQS2	Data Strobe	D9	I/O	GV _{DD}	—
D1_MDQS3	Data Strobe	G9	I/O	GV _{DD}	—
D1_MDQS4	Data Strobe	AD5	I/O	GV _{DD}	—
D1_MDQS5	Data Strobe	AH6	I/O	GV _{DD}	—
D1_MDQS6	Data Strobe	AM10	I/O	GV _{DD}	—
D1_MDQS7	Data Strobe	AT12	I/O	GV _{DD}	—
D1_MDQS8	Data Strobe	K6	I/O	GV _{DD}	—
<u>D1_MDQS0</u>	Data Strobe	B16	I/O	GV _{DD}	—
<u>D1_MDQS1</u>	Data Strobe	F14	I/O	GV _{DD}	—
<u>D1_MDQS2</u>	Data Strobe	D8	I/O	GV _{DD}	—
<u>D1_MDQS3</u>	Data Strobe	G8	I/O	GV _{DD}	—
<u>D1_MDQS4</u>	Data Strobe	AD4	I/O	GV _{DD}	—
<u>D1_MDQS5</u>	Data Strobe	AH5	I/O	GV _{DD}	—
<u>D1_MDQS6</u>	Data Strobe	AM9	I/O	GV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS7	Data Strobe	AT11	I/O	GV _{DD}	—
D1_MDQS8	Data Strobe	K5	I/O	GV _{DD}	—
D1_MBA0	Bank Select	AA8	O	GV _{DD}	—
D1_MBA1	Bank Select	Y10	O	GV _{DD}	—
D1_MBA2	Bank Select	M8	O	GV _{DD}	—
D1_MA00	Address	Y9	O	GV _{DD}	—
D1_MA01	Address	U6	O	GV _{DD}	—
D1_MA02	Address	U7	O	GV _{DD}	—
D1_MA03	Address	U9	O	GV _{DD}	—
D1_MA04	Address	U10	O	GV _{DD}	—
D1_MA05	Address	T8	O	GV _{DD}	—
D1_MA06	Address	T9	O	GV _{DD}	—
D1_MA07	Address	R8	O	GV _{DD}	—
D1_MA08	Address	R7	O	GV _{DD}	—
D1_MA09	Address	P6	O	GV _{DD}	—
D1_MA10	Address	AA7	O	GV _{DD}	—
D1_MA11	Address	P7	O	GV _{DD}	—
D1_MA12	Address	N6	O	GV _{DD}	—
D1_MA13	Address	AE8	O	GV _{DD}	—
D1_MA14	Address	M7	O	GV _{DD}	—
D1_MA15	Address	L6	O	GV _{DD}	—
D1_MWE	Write Enable	AB8	O	GV _{DD}	—
D1_MRAS	Row Address Strobe	AA10	O	GV _{DD}	—
D1_MCAS	Column Address Strobe	AC10	O	GV _{DD}	—
D1_MCS0	Chip Select	AC9	O	GV _{DD}	—
D1_MCS1	Chip Select	AE9	O	GV _{DD}	—
D1_MCS2	Chip Select	AB9	O	GV _{DD}	—
D1_MCS3	Chip Select	AF9	O	GV _{DD}	—
D1_MCKE0	Clock Enable	P10	O	GV _{DD}	—
D1_MCKE1	Clock Enable	R10	O	GV _{DD}	—
D1_MCKE2	Clock Enable	P9	O	GV _{DD}	—
D1_MCKE3	Clock Enable	N9	O	GV _{DD}	—
D1_MCK0	Clock	W6	O	GV _{DD}	—
D1_MCK1	Clock	V6	O	GV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCK2	Clock	V8	O	GV _{DD}	—
D1_MCK3	Clock	W9	O	GV _{DD}	—
D1_MCK0	Clock Complements	W5	O	GV _{DD}	—
D1_MCK1	Clock Complements	V5	O	GV _{DD}	—
D1_MCK2	Clock Complements	V9	O	GV _{DD}	—
D1_MCK3	Clock Complements	W8	O	GV _{DD}	—
D1_MODT0	On Die Termination	AD10	O	GV _{DD}	—
D1_MODT1	On Die Termination	AG10	O	GV _{DD}	—
D1_MODT2	On Die Termination	AD8	O	GV _{DD}	—
D1_MODT3	On Die Termination	AF10	O	GV _{DD}	—
D1_MDIC0	Driver Impedance Calibration	T6	I/O	GV _{DD}	16
D1_MDIC1	Driver Impedance Calibration	AA5	I/O	GV _{DD}	16
DDR SDRAM Memory Interface 2					
D2_MDQ00	Data	C13	I/O	GV _{DD}	34
D2_MDQ01	Data	A12	I/O	GV _{DD}	34
D2_MDQ02	Data	B9	I/O	GV _{DD}	34
D2_MDQ03	Data	A8	I/O	GV _{DD}	34
D2_MDQ04	Data	A13	I/O	GV _{DD}	34
D2_MDQ05	Data	B13	I/O	GV _{DD}	34
D2_MDQ06	Data	B10	I/O	GV _{DD}	34
D2_MDQ07	Data	A9	I/O	GV _{DD}	34
D2_MDQ08	Data	A7	I/O	GV _{DD}	34
D2_MDQ09	Data	D6	I/O	GV _{DD}	34
D2_MDQ10	Data	A4	I/O	GV _{DD}	34
D2_MDQ11	Data	B4	I/O	GV _{DD}	34
D2_MDQ12	Data	C7	I/O	GV _{DD}	34
D2_MDQ13	Data	B7	I/O	GV _{DD}	34
D2_MDQ14	Data	C5	I/O	GV _{DD}	34
D2_MDQ15	Data	D5	I/O	GV _{DD}	34
D2_MDQ16	Data	B1	I/O	GV _{DD}	34
D2_MDQ17	Data	B3	I/O	GV _{DD}	34
D2_MDQ18	Data	D3	I/O	GV _{DD}	34
D2_MDQ19	Data	E1	I/O	GV _{DD}	34
D2_MDQ20	Data	A3	I/O	GV _{DD}	34

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ21	Data	A2	I/O	GV _{DD}	34
D2_MDQ22	Data	D1	I/O	GV _{DD}	34
D2_MDQ23	Data	D2	I/O	GV _{DD}	34
D2_MDQ24	Data	F4	I/O	GV _{DD}	34
D2_MDQ25	Data	F5	I/O	GV _{DD}	34
D2_MDQ26	Data	H4	I/O	GV _{DD}	34
D2_MDQ27	Data	H6	I/O	GV _{DD}	34
D2_MDQ28	Data	E4	I/O	GV _{DD}	34
D2_MDQ29	Data	E3	I/O	GV _{DD}	34
D2_MDQ30	Data	H3	I/O	GV _{DD}	34
D2_MDQ31	Data	H1	I/O	GV _{DD}	34
D2_MDQ32	Data	AG4	I/O	GV _{DD}	34
D2_MDQ33	Data	AG2	I/O	GV _{DD}	34
D2_MDQ34	Data	AJ3	I/O	GV _{DD}	34
D2_MDQ35	Data	AJ1	I/O	GV _{DD}	34
D2_MDQ36	Data	AF4	I/O	GV _{DD}	34
D2_MDQ37	Data	AF3	I/O	GV _{DD}	34
D2_MDQ38	Data	AH1	I/O	GV _{DD}	34
D2_MDQ39	Data	AJ4	I/O	GV _{DD}	34
D2_MDQ40	Data	AL6	I/O	GV _{DD}	34
D2_MDQ41	Data	AL5	I/O	GV _{DD}	34
D2_MDQ42	Data	AN4	I/O	GV _{DD}	34
D2_MDQ43	Data	AN5	I/O	GV _{DD}	34
D2_MDQ44	Data	AK5	I/O	GV _{DD}	34
D2_MDQ45	Data	AK4	I/O	GV _{DD}	34
D2_MDQ46	Data	AM6	I/O	GV _{DD}	34
D2_MDQ47	Data	AM7	I/O	GV _{DD}	34
D2_MDQ48	Data	AN1	I/O	GV _{DD}	34
D2_MDQ49	Data	AP3	I/O	GV _{DD}	34
D2_MDQ50	Data	AT1	I/O	GV _{DD}	34
D2_MDQ51	Data	AT2	I/O	GV _{DD}	34
D2_MDQ52	Data	AM1	I/O	GV _{DD}	34
D2_MDQ53	Data	AN2	I/O	GV _{DD}	34
D2_MDQ54	Data	AR3	I/O	GV _{DD}	34

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ55	Data	AT3	I/O	GV _{DD}	34
D2_MDQ56	Data	AP5	I/O	GV _{DD}	34
D2_MDQ57	Data	AT5	I/O	GV _{DD}	34
D2_MDQ58	Data	AP8	I/O	GV _{DD}	34
D2_MDQ59	Data	AT8	I/O	GV _{DD}	34
D2_MDQ60	Data	AR4	I/O	GV _{DD}	34
D2_MDQ61	Data	AT4	I/O	GV _{DD}	34
D2_MDQ62	Data	AR7	I/O	GV _{DD}	34
D2_MDQ63	Data	AT7	I/O	GV _{DD}	34
D2_MECC0	Error Correcting Code	J1	I/O	GV _{DD}	34
D2_MECC1	Error Correcting Code	K3	I/O	GV _{DD}	34
D2_MECC2	Error Correcting Code	M5	I/O	GV _{DD}	34
D2_MECC3	Error Correcting Code	N5	I/O	GV _{DD}	34
D2_MECC4	Error Correcting Code	J4	I/O	GV _{DD}	34
D2_MECC5	Error Correcting Code	J2	I/O	GV _{DD}	34
D2_MECC6	Error Correcting Code	L3	I/O	GV _{DD}	34
D2_MECC7	Error Correcting Code	L4	I/O	GV _{DD}	34
D2_MAPAR_ERR	Address Parity Error	N2	I	GV _{DD}	34, 40
D2_MAPAR_OUT	Address Parity Out	Y1	O	GV _{DD}	34
D2_MDM0	Data Mask	B12	O	GV _{DD}	34
D2_MDM1	Data Mask	B6	O	GV _{DD}	34
D2_MDM2	Data Mask	C4	O	GV _{DD}	34
D2_MDM3	Data Mask	G3	O	GV _{DD}	34
D2_MDM4	Data Mask	AG1	O	GV _{DD}	34
D2_MDM5	Data Mask	AL3	O	GV _{DD}	34
D2_MDM6	Data Mask	AP2	O	GV _{DD}	34
D2_MDM7	Data Mask	AP6	O	GV _{DD}	34
D2_MDM8	Data Mask	K2	O	GV _{DD}	34
D2_MDQS0	Data Strobe	A10	I/O	GV _{DD}	34
D2_MDQS1	Data Strobe	A5	I/O	GV _{DD}	34
D2_MDQS2	Data Strobe	C2	I/O	GV _{DD}	34
D2_MDQS3	Data Strobe	G6	I/O	GV _{DD}	34
D2_MDQS4	Data Strobe	AH2	I/O	GV _{DD}	34
D2_MDQS5	Data Strobe	AM4	I/O	GV _{DD}	34

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQS6	Data Strobe	AR1	I/O	GV _{DD}	34
D2_MDQS7	Data Strobe	AR6	I/O	GV _{DD}	34
D2_MDQS8	Data Strobe	L1	I/O	GV _{DD}	34
D2_MDQS $\overline{0}$	Data Strobe	A11	I/O	GV _{DD}	34
D2_MDQS $\overline{1}$	Data Strobe	A6	I/O	GV _{DD}	34
D2_MDQS $\overline{2}$	Data Strobe	C1	I/O	GV _{DD}	34
D2_MDQS $\overline{3}$	Data Strobe	G5	I/O	GV _{DD}	34
D2_MDQS $\overline{4}$	Data Strobe	AH3	I/O	GV _{DD}	34
D2_MDQS $\overline{5}$	Data Strobe	AM3	I/O	GV _{DD}	34
D2_MDQS $\overline{6}$	Data Strobe	AP1	I/O	GV _{DD}	34
D2_MDQS $\overline{7}$	Data Strobe	AT6	I/O	GV _{DD}	34
D2_MDQS $\overline{8}$	Data Strobe	K1	I/O	GV _{DD}	34
D2_MBA0	Bank Select	AA3	O	GV _{DD}	34
D2_MBA1	Bank Select	AA1	O	GV _{DD}	34
D2_MBA2	Bank Select	M1	O	GV _{DD}	34
D2_MA00	Address	Y4	O	GV _{DD}	34
D2_MA01	Address	U1	O	GV _{DD}	34
D2_MA02	Address	U4	O	GV _{DD}	34
D2_MA03	Address	T1	O	GV _{DD}	34
D2_MA04	Address	T2	O	GV _{DD}	34
D2_MA05	Address	T3	O	GV _{DD}	34
D2_MA06	Address	R1	O	GV _{DD}	34
D2_MA07	Address	R4	O	GV _{DD}	34
D2_MA08	Address	R2	O	GV _{DD}	34
D2_MA09	Address	P1	O	GV _{DD}	34
D2_MA10	Address	AA2	O	GV _{DD}	34
D2_MA11	Address	P3	O	GV _{DD}	34
D2_MA12	Address	N1	O	GV _{DD}	34
D2_MA13	Address	AC4	O	GV _{DD}	34
D2_MA14	Address	N3	O	GV _{DD}	34
D2_MA15	Address	M2	O	GV _{DD}	34
D2_MWE	Write Enable	AB2	O	GV _{DD}	34
D2_MRAS	Row Address Strobe	AB1	O	GV _{DD}	34
D2_MCAS	Column Address Strobe	AC3	O	GV _{DD}	34

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MCS0	Chip Select	AC1	O	GV _{DD}	34
D2_MCS1	Chip Select	AE1	O	GV _{DD}	34
D2_MCS2	Chip Select	AB3	O	GV _{DD}	34
D2_MCS3	Chip Select	AE2	O	GV _{DD}	34
D2_MCKE0	Clock Enable	R5	O	GV _{DD}	34
D2_MCKE1	Clock Enable	T5	O	GV _{DD}	34
D2_MCKE2	Clock Enable	P4	O	GV _{DD}	34
D2_MCKE3	Clock Enable	M4	O	GV _{DD}	34
D2_MCK0	Clock	W3	O	GV _{DD}	34
D2_MCK1	Clock	V3	O	GV _{DD}	34
D2_MCK2	Clock	V1	O	GV _{DD}	34
D2_MCK3	Clock	W2	O	GV _{DD}	34
D2_MCK0	Clock Complements	W4	O	GV _{DD}	34
D2_MCK1	Clock Complements	V4	O	GV _{DD}	34
D2_MCK2	Clock Complements	V2	O	GV _{DD}	34
D2_MCK3	Clock Complements	W1	O	GV _{DD}	34
D2_MODT0	On Die Termination	AD2	O	GV _{DD}	34
D2_MODT1	On Die Termination	AF1	O	GV _{DD}	34
D2_MODT2	On Die Termination	AD1	O	GV _{DD}	34
D2_MODT3	On Die Termination	AE3	O	GV _{DD}	34
D2_MDIC0	Driver Impedance Calibration	AA4	I/O	GV _{DD}	16,34
D2_MDIC1	Driver Impedance Calibration	Y6	I/O	GV _{DD}	16,34
Local bus controller interface					
LAD00	Muxed Data/Address	K26	I/O	BV _{DD}	3
LAD01	Muxed Data/Address	L26	I/O	BV _{DD}	3
LAD02	Muxed Data/Address	J26	I/O	BV _{DD}	3
LAD03	Muxed Data/Address	H25	I/O	BV _{DD}	3
LAD04	Muxed Data/Address	F25	I/O	BV _{DD}	3
LAD05	Muxed Data/Address	H24	I/O	BV _{DD}	3
LAD06	Muxed Data/Address	G24	I/O	BV _{DD}	3
LAD07	Muxed Data/Address	G23	I/O	BV _{DD}	3
LAD08	Muxed Data/Address	E23	I/O	BV _{DD}	3
LAD09	Muxed Data/Address	D23	I/O	BV _{DD}	3
LAD10	Muxed Data/Address	J22	I/O	BV _{DD}	3

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LAD11	Muxed Data/Address	G22	I/O	BV _{DD}	3
LAD12	Muxed Data/Address	F19	I/O	BV _{DD}	3
LAD13	Muxed Data/Address	J18	I/O	BV _{DD}	3
LAD14	Muxed Data/Address	K18	I/O	BV _{DD}	3
LAD15	Muxed Data/Address	J17	I/O	BV _{DD}	3
LAD16	Muxed Data/Address	J25	I/O	BV _{DD}	3
LAD17	Muxed Data/Address	G25	I/O	BV _{DD}	3
LAD18	Muxed Data/Address	H23	I/O	BV _{DD}	3, 35
LAD19	Muxed Data/Address	F22	I/O	BV _{DD}	3, 35
LAD20	Muxed Data/Address	H22	I/O	BV _{DD}	3, 35
LAD21	Muxed Data/Address	E21	I/O	BV _{DD}	3, 35
LAD22	Muxed Data/Address	F21	I/O	BV _{DD}	3, 35
LAD23	Muxed Data/Address	H21	I/O	BV _{DD}	3
LAD24	Muxed Data/Address	K21	I/O	BV _{DD}	3
LAD25	Muxed Data/Address	G20	I/O	BV _{DD}	3, 35
LAD26	Muxed Data/Address	J20	I/O	BV _{DD}	32
LAD27	Muxed Data/Address	D26	I/O	BV _{DD}	—
LAD28	Muxed Data/Address	E18	I/O	BV _{DD}	—
LAD29	Muxed Data/Address	F18	I/O	BV _{DD}	—
LAD30	Muxed Data/Address	J15	I/O	BV _{DD}	—
LAD31	Muxed Data/Address	F17	I/O	BV _{DD}	—
LDP0	Data Parity	J24	I/O	BV _{DD}	—
LDP1	Data Parity	K23	I/O	BV _{DD}	—
LDP2	Data Parity	H17	I/O	BV _{DD}	—
LDP3	Data Parity	H16	I/O	BV _{DD}	—
LA27	Address	K20	O	BV _{DD}	—
LA28	Address	G19	O	BV _{DD}	35
LA29	Address	H19	O	BV _{DD}	35
LA30	Address	J19	O	BV _{DD}	35
LA31	Address	G18	O	BV _{DD}	35
$\overline{\text{LCS0}}$	Chip Selects	D19	O	BV _{DD}	5
$\overline{\text{LCS1}}$	Chip Selects	D20	O	BV _{DD}	5
$\overline{\text{LCS2}}$	Chip Selects	E20	O	BV _{DD}	5
$\overline{\text{LCS3}}$	Chip Selects	D21	O	BV _{DD}	5

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{LCS4}}$	Chip Selects	D22	O	BV _{DD}	5
$\overline{\text{LCS5}}$	Chip Selects	B23	O	BV _{DD}	5
$\overline{\text{LCS6}}$	Chip Selects	F24	O	BV _{DD}	5
$\overline{\text{LCS7}}$	Chip Selects	G26	O	BV _{DD}	5
$\overline{\text{LWE0}}$	Write Enable	D24	O	BV _{DD}	—
$\overline{\text{LWE1}}$	Write Enable	A24	O	BV _{DD}	—
$\overline{\text{LWE2}}$	Write Enable	J16	O	BV _{DD}	—
$\overline{\text{LWE3}}$	Write Enable	K15	O	BV _{DD}	—
LBCTL	Buffer Control	C22	O	BV _{DD}	—
LALE	Address Latch Enable	A23	I/O	BV _{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	B25	O	BV _{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	E25	O	BV _{DD}	3, 4
LGPL2/ $\overline{\text{LOE}}$ / $\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	D25	O	BV _{DD}	3, 4
LGPL3/ $\overline{\text{LFWP}}$	UPM General Purpose Line 3/ LFWP_B—FCM	H26	O	BV _{DD}	3, 4
LGPL4/LGTA/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	C25	I/O	BV _{DD}	39
LGPL5	UPM General Purpose Line 5 / Amux	E26	O	BV _{DD}	3, 4
LCLK0	Local Bus Clock	C24	O	BV _{DD}	—
LCLK1	Local Bus Clock	C23	O	BV _{DD}	—
DMA					
$\overline{\text{DMA1_DREQ0}}/\text{GPIO18}$	DMA1 Channel 0 Request	AP21	I	OV _{DD}	26
$\overline{\text{DMA1_DACK0}}/\text{GPIO19}$	DMA1 Channel 0 Acknowledge	AL19	O	OV _{DD}	26
$\overline{\text{DMA1_DDONE0}}$	DMA1 Channel 0 Done	AN21	O	OV _{DD}	27
$\overline{\text{DMA2_DREQ0}}/\text{GPIO20}/\text{ALT_MDVAL}$	DMA2 Channel 0 Request	AJ20	I	OV _{DD}	26
$\overline{\text{DMA2_DACK0}}/\text{EVT7}/\text{ALT_MDSRCID0}$	DMA2 Channel 0 Acknowledge	AG19	O	OV _{DD}	26
$\overline{\text{DMA2_DDONE0}}/\text{EVT8}/\text{ALT_MDSRCID1}$	DMA2 Channel 0 Done	AP20	O	OV _{DD}	26
USB port 1					
$\overline{\text{USB1_UDP}}$	USB1 PHY Data Plus	AT27	I/O	USB_V _D D_3P3	—
$\overline{\text{USB1_UDM}}$	USB1 PHY Data Minus	AT26	I/O	USB_V _D D_3P3	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signal	AK25	I	USB_V _D D_3P3	38
USB1_UID	USB1 PHY ID Detect	AK24	I	USB1_V _{DD-1P8} _DECA P	—
USB1_DRVVBUS/GPIO04	USB1 5V Supply Enable	AH21	O	OV _{DD}	26,38
USB1_PWRFAULT/GPIO05	USB1 Power Fault	AJ21	O	OV _{DD}	26,38
USB_CLKIN	USB PHY Clock Input	AM24	I	OV _{DD}	—
USB Port 2					
USB2_UDP	USB2 PHY Data Plus	AP27	I/O	USB_V _D D_3P3	—
USB2_UDM	USB2 PHY Data Minus	AP26	I/O	USB_V _D D_3P3	—
USB2_VBUS_CLMP	USB2 PHY VBUS Divided Signal	AK26	I	USB_V _D D_3P3	38
USB2_UID	USB2 PHY ID Detect	AK27	I	USB2_V _{DD-1P8} _DECA P	—
USB2_DRVVBUS/GPIO06	USB2 5V Supply Enable	AK21	O	OV _{DD}	26,38
USB2_PWRFAULT/GPIO07	USB2 Power Fault	AG20	O	OV _{DD}	26,38
Programmable interrupt controller					
IRQ00	External Interrupts	AJ16	I	OV _{DD}	—
IRQ01	External Interrupts	AH16	I	OV _{DD}	—
IRQ02	External Interrupts	AK12	I	OV _{DD}	—
IRQ03/GPIO21	External Interrupts	AJ15	I	OV _{DD}	26
IRQ04/GPIO22	External Interrupts	AH17	I	OV _{DD}	26
IRQ05/GPIO23	External Interrupts	AJ13	I	OV _{DD}	26
IRQ06/GPIO24	External Interrupts	AG17	I	OV _{DD}	26
IRQ07/GPIO25	External Interrupts	AM13	I	OV _{DD}	26
IRQ08/GPIO26	External Interrupts	AG13	I	OV _{DD}	26
IRQ09/GPIO27	External Interrupts	AK11	I	OV _{DD}	26
IRQ10/GPIO28	External Interrupts	AH14	I	OV _{DD}	26
IRQ11/GPIO29	External Interrupts	AL12	I	OV _{DD}	26
IRQ_OUT/EVT9	Interrupt Output	AK14	O	OV _{DD}	1, 2, 26
Trust					

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{TMP_DETECT}}$	Tamper Detect	AN19	I	OV_{DD}	27
$\overline{\text{LP_TMP_DETECT}}$	Low Power Tamper Detect	AE28	I	$\text{V}_{\text{DD_LP}}$	—
eSDHC					
SDHC_CMD	Command/Response	AG23	I/O	CV_{DD}	—
$\overline{\text{SDHC_DAT0}}$	Data	AP24	I/O	CV_{DD}	—
$\overline{\text{SDHC_DAT1}}$	Data	AT24	I/O	CV_{DD}	—
$\overline{\text{SDHC_DAT2}}$	Data	AM23	I/O	CV_{DD}	—
$\overline{\text{SDHC_DAT3}}$	Data	AG22	I/O	CV_{DD}	—
$\overline{\text{SDHC_DAT4/SPI_CS0}}$	Data	AN29	I/O	CV_{DD}	26, 31
$\overline{\text{SDHC_DAT5/SPI_CS1}}$	Data	AJ28	I/O	CV_{DD}	26, 31
$\overline{\text{SDHC_DAT6/SPI_CS2}}$	Data	AR29	I/O	CV_{DD}	26, 31
$\overline{\text{SDHC_DAT7/SPI_CS3}}$	Data	AM29	I/O	CV_{DD}	26, 31
SDHC_CLK	Host to Card Clock	AL23	O	CV_{DD}	—
$\overline{\text{SDHC_CD/IIC3_SCL/GPIO16}}$	Card Detection	AK13	I	OV_{DD}	26,27,31
$\overline{\text{SDHC_WP/IIC3_SDA/GPIO17}}$	Card Write Protection	AM14	I	OV_{DD}	26,27,31
eSPI					
SPI_MOSI	Master Out Slave In	AT29	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	AH28	I	CV_{DD}	—
SPI_CLK	eSPI clock	AK29	O	CV_{DD}	—
$\overline{\text{SPI_CS0/SDHC_DAT4}}$	eSPI chip select	AN29	O	CV_{DD}	26
$\overline{\text{SPI_CS1/SDHC_DAT5}}$	eSPI chip select	AJ28	O	CV_{DD}	26
$\overline{\text{SPI_CS2/SDHC_DAT6}}$	eSPI chip select	AR29	O	CV_{DD}	26
$\overline{\text{SPI_CS3/SDHC_DAT7}}$	eSPI chip select	AM29	O	CV_{DD}	26
IEEE 1588					
TSEC_1588_CLK_IN	Clock In	AL35	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger In 1	AL36	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RX_ER	Trigger In 2	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Alarm Out 1	AJ36	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/EC1_COL/GPIO30	Alarm Out 2	AK35	O	LV_{DD}	26
TSEC_1588_CLK_OUT	Clock Out	AM30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1	Pulse Out1	AL30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_CRIS/GPIO31	Pulse Out2	AJ34	O	LV_{DD}	26
Ethernet Management Interface 1					

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EMI1_MDC	Management Data Clock	AJ33	O	LV _{DD}	—
EMI1_MDIO	Management Data In/Out	AL32	I/O	LV _{DD}	—
Ethernet management interface 2					
EMI2_MDC	Management Data Clock	AK30	O	1.2 V	2, 18, 22
EMI2_MDIO	Management Data In/Out	AJ30	I/O	1.2 V	2, 18, 22
Ethernet reference clock					
EC1_GTX_CLK125/ EC1_TX_CLK	Reference Clock (RGMII) Transmit Clock (MII)	AK34	I	LV _{DD}	27
EC2_GTX_CLK125/ EC2_TX_CLK	Reference Clock (RGMII) Transmit Clock (MII)	AL33	I	LV _{DD}	27
Ethernet external timestamping					
EC_XTRNL_TX_STMP1	External Timestamp Transmit 1	AM31	I	LV _{DD}	—
EC_XTRNL_RX_STMP1	External Timestamp Receive 1	AK32	I	LV _{DD}	—
EC_XTRNL_TX_STMP2/EC2_COL	External Timestamp Transmit 2	AJ31	I	LV _{DD}	—
EC_XTRNL_RX_STMP2/EC2_CRS	External Timestamp Receive 2	AK31	I	LV _{DD}	—
Three-speed Ethernet controller 1					
EC1_TXD3	Transmit Data	AP36	O	LV _{DD}	35
EC1_TXD2	Transmit Data	AT34	O	LV _{DD}	35
EC1_TXD1	Transmit Data	AR34	O	LV _{DD}	35
EC1_TXD0	Transmit Data	AT35	O	LV _{DD}	35
EC1_TX_EN	Transmit Enable	AR36	O	LV _{DD}	15
EC1_GTX_CLK/ EC1_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AP35	O	LV _{DD}	26
EC1_RXD3	Receive Data	AM33	I	LV _{DD}	27
EC1_RXD2	Receive Data	AN34	I	LV _{DD}	27
EC1_RXD1	Receive Data	AN35	I	LV _{DD}	27
EC1_RXD0	Receive Data	AN36	I	LV _{DD}	27
EC1_RX_DV	Receive Data Valid	AM34	I	LV _{DD}	27
EC1_RX_CLK	Receive Clock	AM36	I	LV _{DD}	27
EC1_RX_ER/TSEC_1588_TRIG_IN2	Receive Error (MII)	AK36	I	LV _{DD}	—
EC1_COL/GPIO30/TSEC_1588_ALARM_OUT2	Collision Detect (MII)	AK35	O	LV _{DD}	26
EC1_CRS/GPIO31/TSEC_1588_PULSE_OUT2	Carrier Sense (MII)	AJ34	O	LV _{DD}	26
Three-speed Ethernet controller 2					
EC2_TXD3	Transmit Data	AT31	O	LV _{DD}	35

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC2_TXD2	Transmit Data	AP30	O	LV _{DD}	35
EC2_TXD1	Transmit Data	AR30	O	LV _{DD}	35
EC2_TXD0	Transmit Data	AT30	O	LV _{DD}	35
EC2_TX_EN	Transmit Enable	AR31	O	LV _{DD}	15
EC2_GTX_CLK/ EC2_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AN31	O	LV _{DD}	26
EC2_RXD3	Receive Data	AP33	I	LV _{DD}	27
EC2_RXD2	Receive Data	AN32	I	LV _{DD}	27
EC2_RXD1	Receive Data	AP32	I	LV _{DD}	26, 27
EC2_RXD0	Receive Data	AT32	I	LV _{DD}	26, 27
EC2_RX_DV	Receive Data Valid	AR33	I	LV _{DD}	27
EC2_RX_CLK	Receive Clock	AT33	I	LV _{DD}	27
EC2_RX_ER	Receive Error (MII)	AH29	I	LV _{DD}	—
EC2_COL/EC_XTRNL_TX_STMP2	Collision Detect (MII)	AJ31	O	LV _{DD}	26
EC2_CRS/EC_XTRNL_RX_STMP2	Carrier Sense (MII)	AK31	O	LV _{DD}	26
UART					
UART1_SOUT/GPIO8	Transmit Data	AL22	O	OV _{DD}	26
UART2_SOUT/GPIO9	Transmit Data	AJ22	O	OV _{DD}	26
UART1_SIN/GPIO10	Receive Data	AR23	I	OV _{DD}	26
UART2_SIN/GPIO11	Receive Data	AN23	I	OV _{DD}	26
UART1_RTS/UART3_SOUT/GPIO12	Ready to Send	AM22	O	OV _{DD}	26
UART2_RTS/UART4_SOUT/GPIO13	Ready to Send	AK23	O	OV _{DD}	26
UART1_CTS/UART3_SIN/GPIO14	Clear to Send	AP22	I	OV _{DD}	26
UART2_CTS/UART4_SIN/GPIO15	Clear to Send	AH23	I	OV _{DD}	26
I²C interface					
IIC1_SCL	Serial Clock	AH15	I/O	OV _{DD}	2, 14
IIC1_SDA	Serial Data	AN14	I/O	OV _{DD}	2, 14
IIC2_SCL	Serial Clock	AM15	I/O	OV _{DD}	2, 14
IIC2_SDA	Serial Data	AL14	I/O	OV _{DD}	2, 14
IIC3_SCL/SDHC_CD/GPIO16	Serial Clock	AK13	I/O	OV _{DD}	2, 14, 27
IIC3_SDA/SDHC_WP/GPIO17	Serial Data	AM14	I/O	OV _{DD}	2, 14, 27
IIC4_SCL/EVT5	Serial Clock	AG14	I/O	OV _{DD}	2, 14
IIC4_SDA/EVT6	Serial Data	AL15	I/O	OV _{DD}	2, 14
SerDes (x18) PCIe, sRIO, Aurora, 10GE, 1GE					

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_TX17	Transmit Data (positive)	AG31	O	XV _{DD}	—
SD_TX16	Transmit Data (positive)	AE31	O	XV _{DD}	—
SD_TX15	Transmit Data (positive)	AB33	O	XV _{DD}	—
SD_TX14	Transmit Data (positive)	AA31	O	XV _{DD}	—
SD_TX13	Transmit Data (positive)	Y29	O	XV _{DD}	—
SD_TX12	Transmit Data (positive)	W31	O	XV _{DD}	—
SD_TX11	Transmit Data (positive)	T30	O	XV _{DD}	—
SD_TX10	Transmit Data (positive)	P31	O	XV _{DD}	—
SD_TX09	Transmit Data (positive)	N33	O	XV _{DD}	—
SD_TX08	Transmit Data (positive)	M31	O	XV _{DD}	—
SD_TX07	Transmit Data (positive)	K31	O	XV _{DD}	—
SD_TX06	Transmit Data (positive)	J33	O	XV _{DD}	—
SD_TX05	Transmit Data (positive)	G33	O	XV _{DD}	—
SD_TX04	Transmit Data (positive)	D34	O	XV _{DD}	—
SD_TX03	Transmit Data (positive)	F31	O	XV _{DD}	—
SD_TX02	Transmit Data (positive)	H30	O	XV _{DD}	—
SD_TX01	Transmit Data (positive)	F29	O	XV _{DD}	—
SD_TX00	Transmit Data (positive)	H28	O	XV _{DD}	—
$\overline{\text{SD_TX17}}$	Transmit Data (negative)	AG32	O	XV _{DD}	—
$\overline{\text{SD_TX16}}$	Transmit Data (negative)	AE32	O	XV _{DD}	—
$\overline{\text{SD_TX15}}$	Transmit Data (negative)	AB34	O	XV _{DD}	—
$\overline{\text{SD_TX14}}$	Transmit Data (negative)	AA32	O	XV _{DD}	—
$\overline{\text{SD_TX13}}$	Transmit Data (negative)	Y30	O	XV _{DD}	—
$\overline{\text{SD_TX12}}$	Transmit Data (negative)	W32	O	XV _{DD}	—
$\overline{\text{SD_TX11}}$	Transmit Data (negative)	T31	O	XV _{DD}	—
$\overline{\text{SD_TX10}}$	Transmit Data (negative)	P32	O	XV _{DD}	—
$\overline{\text{SD_TX09}}$	Transmit Data (negative)	N34	O	XV _{DD}	—
$\overline{\text{SD_TX08}}$	Transmit Data (negative)	M32	O	XV _{DD}	—
$\overline{\text{SD_TX07}}$	Transmit Data (negative)	K32	O	XV _{DD}	—
$\overline{\text{SD_TX06}}$	Transmit Data (negative)	J34	O	XV _{DD}	—
$\overline{\text{SD_TX05}}$	Transmit Data (negative)	F33	O	XV _{DD}	—
$\overline{\text{SD_TX04}}$	Transmit Data (negative)	E34	O	XV _{DD}	—
$\overline{\text{SD_TX03}}$	Transmit Data (negative)	E31	O	XV _{DD}	—
$\overline{\text{SD_TX02}}$	Transmit Data (negative)	G30	O	XV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_TX01	Transmit Data (negative)	E29	O	XV _{DD}	—
SD_TX00	Transmit Data (negative)	G28	O	XV _{DD}	—
SD_RX17	Receive Data (positive)	AG36	I	XV _{DD}	—
SD_RX16	Receive Data (positive)	AF34	I	XV _{DD}	—
SD_RX15	Receive Data (positive)	AC36	I	XV _{DD}	—
SD_RX14	Receive Data (positive)	AA36	I	XV _{DD}	—
SD_RX13	Receive Data (positive)	Y34	I	XV _{DD}	—
SD_RX12	Receive Data (positive)	W36	I	XV _{DD}	—
SD_RX11	Receive Data (positive)	T34	I	XV _{DD}	—
SD_RX10	Receive Data (positive)	P36	I	XV _{DD}	—
SD_RX09	Receive Data (positive)	M36	I	XV _{DD}	—
SD_RX08	Receive Data (positive)	L34	I	XV _{DD}	—
SD_RX07	Receive Data (positive)	K36	I	XV _{DD}	—
SD_RX06	Receive Data (positive)	H36	I	XV _{DD}	—
SD_RX05	Receive Data (positive)	F36	I	XV _{DD}	—
SD_RX04	Receive Data (positive)	D36	I	XV _{DD}	—
SD_RX03	Receive Data (positive)	A31	I	XV _{DD}	—
SD_RX02	Receive Data (positive)	C30	I	XV _{DD}	—
SD_RX01	Receive Data (positive)	A29	I	XV _{DD}	—
SD_RX00	Receive Data (positive)	C28	I	XV _{DD}	—
$\overline{\text{SD_RX17}}$	Receive Data (negative)	AG35	I	XV _{DD}	—
$\overline{\text{SD_RX16}}$	Receive Data (negative)	AF33	I	XV _{DD}	—
$\overline{\text{SD_RX15}}$	Receive Data (negative)	AC35	I	XV _{DD}	—
$\overline{\text{SD_RX14}}$	Receive Data (negative)	AA35	I	XV _{DD}	—
$\overline{\text{SD_RX13}}$	Receive Data (negative)	Y33	I	XV _{DD}	—
$\overline{\text{SD_RX12}}$	Receive Data (negative)	W35	I	XV _{DD}	—
$\overline{\text{SD_RX11}}$	Receive Data (negative)	T33	I	XV _{DD}	—
$\overline{\text{SD_RX10}}$	Receive Data (negative)	P35	I	XV _{DD}	—
$\overline{\text{SD_RX09}}$	Receive Data (negative)	M35	I	XV _{DD}	—
$\overline{\text{SD_RX08}}$	Receive Data (negative)	L33	I	XV _{DD}	—
$\overline{\text{SD_RX07}}$	Receive Data (negative)	K35	I	XV _{DD}	—
$\overline{\text{SD_RX06}}$	Receive Data (negative)	H35	I	XV _{DD}	—
$\overline{\text{SD_RX05}}$	Receive Data (negative)	F35	I	XV _{DD}	—
$\overline{\text{SD_RX04}}$	Receive Data (negative)	C36	I	XV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_RX03	Receive Data (negative)	B31	I	XV _{DD}	—
SD_RX02	Receive Data (negative)	D30	I	XV _{DD}	—
SD_RX01	Receive Data (negative)	B29	I	XV _{DD}	—
SD_RX00	Receive Data (negative)	D28	I	XV _{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	A35	I	XV _{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock Complement	B35	I	XV _{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	V34	I	XV _{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock Complement	V33	I	XV _{DD}	—
SD_REF_CLK3	SerDes Bank 3 PLL Reference Clock	AC32	I	XV _{DD}	—
SD_REF_CLK3	SerDes Bank 3 PLL Reference Clock Complement	AC31	I	XV _{DD}	—
General-Purpose Input/Output					
GPIO00	General Purpose Input / Output	AL21	I/O	OV _{DD}	—
GPIO01	General Purpose Input / Output	AK22	I/O	OV _{DD}	—
GPIO02	General Purpose Input / Output	AM20	I/O	OV _{DD}	—
GPIO03	General Purpose Input / Output	AN20	I/O	OV _{DD}	—
GPIO04/USB1_DRVVBUS	General Purpose Input / Output	AH21	I/O	OV _{DD}	—
GPIO05/USB1_PWRFAULT	General Purpose Input / Output	AJ21	I/O	OV _{DD}	—
GPIO06/USB2_DRVVBUS	General Purpose Input / Output	AK21	I/O	OV _{DD}	—
GPIO07/USB2_PWRFAULT	General Purpose Input / Output	AG20	I/O	OV _{DD}	—
GPIO08/UART1_SOUT	General Purpose Input / Output	AL22	I/O	OV _{DD}	—
GPIO09/UART2_SOUT	General Purpose Input / Output	AJ22	I/O	OV _{DD}	—
GPIO10/UART1_SIN	General Purpose Input / Output	AR23	I/O	OV _{DD}	—
GPIO11/UART2_SIN	General Purpose Input / Output	AN23	I/O	OV _{DD}	—
GPIO12/UART1_RTS/UART3_SOUT	General Purpose Input / Output	AM22	I/O	OV _{DD}	—
GPIO13/UART2_RTS/UART4_SOUT	General Purpose Input / Output	AK23	I/O	OV _{DD}	—
GPIO14/UART1_CTS/UART3_SIN	General Purpose Input / Output	AP22	I/O	OV _{DD}	—
GPIO15/UART2_CTS/UART4_SIN	General Purpose Input / Output	AH23	I/O	OV _{DD}	—
GPIO16/IIC3_SCL/SDHC_CD	General Purpose Input / Output	AK13	I/O	OV _{DD}	27
GPIO17/IIC3_SDA/SDHC_WP	General Purpose Input / Output	AM14	I/O	OV _{DD}	27
GPIO18/DMA1_DREQ0	General Purpose Input / Output	AP21	I/O	OV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO19/DMA1_DACK0	General Purpose Input / Output	AL19	I/O	OV _{DD}	—
GPIO20/DMA2_DREQ0/ALT_MDVAL	General Purpose Input / Output	AJ20	I/O	OV _{DD}	—
GPIO21/IRQ3	General Purpose Input / Output	AJ15	I/O	OV _{DD}	—
GPIO22/IRQ4	General Purpose Input / Output	AH17	I/O	OV _{DD}	—
GPIO23/IRQ5	General Purpose Input / Output	AJ13	I/O	OV _{DD}	—
GPIO24/IRQ6	General Purpose Input / Output	AG17	I/O	OV _{DD}	—
GPIO25/IRQ7	General Purpose Input / Output	AM13	I/O	OV _{DD}	—
GPIO26/IRQ8	General Purpose Input / Output	AG13	I/O	OV _{DD}	—
GPIO27/IRQ9	General Purpose Input / Output	AK11	I/O	OV _{DD}	—
GPIO28/IRQ10	General Purpose Input / Output	AH14	I/O	OV _{DD}	—
GPIO29/IRQ11	General Purpose Input / Output	AL12	I/O	OV _{DD}	—
GPIO30/TSEC_1588_ALARM_OUT2	General Purpose Input / Output	AK35	I/O	LV _{DD}	25
GPIO31/TSEC_1588_PULSE_OUT2	General Purpose Input / Output	AJ34	I/O	LV _{DD}	25
System Control					
PORESET	Power On Reset	AP17	I	OV _{DD}	—
HRESET	Hard Reset	AR17	I/O	OV _{DD}	1, 2
RESET_REQ	Reset Request	AT16	O	OV _{DD}	35
CKSTP_OUT	Checkstop Out	AM19	O	OV _{DD}	1, 2
Debug					
EVT0	Event 0	AJ17	I/O	OV _{DD}	20
EVT1	Event 1	AK17	I/O	OV _{DD}	—
EVT2	Event 2	AN16	I/O	OV _{DD}	—
EVT3	Event 3	AK16	I/O	OV _{DD}	—
EVT4	Event 4	AM16	I/O	OV _{DD}	—
EVT5/IIC4_SCL	Event 5	AG14	I/O	OV _{DD}	—
EVT6/IIC4_SDA	Event 6	AL15	I/O	OV _{DD}	—
EVT7/DMA2_DACK0/ALT_MSRCID0	Event 7	AG19	I/O	OV _{DD}	—
EVT8/DMA2_DDONE0/ALT_MSRCID1	Event 8	AP20	I/O	OV _{DD}	—
EVT9/IRQ_OUT	Event 9	AK14	I/O	OV _{DD}	—
MDVAL	Debug Data Valid	AR15	O	OV _{DD}	—
MSRCID0	Debug Source ID 0	AH20	O	OV _{DD}	4, 20, 35
MSRCID1	Debug Source ID 1	AJ19	O	OV _{DD}	—
MSRCID2	Debug Source ID 2	AH18	O	OV _{DD}	—
ALT_MDVAL/DMA2_DREQ0/GPIO20	Alternate Debug Data Valid	AJ20	O	OV _{DD}	26

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
ALT_MSRCID0/DMA2_DACK0/EVT7	Alternate Debug Source ID 0	AG19	O	OV _{DD}	26
ALT_MSRCID1/DMA2_DDONE0/EVT8	Alternate Debug Source ID 1	AP20	O	OV _{DD}	26
CLK_OUT	Clock Out	AK20	O	OV _{DD}	6
Clock					
RTC	Real Time Clock	AN24	I	OV _{DD}	—
SYSCLK	System Clock	AT23	I	OV _{DD}	—
JTAG					
TCK	Test Clock	AR22	I	OV _{DD}	—
TDI	Test Data In	AN17	I	OV _{DD}	7
TDO	Test Data Out	AP15	O	OV _{DD}	6
TMS	Test Mode Select	AR20	I	OV _{DD}	7
TRST	Test Reset	AR19	I	OV _{DD}	7
DFT					
SCAN_MODE	Scan Mode	AL17	I	OV _{DD}	12
TEST_SEL	Test Mode Select	AT21	I	OV _{DD}	12,28
Power management					
ASLEEP	Asleep	AR21	O	OV _{DD}	35
Input / output voltage select					
IO_VSEL0	I/O Voltage Select	AL18	I	OV _{DD}	30
IO_VSEL1	I/O Voltage Select	AP18	I	OV _{DD}	30
IO_VSEL2	I/O Voltage Select	AK18	I	OV _{DD}	30
IO_VSEL3	I/O Voltage Select	AM18	I	OV _{DD}	30
IO_VSEL4	I/O Voltage Select	AH19	I	OV _{DD}	30
Power and Ground Signals					
GND	Ground	C3	—	—	—
GND	Ground	B5	—	—	—
GND	Ground	F3	—	—	—
GND	Ground	E5	—	—	—
GND	Ground	D7	—	—	—
GND	Ground	C9	—	—	—
GND	Ground	B11	—	—	—
GND	Ground	J3	—	—	—
GND	Ground	H5	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	G7	—	—	—
GND	Ground	G17	—	—	—
GND	Ground	F9	—	—	—
GND	Ground	E11	—	—	—
GND	Ground	D13	—	—	—
GND	Ground	C15	—	—	—
GND	Ground	K19	—	—	—
GND	Ground	B20	—	—	—
GND	Ground	B22	—	—	—
GND	Ground	E19	—	—	—
GND	Ground	L22	—	—	—
GND	Ground	J23	—	—	—
GND	Ground	A22	—	—	—
GND	Ground	L20	—	—	—
GND	Ground	A26	—	—	—
GND	Ground	A18	—	—	—
GND	Ground	E17	—	—	—
GND	Ground	F23	—	—	—
GND	Ground	J27	—	—	—
GND	Ground	F27	—	—	—
GND	Ground	G21	—	—	—
GND	Ground	K25	—	—	—
GND	Ground	B18	—	—	—
GND	Ground	L18	—	—	—
GND	Ground	J21	—	—	—
GND	Ground	M27	—	—	—
GND	Ground	G13	—	—	—
GND	Ground	F15	—	—	—
GND	Ground	H11	—	—	—
GND	Ground	J9	—	—	—
GND	Ground	K7	—	—	—
GND	Ground	L5	—	—	—
GND	Ground	M3	—	—	—
GND	Ground	R3	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	P5	—	—	—
GND	Ground	N7	—	—	—
GND	Ground	M9	—	—	—
GND	Ground	V25	—	—	—
GND	Ground	R9	—	—	—
GND	Ground	T7	—	—	—
GND	Ground	U5	—	—	—
GND	Ground	U3	—	—	—
GND	Ground	Y3	—	—	—
GND	Ground	Y5	—	—	—
GND	Ground	W7	—	—	—
GND	Ground	V10	—	—	—
GND	Ground	AA9	—	—	—
GND	Ground	AB7	—	—	—
GND	Ground	AC5	—	—	—
GND	Ground	AD3	—	—	—
GND	Ground	AD9	—	—	—
GND	Ground	AE7	—	—	—
GND	Ground	AF5	—	—	—
GND	Ground	AG3	—	—	—
GND	Ground	AG9	—	—	—
GND	Ground	AH7	—	—	—
GND	Ground	AJ5	—	—	—
GND	Ground	AK3	—	—	—
GND	Ground	AN3	—	—	—
GND	Ground	AM5	—	—	—
GND	Ground	AL7	—	—	—
GND	Ground	AK9	—	—	—
GND	Ground	AJ11	—	—	—
GND	Ground	AH13	—	—	—
GND	Ground	AR5	—	—	—
GND	Ground	AP7	—	—	—
GND	Ground	AN9	—	—	—
GND	Ground	AM11	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	AL13	—	—	—
GND	Ground	AK15	—	—	—
GND	Ground	AG18	—	—	—
GND	Ground	AR11	—	—	—
GND	Ground	AP13	—	—	—
GND	Ground	AN15	—	—	—
GND	Ground	AM17	—	—	—
GND	Ground	AK19	—	—	—
GND	Ground	AF13	—	—	—
GND	Ground	AR18	—	—	—
GND	Ground	AB27	—	—	—
GND	Ground	AP19	—	—	—
GND	Ground	AH22	—	—	—
GND	Ground	AM21	—	—	—
GND	Ground	AL29	—	—	—
GND	Ground	AR16	—	—	—
GND	Ground	AT22	—	—	—
GND	Ground	AP23	—	—	—
GND	Ground	AR32	—	—	—
GND	Ground	AK28	—	—	—
GND	Ground	AE27	—	—	—
GND	Ground	L16	—	—	—
GND	Ground	AP34	—	—	—
GND	Ground	AJ32	—	—	—
GND	Ground	AN30	—	—	—
GND	Ground	AH34	—	—	—
GND	Ground	AT36	—	—	—
GND	Ground	AL34	—	—	—
GND	Ground	AM32	—	—	—
GND	Ground	AE26	—	—	—
GND	Ground	AC26	—	—	—
GND	Ground	AA26	—	—	—
GND	Ground	W26	—	—	—
GND	Ground	U26	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	R26	—	—	—
GND	Ground	N26	—	—	—
GND	Ground	M11	—	—	—
GND	Ground	P11	—	—	—
GND	Ground	T11	—	—	—
GND	Ground	V11	—	—	—
GND	Ground	Y11	—	—	—
GND	Ground	AB11	—	—	—
GND	Ground	AD11	—	—	—
GND	Ground	AE12	—	—	—
GND	Ground	AC12	—	—	—
GND	Ground	AA12	—	—	—
GND	Ground	W12	—	—	—
GND	Ground	U12	—	—	—
GND	Ground	R12	—	—	—
GND	Ground	N12	—	—	—
GND	Ground	M13	—	—	—
GND	Ground	P13	—	—	—
GND	Ground	T13	—	—	—
GND	Ground	V13	—	—	—
GND	Ground	Y13	—	—	—
GND	Ground	AB13	—	—	—
GND	Ground	AD13	—	—	—
GND	Ground	AE14	—	—	—
GND	Ground	AC14	—	—	—
GND	Ground	AA14	—	—	—
GND	Ground	W14	—	—	—
GND	Ground	U14	—	—	—
GND	Ground	R14	—	—	—
GND	Ground	N14	—	—	—
GND	Ground	L14	—	—	—
GND	Ground	M15	—	—	—
GND	Ground	P15	—	—	—
GND	Ground	T15	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	V15	—	—	—
GND	Ground	Y15	—	—	—
GND	Ground	AB15	—	—	—
GND	Ground	AD15	—	—	—
GND	Ground	AF15	—	—	—
GND	Ground	W16	—	—	—
GND	Ground	AC16	—	—	—
GND	Ground	AA16	—	—	—
GND	Ground	AE16	—	—	—
GND	Ground	U16	—	—	—
GND	Ground	R16	—	—	—
GND	Ground	N16	—	—	—
GND	Ground	M17	—	—	—
GND	Ground	P17	—	—	—
GND	Ground	T17	—	—	—
GND	Ground	N18	—	—	—
GND	Ground	R18	—	—	—
GND	Ground	U18	—	—	—
GND	Ground	Y17	—	—	—
GND	Ground	AB17	—	—	—
GND	Ground	AD17	—	—	—
GND	Ground	AF17	—	—	—
GND	Ground	W18	—	—	—
GND	Ground	AC18	—	—	—
GND	Ground	AA18	—	—	—
GND	Ground	AE18	—	—	—
GND	Ground	AF19	—	—	—
GND	Ground	AD19	—	—	—
GND	Ground	AB19	—	—	—
GND	Ground	Y19	—	—	—
GND	Ground	V19	—	—	—
GND	Ground	T19	—	—	—
GND	Ground	P19	—	—	—
GND	Ground	M19	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	N20	—	—	—
GND	Ground	R20	—	—	—
GND	Ground	U20	—	—	—
GND	Ground	AE20	—	—	—
GND	Ground	AA20	—	—	—
GND	Ground	AC20	—	—	—
GND	Ground	W20	—	—	—
GND	Ground	AF21	—	—	—
GND	Ground	AD21	—	—	—
GND	Ground	AB21	—	—	—
GND	Ground	Y21	—	—	—
GND	Ground	V21	—	—	—
GND	Ground	T21	—	—	—
GND	Ground	P21	—	—	—
GND	Ground	M21	—	—	—
GND	Ground	AE22	—	—	—
GND	Ground	AC22	—	—	—
GND	Ground	AA22	—	—	—
GND	Ground	W22	—	—	—
GND	Ground	U22	—	—	—
GND	Ground	R22	—	—	—
GND	Ground	N22	—	—	—
GND	Ground	AF23	—	—	—
GND	Ground	AD23	—	—	—
GND	Ground	AB23	—	—	—
GND	Ground	Y23	—	—	—
GND	Ground	V23	—	—	—
GND	Ground	T23	—	—	—
GND	Ground	P23	—	—	—
GND	Ground	M23	—	—	—
GND	Ground	L24	—	—	—
GND	Ground	N24	—	—	—
GND	Ground	R24	—	—	—
GND	Ground	U24	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	W24	—	—	—
GND	Ground	AA24	—	—	—
GND	Ground	AC24	—	—	—
GND	Ground	AE24	—	—	—
GND	Ground	AF25	—	—	—
GND	Ground	AD25	—	—	—
GND	Ground	AB25	—	—	—
GND	Ground	Y25	—	—	—
GND	Ground	P27	—	—	—
GND	Ground	V17	—	—	—
GND	Ground	T25	—	—	—
GND	Ground	P25	—	—	—
GND	Ground	M25	—	—	—
GND	Ground	T27	—	—	—
GND	Ground	V27	—	—	—
GND	Ground	Y27	—	—	—
GND	Ground	AD27	—	—	—
GND	Ground	L12	—	—	—
XGND	SerDes Transceiver GND	AA30	—	—	—
XGND	SerDes Transceiver GND	AB32	—	—	—
XGND	SerDes Transceiver GND	AC30	—	—	—
XGND	SerDes Transceiver GND	AC34	—	—	—
XGND	SerDes Transceiver GND	AD30	—	—	—
XGND	SerDes Transceiver GND	AD31	—	—	—
XGND	SerDes Transceiver GND	AF32	—	—	—
XGND	SerDes Transceiver GND	AG30	—	—	—
XGND	SerDes Transceiver GND	D33	—	—	—
XGND	SerDes Transceiver GND	E28	—	—	—
XGND	SerDes Transceiver GND	E30	—	—	—
XGND	SerDes Transceiver GND	F32	—	—	—
XGND	SerDes Transceiver GND	G29	—	—	—
XGND	SerDes Transceiver GND	G31	—	—	—
XGND	SerDes Transceiver GND	H29	—	—	—
XGND	SerDes Transceiver GND	H32	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
XGND	SerDes Transceiver GND	H34	—	—	—
XGND	SerDes Transceiver GND	J29	—	—	—
XGND	SerDes Transceiver GND	J31	—	—	—
XGND	SerDes Transceiver GND	K28	—	—	—
XGND	SerDes Transceiver GND	K29	—	—	—
XGND	SerDes Transceiver GND	L29	—	—	—
XGND	SerDes Transceiver GND	L32	—	—	—
XGND	SerDes Transceiver GND	M30	—	—	—
XGND	SerDes Transceiver GND	N29	—	—	—
XGND	SerDes Transceiver GND	N30	—	—	—
XGND	SerDes Transceiver GND	N32	—	—	—
XGND	SerDes Transceiver GND	P29	—	—	—
XGND	SerDes Transceiver GND	P34	—	—	—
XGND	SerDes Transceiver GND	R30	—	—	—
XGND	SerDes Transceiver GND	R32	—	—	—
XGND	SerDes Transceiver GND	U29	—	—	—
XGND	SerDes Transceiver GND	U31	—	—	—
XGND	SerDes Transceiver GND	V29	—	—	—
XGND	SerDes Transceiver GND	V31	—	—	—
XGND	SerDes Transceiver GND	W30	—	—	—
XGND	SerDes Transceiver GND	Y32	—	—	—
XGND	SerDes Transceiver GND	AH31	—	—	—
SGND	SerDes Core Logic GND	A28	—	—	—
SGND	SerDes Core Logic GND	A32	—	—	—
SGND	SerDes Core Logic GND	A36	—	—	—
SGND	SerDes Core Logic GND	AA34	—	—	—
SGND	SerDes Core Logic GND	AB36	—	—	—
SGND	SerDes Core Logic GND	AD35	—	—	—
SGND	SerDes Core Logic GND	AE34	—	—	—
SGND	SerDes Core Logic GND	AF36	—	—	—
SGND	SerDes Core Logic GND	AG33	—	—	—
SGND	SerDes Core Logic GND	B30	—	—	—
SGND	SerDes Core Logic GND	B34	—	—	—
SGND	SerDes Core Logic GND	C29	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SGND	SerDes Core Logic GND	C33	—	—	—
SGND	SerDes Core Logic GND	D31	—	—	—
SGND	SerDes Core Logic GND	D35	—	—	—
SGND	SerDes Core Logic GND	E35	—	—	—
SGND	SerDes Core Logic GND	G34	—	—	—
SGND	SerDes Core Logic GND	G36	—	—	—
SGND	SerDes Core Logic GND	J35	—	—	—
SGND	SerDes Core Logic GND	K33	—	—	—
SGND	SerDes Core Logic GND	L36	—	—	—
SGND	SerDes Core Logic GND	M34	—	—	—
SGND	SerDes Core Logic GND	N35	—	—	—
SGND	SerDes Core Logic GND	R33	—	—	—
SGND	SerDes Core Logic GND	R36	—	—	—
SGND	SerDes Core Logic GND	T35	—	—	—
SGND	SerDes Core Logic GND	U34	—	—	—
SGND	SerDes Core Logic GND	V36	—	—	—
SGND	SerDes Core Logic GND	W33	—	—	—
SGND	SerDes Core Logic GND	Y35	—	—	—
SGND	SerDes Core Logic GND	AH35	—	—	—
SGND	SerDes Core Logic GND	AH33	—	—	—
AGND_SRDS1	SerDes PLL1 GND	B33	—	—	—
AGND_SRDS2	SerDes PLL2 GND	T36	—	—	—
AGND_SRDS3	SerDes PLL3 GND	AE36	—	—	—
SENSEGND_PL1	Platform GND Sense 1	AF12	—	—	8
SENSEGND_PL2	Platform GND Sense 2	K27	—	—	8
SENSEGND_CA	Core Group A GND Sense	K17	—	—	8
SENSEGND_CB	Core Group B GND Sense	AG16	—	—	8
USB1_AGND	USB1 PHY Transceiver GND	AH24	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AJ24	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AL25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AM25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR26	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR27	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_AGND	USB1 PHY Transceiver GND	AR28	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AT25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AT28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AH27	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AL28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AM28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN25	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN26	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN27	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AP25	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AP28	—	—	—
OVDD	General I/O Supply	AN22	—	OV _{DD}	—
OVDD	General I/O Supply	AJ14	—	OV _{DD}	—
OVDD	General I/O Supply	AJ18	—	OV _{DD}	—
OVDD	General I/O Supply	AL16	—	OV _{DD}	—
OVDD	General I/O Supply	AJ12	—	OV _{DD}	—
OVDD	General I/O Supply	AN18	—	OV _{DD}	—
OVDD	General I/O Supply	AG21	—	OV _{DD}	—
OVDD	General I/O Supply	AL20	—	OV _{DD}	—
OVDD	General I/O Supply	AT15	—	OV _{DD}	—
OVDD	General I/O Supply	AJ23	—	OV _{DD}	—
OVDD	General I/O Supply	AP16	—	OV _{DD}	—
OVDD	General I/O Supply	AR24	—	OV _{DD}	—
CVDD	eSPI & eSDHC Supply	AG24	—	CV _{DD}	—
CVDD	eSPI & eSDHC Supply	AJ29	—	CV _{DD}	—
CVDD	eSPI & eSDHC Supply	AP29	—	CV _{DD}	—
GVDD	DDR Supply	B2	—	GV _{DD}	—
GVDD	DDR Supply	B8	—	GV _{DD}	—
GVDD	DDR Supply	B14	—	GV _{DD}	—
GVDD	DDR Supply	C18	—	GV _{DD}	—
GVDD	DDR Supply	C12	—	GV _{DD}	—
GVDD	DDR Supply	C6	—	GV _{DD}	—
GVDD	DDR Supply	D4	—	GV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GVDD	DDR Supply	D10	—	GV _{DD}	—
GVDD	DDR Supply	D16	—	GV _{DD}	—
GVDD	DDR Supply	E14	—	GV _{DD}	—
GVDD	DDR Supply	E8	—	GV _{DD}	—
GVDD	DDR Supply	E2	—	GV _{DD}	—
GVDD	DDR Supply	F6	—	GV _{DD}	—
GVDD	DDR Supply	F12	—	GV _{DD}	—
GVDD	DDR Supply	AR8	—	GV _{DD}	—
GVDD	DDR Supply	G4	—	GV _{DD}	—
GVDD	DDR Supply	G10	—	GV _{DD}	—
GVDD	DDR Supply	G16	—	GV _{DD}	—
GVDD	DDR Supply	H14	—	GV _{DD}	—
GVDD	DDR Supply	H8	—	GV _{DD}	—
GVDD	DDR Supply	H2	—	GV _{DD}	—
GVDD	DDR Supply	J6	—	GV _{DD}	—
GVDD	DDR Supply	K10	—	GV _{DD}	—
GVDD	DDR Supply	K4	—	GV _{DD}	—
GVDD	DDR Supply	L2	—	GV _{DD}	—
GVDD	DDR Supply	L8	—	GV _{DD}	—
GVDD	DDR Supply	M6	—	GV _{DD}	—
GVDD	DDR Supply	N4	—	GV _{DD}	—
GVDD	DDR Supply	N10	—	GV _{DD}	—
GVDD	DDR Supply	P8	—	GV _{DD}	—
GVDD	DDR Supply	P2	—	GV _{DD}	—
GVDD	DDR Supply	R6	—	GV _{DD}	—
GVDD	DDR Supply	T10	—	GV _{DD}	—
GVDD	DDR Supply	T4	—	GV _{DD}	—
GVDD	DDR Supply	J12	—	GV _{DD}	—
GVDD	DDR Supply	U2	—	GV _{DD}	—
GVDD	DDR Supply	U8	—	GV _{DD}	—
GVDD	DDR Supply	V7	—	GV _{DD}	—
GVDD	DDR Supply	AK10	—	GV _{DD}	—
GVDD	DDR Supply	W10	—	GV _{DD}	—
GVDD	DDR Supply	AA6	—	GV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GVDD	DDR Supply	AR2	—	GV _{DD}	—
GVDD	DDR Supply	Y2	—	GV _{DD}	—
GVDD	DDR Supply	Y8	—	GV _{DD}	—
GVDD	DDR Supply	AC2	—	GV _{DD}	—
GVDD	DDR Supply	AD6	—	GV _{DD}	—
GVDD	DDR Supply	AE10	—	GV _{DD}	—
GVDD	DDR Supply	AE4	—	GV _{DD}	—
GVDD	DDR Supply	AF2	—	GV _{DD}	—
GVDD	DDR Supply	AF8	—	GV _{DD}	—
GVDD	DDR Supply	AB4	—	GV _{DD}	—
GVDD	DDR Supply	AB10	—	GV _{DD}	—
GVDD	DDR Supply	AC8	—	GV _{DD}	—
GVDD	DDR Supply	AG6	—	GV _{DD}	—
GVDD	DDR Supply	AH10	—	GV _{DD}	—
GVDD	DDR Supply	AH4	—	GV _{DD}	—
GVDD	DDR Supply	AJ2	—	GV _{DD}	—
GVDD	DDR Supply	AJ8	—	GV _{DD}	—
GVDD	DDR Supply	AR14	—	GV _{DD}	—
GVDD	DDR Supply	AK6	—	GV _{DD}	—
GVDD	DDR Supply	AL4	—	GV _{DD}	—
GVDD	DDR Supply	AL10	—	GV _{DD}	—
GVDD	DDR Supply	AM2	—	GV _{DD}	—
GVDD	DDR Supply	AM8	—	GV _{DD}	—
GVDD	DDR Supply	AP10	—	GV _{DD}	—
GVDD	DDR Supply	AN12	—	GV _{DD}	—
GVDD	DDR Supply	AN6	—	GV _{DD}	—
GVDD	DDR Supply	AP4	—	GV _{DD}	—
BVDD	Local Bus Supply	B24	—	BV _{DD}	—
BVDD	Local Bus Supply	K22	—	BV _{DD}	—
BVDD	Local Bus Supply	F20	—	BV _{DD}	—
BVDD	Local Bus Supply	F26	—	BV _{DD}	—
BVDD	Local Bus Supply	E24	—	BV _{DD}	—
BVDD	Local Bus Supply	E22	—	BV _{DD}	—
BVDD	Local Bus Supply	K24	—	BV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
BVDD	Local Bus Supply	H20	—	BV _{DD}	—
BVDD	Local Bus Supply	H18	—	BV _{DD}	—
SVDD	SerDes Core Logic Supply	A30	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	A34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AA33	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AB35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AD36	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AE33	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AF35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AG34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	B28	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	B32	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	B36	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	C31	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	C34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	C35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	D29	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	E36	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	F34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	G35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	J36	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	K34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	L35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	M33	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	N36	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	R34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	R35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	U33	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	V35	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	W34	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	Y36	—	SV _{DD}	—
SVDD	SerDes Core Logic Supply	AH36	—	SV _{DD}	—
XVDD	SerDes Transceiver Supply	AA29	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	AB30	—	XV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
XVDD	SerDes Transceiver Supply	AB31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	AC33	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	AD32	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	AE30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	AF31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	E32	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	E33	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	F28	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	F30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	G32	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	H31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	H33	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	J28	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	J30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	J32	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	K30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	L30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	L31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	M29	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	N31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	P30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	P33	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	R29	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	R31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	T29	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	T32	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	U30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	V30	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	V32	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	W29	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	Y31	—	XV _{DD}	—
XVDD	SerDes Transceiver Supply	AH32	—	XV _{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AK33	—	LV _{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AP31	—	LV _{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LVDD	Ethernet Controller 1 and 2 Supply	AL31	—	LV _{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AN33	—	LV _{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AJ35	—	LV _{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AR35	—	LV _{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AM35	—	LV _{DD}	—
POVDD	Fuse Programming Override Supply	AT17	—	POV _{DD}	33
VDD_PL	Platform Supply	M26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	P26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	T26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	V26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	Y26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AB26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AD26	—	V _{DD_PL}	—
VDD_PL	Platform Supply	N11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	R11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	W11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AA11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	M12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	P12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	T12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	V12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	Y12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AB12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AD12	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE13	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE15	—	V _{DD_PL}	—
VDD_PL	Platform Supply	V16	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE17	—	V _{DD_PL}	—
VDD_PL	Platform Supply	L11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE19	—	V _{DD_PL}	—
VDD_PL	Platform Supply	U11	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AC11	—	V _{DD_PL}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD_PL	Platform Supply	V20	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE21	—	V _{DD_PL}	—
VDD_PL	Platform Supply	V22	—	V _{DD_PL}	—
VDD_PL	Platform Supply	U13	—	V _{DD_PL}	—
VDD_PL	Platform Supply	R27	—	V _{DD_PL}	—
VDD_PL	Platform Supply	U23	—	V _{DD_PL}	—
VDD_PL	Platform Supply	W23	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AA27	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AC27	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE23	—	V _{DD_PL}	—
VDD_PL	Platform Supply	M24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	P24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	T24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	V24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	Y24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AB24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AD24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	N25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	R25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	U25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	W25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AA25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AC25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	N27	—	V _{DD_PL}	—
VDD_PL	Platform Supply	U27	—	V _{DD_PL}	—
VDD_PL	Platform Supply	W28	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AE25	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AF24	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AF22	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AF20	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AF16	—	V _{DD_PL}	—
VDD_PL	Platform Supply	W13	—	V _{DD_PL}	—
VDD_PL	Platform Supply	AF18	—	V _{DD_PL}	—
VDD_PL	Platform Supply	V14	—	V _{DD_PL}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD_PL	Platform Supply	V18	—	VDD_PL	—
VDD_PL	Platform Supply	L13	—	VDD_PL	—
VDD_PL	Platform Supply	L15	—	VDD_PL	—
VDD_PL	Platform Supply	L17	—	VDD_PL	—
VDD_PL	Platform Supply	L19	—	VDD_PL	—
VDD_PL	Platform Supply	L21	—	VDD_PL	—
VDD_PL	Platform Supply	L23	—	VDD_PL	—
VDD_PL	Platform Supply	L25	—	VDD_PL	—
VDD_PL	Platform Supply	AF14	—	VDD_PL	—
VDD_PL	Platform Supply	N23	—	VDD_PL	—
VDD_PL	Platform Supply	R23	—	VDD_PL	—
VDD_PL	Platform Supply	AA23	—	VDD_PL	—
VDD_PL	Platform Supply	AC23	—	VDD_PL	—
VDD_PL	Platform Supply	U21	—	VDD_PL	—
VDD_PL	Platform Supply	W21	—	VDD_PL	—
VDD_PL	Platform Supply	U15	—	VDD_PL	—
VDD_PL	Platform Supply	AC21	—	VDD_PL	—
VDD_PL	Platform Supply	AD22	—	VDD_PL	—
VDD_PL	Platform Supply	M22	—	VDD_PL	—
VDD_PL	Platform Supply	N13	—	VDD_PL	—
VDD_PL	Platform Supply	AC13	—	VDD_PL	—
VDD_PL	Platform Supply	P22	—	VDD_PL	—
VDD_PL	Platform Supply	T22	—	VDD_PL	—
VDD_PL	Platform Supply	Y22	—	VDD_PL	—
VDD_PL	Platform Supply	AB22	—	VDD_PL	—
VDD_PL	Platform Supply	AA13	—	VDD_PL	—
VDD_PL	Platform Supply	R13	—	VDD_PL	—
VDD_PL	Platform Supply	M14	—	VDD_PL	—
VDD_PL	Platform Supply	U17	—	VDD_PL	—
VDD_PL	Platform Supply	U19	—	VDD_PL	—
VDD_PL	Platform Supply	T14	—	VDD_PL	—
VDD_PL	Platform Supply	AD14	—	VDD_PL	—
VDD_PL	Platform Supply	AD16	—	VDD_PL	—
VDD_PL	Platform Supply	AD18	—	VDD_PL	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD_PL	Platform Supply	AD20	—	V _{DD_PL}	—
VDD_PL	Platform Supply	Y14	—	V _{DD_PL}	—
VDD_CA	Core/L2 Group A Supply	T20	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P20	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R21	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R19	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P14	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N19	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	M20	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N21	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	M16	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N15	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P16	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	T16	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R17	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	T18	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R15	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N17	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	M18	—	V _{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P18	—	V _{DD_CA}	—
VDD_CB	Core/L2 Group B Supply	W15	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	W19	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AA19	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	Y20	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AB14	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AA21	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	Y16	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AA15	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AC15	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AA17	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AC17	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	W17	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	Y18	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AB18	—	V _{DD_CB}	29

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD_CB	Core/L2 Group B Supply	AB16	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AC19	—	V _{DD_CB}	29
VDD_CB	Core/L2 Group B Supply	AB20	—	V _{DD_CB}	29
VDD_LP	Low Power Security Monitor Supply	AD28	—	V _{DD_LP}	—
AVDD_CC1	Core Complex PLL1 Supply	A20	—	—	13
AVDD_CC2	Core Complex PLL2 Supply	AT18	—	—	13
AVDD_PLAT	Platform PLL Supply	AT20	—	—	13
AVDD_DDR	DDR PLL Supply	A19	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	A33	—	—	13
AVDD_SRDS2	SerDes PLL2 Supply	U36	—	—	13
AVDD_SRDS3	SerDes PLL3 Supply	AE35	—	—	13
VDD_PL1	Platform Vdd Sense	AF11	—	—	8
VDD_PL2	Platform Vdd Sense	L27	—	—	8
SENSEVDD_CA	Core Group A Vdd Sense	K16	—	—	8
SENSEVDD_CB	Core Group B Vdd Sense	AG15	—	—	8
USB1_VDD_3P3	USB1 PHY Transceiver 3.3V Supply	AL24	—	—	—
USB1_VDD_3P3	USB1 PHY Transceiver 3.3V Supply	AJ25	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3V Supply	AJ26	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3V Supply	AJ27	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0V Supply	AH25	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0V Supply	AH26	—	—	—
Analog signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	B19	I	GV _{DD} /2	—
SD_IMP_CAL_TX	SerDes Tx Impedance Calibration	AF30	I	200Ω (±1%) to XV _{DD}	23
SD_IMP_CAL_RX	SerDes Rx Impedance Calibration	B27	I	200Ω (±1%) to SV _{DD}	24
TEMP_ANODE	Temperature Diode Anode	C21	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	B21	—	internal diode	9

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	AM26	—	—	36
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	AM27	—	—	36
USB1_VDD_1P8_DECAP	USB1 PHY 1.8V Output to External Decap	AL26	—	—	37
USB2_VDD_1P8_DECAP	USB2 PHY 1.8V Output to External Decap	AL27	—	—	37
No Connection Pins					
NC_A27	No Connection	A27	—	—	11
NC_B26	No Connection	B26	—	—	11
NC_C19	No Connection	C19	—	—	11
NC_C20	No Connection	C20	—	—	11
NC_C26	No Connection	C26	—	—	11
NC_C27	No Connection	C27	—	—	11
NC_D18	No Connection	D18	—	—	11
NC_D27	No Connection	D27	—	—	11
NC_E16	No Connection	E16	—	—	11
NC_E27	No Connection	E27	—	—	11
NC_G27	No Connection	G27	—	—	11
NC_H12	No Connection	H12	—	—	11
NC_H13	No Connection	H13	—	—	11
NC_H15	No Connection	H15	—	—	11
NC_H27	No Connection	H27	—	—	11
NC_J11	No Connection	J11	—	—	11
NC_J13	No Connection	J13	—	—	11
NC_J14	No Connection	J14	—	—	11
NC_K11	No Connection	K11	—	—	11
NC_K12	No Connection	K12	—	—	11
NC_K13	No Connection	K13	—	—	11
NC_K14	No Connection	K14	—	—	11
NC_R28	No Connection	R28	—	—	11
NC_T28	No Connection	T28	—	—	11
NC_U28	No Connection	U28	—	—	11
NC_V28	No Connection	V28	—	—	11

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_W27	No Connection	W27	—	—	11
NC_Y28	No Connection	Y28	—	—	11
NC_AA28	No Connection	AA28	—	—	11
NC_AB28	No Connection	AB28	—	—	11
NC_AB29	No Connection	AB29	—	—	11
NC_AC28	No Connection	AC28	—	—	11
NC_AC29	No Connection	AC29	—	—	11
NC_AD29	No Connection	AD29	—	—	11
NC_AE29	No Connection	AE29	—	—	11
NC_AF26	No Connection	AF26	—	—	11
NC_AF27	No Connection	AF27	—	—	11
NC_AF28	No Connection	AF28	—	—	11
NC_AF29	No Connection	AF29	—	—	11
NC_AG26	No Connection	AG26	—	—	11
NC_AG27	No Connection	AG27	—	—	11
NC_AG28	No Connection	AG28	—	—	11
NC_AG29	No Connection	AG29	—	—	11
NC_AH30	No Connection	AH30	—	—	11
NC_AM12	No Connection	AM12	—	—	11
NC_AN13	No Connection	AN13	—	—	11
NC_AP11	No Connection	AP11	—	—	11
NC_AP14	No Connection	AP14	—	—	11
NC_AT14	No Connection	AT14	—	—	11
Reserved pins					
Reserve_A21	—	A21	—	—	41
Reserve_A25	—	A25	—	—	11
Reserve_C32	—	C32	—	—	11
Reserve_D32	—	D32	—	—	11
Reserve_F1	—	F1	—	—	11
Reserve_F2	—	F2	—	—	11
Reserve_G1	—	G1	—	—	11
Reserve_G2	—	G2	—	—	11
Reserve_L28	—	L28	—	GND	21
Reserve_M28	—	M28	—	GND	21

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Reserve_N28	—	N28	—	GND	21
Reserve_P28	—	P28	—	GND	21
Reserve_U32	—	U32	—	—	11
Reserve_U35	—	U35	—	—	11
Reserve_AD33	—	AD33	—	—	11
Reserve_AD34	—	AD34	—	—	11
Reserve_AG11	—	AG11	—	GND	21
Reserve_AG12	—	AG12	—	GND	21
Reserve_AG25	—	AG25	—	—	11
Reserve_AH11	—	AH11	—	GND	21
Reserve_AH12	—	AH12	—	GND	21
Reserve_AK1	—	AK1	—	—	11
Reserve_AK2	—	AK2	—	—	11
Reserve_AL1	—	AL1	—	—	11

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Reserve_AL2	—	AL2	—	—	11
Reserve_AT19	—	AT19	—	—	41

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
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Notes:

1. Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend a weak pull-up resistor (2–10 k Ω) be placed on this pin to BV_{DD}, to ensure no random chip select assertion due to possible noise, and so forth.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the correspondent power and ground nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A only with a clear understanding that proper thermal diode operation is not implied and the thermal diode feature may not be available in the production device.
11. Do not connect.
12. These are test signals for factory use only and must be pulled up (100 Ω –1 k Ω) to OV_{DD} for normal chip operation.
13. Independent supplies derived from board V_{DD_PL} (Core Complex, Platform, DDR) or SV_{DD} (SerDes).
14. Recommend a pull-up resistor of 1-k Ω be placed on this pin to OV_{DD} if I2C interface is used.
15. This pin requires an external 1-k Ω pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, Dn_MDIC[0] is grounded through an 20- Ω (full-strength mode) or 40.2- Ω (half-strength mode) precision 1% resistor and Dn_MDIC[1] is connected to GV_{DD} through an 20- Ω (full-strength mode) or 40.2- Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
18. These pins should be pulled up to 1.2V through a 180 $\Omega \pm 1\%$ resistor for EM2_MDC and a 330 $\Omega \pm 1\%$ resistor for EM2_MDIO.
20. Pin has a weak internal pull-up.
21. These pins should be pulled to ground (GND).
22. Ethernet Management Interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
23. This pin requires a 200- Ω pull-up to XV_{DD}.
24. This pin requires a 200- Ω pull-up to SV_{DD}.
25. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
26. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
27. See [Section 3.6, “Connection recommendations,”](#) for additional details on this signal.
28. For P5010, this signal must be pulled low to GND.
29. For P5010, voltage rail must be connected to GND.
30. Warning, incorrect voltage select settings can lead to irreversible device damage. See [Section 3.2, “Supply power default setting.”](#)
31. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
32. The *cfg_xvdd_sel*(LAD[26]) reset configuration pin must select the correct voltage that is being supplied on the XV_{DD} pin. Incorrect voltage select settings can lead to irreversible device damage.

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
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33. See [Section 2.2, “Power up sequencing](#) and [Section 5, “Security fuse processor,”](#) for additional details on this signal.
34. For P5010 mode, the DDR2 controller signals must be left unconnected.
35. Pin must NOT be pulled down during power-on reset.
36. This pin should be connected to GND through a $10\text{k}\Omega \pm 0.1\%$ resistor with a low temperature coefficient of $\leq 25\text{ppm}/^\circ\text{C}$ for bias generation.
37. A 1uF to 1.5uF capacitor connected to GND is required on this signal. A list of recommended capacitors are shown in [Section 3.6.4.2, “USBn_VDD_1P8_DECAP capacitor options.”](#)
38. A divider network is required on this signal. See [Section 3.6.4.1, “USB divider network.”](#)
39. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull-up on LGPL4 is required.
40. Functionally, this pin is an input, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
41. If migration from a P4 device, this pin is allowed to be powered by AVDD_CC2. If not migrating, do not connect.

2 Electrical characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other electrical characteristics.

2.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum operating conditions¹

Parameter	Symbol	Maximum value	Unit	Note
Core Group A (core 0) supply voltage	V _{DD_CA}	−0.3 to 1.21	V	9, 11
Core Group B (core 1) supply voltage	V _{DD_CB}	−0.3 to 1.21	V	9, 11
Platform supply voltage	V _{DD_PL} ⁿ	−0.3 to 1.1	V	9, 10, 11
PLL supply voltage (Core, Platform, DDR)	AV _{DD}	−0.3 to 1.1	V	—
PLL supply voltage (SerDes, filtered from SV _{DD})	AV _{DD_SRDS}	−0.3 to 1.1	V	—
Fuse Programming Override Supply	POV _{DD}	−0.3 to 1.65	V	1
DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV _{DD}	−0.3 to 3.63	V	—
eSPI, eSHDC I/O voltage	CV _{DD}	−0.3 to 3.63 −0.3 to 2.75 −0.3 to 1.98	V	—

Table 2. Absolute maximum operating conditions¹ (continued)

Parameter	Symbol	Maximum value	Unit	Note
DDR3 and DDR3L DRAM I/O voltage	GV_{DD}	–0.3 to 1.65	V	—
Enhanced Local Bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receiver	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transmitter	XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Ethernet I/O, Ethernet Management Interface 1 (EMI1), 1588, GPIO	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3
Ethernet Management Interface 2 (EMI2)	—	–0.3 to 1.32	V	8
USB PHY Transceiver supply voltage	$USB_V_{DD_3P3}$	–0.3 to 3.63	V	—
USB PHY PLL supply voltage	$USB_V_{DD_1P0}$	–0.3 to 1.1	V	—
Low Power Security Monitor Supply	V_{DD_LP}	–0.3 to 1.1	V	—

Table 2. Absolute maximum operating conditions¹ (continued)

Parameter		Symbol	Maximum value	Unit	Note
Input voltage ⁷	DDR3 and DDR3L DRAM signals	MV_{IN}	-0.3 to $(GV_{DD} + 0.3)$	V	2, 7
	DDR3 and DDR3L DRAM reference	MV_{REF}^n	-0.3 to $(GV_{DD}/2 + 0.3)$	V	2, 7
	Ethernet signals (except EMI2)	LV_{IN}	-0.3 to $(LV_{DD} + 0.3)$	V	3, 7
	eSPI, eSHDC signals	CV_{IN}	-0.3 to $(CV_{DD} + 0.3)$	V	4, 7
	Enhanced Local Bus signals	BV_{IN}	-0.3 to $(BV_{DD} + 0.3)$	V	5, 7
	DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O signals	OV_{IN}	-0.3 to $(OV_{DD} + 0.3)$	V	6, 7
	SerDes signals	SV_{IN}	-0.4 to $(SV_{DD} + 0.3)$	V	7
	USB PHY Transceiver signals	$USB_V_{IN_3P3}$	-0.3 to $(USB_V_{DD_3P3} + 0.3)$	V	7
	Ethernet Management Interface 2 (EMI2) signals	—	-0.3 to $(1.2 + 0.3)$	V	7
Storage junction temperature range		T_{stg}	-55 to 150	°C	—

Note:

- Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (C,S,B,G,L,O) V_{IN} may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 8.
- Ethernet Management Interface 2 pins function as open drain I/Os. The interface should conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
- Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
- Implementation may choose either $V_{DD_PL}^n$ pin for feedback loop. If the platform and core groups are supplied by a single regulator, it is recommended that V_{DD_CA} be used.
- V_{DD_PL} voltage must not exceed V_{DD_CA} or V_{DD_CB} .

2.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Parameter	Symbol	Recommended value	Unit	Note
Core Group A (core 0) supply voltage	V_{DD_CA}	1.0 ± 50mV (core frequency = 1200 MHz) 1.1V ± 50mV (core frequency > 1200 MHz)	V	1, 2, 6
Core Group B (core 1) supply voltage	V_{DD_CB}	1.0 ± 50mV (core frequency = 1200 MHz) 1.1V ± 50mV (core frequency > 1200 MHz)	V	1, 2, 6
Platform supply voltage	V_{DD_PL}	1.0 ± 50mV	V	2, 6
PLL supply voltage (Core, Platform, DDR)	AV_{DD}	1.0 ± 50mV	V	—
PLL supply voltage (SerDes)	AV_{DD_SRDS}	1.0 ± 50mV	V	—
Fuse Programming Override Supply	POV_{DD}	1.5 ± 75mV	V	3
DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	3.3 ± 165mV	V	—
eSPI, eSDHC I/O voltage	CV_{DD}	3.3 ± 165mV 2.5 ± 125mV 1.8 ± 90mV	V	—
DDR DRAM I/O voltage DDR3 DDR3L	GV_{DD}	1.5 ± 75mV 1.35 ± 67mV	V	—
Enhanced Local Bus I/O voltage	BV_{DD}	3.3 ± 165mV 2.5 ± 125mV 1.8 ± 90mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receiver	SV_{DD}	1.0 ± 50mV	V	—
Pad power supply for SerDes transmitter	XV_{DD}	1.8 ± 90mV 1.5 ± 75mV	V	—
Ethernet I/O, Ethernet Management Interface 1 (EMI1), 1588, GPIO supply	LV_{DD}	3.3 ± 165mV 2.5 ± 125mV	V	4
USB PHY Transceiver supply voltage	$USB_V_{DD_3P3}$	3.3 ± 165mV	V	—
USB PHY PLL supply voltage	$USB_V_{DD_1P0}$	1.0 ± 50mV	V	—
Low Power Security Monitor Supply	V_{DD_LP}	1.0 ± 50mV	V	—

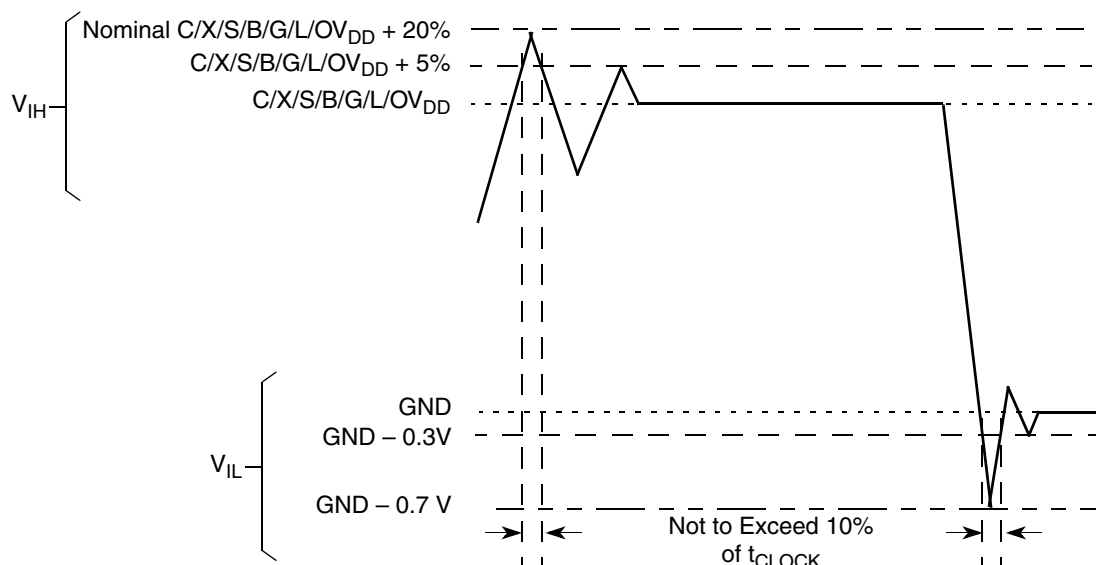
Table 3. Recommended operating conditions (continued)

Parameter		Symbol	Recommended value	Unit	Note
Input voltage	DDR3 and DDR3L DRAM signals	MV _{IN}	GND to GV _{DD}	V	—
	DDR3 and DDR3L DRAM reference	MV _{REF}	GV _{DD} /2 ± 1%	V	—
	Ethernet signals (except EMI2)	LV _{IN}	GND to LV _{DD}	V	—
	eSPI, eSHDC signals	CV _{IN}	GND to CV _{DD}	V	—
	Enhanced Local Bus signals	BV _{IN}	GND to BV _{DD}	V	—
	DUART, I ² C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV _{IN}	GND to OV _{DD}	V	—
	SerDes signals	SV _{IN}	GND to SV _{DD}	V	—
	USB PHY Transceiver signals	USB_V _{IN_3P3}	GND to USB_V _{DD_3P3}	V	—
	Ethernet Management Interface 2 (EMI2) signals	—	GND to 1.2V	V	5
Operating Temperature range	Normal Operation	T _A , T _J	T _A = 0 (min) to T _J = 105 (max)	°C	—
	Extended Temperature	T _A , T _J	T _A = -40 (min) to T _J = 105 (max)	°C	—
	Secure Boot Fuse Programming	T _A , T _J	T _A = 0(min) to T _J = 70 (max)	°C	3

Note:

1. V_{DD_CA} voltage and V_{DD_CB} voltage must be the same value.
2. V_{DD_PL} voltage must not exceed V_{DD_CA} or V_{DD_CB}.
3. POV_{DD} must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in [Section 2.2, “Power up sequencing.”](#)
4. Selecting RGMII limits LV_{DD} to 2.5V.
5. Ethernet Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
6. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

t_{CLOCK} refers to the clock period associated with the respective interface:

For I2C, t_{CLOCK} refers to SYSCLK.

For DDR GV_{DD} , t_{CLOCK} refers to Dn_MCK .

For eSPI CV_{DD} , t_{CLOCK} refers to SPI_CLK.

For eLBC BV_{DD} , t_{CLOCK} refers to LCLK.

For SerDes XV_{DD} , t_{CLOCK} refers to SD_REF_CLK.

For dTSEC LV_{DD} , t_{CLOCK} refers to EC_GTX_CLK125.

For JTAG OV_{DD} , t_{CLOCK} refers to TCK.

For SerDes SV_{DD} , t_{CLOCK} refers to SD_REF_CLK.

Figure 8. Overshoot/undershoot voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/SV_{DD}/XV_{DD}$

The core and platform voltages must always be provided at nominal 1.0 V or 1.1 V. See [Table 3](#) for the actual recommended core voltage conditions. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in [Table 3](#). The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD} , BV_{DD} , OV_{DD} , and LV_{DD} -based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied MV_{REFn} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.5 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output driver characteristics

This table provides information about the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output drive capability

Driver type	Output impedance (Ω)	(Nominal) Supply voltage	Note
Local Bus interface utilities signals	45 45 45	BV _{DD} = 3.3 V BV _{DD} = 2.5 V BV _{DD} = 1.8 V	—
DDR3 signal	20 (full-strength mode) 40 (half-strength mode)	GV _{DD} = 1.5 V	1
DDR3L signal	20 (full-strength mode) 40 (half-strength mode)	GV _{DD} = 1.35 V	1
eTSEC/10/100 signals	45 45	LV _{DD} = 3.3 V LV _{DD} = 2.5 V	—
DUART, system control, JTAG	45	OV _{DD} = 3.3 V	—
I ² C	45	OV _{DD} = 3.3 V	—
eSPI and SD/MMC	45 45 45	CV _{DD} = 3.3 V CV _{DD} = 2.5 V CV _{DD} = 1.8 V	—

Note:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min).

2.2 Power up sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

2. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}, and USB_V_{DD_3P3}. Drive POV_{DD} = GND.
 - PORESET input must be driven asserted and held during this step
 - IO_VSEL inputs must be driven during this step and held stable during normal operation.
 - USB_V_{DD_3P3} rise time (10% to 90%) has a minimum of 350 μ s.
3. Bring up V_{DD_PL}, V_{DD_CA}, V_{DD_CB}, SV_{DD}, AV_{DD} (cores, platform, DDR, SerDes) and USB_V_{DD_1P0}. V_{DD_PL} and USB_V_{DD_1P0} must be ramped up simultaneously.
4. Bring up GV_{DD} and XV_{DD}.
5. Negate PORESET input as long as the required assertion/hold time has been met per [Table 17](#).
6. For secure boot fuse programming: After negation of PORESET, drive POV_{DD} = 1.5 V after a required minimum delay per [Table 5](#). After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled (PORESET assertion) or powered down (V_{DD_PL} ramp down) per the required timing specified in [Table 5](#). See [Section 5, “Security fuse processor,”](#) for additional details.

WARNING

Only two secure boot fuse programming events are permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

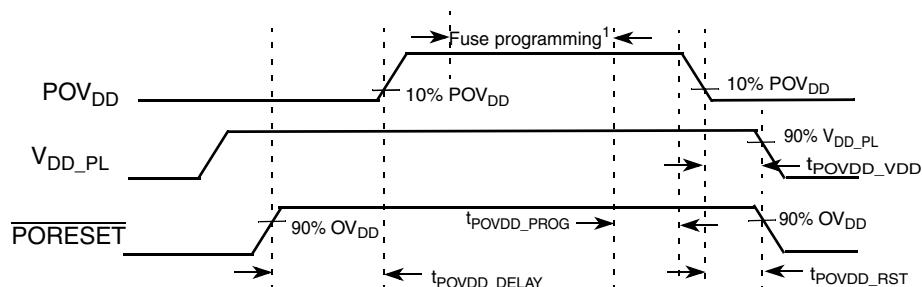
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 9. POV_{DD} timing diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD} .

Table 5. POV_{DD} timing ⁵

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	μ s	2
t_{POVDD_VDD}	0	—	μ s	3
t_{POVDD_RST}	0	—	μ s	4

Note:

1. Delay required from the negation of $\overline{PORESET}$ to driving POV_{DD} ramp up. Delay measured from $\overline{PORESET}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while $POV_{DD} = GND$. After fuse programming is completed, it is required to return $POV_{DD} = GND$.
3. Delay required from POV_{DD} ramp down complete to V_{DD_PL} ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before V_{DD_PL} is at 90% V_{DD} .
4. Delay required from POV_{DD} ramp down complete to $\overline{PORESET}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{PORESET}$ assertion reaches 90% OV_{DD} .
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See [Section 3.2](#), “Supply power default setting.”

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD_CA} , V_{DD_CB} or V_{DD_PL} supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per [Section 2.2, “Power up sequencing,”](#) it is required that $POV_{DD} = GND$ before the system is power cycled ($PORESET$ assertion) or powered down (V_{DD_PL} ramp down) per the required timing specified in [Table 5](#).

V_{DD_PL} and $USB_V_{DD_1P0}$ must be ramped down simultaneously. $USB_V_{DD_1P8_DECAP}$ should start ramping down only after $USB_V_{DD_3P3}$ is below 1.65 V.

2.4 Power characteristics

This table shows the power dissipations of the V_{DD_CA} , V_{DD_CB} , SV_{DD} , and V_{DD_PL} supply for various operating platform clock frequencies versus the core and DDR clock frequencies for the P5020. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers are available after the measurement on the silicon is complete.

Table 6. P5020 power dissipation

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD_PL} , SV_{DD} (V)	V_{DD_CA} , V_{DD_CB} (V)	Junction temp (°C)	Core and platform power ¹ (W)	V_{DD_PL} power (W)	V_{DD_CA} power (W)	V_{DD_CB} power (W)	SV_{DD} power (W)	Note
Typical	2000	800	1333	600	1.0	1.1	65	16	—	—	—	—	2, 3
Thermal							105	28	—	—	—	—	5, 7
Maximum								30	19	8	8	2	4, 6, 7
Typical	1800	700	1300	500	1.0	1.1	65	14	—	—	—	—	2, 3
Thermal							105	26	—	—	—	—	5, 7
Maximum								28	19	7	7	2	4, 6, 7
Typical	1600	600	1200	450	1.0	1.1	65	13	—	—	—	—	2, 3
Thermal							105	22	—	—	—	—	5, 7
Maximum								23	16	6	6	2	4, 6, 7

Table 6. P5020 power dissipation (continued)

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V _{DD_PL} , SV _{DD} (V)	V _{DD_CA} , V _{DD_CB} (V)	Junction temp (°C)	Core and platform power ¹ (W)	V _{DD_PL} power (W)	V _{DD_CA} power (W)	V _{DD_CB} power (W)	SV _{DD} power (W)	Note
Typical	1200	600	1200	450	1.0	1.0	65	13	—	—	—	—	2, 3
Thermal							105	18	—	—	—	—	5, 7
Maximum								18	16	5	5	2	4, 6, 7

Note:

1. Combined power of V_{DD_PL}, V_{DD_CA}, V_{DD_CB}, SV_{DD} with both DDR controllers and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the power dissipations of the V_{DD_CA}, SV_{DD}, and V_{DD_PL} supply for various operating platform clock frequencies versus the core and DDR clock frequencies for the P5010. Note that these numbers are based on design estimates only and are preliminary. More accurate power numbers are available after the measurement on the silicon is complete.

Table 7. P5010 power dissipation

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	PME/FM Freq (MHz)	V _{DD_PL} , SV _{DD} (V)	V _{DD_CA} (V)	Junction Temp (°C)	Core and Platform Power ¹ (W)	V _{DD_PL} Power (W)	V _{DD_CA} Power (W)	SV _{DD} Power (W)	Note
Typical	2000	800	1333	600	1.0	1.1	65	14	—	—	—	2, 3
Thermal							105	24	—	—	—	5, 7
Maximum								25	19	8	2	4, 6, 7
Typical	1800	700	1300	500	1.0	1.1	65	12	—	—	—	2, 3
Thermal							105	22	—	—	—	5, 7
Maximum								23	19	7	2	4, 6, 7
Typical	1600	600	1200	450	1.0	1.1	65	12	—	—	—	2, 3
Thermal							105	19	—	—	—	5, 7
Maximum								19	16	6	2	4, 6, 7

Table 7. P5010 power dissipation (continued)

Power Mode	Core Freq (MHz)	Plat Freq (MHz)	DDR Data Rate (MT/s)	PME/FM Freq (MHz)	V _{DD_PL} , SV _{DD} (V)	V _{DD_CA} , (V)	Junction Temp (°C)	Core and Platform Power ¹ (W)	V _{DD_PL} Power (W)	V _{DD_CA} Power (W)	SV _{DD} Power (W)	Note
Typical	1200	600	1200	450	1.0	1.0	65	12	—	—	—	2, 3
Thermal							105	15	—	—	—	5, 7
Maximum								15	15	2	2	4, 6, 7

Note:

1. Combined power of VDD_PL, VDD_CA, VDD_CB, SVDD with DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% and executing DMA on the platform at 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 80% and executing DMA on the platform at 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the all I/O power supply estimated values.

Table 8. P5020 I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Maximum	Unit	Notes
DDR3 64 Bits Per Controller	667 MT/s data rate	GVdd (1.5V)	0.759	1.897	W	1,2,5,6
	800 MT/s data rate		0.769	1.923		
	1066 MT/s data rate		0.790	1.974		
	1200 MT/s data rate		0.800	2.000		
	1333 MT/s data rate		0.810	2.203		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI	x1, 1.25 G-baud	XVdd (1.5V)	0.078	0.087	W	1
	x2, 1.25 G-baud		0.119	0.134		
	x4, 1.25 G-baud		0.202	0.226		
	x8, 1.25 G-baud		0.367	0.411		
HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUI (cont.)	x1, 2.5/3.0/3.125/5.0 G-baud	XVdd (1.5V)	0.088	0.099	W	1
	x2, 2.5/3.0/3.125/5.0 G-baud		0.139	0.156		
	x4, 2.5/3.0/3.125/5.0 G-baud		0.241	0.270		
	x8, 2.5/3.0/3.125/5.0 G-baud		0.447	0.501		
dTSEC Per Controller	RGMII	LVdd (2.5V)	0.075	0.100	W	1,3,6
IEEE 1588	—	LVdd (2.5V)	0.004	0.005	W	1,3,6
eLBC	32-bit, 100Mhz	BVdd (1.8V)	0.048	0.120	W	1,3,6

Table 8. P5020 I/O power supply estimated values (continued)

	16-bit, 100Mhz	BVdd (2.5V)	0.072	0.193		
		BVdd (3.3V)	0.120	0.277		
		BVdd (1.8V)	0.021	0.030	W	1,3,6
		BVdd (2.5V)	0.036	0.046		
		BVdd (3.3V)	0.057	0.076		
eSDHC	—	OVdd (3.3V)	0.014	0.150	W	1,3,6
eSPI	—	CVdd (1.8V)	0.004	0.005	W	1,3,6
		CVdd (2.5V)	0.006	0.008		
		CVdd (3.3V)	0.010	0.013		
USB	—	USB_V _{DD} _3P3	0.012	0.015	W	1,3,6
I2C	—	OVdd (3.3V)	0.002	0.003	W	1,3,6
DUART	—	OVdd (3.3V)	0.006	0.008	W	1,3,6
GPIO	x8	1.8V	0.005	0.006	W	1,3,4,6
		2.5V	0.007	0.009		
		3.3V	0.009	0.011		
Others (Reset, System Clock, JTAG & Misc)	—	3.3V	0.003	0.015	W	1,3,4,6

Note:

1. The typical values are estimates and based on simulations at 65°C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization
3. Assuming 15 pF total capacitance load
4. GPIO's are supported on 1.8 V, 2.5 V and 3.3 V rails as specified in the hardware specifications.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105°C. The values are not intended to be used as the maximum guaranteed current.

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the chip's PLLs, at allowable voltage levels.

Table 9. AV_{DD} power dissipation

AV _{DD} S	Typical	Maximum	Unit	Note
AV _{DD} _DDR	5	15	mW	1
AV _{DD} _CC1				
AV _{DD} _CC2				
AV _{DD} _PLAT				

Table 9. AV_{DD} power dissipation (continued)

AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}				
AV_{DD_SRDS3}				
USB_ V_{DD_1P0}	—	10	mW	3

Note:

1. V_{DD_CA} , $V_{DD_CB} = 1.1$ V, $T_A = 80^\circ\text{C}$, $T_J = 105^\circ\text{C}$
2. $SV_{DD} = 1.0$ V, $T_A = 80^\circ\text{C}$, $T_J = 105^\circ\text{C}$
3. USB_ $V_{DD_1P0} = 1.0$ V, $T_A = 80^\circ\text{C}$, $T_J = 105^\circ\text{C}$

This table shows the estimated power dissipation on the POV_{DD} supply for the chip, at allowable voltage levels.

Table 10. POV_{DD} power dissipation

Supply	Maximum	Unit	Note
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the chip, at allowable voltage levels.

Table 11. V_{DD_LP} power dissipation

Supply	Maximum	Unit	Note
V_{DD_LP} (P5020/P5010 on, 105C)	1.5	mW	1
V_{DD_LP} (P5020/P5010 off, 70C)	195	uW	2
V_{DD_LP} (P5020/P5010 off, 40C)	132	uW	2

Note:

1. $V_{DD_LP} = 1.0$ V, $T_J = 105^\circ\text{C}$.
2. When P5020/P5010 is off, V_{DD_LP} may be supplied by battery power to the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches V_{DD_LP} to battery when P5020/P5010 is powered down. See P5020/P5010 Reference Manual Trust Architecture chapter for more information.

2.5 Thermal

This table shows the thermal characteristics for the chip.

Table 12. Package thermal characteristics ⁶

Rating	Board	Symbol	Value	Unit	Note
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	14	$^\circ\text{C/W}$	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	10	$^\circ\text{C/W}$	1, 2
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	9	$^\circ\text{C/W}$	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	$^\circ\text{C/W}$	1, 2

Table 12. Package thermal characteristics (continued)⁶

Rating	Board	Symbol	Value	Unit	Note
Junction to board	—	$R_{\Theta JB}$	3	°C/W	3
Junction to case top	—	$R_{\Theta JCtop}$	0.44	°C/W	4
Junction to lid top	—	$R_{\Theta JClid}$	0.17	°C/W	5

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. Reference [Section 3.8, “Thermal management information,”](#) for additional details.

2.6 Input clocks

This section discusses the system clock timing specifications for DC and AC power, spread spectrum sources, real time clock timing, and dTSEC gigabit Ethernet reference clocks AC timing.

2.6.1 System clock (SYSCLK) timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 13. SYSCLK DC electrical characteristics ($OV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	—	15	pf	—
Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$)	I_{IN}	—	—	±40	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
2. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

Electrical characteristics

This table provides the system clock (SYSCLK) AC timing specifications.

Table 14. SYSCLK AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	100	—	166	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	6	—	10	ns	1, 2
SYSCLK duty cycle	$t_{\text{KHK}} / t_{\text{SYSCLK}}$	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	150	ps	—
SYSCLK jitter phase noise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{\text{DD}}/2$.
3. Slew rate as measured from $\pm 0.3 \Delta V_{\text{AC}}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.6.2 Spread spectrum sources

Spread spectrum clock sources is an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in [Table 15](#) considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread spectrum sources if the recommendations listed in [Table 15](#) are observed.

Table 15. Spread spectrum clock source recommendations

For recommended operating conditions, see [Table 3](#).

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in [Table 14](#).
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

2.6.3 Real time clock timing

The real time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum pulse width of the RTC signal should be greater than $16\times$ the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 dTSEC gigabit Ethernet reference clock timing

This table provides the dTSEC gigabit Ethernet reference clocks AC timing specifications.

Table 16. EC_GTX_CLK125 AC timing specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV _{DD} = 2.5 V LV _{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	—	53	%	2
EC_GTX_CLK125 jitter	—	—	—	± 150	ps	2

Note:

1. Rise and fall times for EC_GTX_CLK125 are measured from 20% to 80% (rise time) and 80% to 20% (fall time) of LV_{DD}.
2. EC_GTX_CLK125 is used to generate the GTX clock for the dTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the dTSEC GTX_CLK. See [Section 2.12.2.3, “RGMII AC timing specifications,”](#) for duty cycle for 10Base-T and 100Base-T reference clock.

2.6.5 Other input clocks

A description of the overall clocking of this device is available in the reference manual for your chip in the form of a clock subsystem block diagram. For information on the input clock requirements of functional blocks sourced external of the device, such as SerDes, Ethernet Management, eSDHC, Local Bus, see the specific interface section.

2.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications.

Table 17. RESET initialization timing specifications

Parameter	Min	Max	Unit ¹	Note
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2

Table 17. RESET initialization timing specifications (continued)

Parameter	Min	Max	Unit ¹	Note
Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the chip.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of $\overline{\text{HRESET}}$ negation is documented in Section 4.4.1 “Power-On Reset Sequence,” of the reference manual for your chip.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to [Section 2.2](#), “Power up sequencing.”

This table provides the PLL lock times.

Table 18. PLL lock times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

2.8 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 19. Power supply ramp rate

Parameter	Min	Max	Unit	Note
Required ramp rate for all voltage supplies (including OV_{DD} / CV_{DD} / GV_{DD} / BV_{DD} / SV_{DD} / XV_{DD} / LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see [Table 3](#)).

2.9 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required $\text{GV}_{\text{DD}}(\text{typ})$ voltage is 1.5 V when interfacing to DDR3 SDRAM and $\text{GV}_{\text{DD}}(\text{typ})$ voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.9.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 20. DDR3 SDRAM interface DC electrical characteristics ($GV_{DD} = 1.5\text{ V}$)¹

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REFn}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	$MV_{REFn} + 0.100$	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REFn} - 0.100$	V	5
I/O leakage current	I_{OZ}	-50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$ and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed the MV_{REFn} DC level by more than $\pm 1\%$ of the DC value (that is, $\pm 15\text{ mV}$).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REFn} with a min value of $MV_{REFn} - 0.04$ and a max value of $MV_{REFn} + 0.04$. V_{TT} should track variations in the DC level of MV_{REFn} .
4. The voltage regulator for MV_{REFn} must meet the specifications stated in [Table 23](#).
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 21. DDR3L SDRAM interface DC electrical characteristics ($GV_{DD} = 1.35\text{ V}$)¹

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REFn}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	$MV_{REFn} + 0.090$	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	$MV_{REFn} - 0.090$	V	5

Electrical characteristics

Table 21. DDR3L SDRAM interface DC electrical characteristics ($GV_{DD} = 1.35\text{ V}$)¹ (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
I/O leakage current	I_{OZ}	-50	50	μA	6
Output high current ($V_{OUT} = 0.641\text{ V}$)	I_{OH}	—	-23.3	mA	7, 8
Output low current ($V_{OUT} = 0.641\text{ V}$)	I_{OL}	23.3	—	mA	7, 8

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$ and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed the MV_{REFn} DC level by more than $\pm 1\%$ of the DC value (that is, $\pm 13.5\text{ mV}$).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REFn} with a min value of $MV_{REFn} - 0.04$ and a max value of $MV_{REFn} + 0.04$. V_{TT} should track variations in the DC level of MV_{REFn} .
4. The voltage regulator for MV_{REFn} must meet the specifications stated in [Table 23](#).
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. I_{OH} and I_{OL} are measured at $GV_{DD} = 1.283\text{ V}$

This table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 22. DDR3 and DDR3L SDRAM capacitance

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. $GV_{DD} = 1.5\text{ V} \pm 0.075\text{ V}$ (for DDR3), $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.150 V.
2. This parameter is sampled. $GV_{DD} = 1.35\text{ V} - 0.067\text{ V} \div + 0.100\text{ V}$ (for DDR3L), $f = 1\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.167 V.

This table provides the current draw characteristics for MV_{REFn} .

Table 23. Current draw characteristics for MV_{REFn}

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MV_{REFn}	MIV_{REFn}	—	1250	μA	—
Current draw for DDR3L SDRAM for MV_{REFn}	MIV_{REFn}	—	1250	μA	—

2.9.2 DDR3 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required $GV_{DD}(\text{typ})$ voltage is 1.5 V when interfacing to DDR3 SDRAM and the required $GV_{DD}(\text{typ})$ voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.9.2.1 DDR3 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 24. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

Parameter		Symbol	Min	Max	Unit	Note
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	—	$MVREF_n - 0.150$	V	—
	≤ 1200 MT/s data rate			$MVREF_n - 0.175$		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	$MVREF_n + 0.150$	—	V	—
	≤ 1200 MT/s data rate		$MVREF_n + 0.175$			

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 25. DDR3L SDRAM interface input AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter		Symbol	Min	Max	Unit	Note
AC input low voltage	> 1067 MT/s data rate	V_{ILAC}	—	$MVREF_n - 0.135$	V	—
	≤ 1067 MT/s data rate		—	$MVREF_n - 0.160$		
AC input high voltage	> 1067 MT/s data rate	V_{IHAC}	$MVREF_n + 0.135$	—	V	—
	≤ 1067 MT/s data rate		$MVREF_n + 0.160$	—		

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 26. DDR3 and DDR3L SDRAM interface input AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1
1333 MT/s data rate		–125	125		
1200 MT/s data rate		–147.5	147.5		
1066 MT/s data rate		–170	170		
800 MT/s data rate		–200	200		
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}			ps	2
1333 MT/s data rate		–250	250		

Electrical characteristics

Table 26. DDR3 and DDR3L SDRAM interface input AC timing specifications (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
1200 MT/s data rate	t_{DISKEW}	-275	275	ps	2
1066 MT/s data rate		-300	300		
800 MT/s data rate		-425	425		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

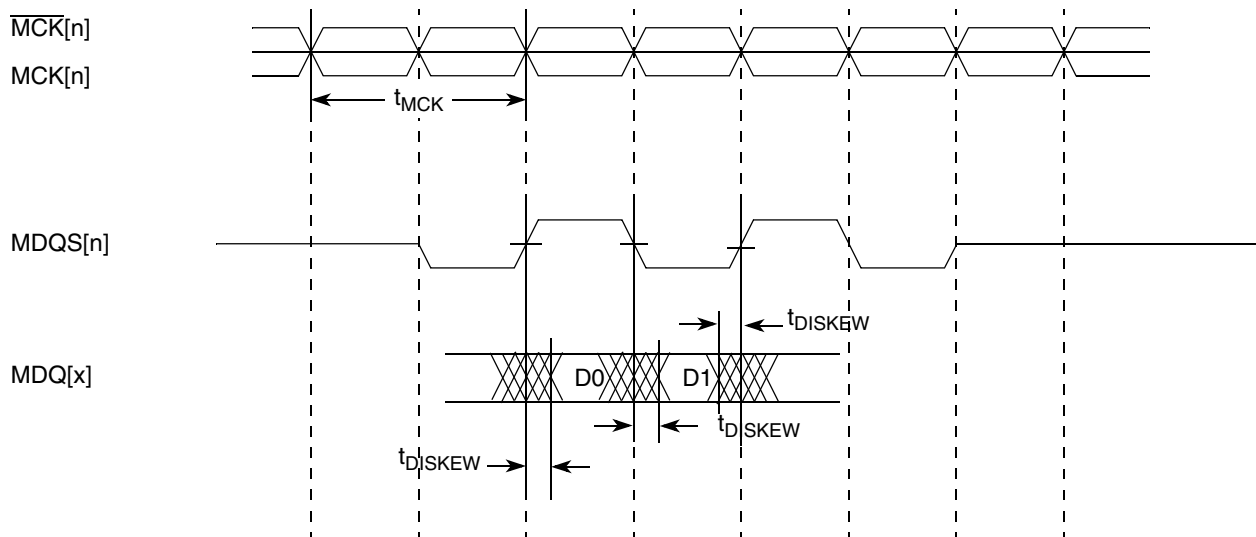


Figure 10. DDR3 and DDR3L SDRAM interface input timing diagram

2.9.2.2 DDR3 and DDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

Table 27. DDR3 and DDR3L SDRAM interface output AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	1.5	2.5	ns	2

Table 27. DDR3 and DDR3L SDRAM interface output AC timing specifications (continued)For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
ADDR/CMD output setup with respect to MCK 1333 MT/s data rate 1200 MT/s data rate 1066 MT/s data rate 800 MT/s data rate	t_{DDKHAS}	0.606 0.675 0.744 0.917	— — — —	ns	3
ADDR/CMD output hold with respect to MCK 1333 MT/s data rate 1200 MT/s data rate 1066 MT/s data rate 800 MT/s data rate	t_{DDKHAX}	0.606 0.675 0.744 0.917	— — — —	ns	3
MCS[n] output setup with respect to MCK 1333 MT/s data rate 1200 MT/s data rate 1066 MT/s data rate 800 MT/s data rate	t_{DDKHCS}	0.606 0.675 0.744 0.917	— — — —	ns	3
MCS[n] output hold with respect to MCK 1333 MT/s data rate 1200 MT/s data rate 1066 MT/s data rate 800 MT/s data rate	t_{DDKHCX}	0.606 0.675 0.744 0.917	— — — —	ns	3
MCK to MDQS Skew ≥ 1066 MT/s data rate 800 MT/s data rate	t_{DDKMHM}	−0.245 −0.375	0.245 0.375	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 1333 MT/s data rate 1200 MT/s data rate 1066 MT/s data rate 800 MT/s data rate	t_{DDKHDS} , t_{DDKLDS}	250 275 300 375	— — — —	ps	5

Table 27. DDR3 and DDR3L SDRAM interface output AC timing specifications (continued)For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX} , t_{DDKLDX}			ps	5
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/MCK and MDQS/MDQS referenced measurements are made from the crossing of the two signals.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the reference manual for your chip for a description and explanation of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
- Note that for data rates of 1200 MT/s or higher, it is required to program the start value of the DQS adjust for write leveling.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 27](#), it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHHM}).

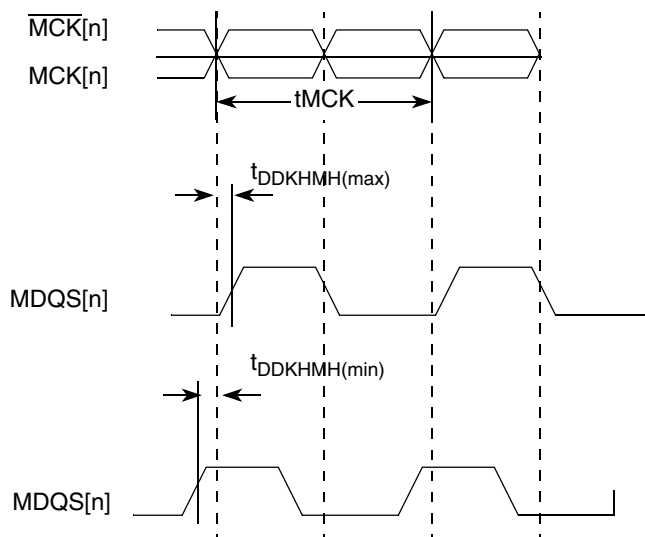


Figure 11. t_{DDKHHM} timing diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

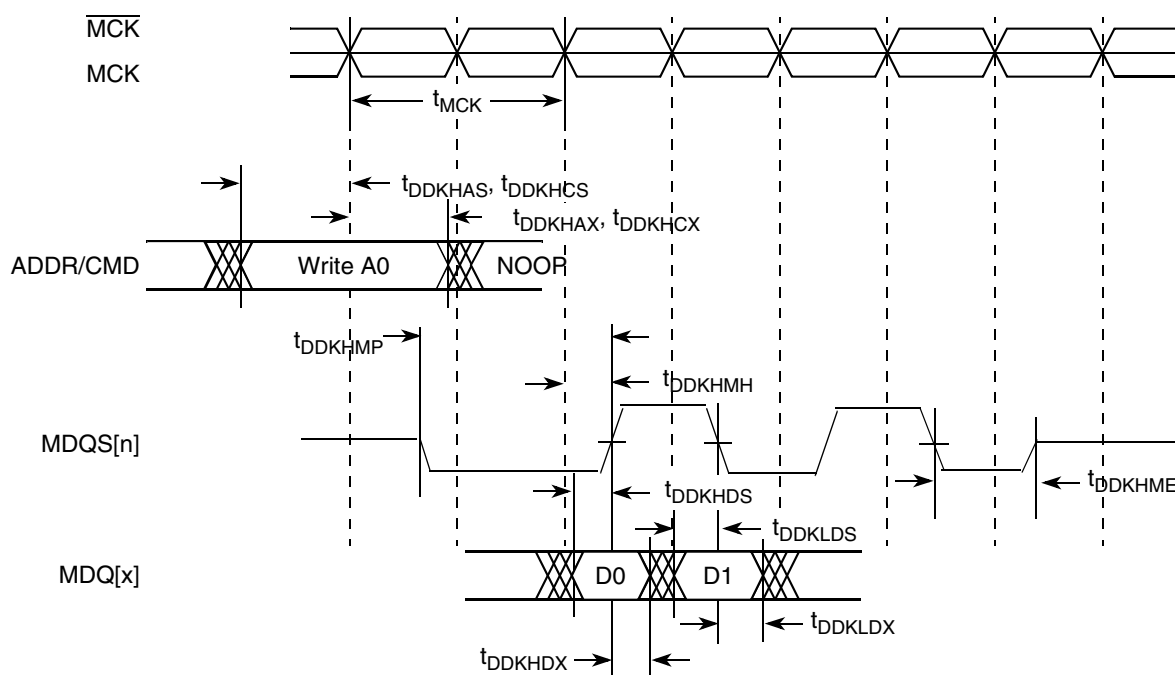


Figure 12. DDR3 and DDR3L output timing diagram

Electrical characteristics

This figure provides the AC test load for the DDR3 and DDR3L controller bus.

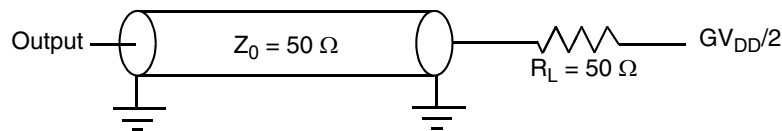


Figure 13. DDR3 and DDR3L controller bus AC test load

2.10 eSPI

This section describes the DC and AC electrical specifications for the eSPI interface.

2.10.1 eSPI DC electrical characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 3.3$ V.

Table 28. eSPI DC electrical characteristics ($CV_{DD} = 3.3$ V)^{1,2}

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($V_{IN} = 0$ V or $V_{IN} = CV_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD} = \text{min}$, $I_{OH} = -2$ mA)	V_{OH}	2.4	—	V	—
Output low voltage ($CV_{DD} = \text{min}$, $I_{OL} = 2$ mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 2.5$ V.

Table 29. eSPI DC electrical characteristics ($CV_{DD} = 2.5$ V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current ($V_{IN} = 0$ V or $V_{IN} = CV_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD} = \text{min}$, $I_{OH} = -1$ mA)	V_{OH}	2.0	—	V	—
Output low voltage ($CV_{DD} = \text{min}$, $I_{OL} = 1$ mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 1.8$ V.

Table 30. eSPI DC electrical characteristics ($CV_{DD} = 1.8$ V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($V_{IN} = 0$ V or $V_{IN} = CV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($CV_{DD} = \text{min}$, $I_{OH} = -0.5$ mA)	V_{OH}	1.35	—	V	—
Output low voltage ($CV_{DD} = \text{min}$, $I_{OL} = 0.5$ mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, "Recommended operating conditions."](#)

2.10.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 31. eSPI AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	$2.36 +$ $(t_{PLATFORM_CLK} * SP$ $MODE[HO_ADJ])$	— —	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	$5.24 +$ $(t_{PLATFORM_CLK} * SP$ $MODE[HO_ADJ])$	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the applicable chip reference manual for details on the SPMODE register.

Electrical characteristics

This figure provides the AC test load for the eSPI.

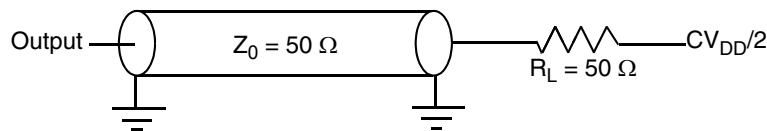


Figure 14. eSPI AC test load

This figure represents the AC timing from Table 31 in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, this figure also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

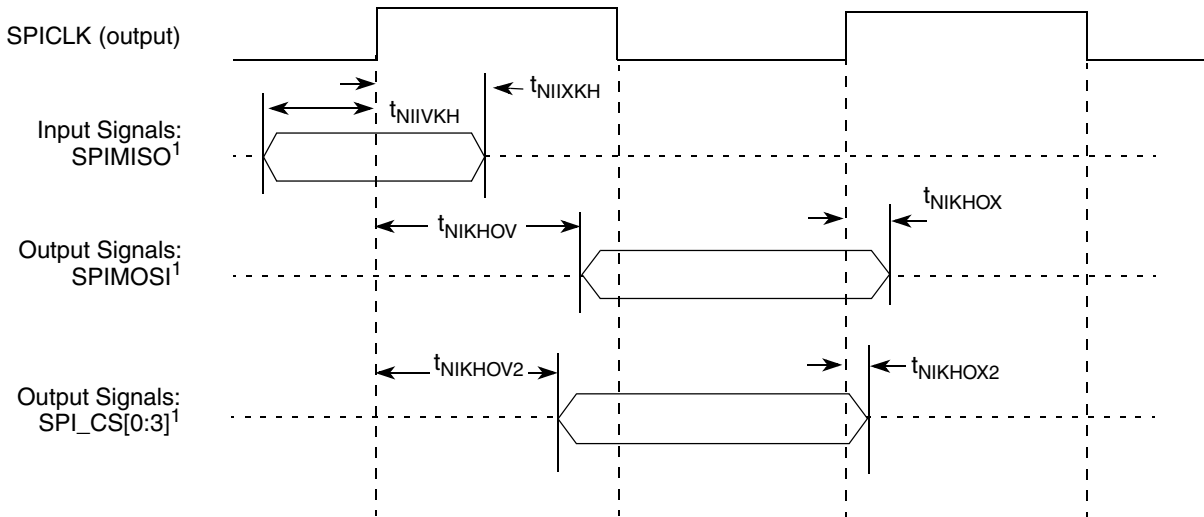


Figure 15. eSPI AC timing in master mode (internal clock) diagram

2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 32. DUART DC electrical characteristics ($OV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

Table 32. DUART DC electrical characteristics ($OV_{DD} = 3.3\text{ V}$) (continued)For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$)	V_{OH}	2.4	—	V	—
Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

1. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 3](#).
2. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

2.11.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 33. DUART AC timing specificationsFor recommended operating conditions, see [Table 3](#).

Parameter	Value	Unit	Note
Minimum baud rate	$f_{PLAT}/(2*1,048,576)$	baud	1
Maximum baud rate	$f_{PLAT}/(2*16)$	baud	1, 2
Oversample rate	16	—	3

Note:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.12 Ethernet: Datapath three-speed Ethernet (dTSEC), management interface, IEEE Std 1588

This section provides the AC and DC electrical characteristics for the datapath three-speed Ethernet controller, the Ethernet management interface, and the IEEE Std 1588 interface.

2.12.1 SGMIi timing specifications

Refer to [Section 2.20.9, “SGMIi interface.”](#)

2.12.2 MII and RGMII timing specifications

This section discusses the electrical characteristics for the MII and RGMII interfaces.

2.12.2.1 MII and RGMII DC electrical characteristics

This table shows the MII DC electrical characteristics when operating at $LV_{DD} = 3.3$ V supply.

Table 34. MII DC electrical characteristics ($LV_{DD} = 3.3$ V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$)	I_{IH}	—	40	μ A	2
Input low current ($V_{IN} = GND$)	I_{IL}	−600	—	μ A	2
Output high voltage ($LV_{DD} = \min$, $I_{OH} = -4.0$ mA)	V_{OH}	2.4	$LV_{DD} + 0.3$	V	—
Output low voltage ($LV_{DD} = \min$, $I_{OL} = 4.0$ mA)	V_{OL}	GND	0.50	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the LV_{IN} symbols referenced in [Table 2](#) and [Table 3](#).

This table shows the MII and RGMII DC electrical characteristics when operating at $LV_{DD} = 2.5$ V supply.

Table 35. MII and RGMII DC electrical characteristics ($LV_{DD} = 2.5$ V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current ($LV_{IN} = 0$ V or $LV_{IN} = LV_{DD}$)	I_{IH}	—	± 40	μ A	2
Output high voltage ($LV_{DD} = \min$, $I_{OH} = -1.0$ mA)	V_{OH}	2.0	—	V	—
Output low voltage ($LV_{DD} = \min$, $I_{OL} = 1.0$ mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the LV_{IN} symbols referenced in [Table 2](#) and [Table 3](#).

2.12.2.2 MII AC timing specifications

This section describes the MII transmit and receive AC timing specifications.

This table provides the MII transmit AC timing specifications.

Table 36. MII transmit AC timing specifications

For recommended operating conditions, see [Table 3](#).

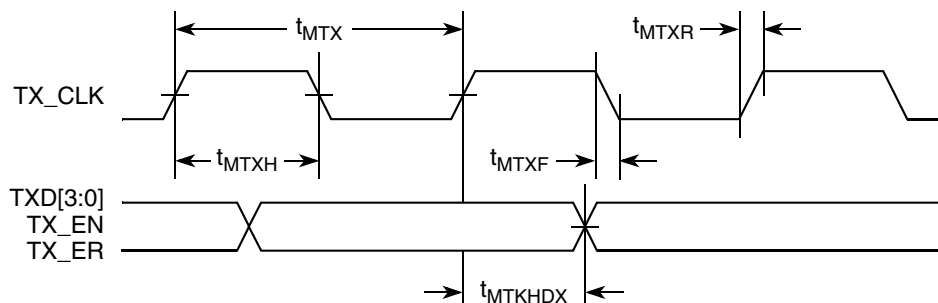
Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns

Table 36. MII transmit AC timing specifications (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

This figure shows the MII transmit AC timing diagram.

**Figure 16. MII transmit AC timing diagram**

This table provides the MII receive AC timing specifications.

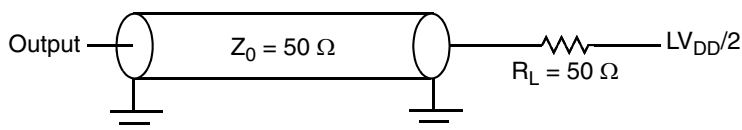
Table 37. MII receive AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note: The frequency of RX_CLK should not exceed frequency of GTX_CLK125 by more than 300ppm.

This figure provides the AC test load for eTSEC.

**Figure 17. eTSEC AC test load**

Electrical characteristics

This figure shows the MII receive AC timing diagram.

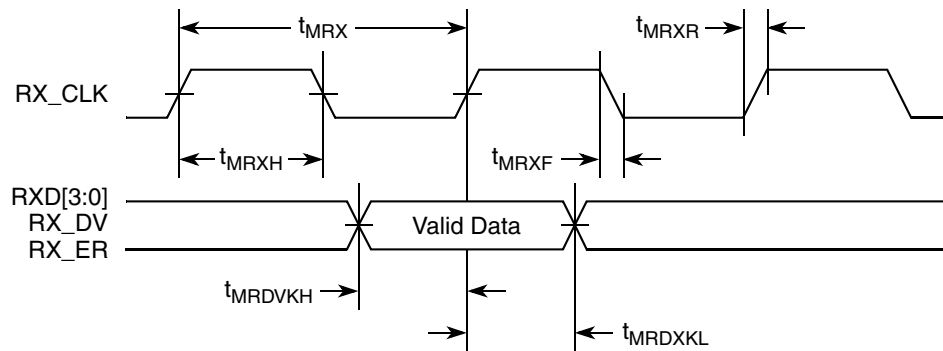


Figure 18. MII receive AC timing diagram

2.12.2.3 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

Table 38. RGMII AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol ¹	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Note:

- In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- The t_{SKRGT_RX} specification implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns $\pm$ 40 ns and 40 ns $\pm$ 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- The frequency of RX_CLK should not exceed frequency of GTX_CLK125 by more than 300ppm.

This figure shows the RGMII AC timing and multiplexing diagrams.

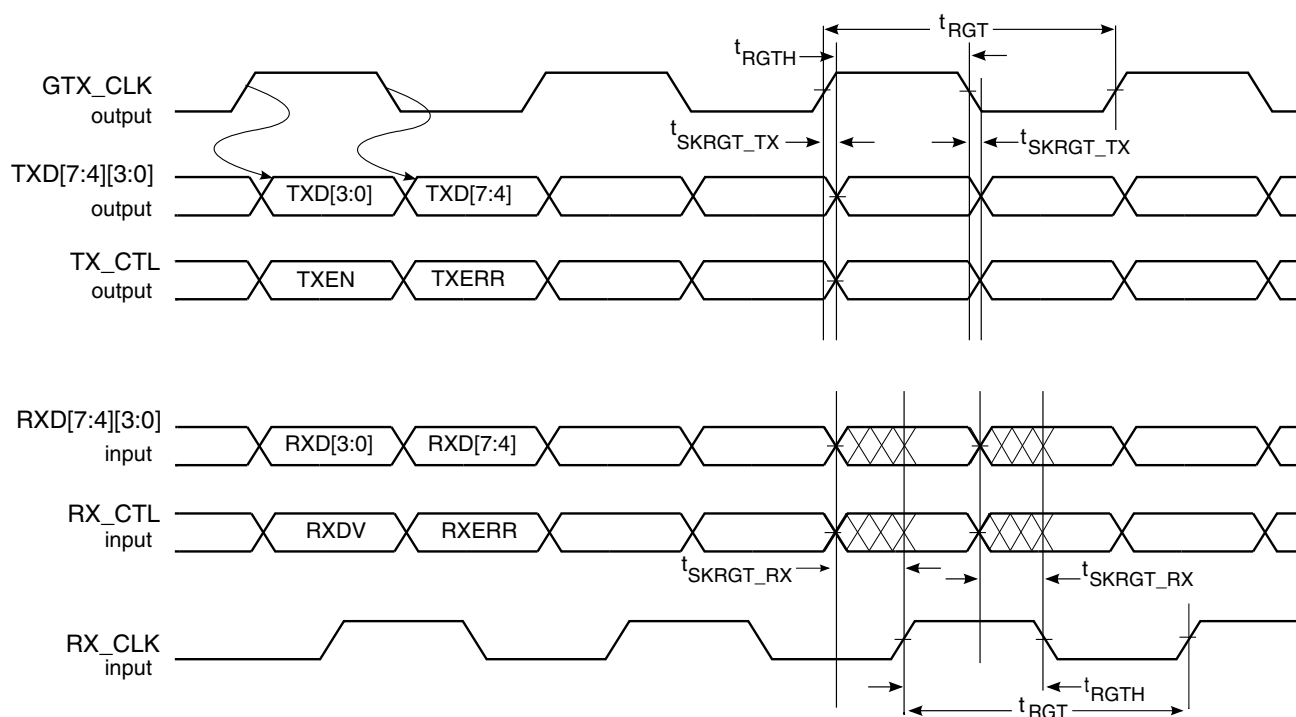


Figure 19. RGMII AC timing and multiplexing diagrams

2.12.3 Ethernet management interface

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces. EMI1 is the PHY management interface controlled by the MDIO controller associated with Frame Manager 1 1GMAC-1. EMI2 is the XAUI PHY management interface controlled by the MDIO controller associated with Frame Manager 1 10GMAC-0.

2.12.3.1 Ethernet management interface 1 DC electrical characteristics

The Ethernet management interface 1 is defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 39. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V _{IH}	2.0	—	V	2
Input low voltage	V _{IL}	—	0.9	V	2
Input high current (LV _{DD} = Max, V _{IN} = 2.1 V)	I _{IH}	—	40	μA	1

Electrical characteristics

Table 39. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input low current (LV _{DD} = Max, V _{IN} = 0.5 V)	I _{IL}	−600	—	μA	1
Output high voltage (LV _{DD} = Min, I _{OH} = −1.0 mA)	V _{OH}	2.4	—	V	—
Output low voltage (LV _{DD} = Min, I _{OL} = 1.0 mA)	V _{OL}	—	0.4	V	—

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Table 2](#) and [Table 3](#).
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in [Table 3](#).

The Ethernet management interface 1 is defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for the Ethernet management interface 1 is provided in [Table 39](#).

Table 40. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V _{IH}	1.7	—	V	1
Input low voltage	V _{IL}	—	0.7	V	1
Input current (LV _{IN} = 0 V or LV _{IN} = LV _{DD})	I _{IH}	—	±40	μA	2
Output high voltage (LV _{DD} = Min, I _{OH} = −1.0 mA)	V _{OH}	2.4	—	V	—
Output low voltage (LV _{DD} = Min, I _{OL} = 1.0 mA)	V _{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

2.12.3.2 Ethernet management interface 2 DC electrical characteristics

Ethernet Management Interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 41. Ethernet management interface 2 DC electrical characteristics (1.2 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V _{IH}	0.84	—	V	—
Input low voltage	V _{IL}	—	0.36	V	—
Output low voltage (I _{OL} = 100 μA)	V _{OL}	—	0.2	V	—
Output low current (V _{OL} = 0.2 V)	I _{OL}	4	—	mA	—
Input capacitance	C _{IN}	—	10	pF	—

2.12.3.3 Ethernet management interface 1 AC timing specifications

This table provides the Ethernet management interface 1 AC timing specifications.

Table 42. Ethernet management interface 1 AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb_clk}) - 6$	—	$(16 \times t_{plb_clk}) + 6$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the frame manager clock frequency. The delay is equal to 16 frame manager clock periods ± 6 ns. For example, with a frame manager clock of 333 MHz, the min/max delay is 48 ns ± 6 ns. Similarly, if the frame manager clock is 400 MHz, the min/max delay is 40 ns ± 6 ns.
4. t_{plb_clk} is the frame manager clock period.

2.12.3.4 Ethernet management interface 2 AC electrical characteristics

Table 43. Ethernet management interface 2 AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter/condition	Symbol ¹	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—

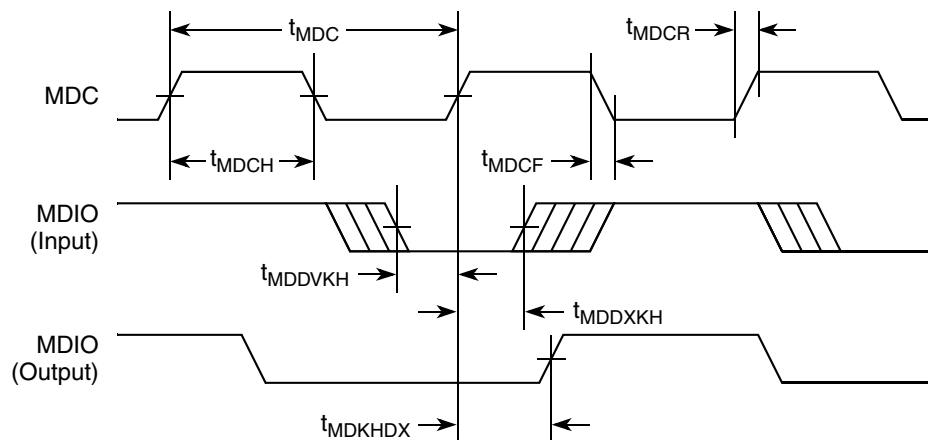
Table 43. Ethernet management interface 2 AC timing specifications (continued)For recommended operating conditions, see [Table 3](#).

Parameter/condition	Symbol ¹	Min	Typ	Max	Unit	Note
MDC to MDIO delay	t_{MDKHDX}	$(0.5 \times (1/f_{MDC})) - 6$	—	$(0.5 \times (1/f_{MDC})) + 6$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the frame manager clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the management data clock frequency, f_{MDC} . The delay is equal to 0.5 management data clock period ± 6 ns. For example, with a management data clock of 2.5 MHz, the min/max delay is 200 ns ± 6 ns.

This figure shows the Ethernet Management Interface timing diagram.

**Figure 20. Ethernet management interface timing diagram****2.12.4 eTSEC IEEE std 1588 AC specifications**

This table provides the IEEE 1588 AC timing specifications.

Table 44. eTSEC IEEE 1588 AC timing specificationsFor recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	$T_{RX_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—

Table 44. eTSEC IEEE 1588 AC timing specifications (continued)

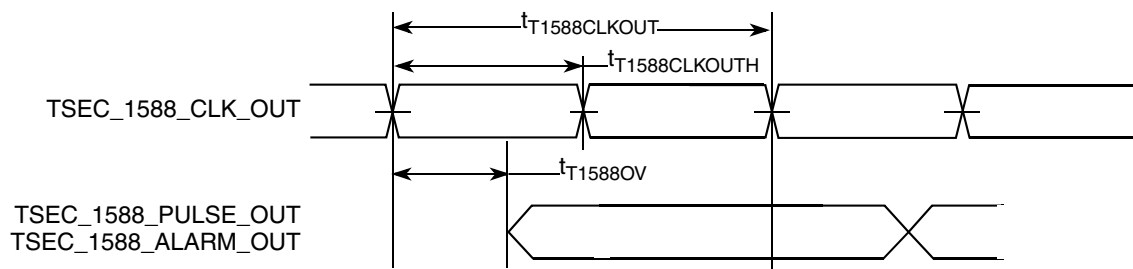
For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT, TSEC_1588_ALARM_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK_MAX}$	—	—	ns	2

Note:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK} , but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ be 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

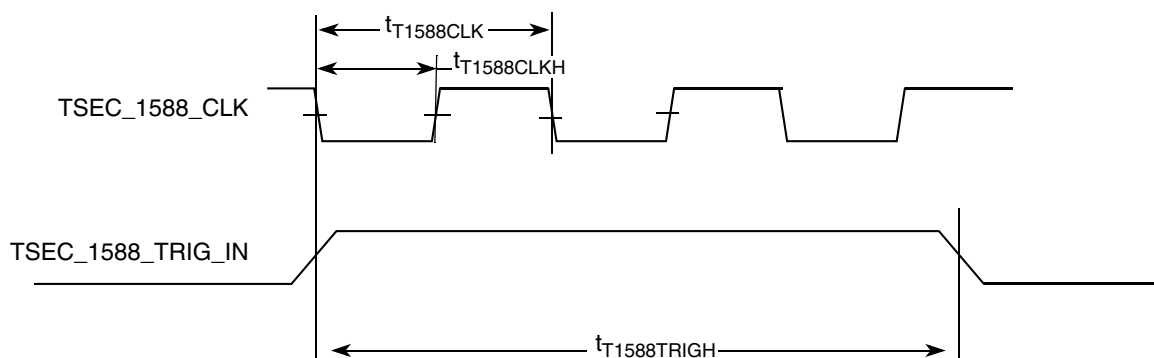
This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 21. eTSEC IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

**Figure 22. eTSEC IEEE 1588 input AC timing**

2.13 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.13.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at $USB_V_{DD_3P3} = 3.3\text{ V}$.

Table 45. USB DC electrical characteristics ($USB_V_{DD_3P3} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage ¹	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($USB_V_{IN_3P3} = 0\text{ V}$ or $USB_V_{IN_3P3} = USB_V_{DD_3P3}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($USB_V_{DD_3P3} = \text{min}$, $I_{OH} = -2\text{ mA}$)	V_{OH}	2.8	—	V	
Output low voltage ($USB_V_{DD_3P3} = \text{min}$, $I_{OL} = 2\text{ mA}$)	V_{OL}	—	0.3	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max $USB_V_{IN_3P3}$ values found in [Table 3](#).
2. The symbol $USB_V_{IN_3P3}$, in this case, represents the $USB_V_{IN_3P3}$ symbol referenced in [Section 2.1.2](#), “Recommended operating conditions.”

2.13.2 USB AC electrical specifications

This table provides the USB clock input ($USBn_CLKIN$) AC timing specifications.

Table 46. $USBn_CLKIN$ AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB_CLK_IN}$	—	24	—	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	-0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second-order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	5	ps

This figure provides the USB AC test load.

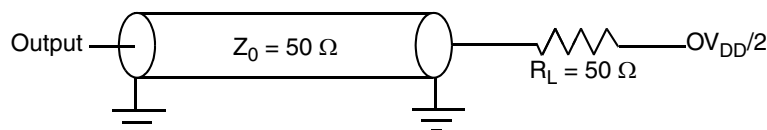


Figure 23. USB AC test load

2.14 Enhanced local bus interface

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.14.1 Enhanced local bus DC electrical characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 3.3\text{ V}$.

Table 47. Enhanced local bus DC electrical characteristics ($BV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = BV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$)	V_{OH}	2.4	—	V	—
Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 2.5\text{ V}$.

Table 48. Enhanced local bus DC electrical characteristics ($BV_{DD} = 2.5\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = BV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -1\text{ mA}$)	V_{OH}	2.0	—	V	—
Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 1\text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 1.8\text{ V}$.

Table 49. Enhanced local bus DC electrical characteristics ($BV_{DD} = 1.8\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1

Electrical characteristics

Table 49. Enhanced local bus DC electrical characteristics ($BV_{DD} = 1.8\text{ V}$) (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = BV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -0.5\text{ mA}$)	V_{OH}	1.35	—	V	—
Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 0.5\text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

2.14.2 Enhanced local bus AC timing specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.14.2.1 Test condition

This figure provides the AC test load for the enhanced local bus.

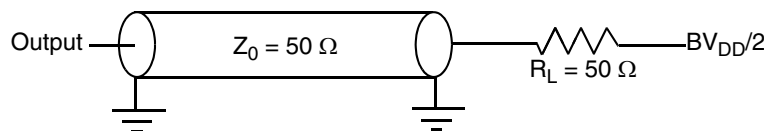


Figure 24. Enhanced local bus AC test load

2.14.2.2 Local bus AC timing specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the timing specifications of the local bus interface.

Table 50. Enhanced local bus timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	10	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—

Table 50. Enhanced local bus timing specifications (continued)For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	–3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	2 platform clock cycles - 1ns (LBCR[AHD] = 1)	—	ns	4
		4 platform clock cycles - 1ns (LBCR[AHD]=0)	—		

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle x LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

This figure shows the AC timing diagram of the local bus interface.

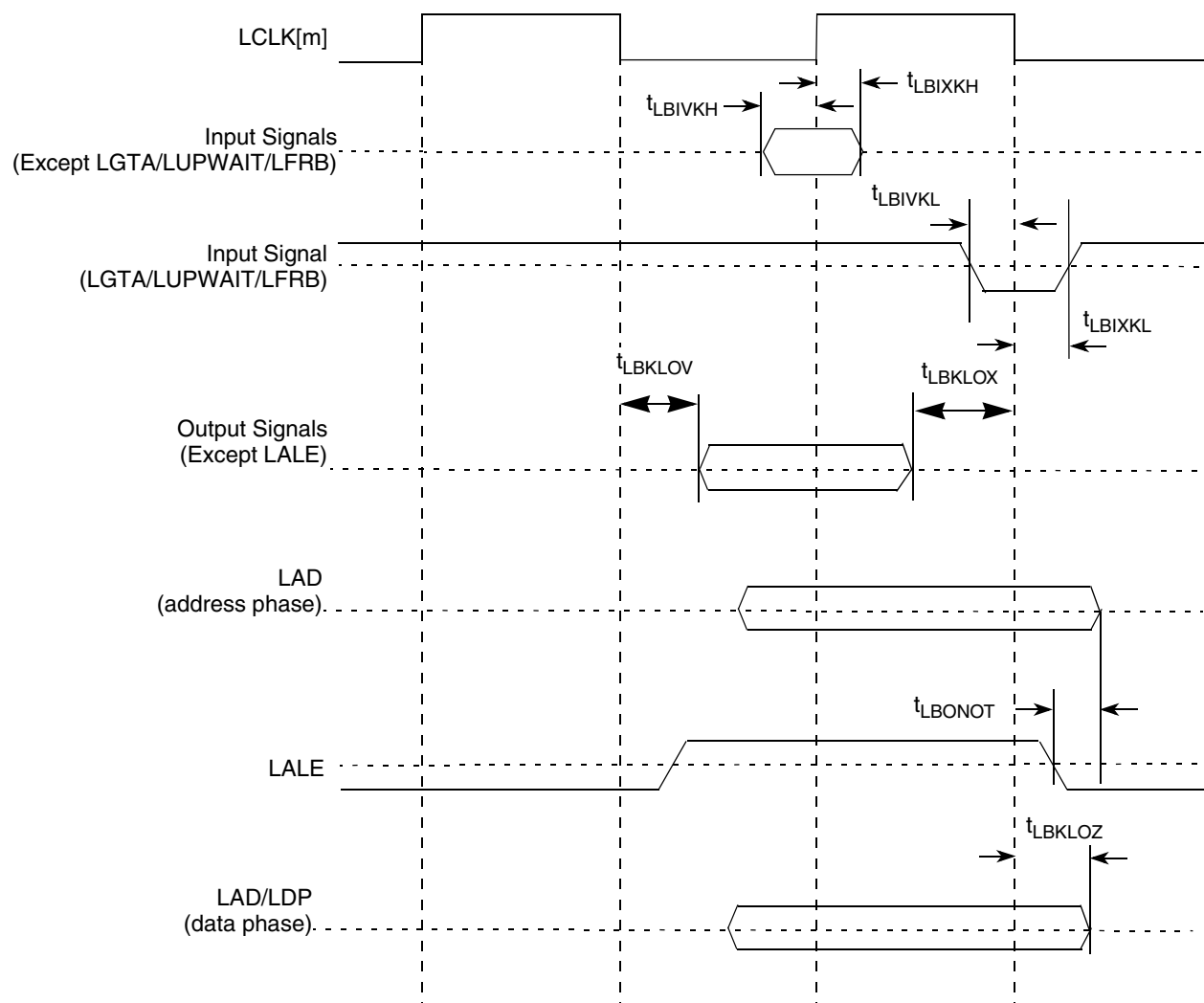


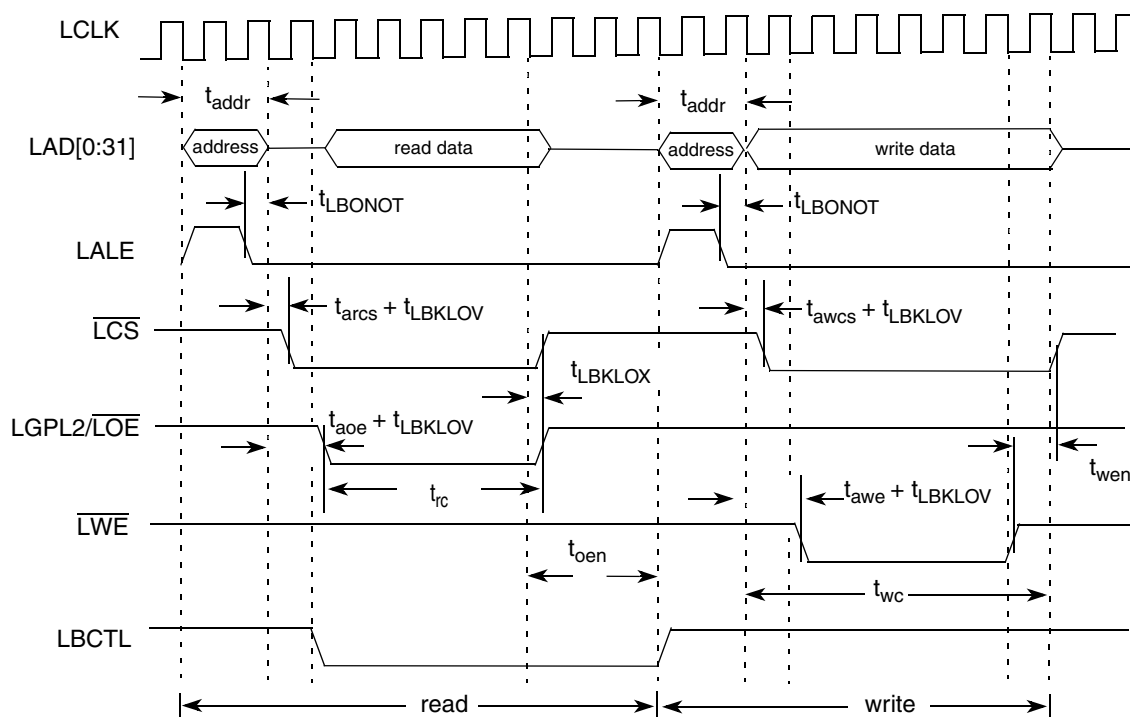
Figure 25. Enhanced local bus signals

Figure 26 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the Local Bus AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, $\frac{1}{4}$, $\frac{1}{2}$, 1, $1 + \frac{1}{4}$, $1 + \frac{1}{2}$, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

This figure shows how the Local Bus AC timing diagram applies to GPCM. The same principle applies to UPM and FCM.



¹ t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].

² t_{arcs} , t_{awcs} , t_{aoe} , t_{rc} , t_{oen} , t_{awe} , t_{wc} , t_{wen} are determined by ORx. See the *P5020 QorIQ Integrated Multicore Communication Processor Family Reference Manual*.

Figure 26. GPCM output timing diagram

2.15 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.15.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 51. eSDHC interface DC electrical characteristics

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	$0.625 \times CV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	—	$0.25 \times CV_{DD}$	V	1
Input/output leakage current	I_{IN}/I_{OZ}	—	–50	50	μA	—
Output high voltage	V_{OH}	$I_{OH} = -100 \mu A$ at $CV_{DD} \text{ min}$	$0.75 \times CV_{DD}$	—	V	—

Electrical characteristics

Table 51. eSDHC interface DC electrical characteristics (continued)

For recommended operating conditions, see [Table 3](#).

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	$I_{OL} = 100\mu A$ at CV_{DD} min	—	$0.125 \times CV_{DD}$	V	—
Output high voltage	V_{OH}	$I_{OH} = -100\mu A$ at CV_{DD} min	$CV_{DD} - 0.2$	—	V	2
Output low voltage	V_{OL}	$I_{OL} = 2\text{ mA}$ at CV_{DD} min	—	0.3	V	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
2. Open drain mode for MMC cards only.

2.15.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in [Figure 27](#) and [Figure 28](#).

Table 52. eSDHC AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
SD_CLK clock frequency: SD Full speed/high speed mode MMC Full speed/high speed mode	f_{SHSCK}	0	25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	$t_{SHSCKR}/$ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	—	ns	3, 4, 5
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 5
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	−3	3	ns	4, 5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})}$ (reference)(state) for inputs and $t_{(\text{first three letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{FHSKH OV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–50 MHz for an SD card and 0–52 MHz for an MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way routing delay between Host and Card on SD_CLK, SD_CMD and SD_DATx should not exceed 1.5 ns.
4. $C_{CARD} \leq 10\text{ pF}$, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40\text{ pF}$
5. The parameter values apply to both full-speed and high-speed modes.

This figure provides the eSDHC clock input timing diagram.

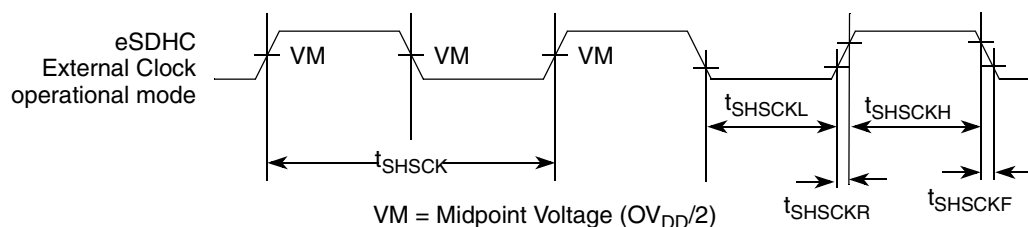


Figure 27. eSDHC clock input timing diagram

This figure provides the data and command input/output timing diagram.

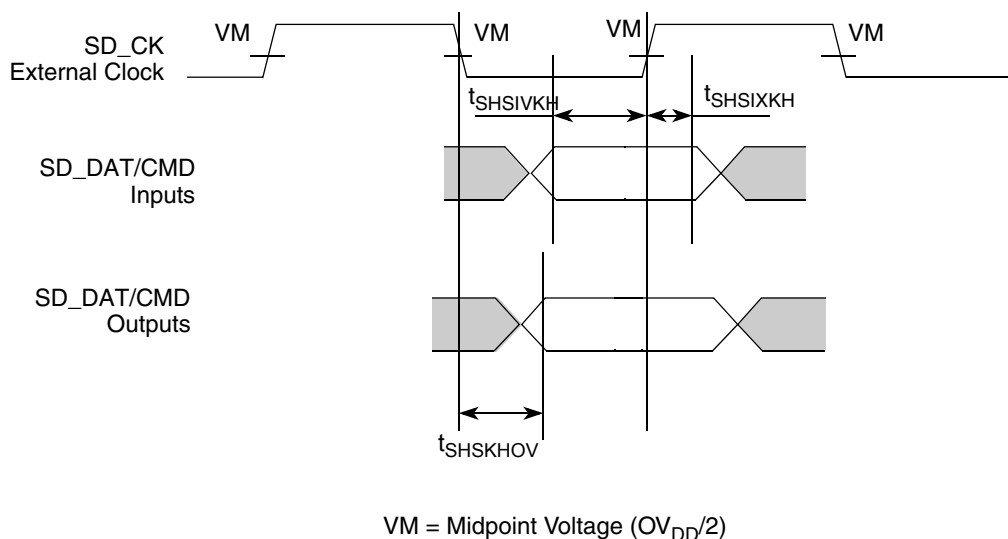


Figure 28. eSDHC data and command input/output timing diagram referenced to clock

2.16 Multicore programmable interrupt controller (MPIC) specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 53. MPIC DC electrical characteristics ($OV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

Electrical characteristics

Table 53. MPIC DC electrical characteristics ($OV_{DD} = 3.3\text{ V}$) (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$)	V_{OH}	2.4	—	V	—
Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in [Table 3](#).
2. The symbol OV_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 3](#).

2.16.2 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

Table 54. MPIC input AC timing specifications

For recommended operating conditions, see [Table 3](#).

Characteristic	Symbol	Min	Max	Unit	Note
MPIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLKs	1

Note:

1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs should be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

2.17 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

2.17.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 55. JTAG DC electrical characteristics ($OV_{DD} = 3.3\text{ V}$)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$)	I_{IN}	—	± 40	μA	2
Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2\text{ mA}$)	V_{OH}	2.4	—	V	—
Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2\text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol found in [Table 3](#).

2.17.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 29 through Figure 32.

Table 56. JTAG AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol ¹	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at ($OV_{DD}/2$)	t_{JKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JGR}/t_{JGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	2
Input setup times					
Boundary-scan USB only	t_{JTDVKH}	14	—	ns	
Boundary-scan except USB		4	—		
TDI, and TMS		4	—		
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times					
Boundary-scan data	t_{JKLDV}	—	15	ns	3
TDO		—	10		
Output hold times	t_{JKLDX}	0	—	ns	3

Note:

1. The symbols used for timing specifications follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{CLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

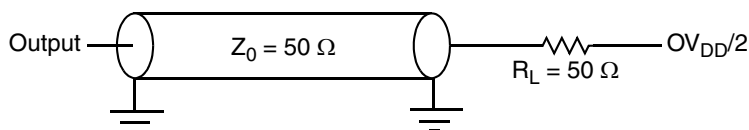


Figure 29. AC test load for the JTAG interface

Electrical characteristics

This figure provides the JTAG clock input timing diagram.

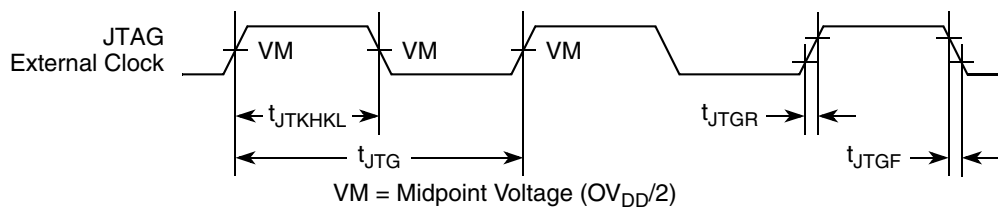


Figure 30. JTAG clock input timing diagram

This figure provides the $\overline{TRST}$ timing diagram.

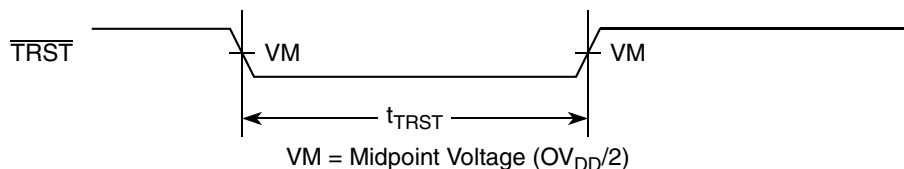


Figure 31. $\overline{TRST}$ timing diagram

This figure provides the boundary-scan timing diagram.

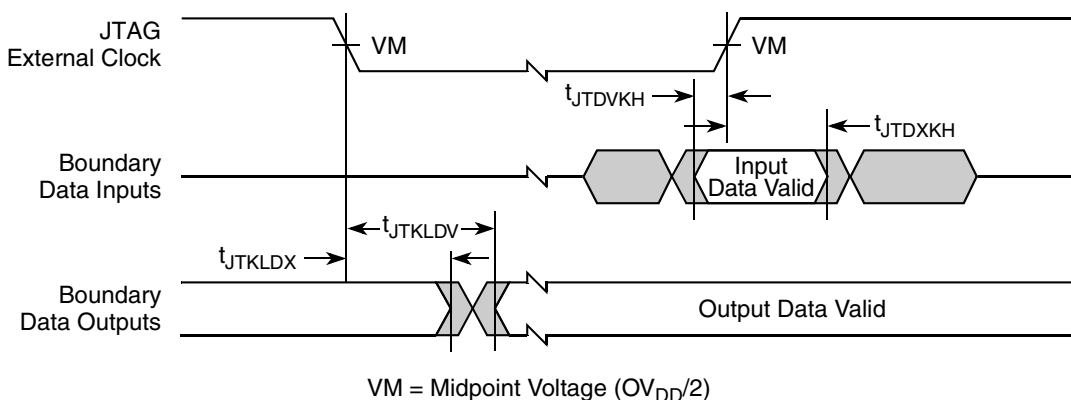


Figure 32. Boundary-scan timing diagram

2.18 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

2.18.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 57. I²C DC electrical characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V _{IH}	2.0	—	V	1
Input low voltage	V _{IL}	—	0.8	V	1
Output low voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV _{DD} and 0.9 × OV _{DD} (max))	I _I	−40	40	μA	4
Capacitance for each I/O pin	C _I	—	10	pF	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the reference manual for your chip for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I²C AC electrical specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 58. I²C AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	—	μs	—
High period of the SCL clock	t _{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXXL}	0.6	—	μs	—
Data setup time	t _{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	— 0	— —	μs	3
Data output delay time	t _{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t _{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μs	—

Electrical characteristics

Table 58. I²C AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol ¹	Min	Max	Unit	Note
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, "Determining the I2C Frequency Divider Ratio for SCL."
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, application note AN2919 referred to in note 2 above is recommended.
4. The maximum t_{I2OVKL} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

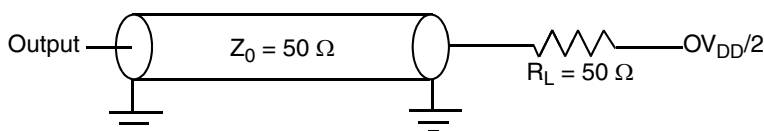


Figure 33. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

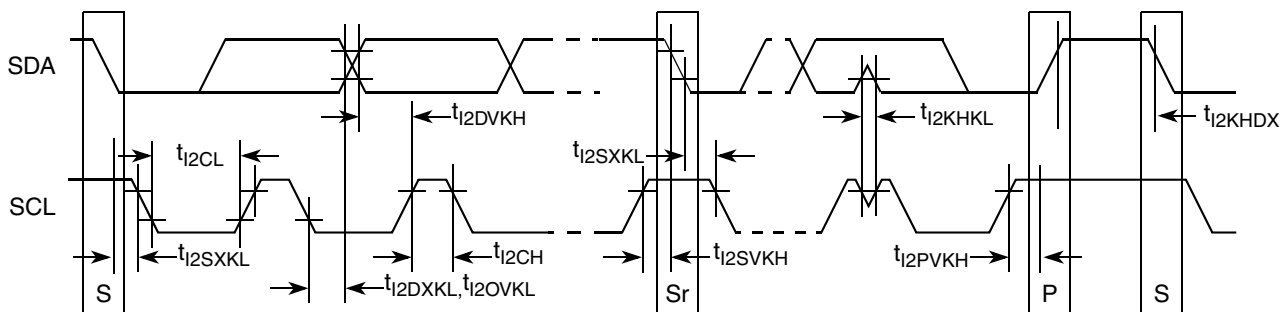


Figure 34. I²C bus AC timing diagram

2.19 GPIO

This section describes the DC and AC electrical characteristics for the GPIO interface.

2.19.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at 3.3 V.

Table 59. GPIO DC electrical characteristics (LV_{DD} or OV_{DD} = 3.3 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V _{IH}	2.0	—	V	1
Input low voltage	V _{IL}	—	0.8	V	1
Input current (OV _{IN} = 0 V or OV _{IN} = OV _{DD})	I _{IN}	—	±40	μA	2
Output high voltage (OV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	2.4	—	V	—
Output low voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the min and max L/OV_{IN} respective values found in [Table 3](#).
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 2.5 V.

Table 60. GPIO DC electrical characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V _{IH}	1.7	—	V	1
Input low voltage	V _{IL}	—	0.7	V	1
Input current (V _{IN} = 0 V or V _{IN} = LV _{DD})	I _{IN}	—	±40	μA	2
Output high voltage (LV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	2.0	—	V	—
Output low voltage (LV _{DD} = min, I _{OH} = 2 mA)	V _{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Section 2.1.2, “Recommended operating conditions.”](#)

2.19.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 61. GPIO input AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1
Trust inputs—minimum pulse width	t_{TIWID}	3	SYSCLK	2

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. Trust inputs are asynchronous to any visible clock. Trust inputs are required to be valid for at least t_{TIWID} to ensure proper operation. For low power trust input pin LP_TMP_DETECT, the voltage is VDD_LP and see [Table 3](#) for the voltage requirement.

This figure provides the AC test load for the GPIO.

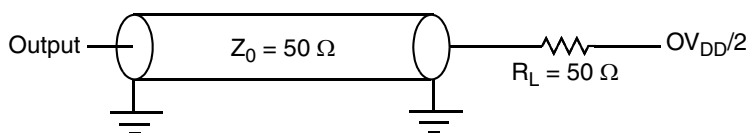


Figure 35. GPIO AC test load

2.20 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, XAUI, Aurora and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.20.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX_n and $\overline{\text{SD_TX}}_n$) or a receiver input (SD_RX_n and $\overline{\text{SD_RX}}_n$). Each signal swings between A volts and B volts where $A > B$.

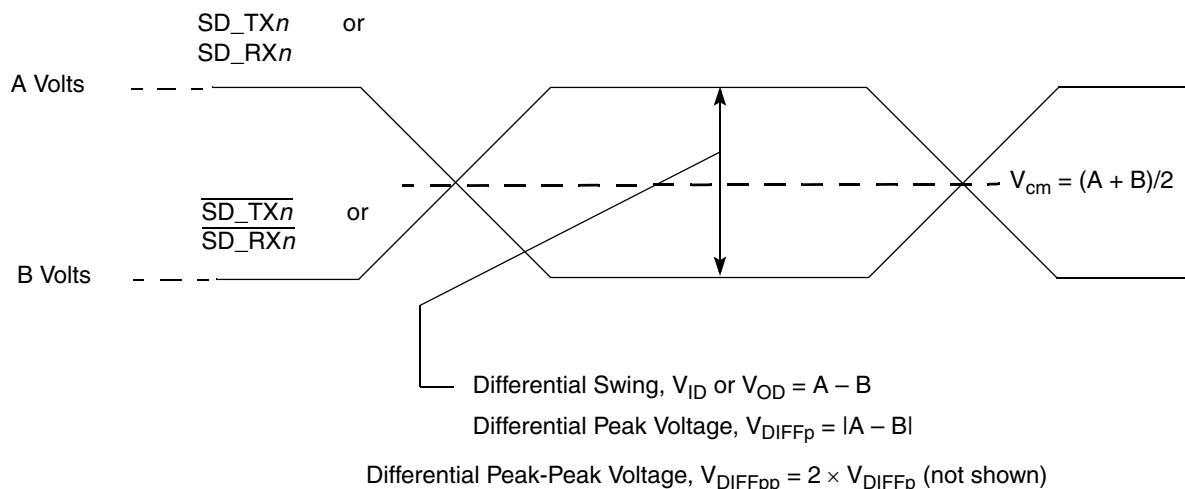


Figure 36. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX_n , $\overline{\text{SD_TX}}_n$, SD_RX_n and $\overline{\text{SD_RX}}_n$ each have a peak-to-peak swing of $A - B$ volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing):

The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{\text{SD_TX}_n} - V_{\overline{\text{SD_TX}}_n}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing):

The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{\text{SD_RX}_n} - V_{\overline{\text{SD_RX}}_n}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |A - B|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{\text{TX-DIFFp-p}} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD_TX}}_n$, for example) from the non-inverting signal (SD_TX_n , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential

waveform is not referenced to ground. See Figure 41, “Differential measurement points for rise and fall time,” as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn} + V_{\overline{SD_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{TD}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD_REF_CLK1}$ for SerDes bank1, SD_REF_CLK2 and $\overline{SD_REF_CLK2}$ for SerDes bank2, and SD_REF_CLK3 and $\overline{SD_REF_CLK3}$ for SerDes bank3.

SerDes banks 1–3 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCL:

- SerDes bank 1: PEX1/2/3/4, sRIO1/2, SGMII (1.25 Gbps only) or Aurora.
- SerDes bank 2: PEX3, SGMII (1.25 or 3.125 GBaud) or XAUI.
- SerDes bank 3: sRIO1, SATA, SGMII (3.125 GBaud) or XAUI.

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

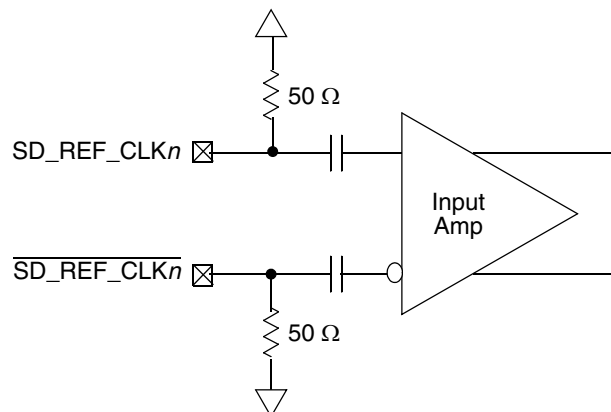


Figure 37. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in [Section 2.1.2](#), “Recommended operating conditions.”
- The SerDes reference clock receiver reference circuit structure is as follows:
 - The SD_REF_CLKn and $\overline{SD_REF_CLKn}$ are internally AC-coupled differential inputs as shown in [Figure 37](#). Each differential clock input (SD_REF_CLKn or $\overline{SD_REF_CLKn}$) has on-chip 50- Ω termination to SGND followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.
 - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ($0.4\text{ V} \div 50 = 8\text{ mA}$) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SD_REF_CLKn and $\overline{SD_REF_CLKn}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For an external DC-coupled connection, as described in [Section 2.20.2.1](#), “SerDes reference clock receiver characteristics,” the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. [Figure 38](#) shows the SerDes reference clock input requirement for DC-coupled connection scheme.

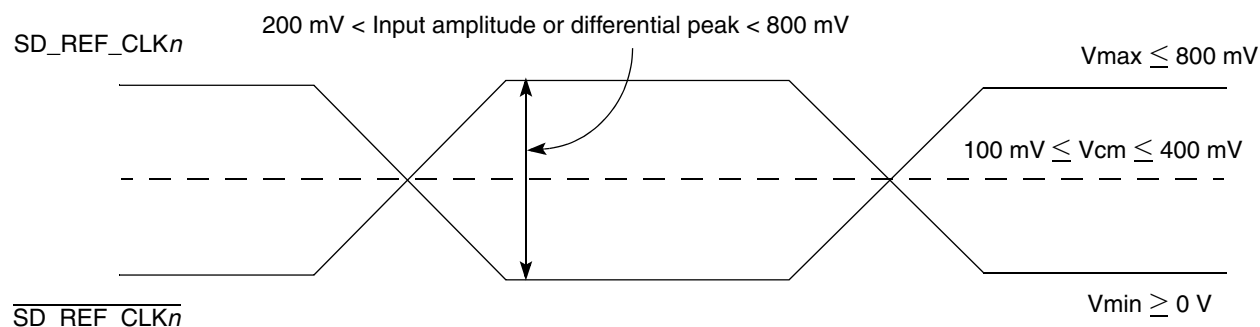


Figure 38. Differential reference clock input DC requirements (external DC-coupled)

Electrical characteristics

- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). Figure 39 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

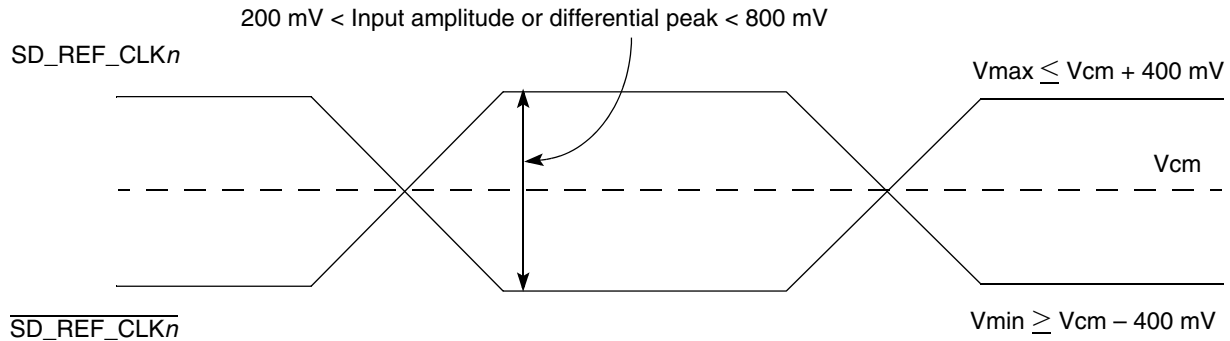


Figure 39. Differential reference clock input DC requirements (external AC-coupled)

- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLKn input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD_REF_CLKn}}$ either left unconnected or tied to ground.
 - The SD_REF_CLKn input average voltage must be between 200 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD_REF_CLKn}}$) through the same source impedance as the clock input (SD_REF_CLKn) in use.

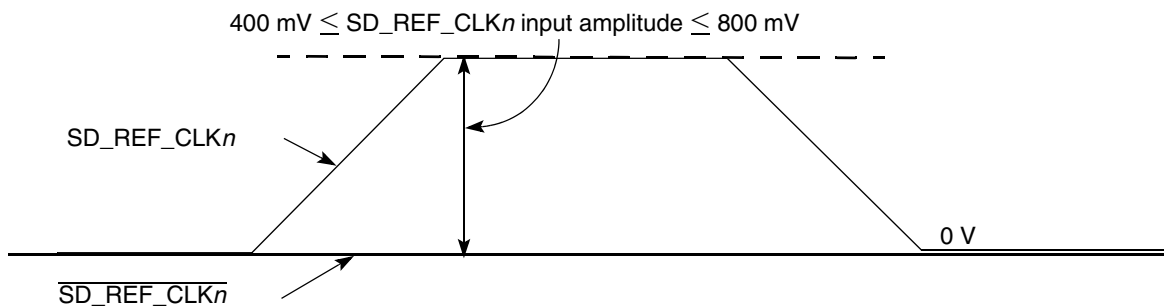


Figure 40. Single-ended reference clock input DC requirements

2.20.2.3 AC requirements for SerDes reference clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 62. SD_REF_CLK $\bar{n}$ and SD_REF_CLK n input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/SD_REF_CLK frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/SD_REF_CLK clock frequency tolerance	t_{CLK_TOL}	-350	—	350	ppm	—
SD_REF_CLK/SD_REF_CLK reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/SD_REF_CLK max deterministic peak-peak jitter at 10 ⁻⁶ BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/SD_REF_CLK total reference clock jitter at 10 ⁻⁶ BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/SD_REF_CLK rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	-200	mV	4
Rising edge rate (SD_REF_CLK $\bar{n}$) to falling edge rate (SD_REF_CLK n) matching	Rise-Fall Matching	—	—	20	%	5, 6

Note:

1. **Caution:** Only 100 and 125 have been tested. In-between values not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK $\bar{n}$ minus SD_REF_CLK n). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See [Figure 41](#).
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK $\bar{n}$ and falling edge rate for SD_REF_CLK n . It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK $\bar{n}$ rising meets SD_REF_CLK n falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK $\bar{n}$ should be compared to the fall edge rate of SD_REF_CLK n , the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 42](#).

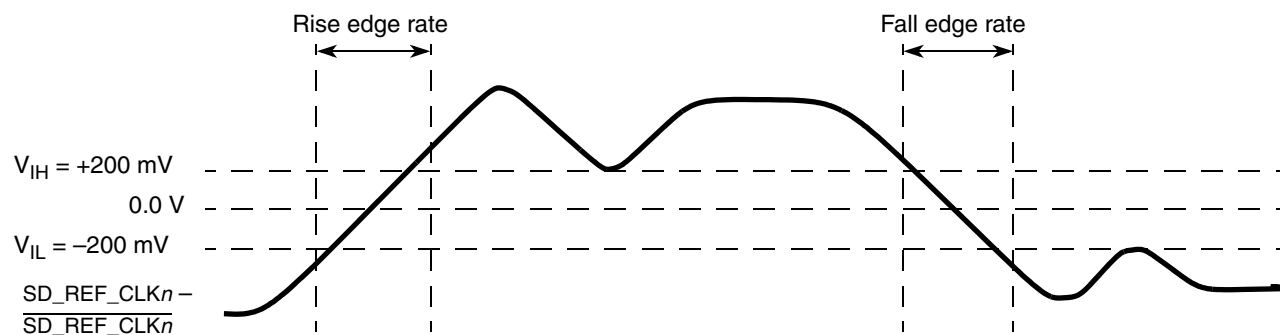


Figure 41. Differential measurement points for rise and fall time

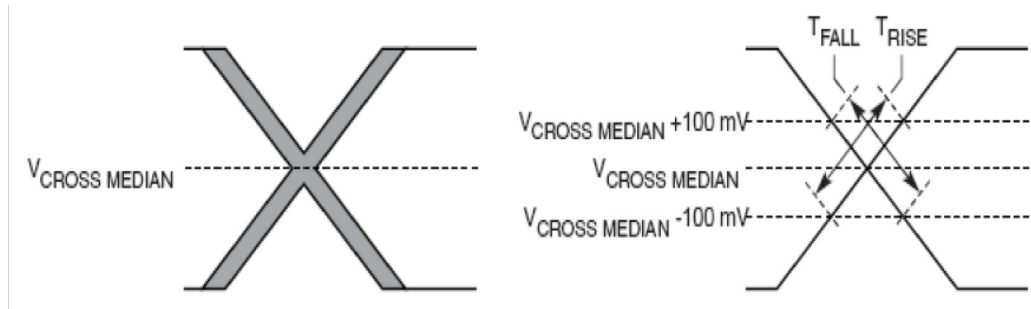


Figure 42. Single-ended measurement points for rise and fall time matching

2.20.2.4 Spread spectrum clock

SD_REF_CLK1/SD_REF_CLK1 were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD_REF_CLK2/SD_REF_CLK2 were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and the industry protocol specifications supports it. For better results, a source without significant unintended modulation should be used.

SD_REF_CLK3/SD_REF_CLK3 are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

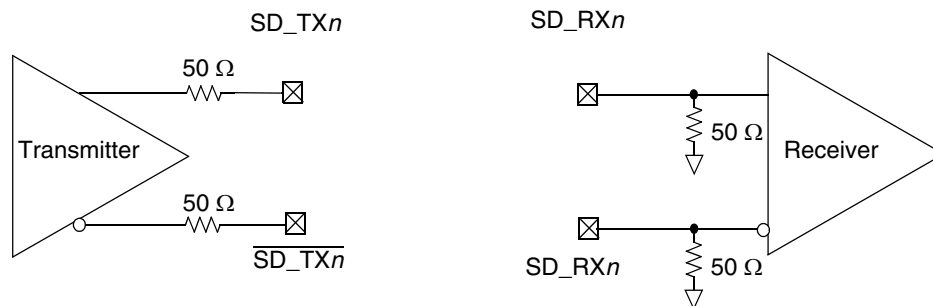


Figure 43. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- [Section 2.20.4, “PCI Express”](#)
- [Section 2.20.5, “Serial RapidIO \(sRIO\)”](#)
- [Section 2.20.6, “XAUI”](#)
- [Section 2.20.7, “Aurora”](#)
- [Section 2.20.8, “Serial ATA \(SATA\)”](#)
- [Section 2.20.9, “SGMII interface”](#)

Note that external AC-coupling capacitor is required for the above serial transmission protocols per the protocol's standard requirements.

2.20.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.20.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

2.20.4.2 PCI Express clocking requirements for SD_REF_CLK n and SD_REF_CLK n

SerDes banks 1–2 (SD_REF_CLK[1:2] and $\overline{\text{SD_REF_CLK[1:2]}}$) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes bank 3.

For more information on these specifications, see [Section 2.20.2](#), “SerDes reference clocks.”

2.20.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 63. PCI Express 2.0 (2.5 GT/s) differential transmitter (Tx) output DC specifications
($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{\text{TX-DIFFp-p}}$	800	—	1200	mV	$V_{\text{TX-DIFFp-p}} = 2 \times V_{\text{TX-D+}} - V_{\text{TX-D-}} $ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{\text{TX-DE-RATIO}}$	3.0	3.5	4.0	dB	Ratio of the $V_{\text{TX-DIFFp-p}}$ of the second and following bits after a transition divided by the $V_{\text{TX-DIFFp-p}}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{\text{TX-DIFF-DC}}$	80	100	120	Ω	Tx DC differential mode low Impedance
Transmitter DC impedance	$Z_{\text{TX-DC}}$	40	50	60	Ω	Required Tx D+ as well as D– DC Impedance during all states

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

Electrical characteristics

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 64. PCI Express 2.0 (5 GT/s) differential transmitter (Tx) output DC specifications
($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	—	1200	mV	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $ See Note 1.
Low Power differential peak-to-peak output voltage	$V_{TX-DIFFp-p_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1.
DC differential Tx impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Tx DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required Tx D+ as well as D– DC impedance during all states

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.4.4 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (2.5 GT/s) differential receiver (Rx) input DC specifications ($SV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	mV	$V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC differential mode impedance. See Note 2

Table 65. PCI Express 2.0 (2.5 GT/s) differential receiver (Rx) input DC specifications (SV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance ($50 \pm 20\%$ tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50 k	—	—	Ω	Required Rx D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver

Note:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 66. PCI Express 2.0 (5 GT/s) differential receiver (Rx) input DC specifications (SV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	V	$V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Rx DC Differential mode impedance. See Note 2

Electrical characteristics

Table 66. PCI Express 2.0 (5 GT/s) differential receiver (Rx) input DC specifications (SV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required Rx D+ as well as D– DC Impedance ($50 \pm 20\%$ tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	k Ω	Required Rx D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver

Note:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.

2.20.4.5 PCI Express AC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.5.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications 2.5 GT/s, and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 67. PCI Express 2.0 (2.5 GT/s) differential transmitter (Tx) output AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread spectrum or RefCLK jitter. Includes device random jitter at 10^{-12} . See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFP-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2 and 3.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in [Figure 44](#) and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

Electrical characteristics

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 68. PCI Express 2.0 (5 GT/s) differential transmitter (Tx) output AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in [Figure 44](#) and measured over any 250 consecutive Tx UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.20.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 69. PCI Express 2.0 (2.5 GT/s) differential receiver (Rx) input AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. See Notes 2, 3 and 4.

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 44](#) should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Electrical characteristics

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 70. PCI Express 2.0 (5 GT/s) differential receiver (Rx) input AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max Rx inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common RefClk Rx architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max Rx inherent total timing error
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture
Max Rx inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common RefClk Rx architecture

Note:

1. No test load is necessarily associated with this value.

2.20.4.6 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in [Figure 44](#).

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

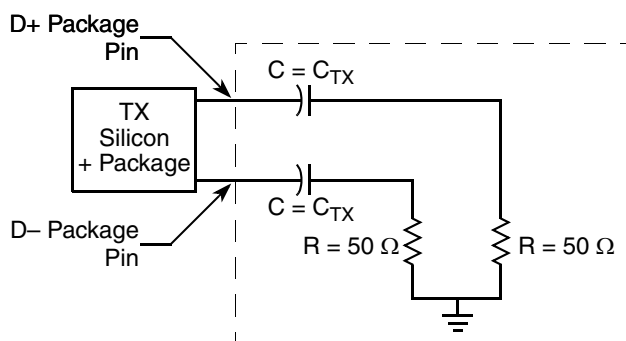


Figure 44. Test/Measurement Load

2.20.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125 and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.20.5.1 Signal definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. Figure 45 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where $A > B$. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ —each have a peak-to-peak swing of $A - B$ volts.
- The differential output signal of the transmitter, V_{OD} , is defined as $V_{\text{TD}} - V_{\overline{\text{TD}}}$
- The differential input signal of the receiver, V_{ID} , is defined as $V_{\text{RD}} - V_{\overline{\text{RD}}}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts.
- The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$ volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B)$ volts.

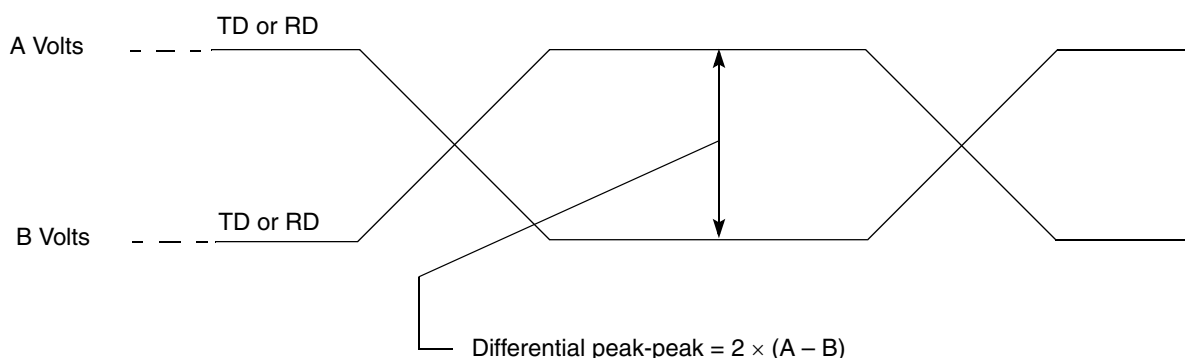


Figure 45. Differential peak-peak voltage of transmitter or receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.20.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.20.5.3 Serial RapidIO clocking requirements for SD_REF_CLK_n and SD_REF_CLK_n

SerDes bank 1 and bank 3 (SD_REF_CLK1 and SD_REF_CLK1) may be used for various SerDes serial RapidIO configurations based on the RCW Configuration field SRDS_PRTCL. The serial RapidIO interface is not supported on SerDes banks 2.

For more information on these specifications, see [Section 2.20.2, “SerDes reference clocks.”](#)

2.20.5.4 DC requirements for serial RapidIO

This section explains the DC requirements for the serial RapidIO interface.

2.20.5.4.1 DC serial RapidIO timing transmitter specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case is better than the following:

- -10 dB for $(\text{Baud Frequency}) \div 10 < \text{Freq}(f) < 625 \text{ MHz}$
- $-10 \text{ dB} + 10\log(f \div 625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \leq \text{Freq}(f) \leq \text{Baud Frequency}$

The reference impedance for the differential return loss measurements is 100-Ω resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 20 ps at 2.50 GBaud and 15 ps at 3.125 GBaud.

This table defines the transmitter DC specifications for the serial RapidIO interface operating at $XV_{DD} = 1.5 \text{ V}$ or 1.8 V .

Table 71. sRIO transmitter DC timing specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Voltage,	V_O	−0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—

Note:

1. Voltage relative to COMMON of either signal comprising a differential pair.

2.20.5.4.2 DC serial RapidIO receiver specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $(0.8) \times (\text{Baud Frequency})$. This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100- Ω resistive for differential return loss and 25- Ω resistive for common mode.

This table defines the receiver DC specifications for the serial RapidIO interface operating at $\text{SV}_{\text{DD}} = 1.5 \text{ V}$ or 1.8 V .

Table 72. sRIO receiver DC timing specifications—2.5 GBaud, 3.125 GBaud, 5 GBaud

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1

Note:

1. Measured at the receiver.

2.20.5.5 AC requirements for serial RapidIO

This section explains the AC requirements for the serial RapidIO interface.

2.20.5.5.1 AC requirements for serial RapidIO transmitter

This table defines the transmitter AC specifications for the serial RapidIO interface. The AC timing specifications do not include RefClk jitter.

Table 73. sRIO transmitter AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_{D}	—	—	0.17	UI p-p
Total jitter	J_{T}	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100ppm	200	200 + 100ppm	ps

This table defines the receiver AC specifications for the serial RapidIO interface. The AC timing specifications do not include RefClk jitter.

Table 74. sRIO receiver AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_{D}	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance ²	J_{T}	0.65	—	—	UI p-p	1
Bit error rate	BER	—	—	10^{-12}	—	—

Electrical characteristics

Table 74. sRIO receiver AC timing specifications (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100ppm	200	200 + 100ppm	ps	—

Note:

1. Measured at receiver.
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 46](#). The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

This figure shows the single-frequency sinusoidal jitter limits.

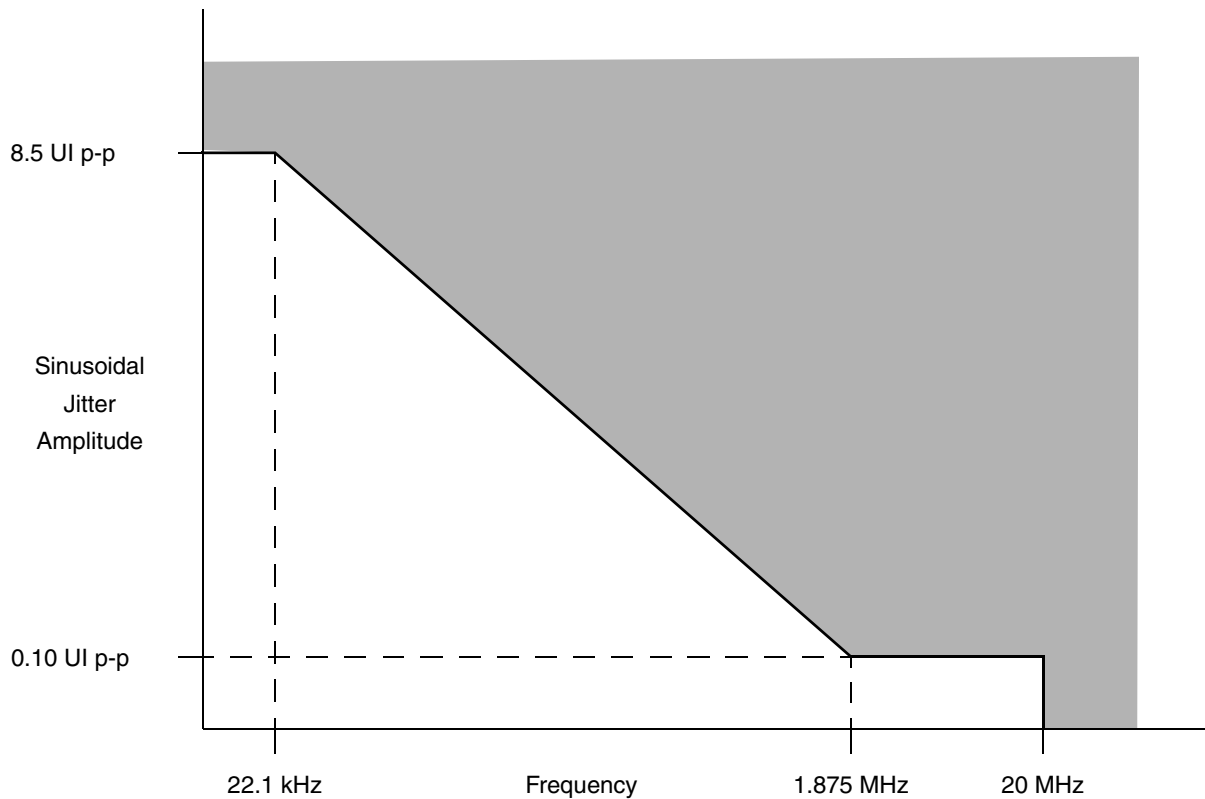


Figure 46. Single-frequency sinusoidal jitter limits

2.20.6 XAUI

This section describes the DC and AC electrical specifications for the XAUI bus.

2.20.6.1 XAUI DC electrical characteristics

This section discusses the XAUI DC electrical characteristics for the clocking signals, transmitter, and receiver.

2.20.6.1.1 DC requirements for XAUI SD_REF_CLK n and $\overline{\text{SD_REF_CLK}}_n$

Only SerDes banks 2–3 (SD_REF_CLK[2:3] and $\overline{\text{SD_REF_CLK}}[2:3]$) may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

For more information on these specifications, see [Section 2.20.2.2, “DC level requirement for SerDes reference clocks.”](#)

2.20.6.1.2 XAUI transmitter DC electrical characteristics

This table defines the XAUI transmitter DC electrical characteristics.

Table 75. XAUI transmitter DC electrical characteristics ($\text{XV}_{\text{DD}} = 1.5 \text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Output voltage	V_{O}	−0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—

Note:

1. Absolute output voltage limit

2.20.6.1.3 XAUI receiver DC electrical characteristics

This table defines the XAUI receiver DC electrical characteristics.

Table 76. XAUI receiver DC timing specifications ($\text{SV}_{\text{DD}} = 1.5 \text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:

1. Measured at the receiver.

2.20.6.2 XAUI AC timing specifications

This section discusses the XAUI AC timing specifications for the clocking signals, transmitter, and receiver.

2.20.6.2.1 AC requirements for XAUI SD_REF_CLK n and $\overline{\text{SD_REF_CLK}}_n$

This table specifies AC requirements for SD_REF_CLK n and $\overline{\text{SD_REF_CLK}}_n$, where $n = [2:3]$. Only SerDes banks 2–3 may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

Table 77. XAUI AC SD_REF_CLK n and $\overline{\text{SD_REF_CLK}}_n$ input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ frequency range	$t_{\text{CLK_REF}}$	—	125/ 156.25	—	MHz	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ clock frequency tolerance	$t_{\text{CLK_TOL}}$	–100	—	100	ppm	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ reference clock duty cycle (measured at 1.6 V)	$t_{\text{CLK_DUTY}}$	40	50	60	%	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ cycle to cycle jitter (period jitter at refClk input)	$t_{\text{CLK_CJ}}$	—	—	100	ps	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ total reference clock jitter (peak-to-peak phase jitter at refClk input)	$t_{\text{CLK_PJ}}$	–50	—	50	ps	—
SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ rising/falling edge rate	$t_{\text{CLKRR}}/t_{\text{CLKFR}}$	1	—	4	V/ns	1
Differential input high voltage	V_{IH}	200	—	—	mV	2
Differential input low voltage	V_{IL}	—	—	–200	mV	2
Rising edge rate (SD_REF_CLK n) to falling edge rate ($\overline{\text{SD_REF_CLK}}_n$) matching	Rise-Fall Matching	—	—	20	%	3, 4

Note:

1. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK n minus $\overline{\text{SD_REF_CLK}}_n$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See [Figure 41](#).
2. Measurement taken from differential waveform
3. Measurement taken from single-ended waveform
4. Matching applies to rising edge for SD_REF_CLK n and falling edge rate for $\overline{\text{SD_REF_CLK}}_n$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK n rising meets $\overline{\text{SD_REF_CLK}}_n$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK n should be compared to the fall edge rate of $\overline{\text{SD_REF_CLK}}_n$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 42](#).

2.20.6.2.2 XAUI transmitter AC timing specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 78. XAUI transmitter AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter	J_{D}	—	—	0.17	UI p-p	—
Total jitter	J_{T}	—	—	0.35	UI p-p	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

2.20.6.2.3 XAUI receiver AC timing specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

Table 79. XAUI receiver AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 46](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

2.20.7 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.7.1 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.7.1.1 Aurora DC clocking requirements for $\overline{SD_REF_CLKn}$ and $\overline{SD_REF_CLKn}$

Only SerDes bank 1 ($\overline{SD_REF_CLK1}$ and $\overline{SD_REF_CLK1}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2-3.

For more information on these specifications, see [Section 2.20.2](#), “SerDes reference clocks.”

2.20.7.1.2 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 80. Aurora transmitter DC electrical characteristics ($V_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p

2.20.7.1.3 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for Aurora.

Table 81. Aurora receiver DC electrical characteristics (SV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V _{IN}	120	900	1200	mV p-p	1

Note:

1. Measured at receiver

2.20.7.2 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

2.20.7.2.1 Aurora AC clocking requirements for SD_REF_CLK_n and $\overline{\text{SD_REF_CLK}}_n$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD_REF_CLK}}_1$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2–3.

Note that the XAUI clock requirements for SD_REF_CLK_n and $\overline{\text{SD_REF_CLK}}_n$ are intended to be used within the clocking guidelines specified by either [Section 2.20.2.3, “AC requirements for SerDes reference clocks](#) or [Section 2.20.8.2.1, “AC requirements for SATA REF_CLK.”](#)

2.20.7.2.2 Aurora transmitter AC timing specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 82. Aurora transmitter AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J _D	—	—	0.17	UI p-p
Total jitter	J _T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.20.7.2.3 Aurora receiver AC timing specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 83. Aurora receiver AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	—

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 46](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

2.20.8 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

2.20.8.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

2.20.8.1.1 SATA DC transmitter output characteristics

This table provides the DC differential transmitter output DC characteristics for the transmission.

Table 84. Gen1i/1.5G transmitter (Tx) DC specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	—	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	2

Note:

1. Terminated by $50\ \Omega$ load.
2. DC impedance

Electrical characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 85. Gen 2i/3G transmitter (Tx) DC specifications ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Tx diff output voltage	$V_{\text{SATA_TXDIFF}}$	400	—	700	mV p-p	1
Tx differential pair impedance	$Z_{\text{SATA_TXDIFFIM}}$	85	100	115	Ω	—

Note:

1. Terminated by $50\ \Omega$ load.

2.20.8.1.2 SATA DC receiver (Rx) input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 86. Gen1i/1.5 G receiver (Rx) input DC specifications ($SV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	$V_{\text{SATA_RXDIFF}}$	240	—	600	mV p-p	1
Differential Rx input impedance	$Z_{\text{SATA_RXSEIM}}$	85	100	115	Ω	2
OOB signal detection threshold	$V_{\text{SATA_OOB}}$	50	120	240	mV p-p	2

Note:

1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 87. Gen2i/3 G receiver (Rx) input DC specifications ($SV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	$V_{\text{SATA_RXDIFF}}$	275	—	750	mV p-p	1
Differential Rx input impedance	$Z_{\text{SATA_RXSEIM}}$	85	100	115	Ω	2
OOB signal detection threshold	$V_{\text{SATA_OOB}}$	75	120	240	mV p-p	2

Note:

1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.20.8.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

2.20.8.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

Table 88. SATA reference clock input requirements

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
SD_REF_CLK/SD_REF_CLK frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/SD_REF_CLK clock frequency tolerance	t_{CLK_TOL}	−350	—	+350	ppm	—
SD_REF_CLK/SD_REF_CLK reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/SD_REF_CLK cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD_REF_CLK/SD_REF_CLK total reference clock jitter, phase jitter (peak-peak)	t_{CLK_PJ}	−50	—	+50	ps	2, 3, 4

Note:

1. **Caution:** Only 100, and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter should be less than or equal to 50 ps.

This figure shows the reference clock timing waveform.

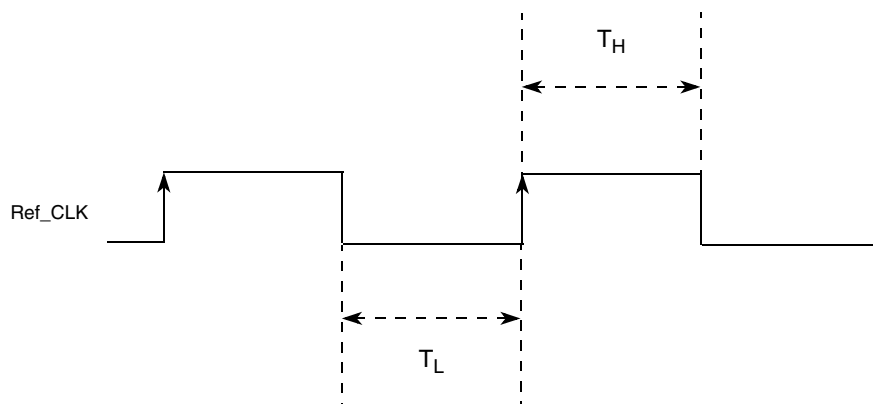


Figure 47. Reference clock timing waveform

2.20.8.3 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 89. Gen1i/1.5 G transmitter (Tx) AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	—	—	0.22	UI p-p	1

Note:

1. Measured at Tx output pins peak to peak phase variation, random data pattern

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 90. Gen 2i/3 G transmitter (Tx) AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXTJfB/10}$	—	—	0.3	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at Tx output pins peak-to-peak phase variation, random data pattern

2.20.8.4 AC differential receiver input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 91. Gen 1i/1.5G receiver (Rx) AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 92. Gen 2i/3G receiver (Rx) AC specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver.

2.20.9 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in [Figure 48](#), where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 43](#).

2.20.9.0.1 SGMII clocking requirements for SD_REF_CLKn and $\overline{SD_REF_CLKn}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on $SD_REF_CLK[1:3]$ and $\overline{SD_REF_CLK}[1:3]$ pins. SerDes banks 1-3 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see [Section 2.20.2, “SerDes reference clocks.”](#)

2.20.9.1 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.9.1.1 SGMII transmit DC timing specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX n and $\overline{\text{SD_TX}}n$) as shown in Figure 49.

Table 93. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output high voltage	V _{OH}	—	—	1.5 x V _{ODI} _{-max}	mV	1
Output low voltage	V _{OL}	V _{ODI} _{-min} /2	—	—	mV	1
Output differential voltage ^{2, 3, 4} (XV _{DD} -Typ at 1.5 V and 1.8 V)	V _{ODI}	320	500.0	725.0	mV	B(1-3)TECR(lane)0[A MP_RED] =0b000000
		293.8	459.0	665.6		B(1-3)TECR(lane)0[A MP_RED] =0b000010
		266.9	417.0	604.7		B(1-3)TECR(lane)0[A MP_RED] =0b000101
		240.6	376.0	545.2		B(1-3)TECR(lane)0[A MP_RED] =0b001000
		213.1	333.0	482.9		B(1-3)TECR(lane)0[A MP_RED] =0b001100
		186.9	292.0	423.4		B(1-3)TECR(lane)0[A MP_RED] =0b001111
		160.0	250.0	362.5		B(1-3)TECR(lane)0[A MP_RED] =0b010011
Output impedance (single-ended)	R _O	40	50	60	Ω	—

Note:

1. This does not align to DC-coupled SGMII.
2. $|V_{ODI}| = |V_{SD_TXn} - V_{\overline{\text{SD_TX}}n}|$. $|V_{ODI}|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \cdot |V_{ODI}|$.
3. Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
4. The $|V_{ODI}|$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.5 V or 1.8 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD_TX n and $\overline{\text{SD_TX}}n$.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

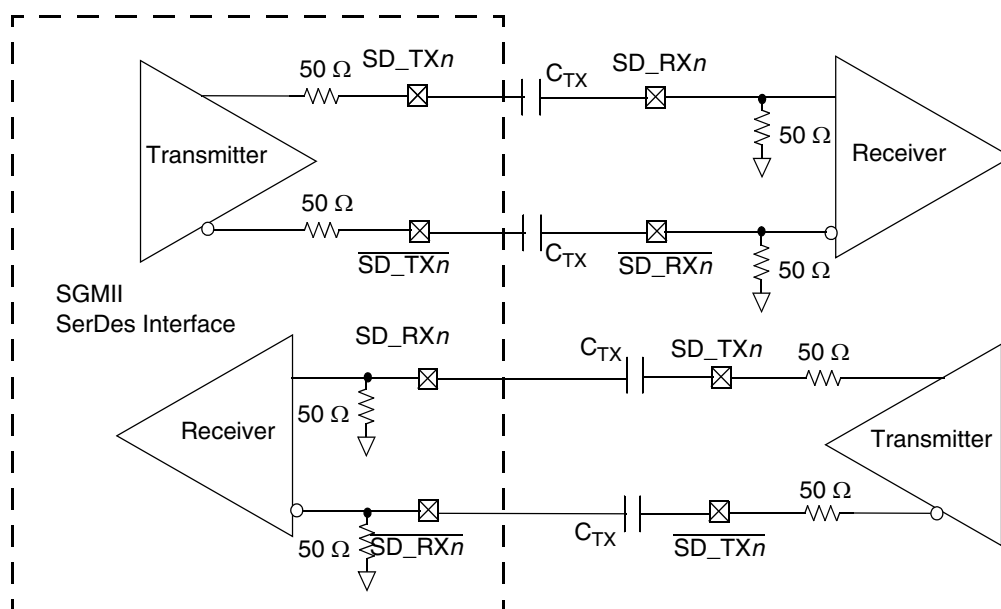


Figure 48. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

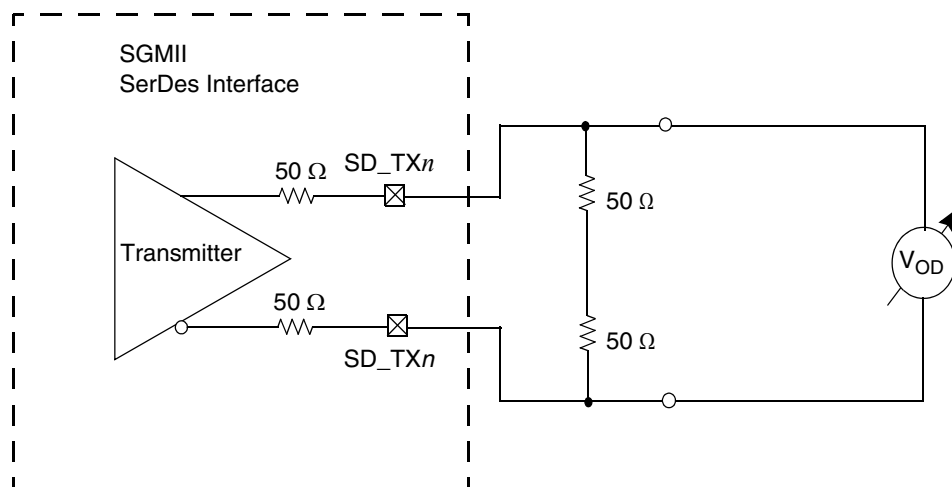


Figure 49. SGMII transmitter DC measurement circuit

Electrical characteristics

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 94. SGMII 2.5x transmitter DC electrical characteristics ($XV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Output voltage	V_O	-0.40	—	2.30	V	1
Differential output voltage	V_{DIFFP}	800	—	1600	mV p-p	—

Note:

1. Absolute output voltage limit

2.20.9.1.2 SGMII DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics for 1.25 GBaud. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 95. SGMII DC receiver electrical characteristics ($SV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter		Symbol	Min	Typ	Max	Unit	Note
DC Input voltage range		—	N/A			—	1
Input differential voltage	REIDL_CTL = 001xx	V _{RX_DIFFp-p}	100	—	1200	mV	2, 4
	REIDL_CTL = 100xx		175	—			
Loss of signal threshold	REIDL_CTL = 001xx	V _{LOS}	30	—	100	mV	3, 4
	REIDL_CTL = 100xx		65	—	175		
Receiver differential input impedance		Z _{RX_DIFF}	80	—	120	Ω	—

Note:

1. Input must be externally AC coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to [Section 2.20.4.4, “PCI Express DC physical layer receiver specifications,”](#) and [Section 2.20.4.5.2, “PCI Express AC physical layer receiver specifications,”](#) for further explanation.
4. The REIDL_CTL shown in the table refers to the chip's SerDes control register B(1-3)GCR(lane)1[REIDL_CTL] bit field.

[Table 76](#) defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 96. SGMII 2.5x receiver DC timing specifications ($SV_{DD} = 1.5\text{ V}$ or 1.8 V)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input voltage	V_{IN}	200	900	1600	mV p-p	1

Note:

1. Measured at the receiver.

2.20.9.2 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

2.20.9.2.1 SGMII transmit AC timing specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 97. SGMII transmit AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	1
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
AC coupling capacitor	C_{TX}	10	—	200	nF	2

Note:

1. See [Figure 46](#) for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.9.2.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TXn and $\overline{SD_TXn}$) or at the receiver inputs (SD_RXn and $\overline{SD_RXn}$) respectively, as depicted in this figure.

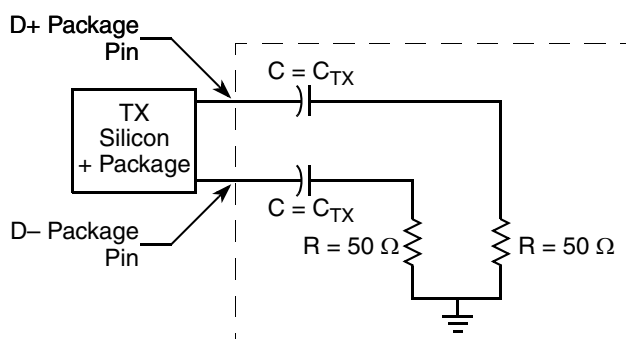


Figure 50. SGMII AC test/measurement load

2.20.9.2.3 SGMII receiver AC timing specification

The following table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 98. SGMII receive AC timing specifications

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1, 2, 3

Table 98. SGMII receive AC timing specifications (continued)

For recommended operating conditions, see [Table 3](#).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Note:

1. Measured at receiver.
2. Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 46](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of [Figure 46](#).

3 Hardware design considerations

3.1 System clocking

This section describes the PLL configuration of the chip.

This device includes 7 PLLs, as follows:

- There are 2 selectable core Complex PLLs which generate a core clock from the externally supplied SYSCLK input. Core complex 0-1 can select from CC1 PLL or CC2 PLL. The frequency ratio between the core Complex PLLs and SYSCLK is selected using the configuration bits as described in [Section 3.1.3, “e5500-64 core complex to SYSCLK PLL ratio.”](#) The frequency for each core complex 0-1 is selected using the configuration bits as described in [Table 102](#).
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 3.1.2, “Platform to SYSCLK PLL ratio.”](#)
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in [Section 3.1.5, “DDR controller PLL ratios.”](#)
- Each of the three SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK n /SD_REF_CLK $\bar{n}$ inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in [Section 3.1.6, “Frequency options.”](#)

3.1.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 99. Processor clocking specifications

Characteristic	Maximum processor core frequency								Unit	Note
	1200 MHz		1600 MHz		1800 MHz		2000 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e5500 Core PLL Frequency	1200	1200	1333	1600	1333	1800	1333	2000	MHz	1, 4
e5500 Core Frequency	600	1200	667	1600	667	1800	667	2000	MHz	4
Platform Clock Frequency	600	600	600	600	600	700	600	800	MHz	1
Memory bus clock frequency	400	600	400	600	400	650	400	667	MHz	1, 2, 5, 6
Local bus clock frequency	—	75	—	75	—	87.5	—	100	MHz	3
PME	—	300	—	300	—	350	—	400	MHz	7
FM _n	—	450	—	450	—	500	—	600	MHz	8

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e5500 core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, e5500 (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3/DDR3L memory bus clock frequency is limited to min = 400 MT/s.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the reference manual for your chip for more information.
4. The e5500 core can run at e5500 core complex PLL/1 or PLL/2. With a minimum core complex PLL frequency of 1333 MHz, this results in a minimum allowable e5500 core frequency of 667MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The PME runs synchronously to the platform clock, running at a frequency of platform clock/2.
8. For the FM_n: 300 MHz is the minimum to support 1 G. 450 MHz is the minimum to support 10 G. 500 MHz is the minimum to support 10 G with PCD. 600 MHz is the minimum to support 12 G (10 G + 2*1 G) with PCD.

3.1.2 Platform to SYSCLK PLL ratio

The allowed platform clock to SYSCLK ratios are shown in this table.

Note that in synchronous DDR mode, the DDR data rate is the determining factor for selecting the platform bus frequency because the platform frequency must equal the DDR data rate.

In asynchronous DDR mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 100. Platform to SYSCLK PLL ratios

Binary value of SYS_PLL_RAT	Platform:SYSCLK ratio
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
All Others	Reserved

3.1.3 e5500-64 core complex to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the two core complex PLLs is determined at power up by the binary value of the RCW field CCn_PLL_RAT. This table describes the supported ratios. Note that a core complex PLL frequency targeting 1 GHz and above must set RCW field CCn_PLL_CFG = 0b00, for frequency targeting below 1 GHz set CCn_PLL_CFG = 0b01.

This table lists the supported Core Complex to SYSCLK ratios.

Table 101. e5500 core complex PLL to SYSCLK ratios

Binary Value of CCn_PLL_RAT	Core Complex:SYSCLK Ratio
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
0_1110	14:1
0_1111	15:1
1_0000	16:1
1_0001	17:1
1_0010	18:1
All Others	Reserved

3.1.4 e5500 core complex PLL select

The clock frequency of each the e5500 core 0–1 complex is determined by the binary value of the RCW field `CCn_PLL_SEL`. This table describes the supported ratios for each core complex 0-1, where each individual core complex can select a frequency from the table.

For this table, if CC2 PLL is used by core0, then CC2 PLL must be operated at a lower frequency than the CC1 PLL, and its maximum allowed frequency is 80% of the maximum rated frequency of the core at nominal voltage. Similarly, if CC1 PLL is used by core1, then CC1 PLL must be operated at a lower frequency than the CC2 PLL, and its maximum allowed frequency is 80% of the maximum rated frequency of the core at nominal voltage.

Table 102. Core complex [0,1] PLL select

Binary value of <code>C_n_PLL_SEL</code>	e5500 core complex 0 clock	e5500 core complex 1 clock
0000	CC1 PLL /1	CC1 PLL /1
0001	CC1 PLL /2	Reserved
0100	CC2 PLL /1	CC2 PLL /1
0101	Reserved	CC2 PLL /2
All Others	Reserved	Reserved

3.1.5 DDR controller PLL ratios

The dual DDR memory controller complexes can be synchronous with or asynchronous to the platform, depending on configuration. Both DDR controllers operate at the same frequency configuration. For P5010, only the DDR-1 controller is available.

[Table 103](#) describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in [Table 103](#). This ratio is determined by the binary value of the RCW Configuration field `MEM_PLL_RAT[10:14]`.

The RCW Configuration field `MEM_PLL_CFG[8:9]` must be set to `MEM_PLL_CFG[8:9] = 0b01` if the applied DDR PLL reference clock frequency is greater than the cutoff frequency listed in [Table 103](#) and [Table 104](#) for asynchronous and synchronous DDR clock ratios respectively, else set `MEM_PLL_CFG[8:9]=b'00`.

NOTE

The RCW Configuration field `DDR_SYNC` (bit 184) must be set to b'0 for asynchronous mode, and b'1 for synchronous mode.

The RCW Configuration field `DDR_RATE` (bit 232) must be set to b'0 for asynchronous mode, and b'1 for synchronous mode.

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The RCW Configuration field DDR_RSV0 (bit 234) must be set to b'0 for all ratios.

Table 103. Asynchronous DDR clock ratio

Binary value of MEM_PLL_RAT[10:14]	DDR:SYSCLK ratio	Set MEM_PLL_CFG = 01 for SYSCLK freq ¹
0_0101	5:1	>96.7 MHz
0_0110	6:1	>80.6 MHz
0_1000	8:1	>120.9 MHz
0_1001	9:1	>107.4 MHz
0_1010	10:1	>96.7 MHz
0_1100	12:1	>80.6 MHz
0_1101	13:1	>74.4 MHz
All Others	Reserved	—

Note:

1. Set RCW field MEM_PLL_CFG = 0b01 if the applied DDR PLL reference clock (SYSCLK) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 104. Synchronous DDR clock ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK Ratio	Set MEM_PLL_CFG=01 for Platform CLK Freq ¹
0_0001	1:1	>600 MHz
All Others	Reserved	—

Note:

1. Set MEM_PLL_CFG=0b01 if the applied DDR PLL reference clock (Platform clock) frequency is greater than given cutoff, else set to 0b00 for frequency that is less than or equal to cutoff.

3.1.6 Frequency options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 105. SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	100	125	133.3	150	166
	Platform Frequency (MHz) ¹				
4:1				600	664
5:1		625	667	750	
6:1	600	750	800		
7:1	700				
8:1	800				

¹ Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in [Figure 51](#) and [Figure 52](#).

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{8}$$

Figure 51. Gen 1 PEX minimum platform frequency

$$\frac{527 \text{ MHz} \times (\text{PCI Express link width})}{4}$$

Figure 52. Gen 2 PEX minimum platform frequency

See Section 18.1.3.2, “Link Width,” in the reference manual for your chip for PCI Express interface width details. Note that “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

Figure 53. Serial RapidIO minimum platform frequency

See Section 19.4, “LP-Serial Signal Descriptions,” in the reference manual for your chip for Serial RapidIO interface width and frequency details.

3.1.7 SerDes PLL ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied $SD_REF_CLK_n/SD_REF_CLK_n$ inputs is determined by the binary value of the RCW Configuration field $SRDS_RATIO_B_n$ as shown in this table. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field $SRDS_DIV_B_n$ as shown in [Table 107](#) and [Table 108](#).

This table lists the supported SerDes PLL Bank n to $SD_REF_CLK_n$ ratios.

Table 106. SerDes PLL Bank n to $SD_REF_CLK_n$ ratios

Binary value of $SRDS_RATIO_B1$	$SRDS_PLL_n:SD_REF_CLK_n$ ratio		
	$n = 1$ (Bank 1)	$n = 2$ (Bank 2)	$n = 3$ (Bank 3)
001	Reserved	20:1	20:1
010	25:1	25:1	25:1
011	40:1	40:1	40:1
100	50:1	50:1	50:1
101	Reserved	Reserved	24:1
110	Reserved	Reserved	30:1
All Others	Reserved	Reserved	Reserved

This table shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 107. SerDes Bank 1 PLL dividers

Binary Value of $SRDS_DIV_B1[0:4]$	SerDes Bank 1 PLL divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Note:

1. 1 bit (of 5 total $SRDS_DIV_B1$ bits) controls each pair of lanes, where the first bit controls configuration of lanes A/B (or 0/1) and the last bit controls configuration of lanes I/J (or 8/9).

This table shows the PLL dividers supported for each 4 lane group for SerDes Banks 2 and 3.

Table 108. SerDes Banks 2 and 3 PLL Dividers

Binary Value of $SRDS_DIV_B_n$	SerDes Bank n PLL divider
0b0	Divide by 1 off Bank n PLL
0b1	Divide by 2 off Bank n PLL

Note:

1. One bit controls all 4 lanes of each bank.
2. $n = 2$ or 3 (SerDes bank 2 or bank 3)

3.1.8 Frame manager clock select

The frame managers, FM, can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM_CLK_SEL .

Table 109. Frame manager clock select

Binary value of FM_CLK_SEL	FM frequency
0b0	Platform clock frequency /2
0b1	Core complex frequency /2 ¹

Note:

1. For asynchronous mode, max frequency, see [Table 99](#).

3.2 Supply power default setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Table 110. I/O voltage selection

Signals	Value (binary)	VDD voltage selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4] Default (0_0000)	0_0000	3.3 V	3.3 V	3.3 V
	0_0001	3.3 V	3.3 V	2.5 V
	0_0011	3.3 V	2.5 V	3.3 V
	0_0100	3.3 V	2.5 V	2.5 V
	0_0110	3.3 V	1.8 V	3.3 V
	0_0111	3.3 V	1.8 V	2.5 V
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010	2.5 V	3.3 V	2.5 V
	0_1100	2.5 V	2.5 V	3.3 V
	0_1101	2.5 V	2.5 V	2.5 V
	0_1111	2.5 V	1.8 V	3.3 V
	1_0000	2.5 V	1.8 V	2.5 V
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011	1.8 V	3.3 V	2.5 V
	1_0101	1.8 V	2.5 V	3.3 V
	1_0110	1.8 V	2.5 V	2.5 V
	1_1000	1.8 V	1.8 V	3.3 V
	1_1001	1.8 V	1.8 V	2.5 V
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100	3.3 V	3.3 V	3.3 V
	1_1101	3.3 V	3.3 V	3.3 V
	1_1110	3.3 V	3.3 V	3.3 V
	1_1111	3.3 V	3.3 V	3.3 V
	All Others	Reserved		

3.3 Power supply design

3.3.1 PLL power supply filtering

Each of the PLLs described in [Section 3.1, “System clocking,”](#) is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CCn} , AV_{DD_DDR} , and AV_{DD_SRDSn}). AV_{DD_PLAT} , AV_{DD_CCn} and AV_{DD_DDR} voltages must be derived directly from the V_{DD_PL} source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in [Figure 54](#), one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias, as shown in the following figure.

Where:

$$R = 5\ \Omega \pm 5\%$$

$$C1 = 10\ \mu\text{F} \pm 10\%, \text{ 0603, X5R, with } ESL \leq 0.5\ \text{nH}$$

$$C2 = 1.0\ \mu\text{F} \pm 10\%, \text{ 0402, X5R, with } ESL \leq 0.5\ \text{nH}$$

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, $ESL \leq 0.5\ \text{nH}$).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD} .

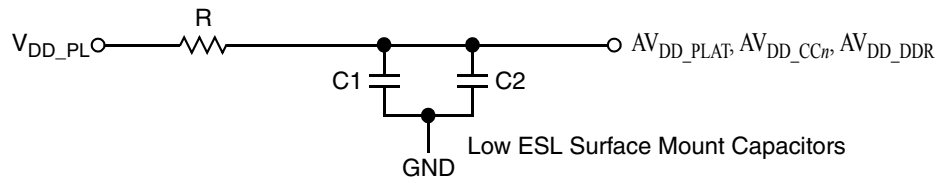


Figure 54. PLL power supply filter circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 55. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD_SRDSn} balls. The 0.003- μF capacitor is closest to the balls, followed by two 2.2- μF capacitors, and finally the 1- Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

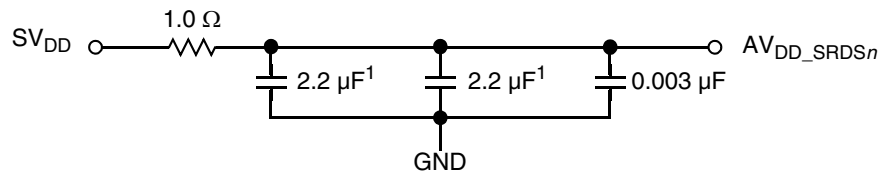


Figure 55. SerDes PLL power supply filter circuit

Note the following:

- AV_{DD_SRDSn} should be a filtered version of SV_{DD} .
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn} .
- An 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} power supply filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered 1.5 V or 1.8 V voltage source. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where 1.5 V or 1.8 V is sourced from voltage source (for example, GV_{DD} at 1.5 V when using DDR3, or CV_{DD} at 1.8 V), is illustrated in Figure 56. The component values in this example filter is system

Hardware design considerations

dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

$C1 = 2.2 \mu\text{F} \pm 10\%$, X5R, with $\text{ESL} \leq 0.5 \text{ nH}$

$C2 = 2.2 \mu\text{F} \pm 10\%$, X5R, with $\text{ESL} \leq 0.5 \text{ nH}$

$F1 = 120 \Omega$ at 100-MHz 2A 25% 0603 Ferrite

$F2 = 120 \Omega$ at 100-MHz 2A 25% 0603 Ferrite

Bulk and decoupling capacitors are added, as needed, per power supply design.

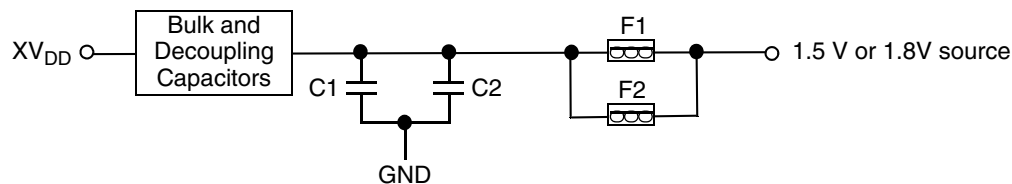


Figure 56. Xv_{DD} power supply filter circuit

3.3.3 USB_VDD_1P0 power supply filtering

USB_VDD_1P0 should be sourced by a filtered V_{DD_PL} using a star connection. An example solution for USB_VDD_1P0 filtering, where USB_VDD_1P0 is sourced from V_{DD_PL} , is illustrated in Figure 57. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

$C1 = 2.2 \mu\text{F} \pm 20\%$, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)

$F1 = 120 \Omega$ at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)

Bulk and decoupling capacitors are added, as needed, per power supply design.

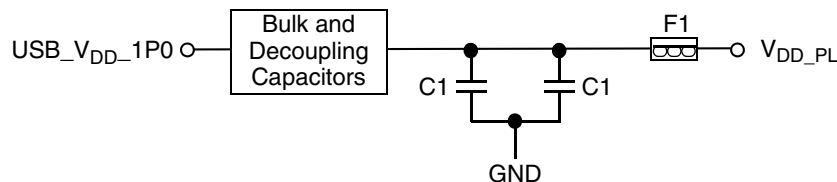


Figure 57. USB_VDD_1P0 power supply filter circuit

3.4 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip's system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , BV_{DD} , OV_{DD} , CV_{DD} , GV_{DD} , and LV_{DD} pin of the chip. These decoupling capacitors should receive their power from separate V_{DD} , BV_{DD} , OV_{DD} , CV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of $0.1 \mu\text{F}$. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , BV_{DD} , OV_{DD} , CV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

3.5 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

- First, the board should have at least $10 \times 10\text{-nF}$ SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a $1\text{-}\mu\text{F}$ ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a $10\text{-}\mu\text{F}$, low ESR SMT tantalum chip capacitor and a $100\text{-}\mu\text{F}$, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

3.6 Connection recommendations

To ensure reliable chip operation, it is highly recommended that the user note the following:

- Connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD} , BV_{DD} , CV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections should be made to all external V_{DD} , BV_{DD} , CV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.
- The Ethernet controllers 1 and/or 2 input pins may be disabled by setting their respective RCW Configuration field EC1 (bits 360–361), and EC2 (bits 363–364), to 0b11 = No parallel mode Ethernet. When disabled, these inputs do not need to be externally pulled to an appropriate signal level.
- ECn_GTX_CLK125 is a 125-MHz input clock on the dTSEC ports. If the dTSEC ports are not used for RGMII, the ECn_GTX_CLK125 input can be tied off to GND.
- If RCW field DMA1=0b1 (RCW bit 384), the DMA1 external interface is not enabled and this pin should be left as a no connect.
- If RCW field I2C = 0b100 or 0b101 (RCW bits 355–357), the SDHC_WP and SDHC_CD input signals are enabled for external use. If SDHC_WP and SDHC_CD are selected and not used, they must be externally pulled low such that $\text{SDHC_WP} = 0$ (write enabled) and $\text{SDHC_CD} = 0$ (card detected). If RCW field I2C != 0b100 or 0b101, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and SDHC_CD are internally driven such that $\text{SDHC_WP} =$ write enabled and $\text{SDHC_CD} =$ card detected and the selected I2C3 or GPIO external pin functionality may be used.
- For P5010 without security (SVR = 0x8221_0010) or P5010E (SVR = 0x8229_0010), TEST_SEL must be connected to GND.
- The TMP_DETECT pin is an active low input to the Security Monitor (see Chapter “Secure Boot and Trust Architecture” in the reference manual for your chip). When using Trust Architecture functionality, external logic must ramp TMP_DETECT with OV_{DD} . If not using Trust Architecture functionality, TMP_DETECT must be tied to OV_{DD} to prevent the input from going low.
- TMP_DETECT pin and LP_TMP_DETECT pin are active low input to the Security Monitor (see the “Secure Boot and Trust Architecture” chapter of the applicable chip reference manual). If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. 1K pull-down resistor strongly recommended. If Trust is used without tamper sensors, tie high. VDD_LP must be connected even if Low Power features are not used. Otherwise the LP Section will generate internal errors, which will prevent the high power trust section from reaching Trusted/Secure state.

- For P5010, the voltage rail VDD_CB must be connected to GND.

3.6.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 59](#). Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 59](#) allows the COP port to independently assert $\overline{\text{PORESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well. The COP interface has a standard header, shown in [Figure 58](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in [Figure 58](#) is common to all known emulators.

3.6.1.1 Termination of unused signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ through a 0 k Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in [Figure 59](#). If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

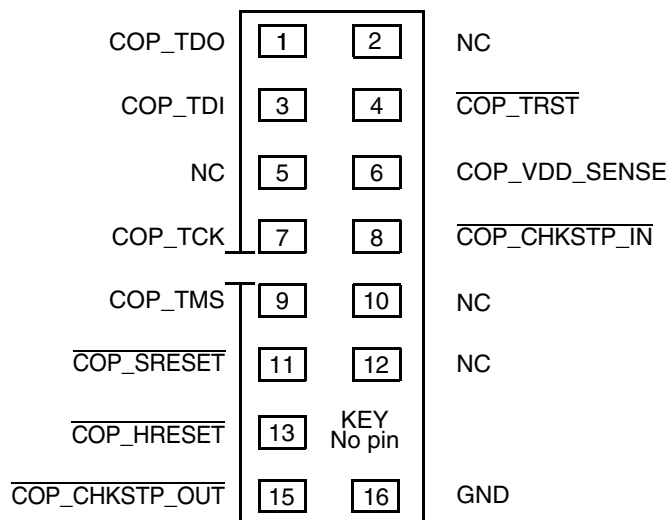
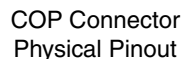


Figure 58. Legacy COP connector physical pinout



1. The COP port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.

6. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.

P5020/P5010

3.6.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in [Figure 60](#) and [Figure 61](#). Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Freescall recommends that the Aurora 22 pin duplex connector be designed into the system as shown in [Figure 62](#) or the 70 pin duplex connector be designed into the system as shown in [Figure 63](#).

If the Aurora interface is not used, Freescall recommends the legacy COP header be designed into the system as described in [Section 3.6.1.1, “Termination of unused signals.”](#)

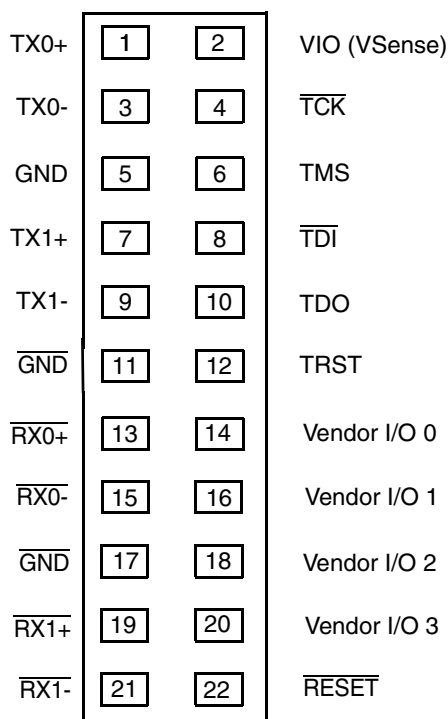


Figure 60. Aurora 22 pin connector duplex pinout

TX0+	1	2	VIO (VSense)
TX0-	3	4	$\overline{\text{TCK}}$
GND	5	6	TMS
TX1+	7	8	$\overline{\text{TDI}}$
TX1-	9	10	TDO
GND	11	12	TRST
$\overline{\text{RX0+}}$	13	14	Vendor I/O 0
$\overline{\text{RX0-}}$	15	16	Vendor I/O 1
GND	17	18	Vendor I/O 2
$\overline{\text{RX1+}}$	19	20	Vendor I/O 3
$\overline{\text{RX1-}}$	21	22	$\overline{\text{RESET}}$
GND	23	24	GND
TX2+	25	26	$\overline{\text{CLK+}}$
TX2-	27	28	$\overline{\text{CLK-}}$
GND	29	30	GND
TX3+	31	32	Vendor I/O 4
TX3-	33	34	Vendor I/O 5
GND	35	36	GND
$\overline{\text{RX2+}}$	37	38	N/C
$\overline{\text{RX2-}}$	39	40	N/C
GND	41	42	GND
$\overline{\text{RX3+}}$	43	44	N/C
$\overline{\text{RX3-}}$	45	46	N/C
GND	47	48	GND
TX4+	49	50	N/C
TX4-	51	52	N/C
GND	53	54	GND
TX5+	55	56	N/C
TX5-	57	58	N/C
GND	59	60	GND
TX6+	61	62	N/C
TX6-	63	64	N/C
GND	65	66	GND
TX7+	67	68	N/C
TX7-	69	70	N/C

Figure 61. Aurora 70 pin connector duplex pinout

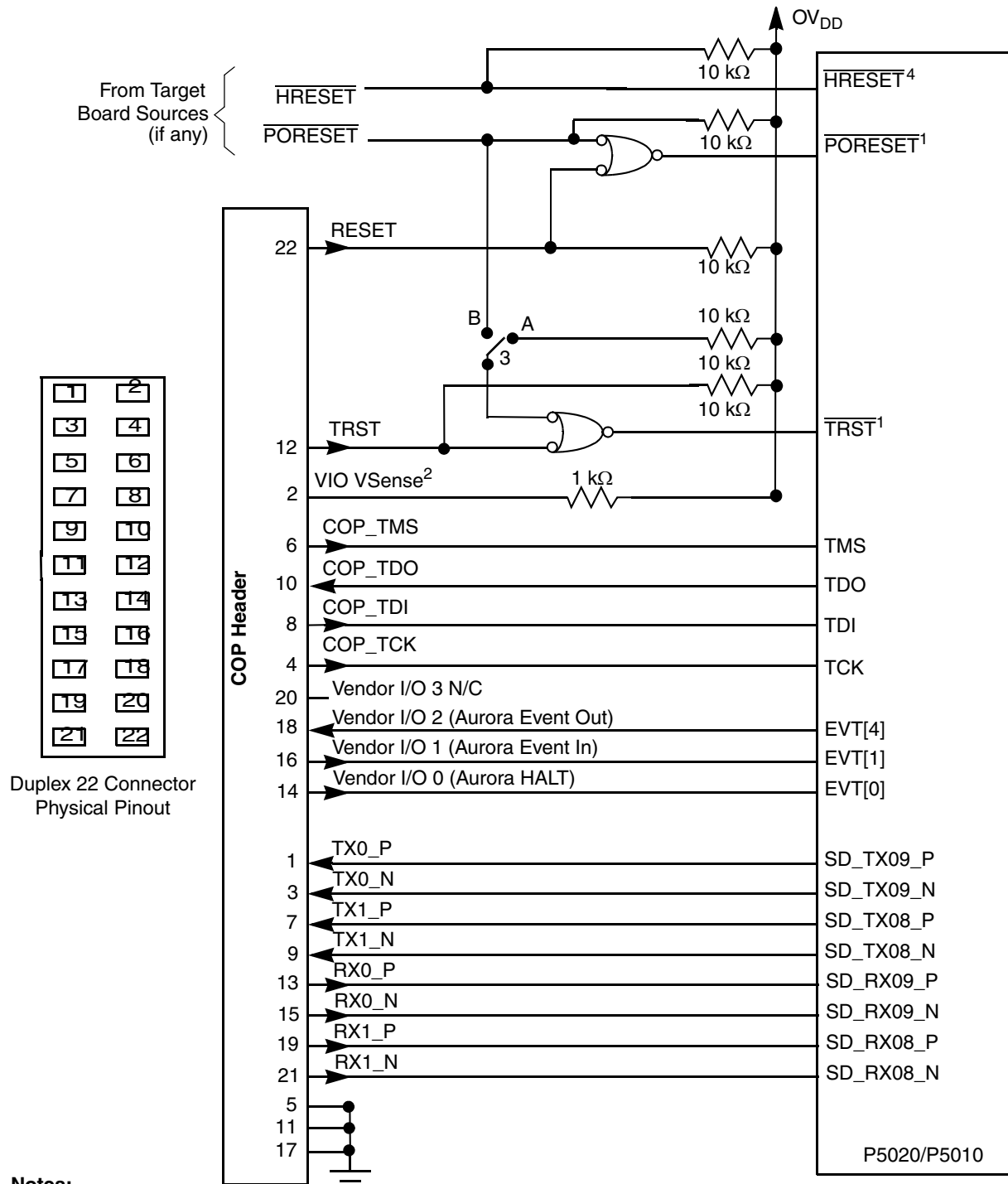


Figure 62. Aurora 22 pin connector duplex interface connection



3.6.3 Guidelines for high-speed interface termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused or when it is partly unused.

3.6.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[17:0]
- $\overline{\text{SD_TX}}[17:0]$
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[17:0]
- $\overline{\text{SD_RX}}[17:0]$
- SD_REF_CLK1, SD_REF_CLK2, SD_REF_CLK3
- $\overline{\text{SD_REF_CLK1}}$, $\overline{\text{SD_REF_CLK2}}$, $\overline{\text{SD_REF_CLK3}}$

The RCW configuration fields SRDS_LPD_B1, SRDS_LPD_B2 and SRDS_LPD_B3, all bits must be set to power down all the lanes in each bank.

The RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN] = 0 powers down the PLLs of all three banks.

Additionally, software may configure SRDSBnRSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Leave these pins unconnected:

- SD_TX[n]
- $\overline{\text{SD_TX}}[n]$

Connect these unused pins to SGND:

- SD_RX[n]
- $\overline{\text{SD_RX}}[n]$
- SD_REF_CLK1, $\overline{\text{SD_REF_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD_REF_CLK2}}$ (If entire SerDes bank 2 unused)
- SD_REF_CLK3, $\overline{\text{SD_REF_CLK3}}$ (If entire SerDes bank 3 unused)

In the RCW configuration field for each bank SRDS_LPD_Bn with unused lanes, the respective bit for each unused lane must be set to power down the lane.

3.6.4 USB controller connections

This section details the hardware connections required for the USB controllers.

3.6.4.1 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are as follows:

- Both resistors require 0.1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an $I_F = 10$ mA, $I_R < 500$ nA and $V_{F(Max)} = 0.8$ V.

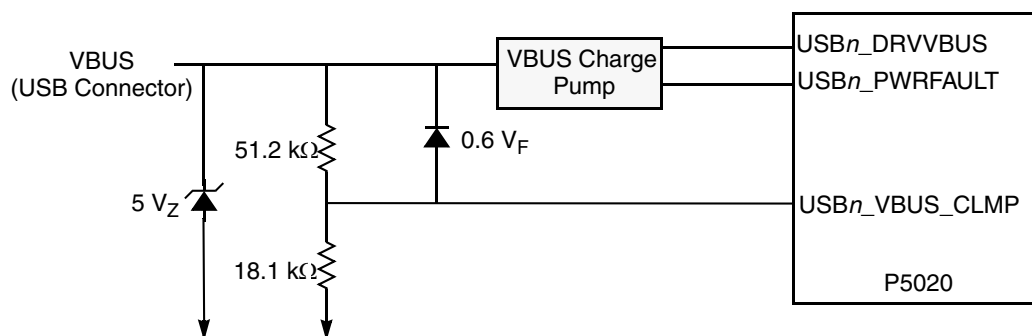


Figure 64. Divider network at VBUS

USB1_DRVVBUS and USB1_PWRFAULT are muxed on GPIO[4:5] pins, respectively. USB2_DRVVBUS and USB2_PWRFAULT are muxed on GPIO[6:7] pins, respectively. Setting the RCW[GPIO] bit selects USB functionality on the GPIO pins.

3.6.4.2 USB_n_V_{DD}_1P8_DECAP capacitor options

The USB_n_V_{DD}_1P8_DECAP pins require a capacitor connected to GND. This table lists the recommended capacitors for the USB_n_V_{DD}_1P8_DECAP signal.

Table 111. Recommended capacitor parts for USB_n_V_{DD}_1P8_DECAP

Manufacturer	Part Number	Value	ESR	Package
Kemet	T494B105(1)025A(2)	1 μ F, 25 V	2 Ω	B(3528)
	T494B155(1)025A(2)	1.5 μ F, 25 V	1.5 Ω	—
NIC	NMC0603X7R106KTRPF	1 μ F, 10 V	Low ESR	0603
TDK Corporation	CERB2CX5R0G105M	1 μ F, 4 V	200 m- Ω	0603
Vishay	TR3B105(1)035(2)1500	1 μ F, 35 V	1.5 Ω	B(3528)

3.7 Recommended thermal mode

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal management information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in this figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

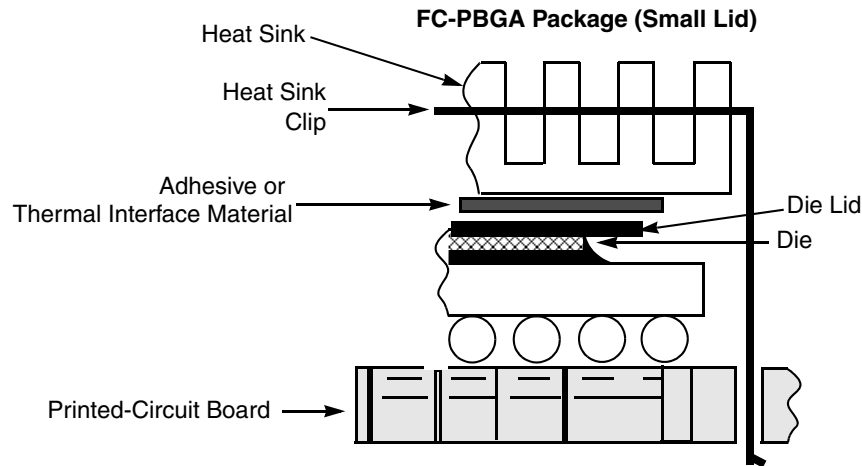


Figure 65. Package exploded cross-sectional view—FC-PBGA (w/ lid) package

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

Package information

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

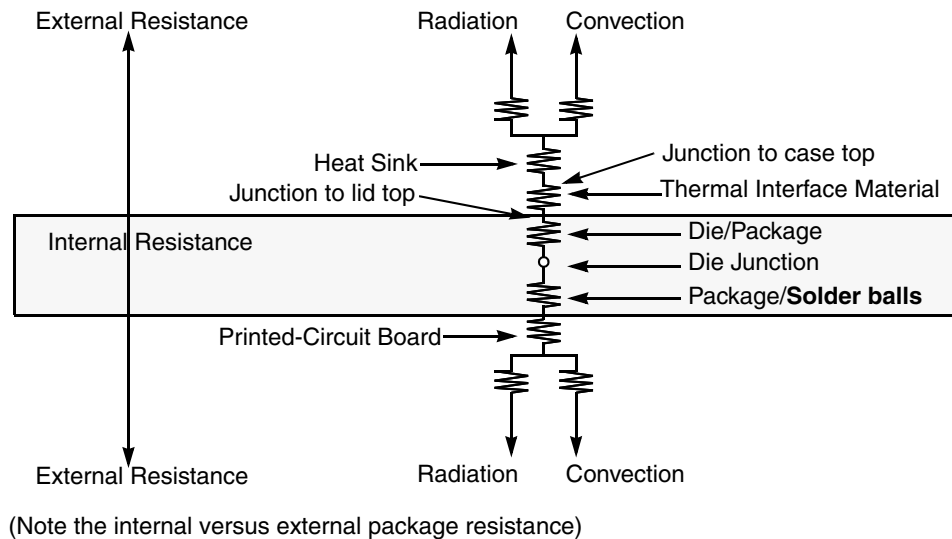


Figure 66. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.8.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see [Figure 65](#)).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8.3 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: 10 – 230 μ A
- Ideality factor over 13.5 – 220 μ A: $n = 1.00569 \pm 0.008$

4 Package information

The following section describes the detailed content and mechanical description of the package.

4.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 37.5 mm $\times$ 37.5 mm, 1295 flip chip plastic ball grid array (FC-PBGA).

Package outline	37.5 mm × 37.5 mm
Interconnects	1295
Ball Pitch	1.0 mm
Ball Diameter (typical)	0.60 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.88 mm to 3.53 mm (maximum)

4.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

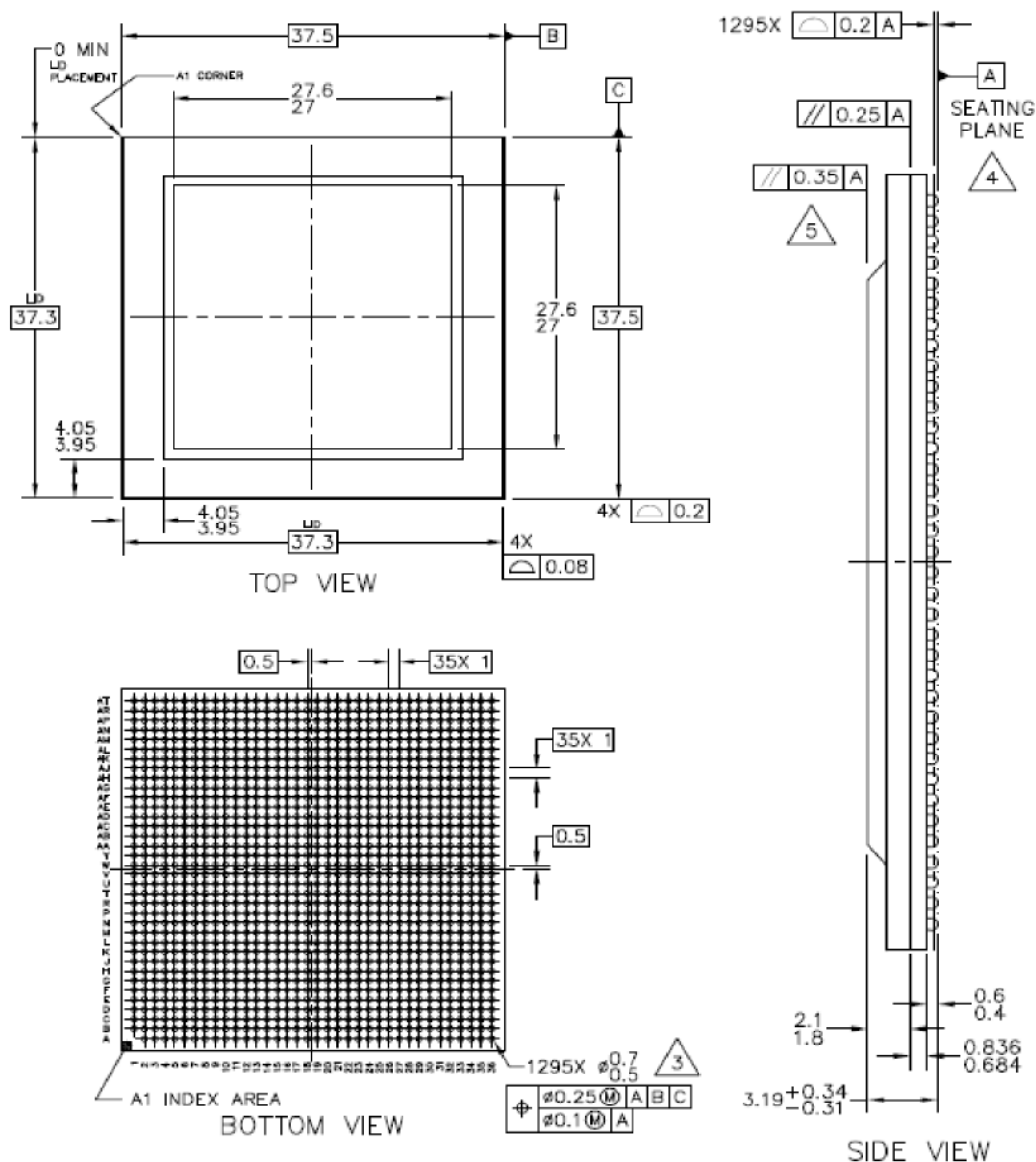


Figure 67. Mechanical dimensions of the FC-PBGA with full lid

Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement excludes any effect of mark on top surface of package.

5 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the reference manual for your chip.

To program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per [Section 2.2, "Power up sequencing."](#) POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, connect POV_{DD} to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in [Figure 9](#). To ensure chip reliability, fuse programming must be performed within the recommended fuse programming temperature range per [Table 3](#).

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering information

Contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part numbering nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature.

Table 112. Part numbering nomenclature

<i>p</i>	<i>n</i>	<i>nn</i>	<i>n</i>	<i>x</i>	<i>t</i>	<i>e</i>	<i>n</i>	<i>c</i>	<i>d</i>	<i>r</i>
Generation	Platform	Number of cores	Derivative	Qual status	Temperature range	Encryption	Package type	CPU speed	DDR data rate	Die revision
P = 45 nm	5	01 = 1 core 02 = 2 core	0	P = Prototype N = Industrial Qualification	S = Std Temp X = Extended temp (–40 °C to 105 °C)	E = SEC Present N = SEC Not Present	1 = FC-PBGA Pb free 7 = FC-PBGA C4/C5 Pb free	M = 1200 MHz Q = 1600 MHz T = 1800 MHz V = 2000 MHz	M = 1200 N = 1333	A = Rev 1.0 B = Rev 2.0

6.2 Orderable part numbers addressed by this document

This table provides the Freescale orderable part numbers addressed by this document for the chip. Contact your Freescale Sales Representative for more information on orderable parts as not all combinations of orderable part numbers are available.

Table 113. Orderable part numbers addressed by this document

Part Number	<i>p</i>	<i>n</i>	<i>nn</i>	<i>n</i>	<i>x</i>	<i>t</i>	<i>e</i>	<i>n</i>	<i>c</i>	<i>d</i>	<i>r</i>		
P5020NSE1MMB	P	5	02	0	N	S	E	1	M	M	B		
P5020NSN1MMB							N						
P5020NSE1QMB							E		Q				
P5020NSN1QMB							N						
P5020NSE1TNB							E		T	N			
P5020NSN1TNB							N						
P5020NSE1VNB							E		V	N			
P5020NSN1VNB							N						
P5020NXE1QMB						X	E		Q	M			
P5020NXN1QMB							N						
P5020NXE1TNB							E		T	N			
P5020NXN1TNB							N						
P5010NSE1MMB	P	5	01	0	N	S	E	1	M	M	B		
P5010NSN1MMB							N						
P5010NSE1QMB							E		Q				
P5010NSN1QMB							N						
P5010NSE1TNB							E		T	N			
P5010NSN1TNB							N						
P5010NSE1VNB							E		V	N			
P5010NSN1VNB							N						
P5010NXE1QMB						X	E		Q	M			
P5010NXN1QMB							N						
P5010NXE1TNB							E		T	N			
P5010NXN1TNB							N						

Table 113. Orderable part numbers addressed by this document (continued)

Part Number	<i>p</i>	<i>n</i>	<i>nn</i>	<i>n</i>	<i>x</i>	<i>t</i>	<i>e</i>	<i>n</i>	<i>c</i>	<i>d</i>	<i>r</i>
P5020NSE7MMB	P	5	02	0	N	S	E	7	M	M	B
P5020NSN7MMB							N				
P5020NSE7QMB							E		Q		
P5020NSN7QMB							N				
P5020NSE7TNB							E		T	N	
P5020NSN7TNB							N				
P5020NSE7VNB							E		V	N	
P5020NSN7VNB							N				
P5020NXE7QMB						X	E		Q	M	
P5020NXN7QMB							N				
P5020NXE7TNB							E		T	N	
P5020NXN7TNB							N				
P5010NSE7MMB	P	5	01	0	N	S	E	7	M	M	B
P5010NSN7MMB							N				
P5010NSE7QMB							E		Q		
P5010NSN7QMB							N				
P5010NSE7TNB							E		T	N	
P5010NSN7TNB							N				
P5010NSE7VNB							E		V	N	
P5010NSN7VNB							N				
P5010NXE7QMB						X	E		Q	M	
P5010NXN7QMB							N				
P5010NXE7TNB							E		T	N	
P5010NXN7TNB							N				

7 Revision history

This table provides a revision history for this document.

Table 114. Revision history

Revision	Date	Description
1	03/2015	- Updated document title. - Updated the eSDHC and eSPI sections of Table 1, "Pins listed by bus." - Updated Section 3.4, "Decoupling recommendations." - Added footnote 7 to Figure 59, "Legacy JTAG interface connection." - Updated tables in Section 6, "Ordering information."
0	03/2013	Initial public release

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