

FEATURES

- **3MHz Gain Bandwidth**
- **200V/ μ s Slew Rate**
- **250 μ A Supply Current**
- **Available in Tiny MSOP Package**
- **C-Load™ Op Amp Drives All Capacitive Loads**
- **Unity-Gain Stable**
- **Power Saving Shutdown Feature**
- **Maximum Input Offset Voltage: 600 μ V**
- **Maximum Input Bias Current: 50nA**
- **Maximum Input Offset Current: 15nA**
- **Minimum DC Gain, $R_L = 2k$: 30V/mV**
- **Input Noise Voltage: 14nV/ $\sqrt{\text{Hz}}$**
- **Settling Time to 0.1%, 10V Step: 700ns**
- **Settling Time to 0.01%, 10V Step: 1.25 μ s**
- **Minimum Output Swing into 1k: $\pm 13V$**
- **Minimum Output Swing into 500 Ω : $\pm 3.4V$**
- **Specified at $\pm 2.5V$, $\pm 5V$ and $\pm 15V$**

APPLICATIONS

- Battery-Powered Systems
- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

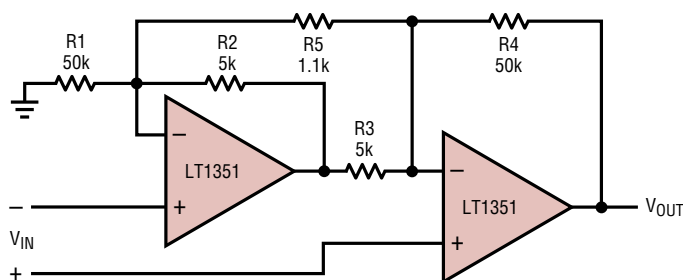
The LT[®]1351 is a low power, high speed, high slew rate operational amplifier with outstanding AC and DC performance. The LT1351 features lower supply current, lower input offset voltage, lower input bias current and higher DC gain than devices with comparable bandwidth. The circuit combines the slewing performance of a current feedback amplifier in a true operational amplifier with matched high impedance inputs. The high slew rate ensures that the large-signal bandwidth is not degraded. The amplifier is a single gain stage with outstanding settling characteristics which make the circuit an ideal choice for data acquisition systems. The output drives a 1k Ω load to $\pm 13V$ with $\pm 15V$ supplies and a 500 Ω load to $\pm 3.4V$ on $\pm 5V$ supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

The LT1351 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced complementary bipolar processing. For dual and quad amplifier versions of the LT1351 see the LT1352/LT1353 data sheet. For higher bandwidth devices with higher supply current see the LT1354 through LT1365 data sheets. Singles, duals and quads of each amplifier are available.

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C-Load is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

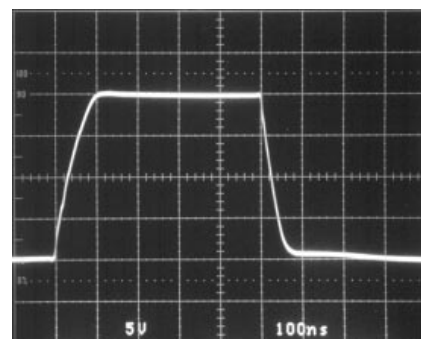
Instrumentation Amplifier



GAIN = $[R4/R3][1 + (1/2)(R2/R1 + R3/R4) + (R2 + R3)/R5] = 102$
 TRIM R5 FOR GAIN
 TRIM R1 FOR COMMON MODE REJECTION
 BW = 30kHz

1351 TA01

Large-Signal Response



$A_V = -1$

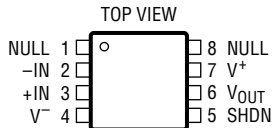
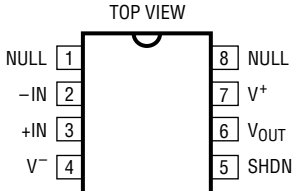
1351 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
 Differential Input Voltage (Transient Only, Note 1) ... $\pm 10V$
 Input Voltage $\pm V_S$
 Output Short-Circuit Duration (Note 2) Indefinite
 Operating Temperature Range -40°C to 85°C

Specified Temperature Range (Note 6) -40°C to 85°C
 Maximum Junction Temperature (See Below)
 Plastic Package 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

 MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 250^\circ\text{C/W}$	ORDER PART NUMBER	 N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$ (N8) $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 190^\circ\text{C/W}$ (S)	ORDER PART NUMBER
	LT1351CMS8		LT1351CN8 LT1351CS8
	MS8 PART MARKING		S8 PART MARKING
	LTBT		1351

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15V$ $\pm 5V$ $\pm 2.5V$		0.2 0.2 0.3	0.6 0.6 0.8	mV mV mV
I_{OS}	Input Offset Current		$\pm 2.5V$ to $\pm 15V$		5	15	nA
I_B	Input Bias Current		$\pm 2.5V$ to $\pm 15V$		20	50	nA
e_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		14		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		0.5		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$ Differential	$\pm 15V$ $\pm 15V$	300	600 20		$\text{M}\Omega$ $\text{M}\Omega$
C_{IN}	Input Capacitance		$\pm 15V$		3		pF
	Positive Input Voltage Range		$\pm 15V$ $\pm 5V$ $\pm 2.5V$	12.0 2.5 0.5	13.5 3.5 1.0		V V V
	Negative Input Voltage Range		$\pm 15V$ $\pm 5V$ $\pm 2.5V$	-13.5 -3.5 -1.0	-12.0 -2.5 -0.5		V V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$ $V_{CM} = \pm 2.5V$ $V_{CM} = \pm 0.5V$	$\pm 15V$ $\pm 5V$ $\pm 2.5V$	80 78 68	94 86 77		dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 15V$		90	106		dB

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 5\text{k}$	$\pm 15\text{V}$	40	80		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	30	60		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	20	40		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 5\text{k}$	$\pm 5\text{V}$	30	60		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	25	50		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	15	30		V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 5\text{k}$	$\pm 2.5\text{V}$	20	40		V/mV
V_{OUT}	Output Swing	$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.5	14.0		$\pm\text{V}$
		$R_L = 2\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.4	13.8		$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.0	13.4		$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.5	4.0		$\pm\text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.4	3.8		$\pm\text{V}$
		$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.3	1.7		$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 13\text{V}$	$\pm 15\text{V}$	13.0	13.4		mA
		$V_{OUT} = \pm 3.4\text{V}$	$\pm 5\text{V}$	6.8	7.6		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	30	45		mA
SR	Slew Rate	$A_V = -1$, $R_L = 5\text{k}$ (Note 3)	$\pm 15\text{V}$	120	200		V/ μs
			$\pm 5\text{V}$	30	50		V/ μs
	Full-Power Bandwidth	10V Peak (Note 4) 3V Peak (Note 4)	$\pm 15\text{V}$		3.2		MHz
			$\pm 5\text{V}$		2.6		MHz
GBW	Gain Bandwidth	$f = 200\text{kHz}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	2.0	3.0		MHz
			$\pm 5\text{V}$	1.8	2.7		MHz
			$\pm 2.5\text{V}$		2.5		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10% to 90%, 0.1V	$\pm 15\text{V}$		46		ns
			$\pm 5\text{V}$		53		ns
	Overshoot	$A_V = 1$, 0.1V	$\pm 15\text{V}$		13		%
			$\pm 5\text{V}$		16		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V	$\pm 15\text{V}$		41		ns
			$\pm 5\text{V}$		52		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		700		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		1250		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		950		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		1400		ns
R_O	Output Resistance	$A_V = 1$, $f = 20\text{kHz}$	$\pm 15\text{V}$		1.5		Ω
I_{SHDN}	Shutdown Input Current	$SHDN = V_{EE} + 0.1\text{V}$	$\pm 15\text{V}$	-10			μA
		$SHDN = V_{CC}$	$\pm 15\text{V}$	0.1	2		μA
I_S	Supply Current	$SHDN = V_{EE} + 0.1\text{V}$	$\pm 15\text{V}$	250	330		μA
			$\pm 5\text{V}$	220	300		μA
			$\pm 5\text{V}$	10			μA

$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$			0.8	mV
			$\pm 5\text{V}$			0.8	mV
			$\pm 2.5\text{V}$			1.0	mV
	Input V_{OS} Drift	(Note 5)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$		3	8	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			20	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$			75	nA

ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	78			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	77			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	67			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V to } \pm 15\text{V}$		89			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 5\text{k}$	$\pm 15\text{V}$	25			V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	20			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 5\text{k}$	$\pm 5\text{V}$	20			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	10			V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 5\text{k}$	$\pm 2.5\text{V}$	15			V/mV
V_{OUT}	Output Swing	$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.4			$\pm \text{V}$
		$R_L = 2\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.3			$\pm \text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 15\text{V}$	12.0			$\pm \text{V}$
		$R_L = 1\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.4			$\pm \text{V}$
		$R_L = 500\Omega$, $V_{IN} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.3			$\pm \text{V}$
		$R_L = 5\text{k}$, $V_{IN} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.2			$\pm \text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 12\text{V}$	$\pm 15\text{V}$	12.0			mA
		$V_{OUT} = \pm 3.3\text{V}$	$\pm 5\text{V}$	6.6			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	24			mA
SR	Slew Rate	$A_V = -1$, $R_L = 5\text{k}$ (Note 3)	$\pm 15\text{V}$	100			V/ μs
			$\pm 5\text{V}$	21			V/ μs
GBW	Gain Bandwidth	$f = 200\text{kHz}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	1.8			MHz
			$\pm 5\text{V}$	1.6			MHz
I_{SHDN}	Shutdown Input Current	$SHDN = V_{EE} + 0.1\text{V}$	$\pm 15\text{V}$		-20		μA
		$SHDN = V_{CC}$	$\pm 15\text{V}$			3	μA
I_S	Supply Current	$SHDN = V_{EE} + 0.1\text{V}$	$\pm 15\text{V}$			380	μA
			$\pm 5\text{V}$			355	μA
			$\pm 5\text{V}$		20		μA

 $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted (Note 6).

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$			1.0	mV
			$\pm 5\text{V}$			1.0	mV
			$\pm 2.5\text{V}$			1.2	mV
	Input V_{OS} Drift	(Note 5)	$\pm 2.5\text{V to } \pm 15\text{V}$		3	8	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V to } \pm 15\text{V}$			30	nA
I_B	Input Bias Current		$\pm 2.5\text{V to } \pm 15\text{V}$			100	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	76			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	76			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V to } \pm 15\text{V}$		87			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 5\text{k}$	$\pm 15\text{V}$	20			V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 5\text{k}$	$\pm 5\text{V}$	15			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 2\text{k}$	$\pm 5\text{V}$	10			V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	8			V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 5\text{k}$	$\pm 2.5\text{V}$	10			V/mV

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted (Note 6).

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 5\text{k}$, $V_{\text{IN}} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.3			$\pm\text{V}$
		$R_L = 2\text{k}$, $V_{\text{IN}} = \pm 10\text{mV}$	$\pm 15\text{V}$	13.2			$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{\text{IN}} = \pm 10\text{mV}$	$\pm 15\text{V}$	10.0			$\pm\text{V}$
		$R_L = 1\text{k}$, $V_{\text{IN}} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.3			$\pm\text{V}$
		$R_L = 500\Omega$, $V_{\text{IN}} = \pm 10\text{mV}$	$\pm 5\text{V}$	3.2			$\pm\text{V}$
		$R_L = 5\text{k}$, $V_{\text{IN}} = \pm 10\text{mV}$	$\pm 2.5\text{V}$	1.1			$\pm\text{V}$
I_{OUT}	Output Current	$V_{\text{OUT}} = \pm 10\text{V}$	$\pm 15\text{V}$	10.0			mA
		$V_{\text{OUT}} = \pm 3.2\text{V}$	$\pm 5\text{V}$	6.4			mA
I_{SC}	Short-Circuit Current	$V_{\text{OUT}} = 0\text{V}$, $V_{\text{IN}} = \pm 3\text{V}$	$\pm 15\text{V}$	20			mA
SR	Slew Rate	$A_V = -1$, $R_L = 5\text{k}$ (Note 3)	$\pm 15\text{V}$	50			$\text{V}/\mu\text{s}$
			$\pm 5\text{V}$	15			$\text{V}/\mu\text{s}$
GBW	Gain Bandwidth	$f = 200\text{kHz}$, $R_L = 10\text{k}$	$\pm 15\text{V}$	1.6			MHz
			$\pm 5\text{V}$	1.4			MHz
I_{SHDN}	Shutdown Input Current	$\text{SHDN} = V_{\text{EE}} + 0.1\text{V}$	$\pm 15\text{V}$		-30		μA
		$\text{SHDN} = V_{\text{CC}}$	$\pm 15\text{V}$			5	μA
I_{S}	Supply Current		$\pm 15\text{V}$			390	μA
			$\pm 5\text{V}$			380	μA
		$\text{SHDN} = V_{\text{EE}} + 0.1\text{V}$	$\pm 5\text{V}$		30		μA

Note 1: Differential inputs of $\pm 10\text{V}$ are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 3: Slew rate is measured between $\pm 8\text{V}$ on the output with $\pm 12\text{V}$ input for $\pm 15\text{V}$ supplies and $\pm 2\text{V}$ on the output with $\pm 3\text{V}$ input for $\pm 5\text{V}$ supplies.

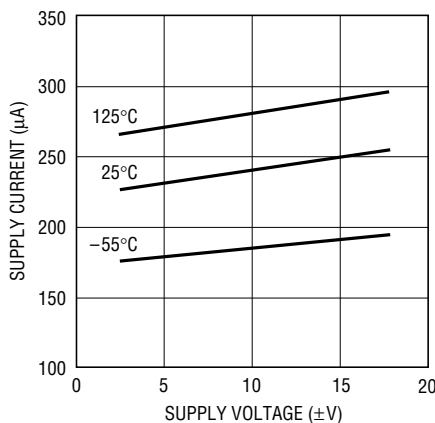
Note 4: Full-power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = (\text{Slew Rate})/2\pi V_p$.

Note 5: This parameter is not 100% tested.

Note 6: The LT1351 is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and at 85°C . Guaranteed I grade parts are available; consult factory.

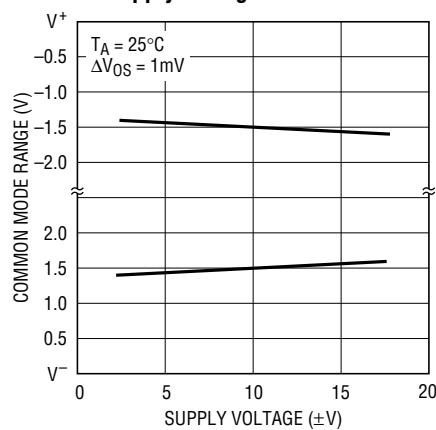
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



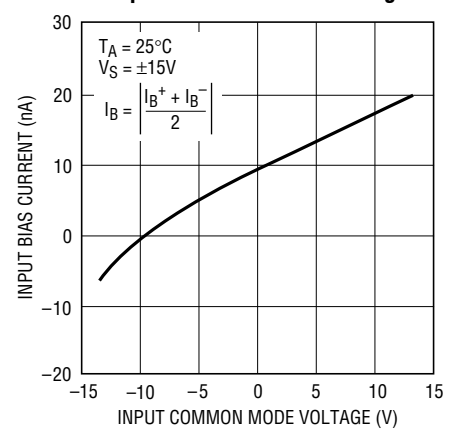
1351 G01

Input Common Mode Range vs Supply Voltage



1351 G02

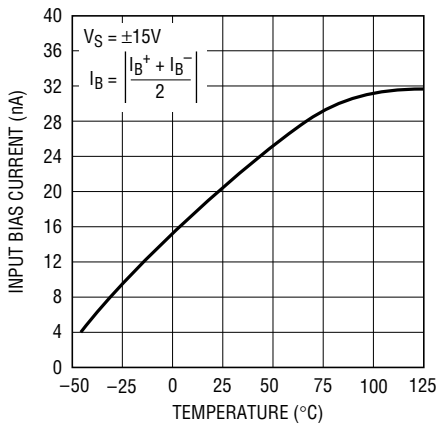
Input Bias Current vs Input Common Mode Voltage



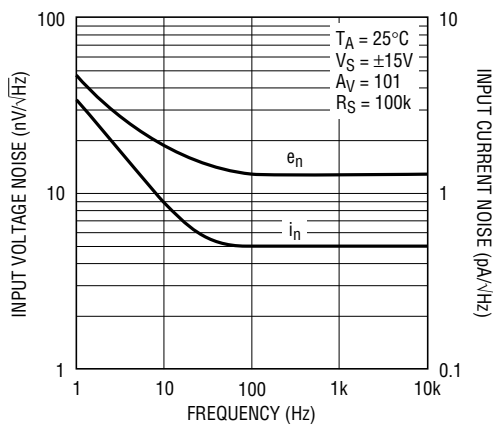
1351 G03

TYPICAL PERFORMANCE CHARACTERISTICS

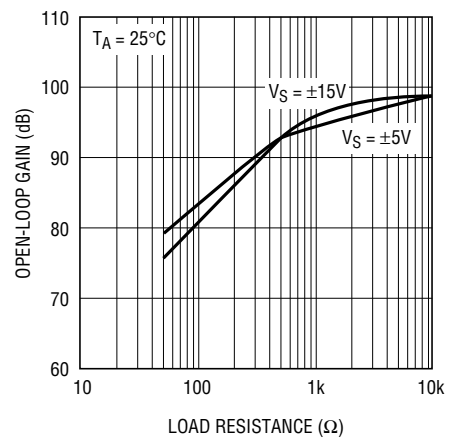
Input Bias Current vs Temperature



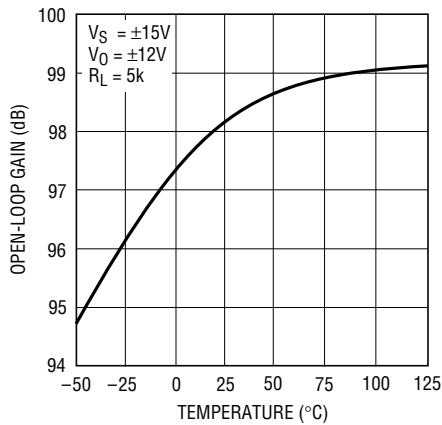
Input Noise Spectral Density



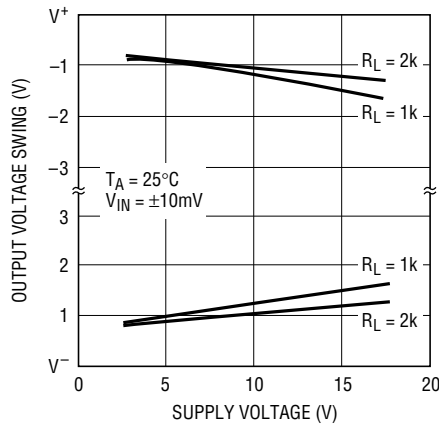
Open-Loop Gain vs Resistive Load



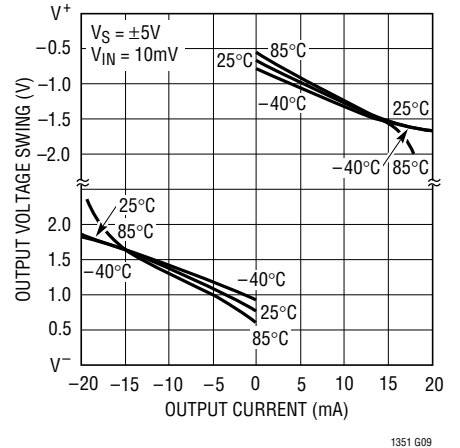
Open-Loop Gain vs Temperature



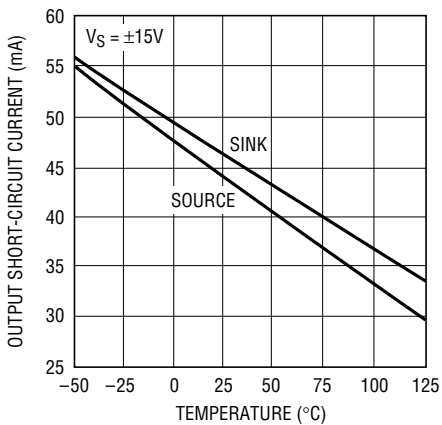
Output Voltage Swing vs Supply Voltage



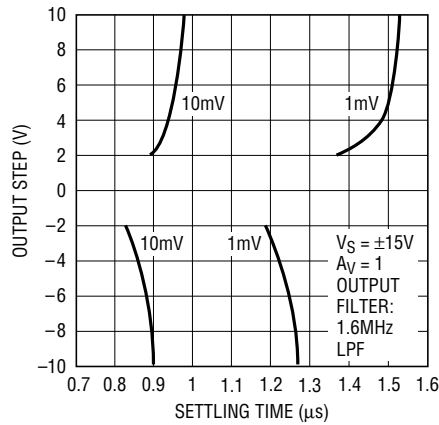
Output Voltage Swing vs Load Current



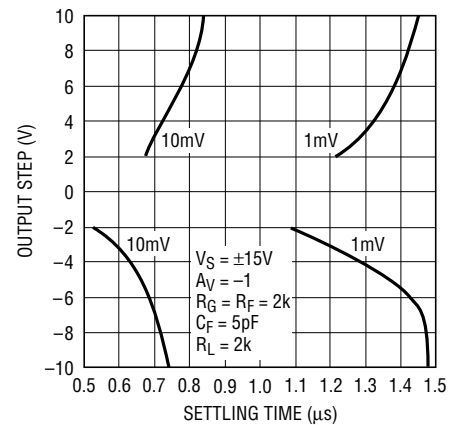
Output Short-Circuit Current vs Temperature



Settling Time vs Output Step (Noninverting)

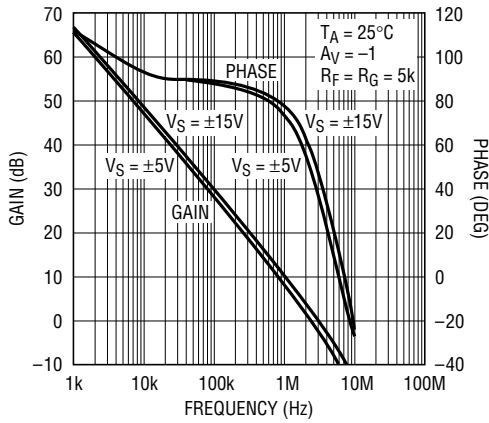


Settling Time vs Output Step (Inverting)



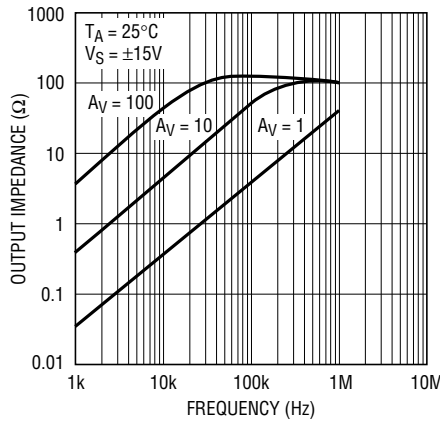
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase vs Frequency



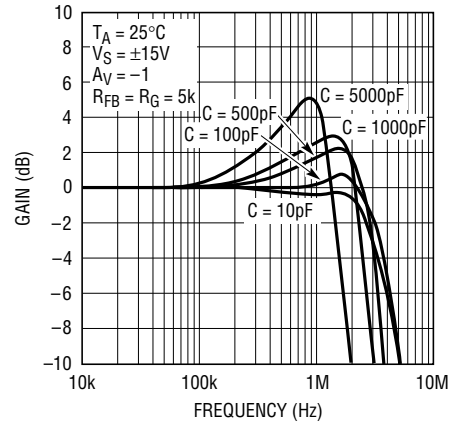
1351 G13

Output Impedance vs Frequency



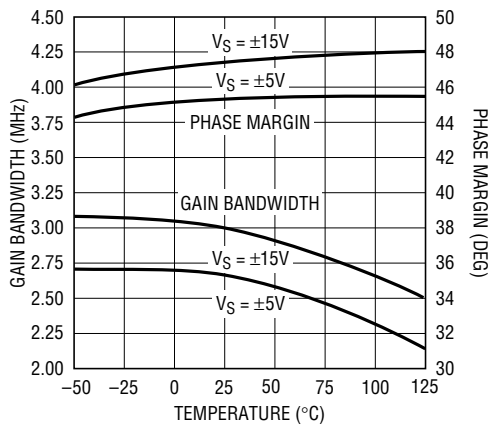
1351 G14

Frequency Response vs Capacitive Load



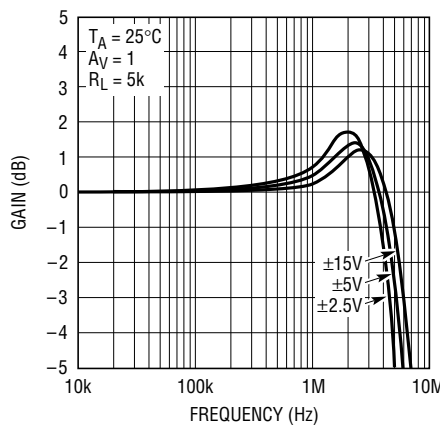
1351 G15

Gain Bandwidth and Phase Margin vs Temperature



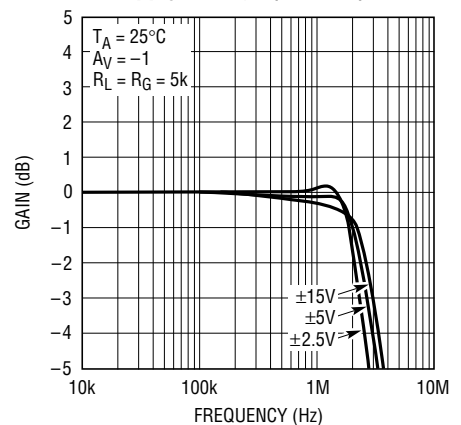
1351 G16

Frequency Response vs Supply Voltage ($A_V = 1$)



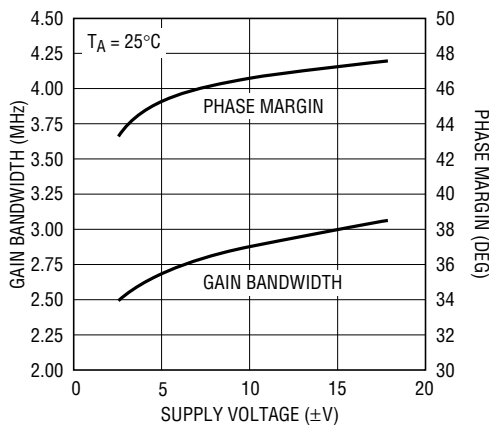
1351 G17

Frequency Response vs Supply Voltage ($A_V = -1$)



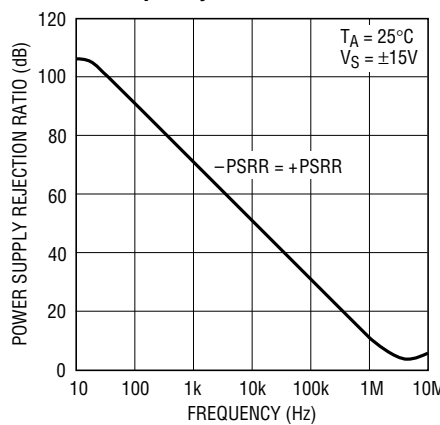
1351 G18

Gain Bandwidth and Phase Margin vs Supply Voltage



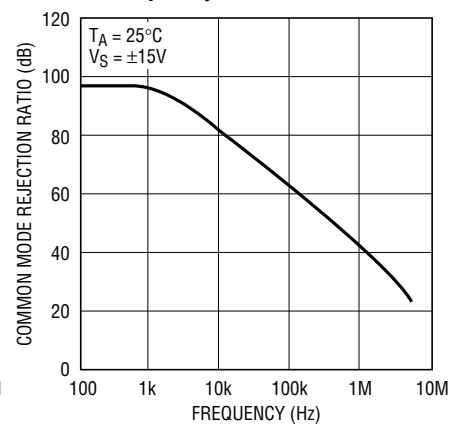
1351 G19

Power Supply Rejection Ratio vs Frequency



1351 G20

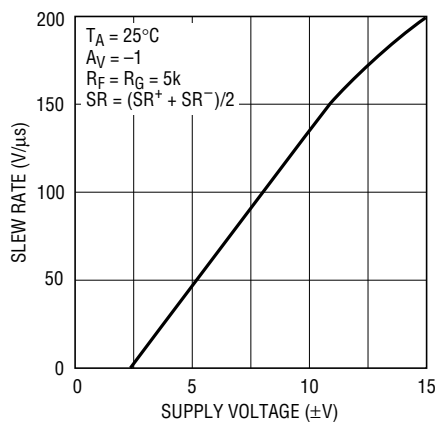
Common Mode Rejection Ratio vs Frequency



1351 G21

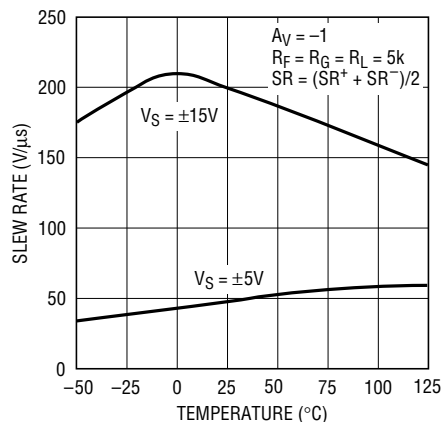
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Supply Voltage



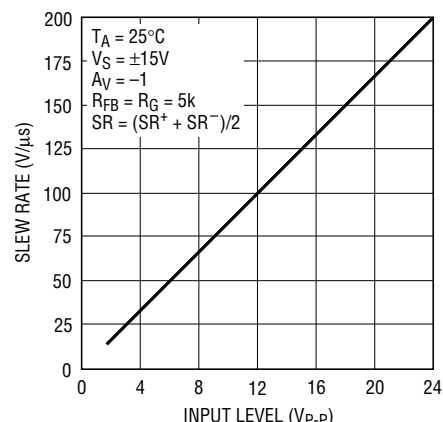
1351 G22

Slew Rate vs Temperature



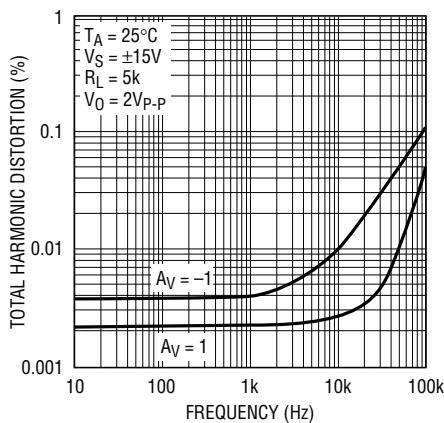
1351 G23

Slew Rate vs Input Level



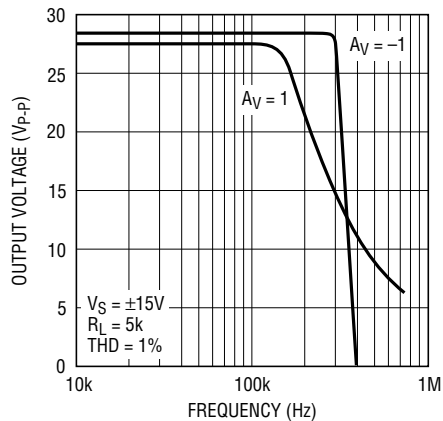
1351 G24

Total Harmonic Distortion vs Frequency



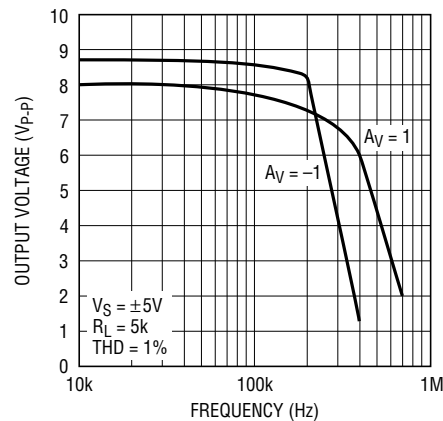
1351 G25

Undistorted Output Swing vs Frequency (±15V)



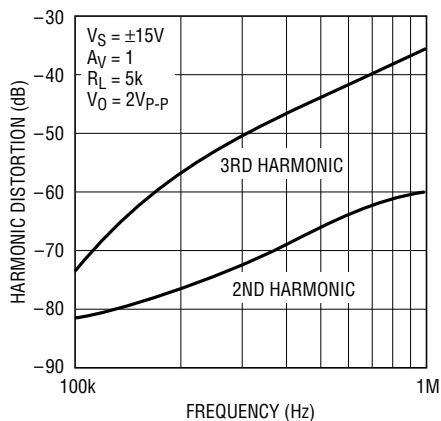
1351 G26

Undistorted Output Swing vs Frequency (±5V)



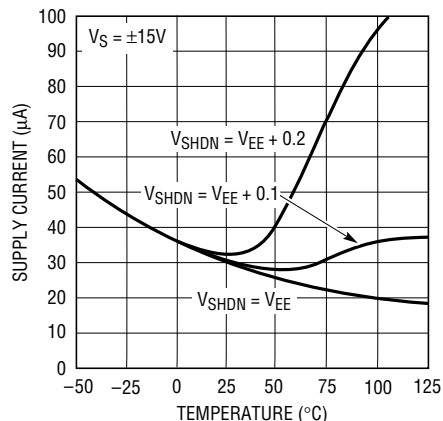
1351 G27

2nd and 3rd Harmonic Distortion vs Frequency



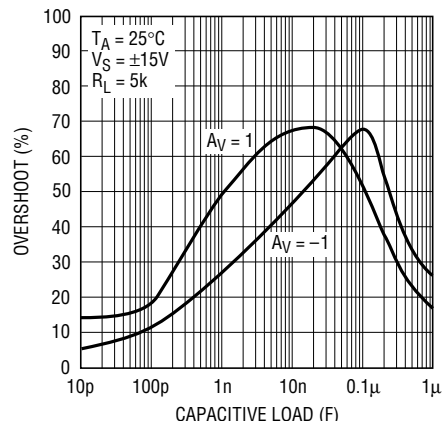
1351 G28

Shutdown Supply Current vs Temperature



1351 G29

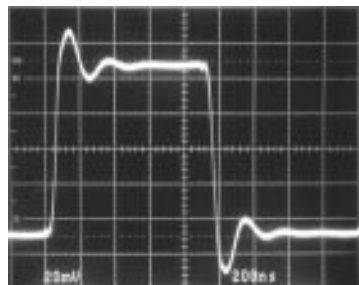
Capacitive Load Handling



1351 G30

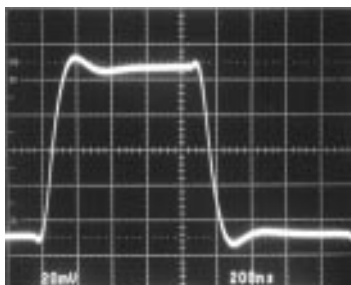
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient
($A_V = 1$)



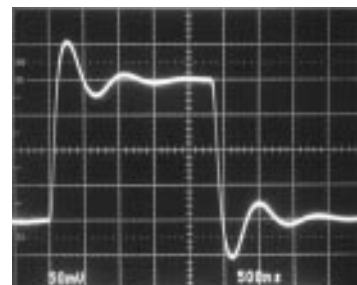
1351 G31

Small-Signal Transient
($A_V = -1$)



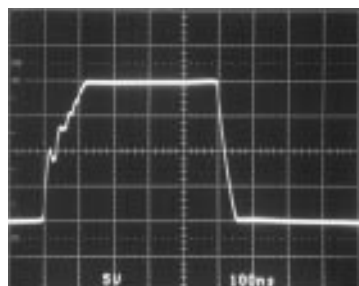
1351 G32

Small-Signal Transient
($A_V = -1$, $C_L = 1000\text{pF}$)



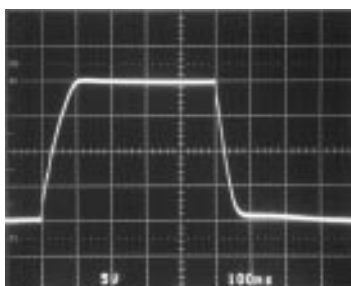
1351 G33

Large-Signal Transient
($A_V = 1$)



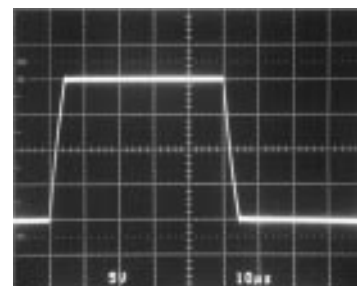
1351 G34

Large-Signal Transient
($A_V = -1$)



1351 G35

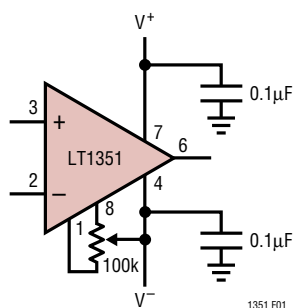
Large-Signal Transient
($A_V = 1$, $C_L = 10,000\text{pF}$)



1351 G36

APPLICATIONS INFORMATION

The LT1351 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1351 is shown in Figure 1.



1351 F01

Figure 1. Offset Nulling

Layout and Passive Components

The LT1351 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths and RF-quality bypass capacitors ($0.01\mu\text{F}$ to $0.1\mu\text{F}$). For high drive current applications use low ESR bypass capacitors ($1\mu\text{F}$ to $10\mu\text{F}$ tantalum). For details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or even oscillations. For feedback resistors greater than 10k , a parallel capacitor of value, $C_F > (R_G)(C_{IN}/R_F)$ should be used to cancel the input pole and optimize dynamic performance. For applications where the DC

APPLICATIONS INFORMATION

noise gain is one and a large feedback resistor is used, C_F should be greater than or equal to C_{IN} . An example would be an I-to-V converter as shown in the Typical Applications section.

Capacitive Loading

The LT1351 is stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Graphs of Frequency Response vs Capacitive Load, Capacitive Load Handling and the transient response photos clearly show these effects.

Input Considerations

Each of the LT1351 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. *The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs.* Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Shutdown

The LT1351 has a Shutdown pin for conserving power. When this pin is open or 2V above the negative supply the part operates normally. When pulled down to V^- the supply current will drop to about 10 μ A. The current out of the Shutdown pin is also typically 10 μ A. In shutdown the amplifier output is not isolated from the inputs so the LT1351 cannot be used in multiplexing applications using the shutdown feature.

A level shift application is shown in the Typical Applications section so that a ground-referenced logic signal can control the Shutdown pin.

Circuit Operation

The LT1351 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic.

The inputs are buffered by complementary NPN and PNP emitter followers which drive R1, a 1k resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node and compensation capacitor C_T . Complementary followers form an output stage which buffers the gain node from the load. The output devices Q19 and Q22 are connected to form a composite PNP and composite NPN.

The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship.

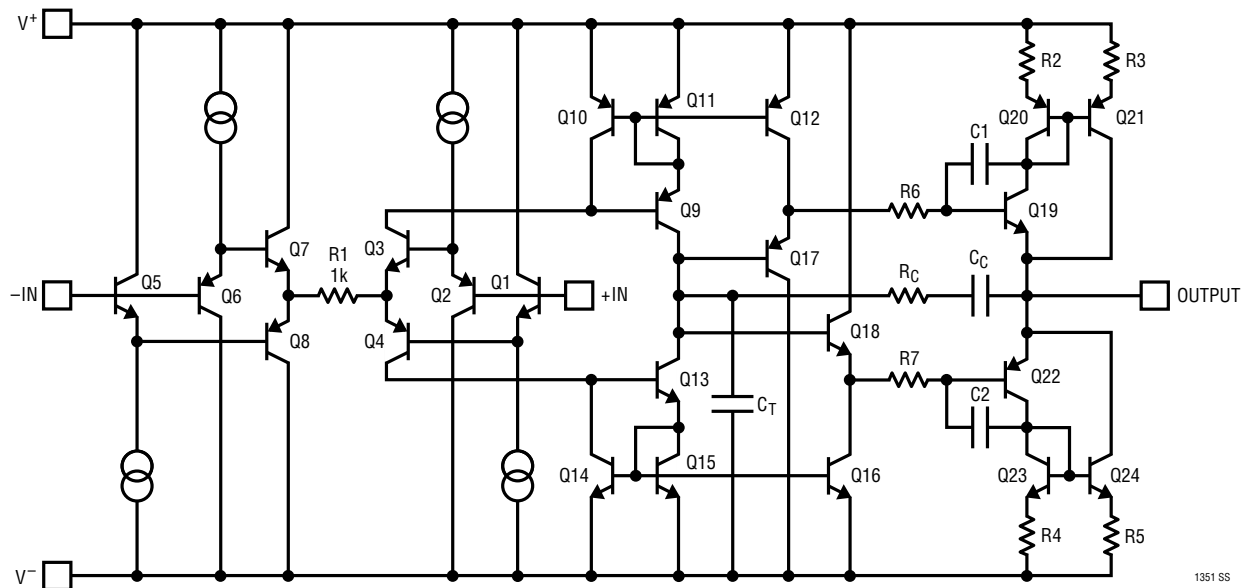
Capacitive load compensation is provided by the R_C , C_C network which is bootstrapped across the output stage. When the amplifier is driving a light load the network has no effect. When driving a capacitive load (or a low value

APPLICATIONS INFORMATION

resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier and a zero is created by the RC combination, both of

which improve the phase margin. The design ensures that even for very large load capacitances the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

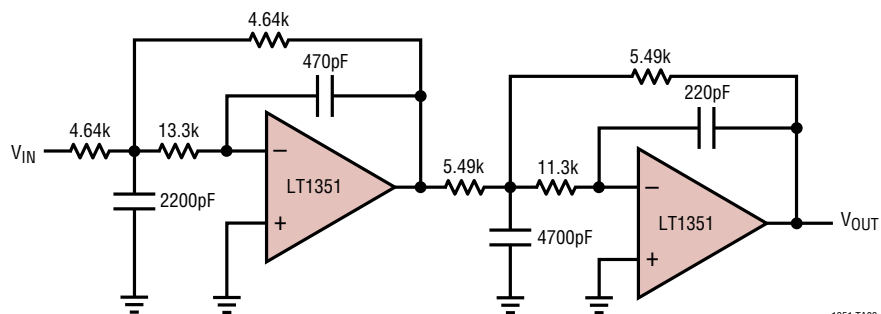
SIMPLIFIED SCHEMATIC



1351 SS

TYPICAL APPLICATIONS

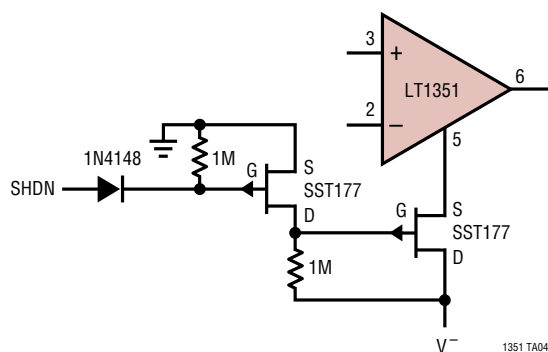
20kHz, 4th Order Butterworth Filter



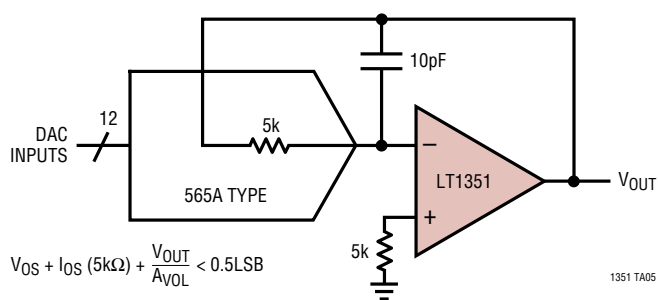
1351 TA03

TYPICAL APPLICATIONS

Shutdown Circuit



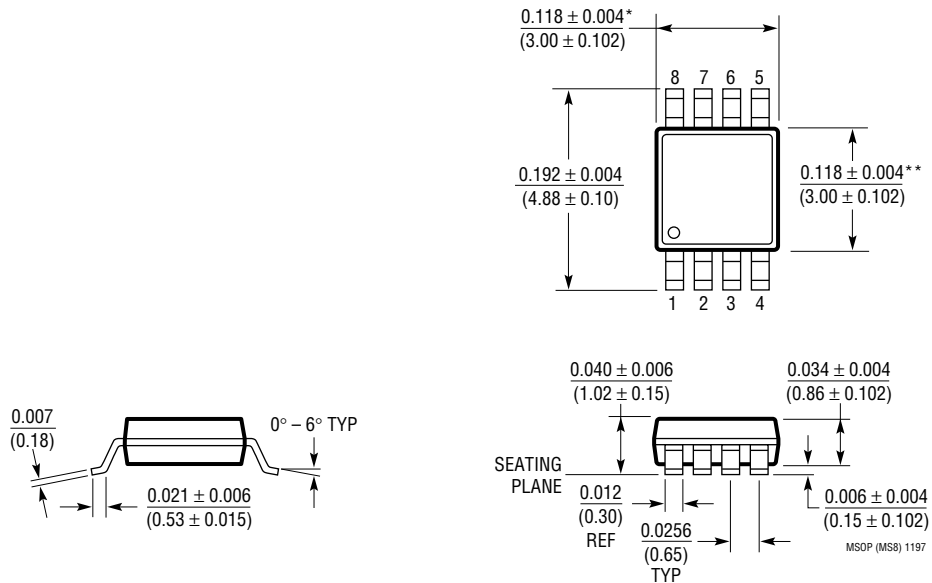
DAC I-to-V Converter



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package 8-Lead Plastic MSOP (LTC DWG # 05-08-1660)



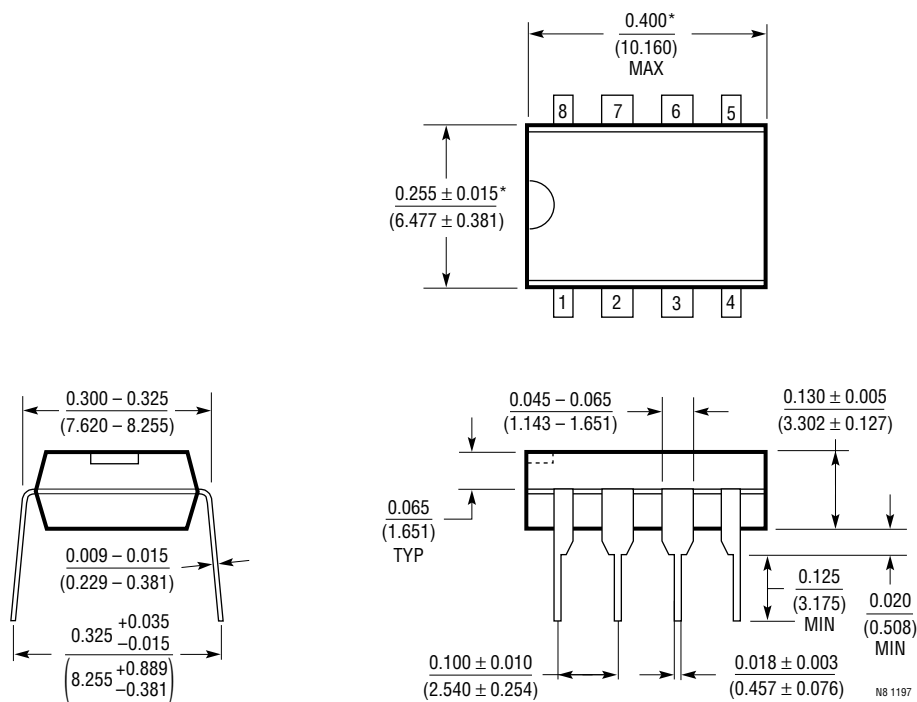
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)

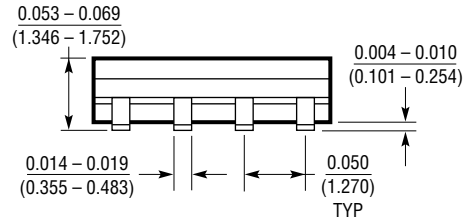
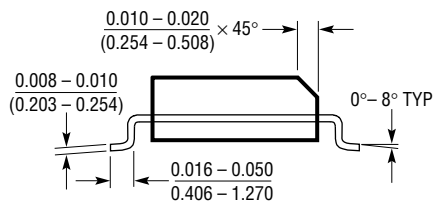
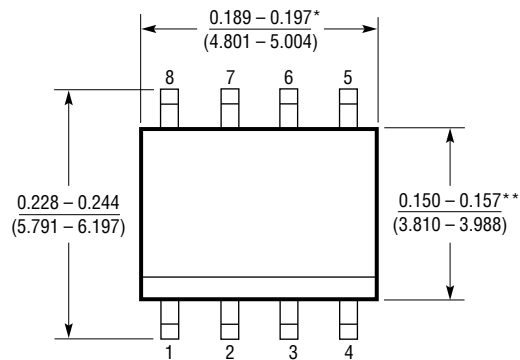


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



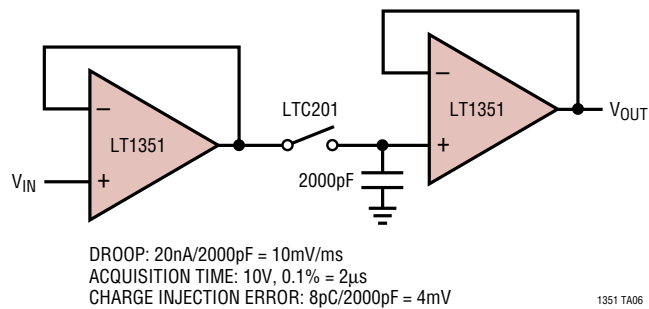
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

TYPICAL APPLICATION

Low Power Sample-and-Hold



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1352/LT1353	Dual/Quad 250μA, 3MHz, 200V/μs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1354	1mA, 12MHz, 400V/μs Op Amp	Good DC Precision, Stable with All Capacitive Loads