



Dual Decade Counter With A and B Inputs

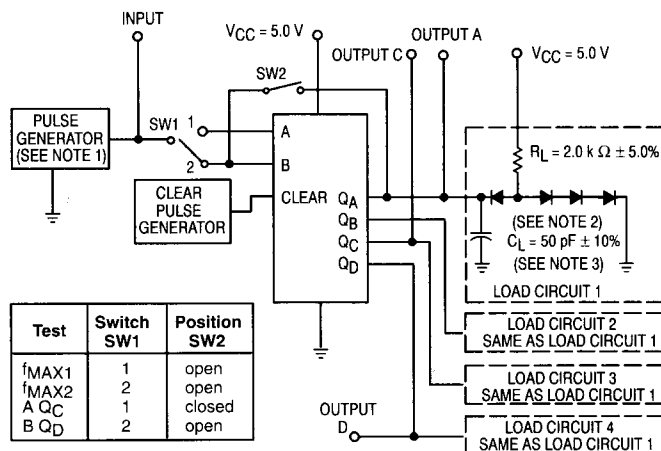
ELECTRICALLY TESTED PER:
MIL-M-38510/32701

The 54LS390 contains a pair of high-speed 4-stage ripple counters. Each half of the 'LS390 is partitioned into a divide-by-two section and divide-by-five section, with separate clock input for each section. The two sections can be connected to count 8.4.2.1 BCD code or they can count in a binary sequence to provide a square wave (50% duty cycle) at the final output.

In the 'LS390 the flip-flops are triggered by a HIGH-to-LOW transition A and B inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Version of the 'LS290
- Separate Clocks Allowing $\div 2$, $\div 2.5$, $\div 5$
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High-Speed Termination Effects

TEST CIRCUIT



NOTES:

- The input pulse generator has the following characteristics:
 $V_{gen} = 3.0 V$, $t_r \leq 6.0 ns$, $t_f \leq 6.0 ns$, $t_p = 0.5 \mu s$, $PRR \leq 1.0 MHz$, $t_{p(clear)} = 25 ns$, and $Z_{OUT} \approx 50 \Omega$.
- All diodes are 1N3064 or equivalent.
- $C_L = 50 pF \pm 10\%$, including scope probe, wiring and stray capacitance.
- Voltage measurements are to be made with respect to network ground terminal.
- f_{MAX}: $t_r = t_f \leq 6.0 ns$.
- Terminal conditions (pins not designated may be high $\geq 2.0 V$, low $\leq 0.7 V$, or open).

Military 54LS390



AVAILABLE AS:

- 1) JAN: JM38510/32701BXA
- 2) SMD: 7802601
- 3) 883: 54LS390/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
A ₁	1	1	2	V _{CC}
CLR ₁	2	2	3	V _{CC}
QA ₁	3	3	4	OPEN
B ₁	4	4	5	V _{CC}
QB ₁	5	5	7	OPEN
QC ₁	6	6	8	OPEN
QD ₁	7	7	9	OPEN
GND	8	8	10	GND
QD ₂	9	9	12	OPEN
QC ₂	10	10	13	OPEN
QB ₂	11	11	14	OPEN
B ₂	12	12	15	V _{CC}
QA ₂	13	13	17	OPEN
CLR ₂	14	14	18	V _{CC}
A ₂	15	15	19	V _{CC}
V _{CC}	16	16	20	V _{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE ($\div 5$)

Count	Outputs		
	Q _D	Q _C	Q _B
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

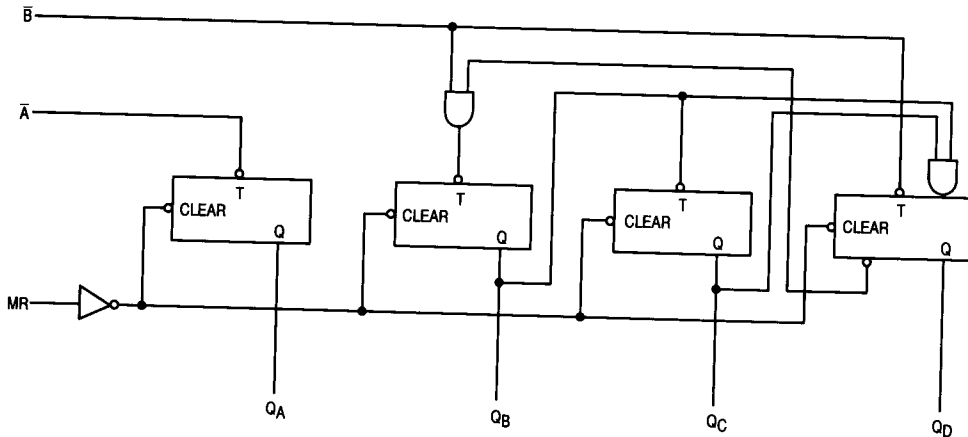
FUNCTIONAL DESCRIPTION

Each half of the 54LS390 contains a + 5 section that is independent except for the common MR function. The + 5 section operates in 4.2.1 binary sequence, as shown in the + 5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a + 10 function having a 50% duty cycle output, connect the input signal to (B) and connect the Q_C output to the (A) input; the Q_A output provides the desired 50% duty cycle output. If the input frequency is connected to (A) and the Q_A output is connected to (B), a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals diverted from combinations of 'LS390 outputs are also subject to decoding spikes. A HIGH signal on MR (CLEAR) forces all outputs LOW and prevents counting.

TRUTH TABLE (BCD)				
Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

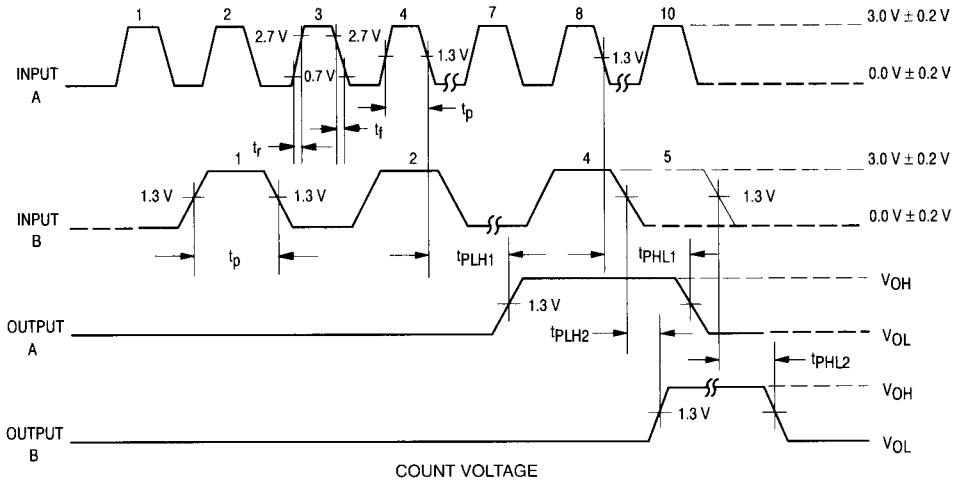
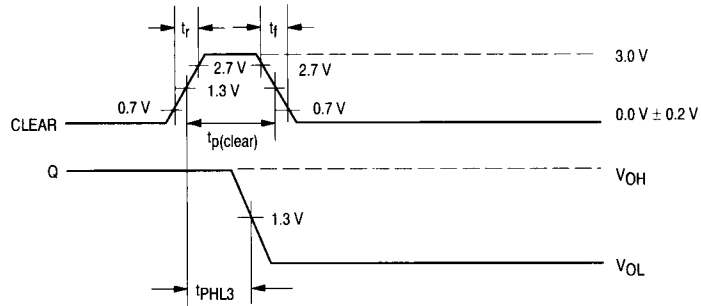
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



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WAVEFORMS



54LS390

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = – 0.4 mA, V _{IN} = (See Note 1), other input = (See Note 2).
V _{OL}	Logical “0” Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IN} = 2.0 V, other input is open, I _{QA} = 6.4 mA.
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} (CLR) = 2.7 V, other inputs are open.
I _{IH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IH} (A) = 2.7 V, other inputs are open.
I _{IH}	Logical “1” Input Current		200		200		200	μA	V _{CC} = 5.5 V, V _{IH} (B) = 2.7 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} (CLR) = 5.5 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		200		200		200	μA	V _{CC} = 5.5 V, V _{IHH} (A) = 5.5 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		400		400		400	μA	V _{CC} = 5.5 V, V _{IHH} (B) = 5.5 V, other inputs are open.
I _{IL}	Logical “0” Input Current	– 0.15	– 0.38	– 0.15	– 0.38	– 0.15	– 0.38	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V (CLR), other inputs are open.
I _{IL}	Logical “0” Input Current	– 0.35	– 1.6	– 0.35	– 1.6	– 0.35	– 1.6	mA	V _{CC} = 5.5 V, V _{IN} (A) = 0.4 V, other input is GND.
I _{IL}	Logical “0” Input Current	– 0.6	– 2.4	– 0.6	– 2.4	– 0.6	– 2.4	mA	V _{CC} = 5.5 V, V _{IN} (B) = 0.4 V, other input is GND.
I _{OS}	Short Circuit Output Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V _{CC} = 5.5 V, CLR = (See Note 2), A = (See Note 1), B = (See Notes 1, 3, 4), V _{OUT} = GND.
I _{CC}	Power Supply Current Off		26		26		26	mA	V _{CC} = 5.5 V, V _{IN} = (See Note 2), other inputs are GND.
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

NOTES:

1. Apply  2.0 V MIN/5.5 V MAX } prior to test after clear pulse.
0.0 V ± 0.2 V
2. Apply  2.0 V MIN/5.5 V MAX } prior to test
0.0 V ± 0.2 V
3. Apply 2 pulses prior to test after clear pulse (See Note 1.)
4. Apply 4 pulses prior to test after clear pulse (See Note 1.)

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output A to Q _n	2.0 —	65 60	2.0 —	84 79	2.0 —	84 79	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output A to Q _n	2.0 —	65 60	2.0 —	84 79	2.0 —	84 79	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output A to Q _n	2.0 —	26 20	2.0 —	34 29	2.0 —	34 29	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output B to Q _n	2.0 —	26 20	2.0 —	34 29	2.0 —	34 29	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
t _{PHL3} t _{PHL3}	Propagation Delay /Data-Output CLR to Q _n	2.0 —	44 39	2.0 —	56 51	2.0 —	56 51	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
f _{MAX1} f _{MAX1}	Maximum Clock Frequency (A-Q _A)	25 25		25		25		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
f _{MAX1} f _{MAX1}	Maximum Clock Frequency (B-Q _B)	12.5 12.5		12.5		12.5		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.

NOTE:

The limit specified for C_L = 15 pF is guaranteed but not tested.