

For Fan Motor Driver

Fractional Pulse Rate Converter (Conversion Ratio, 21:12)

BU6823G

General Description

This IC converts the input clock signal by 12/21 ratio and output it. It is the best when need to output the FG signal equivalent to the 8-pole motor when using the 14-pole motor with the FG signal generated from the Hall sensor signals.

Features

- 5V Power Supply
- Conversion Ratio, 21:12
- Input Frequency Range: 5 Hz to 5 kHz
- Small Package, SSOP5

Applications

- Air Conditioners, Air Purifiers, Water Pumps, Dishwashers and Washing Machines

Key Specifications

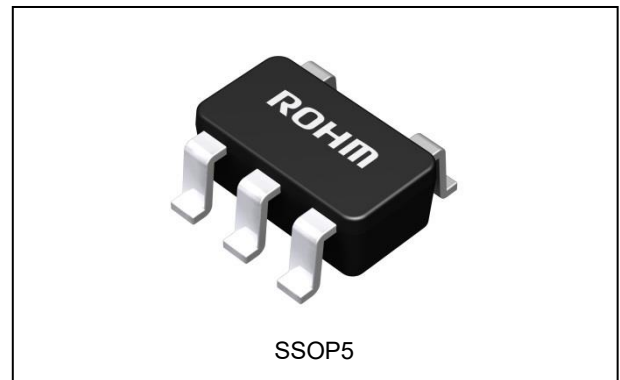
- | | |
|---------------------------------|---------------|
| ■ Input Frequency Range: | 5 Hz to 5 kHz |
| ■ Driver Output Current: | ±5 mA (Max) |
| ■ Maximum Junction Temperature: | +125 °C |

Package

SSOP5

W(Typ) x D(Typ) x H(Max)

2.90 mm x 2.80 mm x 1.25 mm



Typical Application Circuit

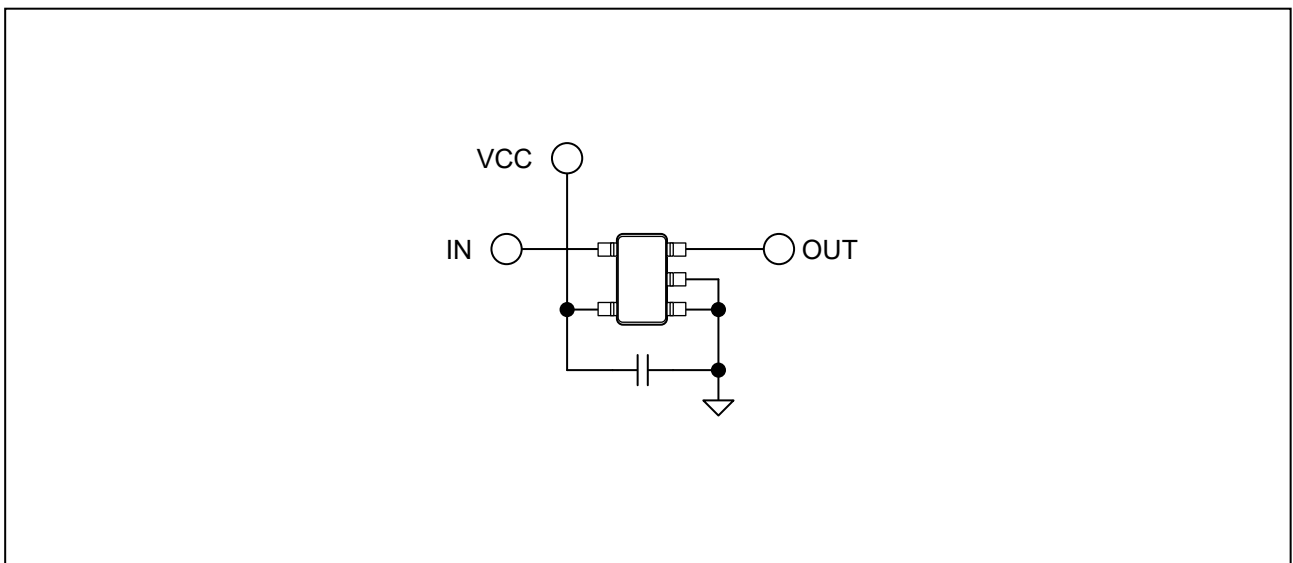


Figure 1. Application Circuit Example

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Block Diagram and Pin Configuration

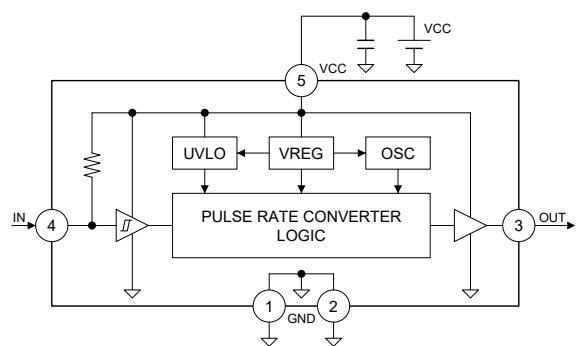


Figure 2. Block Diagram

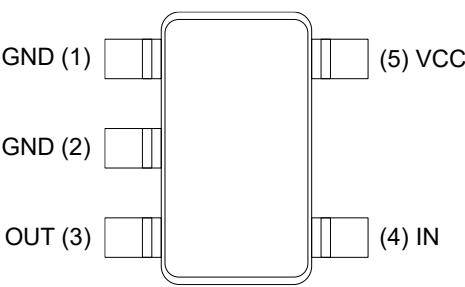


Figure 3. Pin Configuration (Top View)

Pin Description

Pin	Name	Function	Pin	Name	Function
1	GND	Ground	5	VCC	Power supply
2	GND	Ground	-	-	-
3	OUT	Converted signal output	4	IN	Signal input pin

Description of Blocks

1. Pulse Rate Conversion Logic

It divides the input clock signal by 12/21, and output the converted signal. Signal processing is performed with reference to the fall edge of the input signal.
In addition, when the input signal frequency is out of range at signal conversion and it is judged to be too low frequency, the internal logic circuit outputs no conversion signal (pass through). On the other hand, when it is judged to be too high frequency, it outputs 35 kHz (Typ) signal.

2. Signal Input Pin

The IN pin is pulled up to VCC internally by a 500 kΩ (Typ) resistor. When using in conjunction with the open-collector / drain output, the IN pin can be connected directly.

3. Signal Output Pin

The OUT pin is CMOS output. When connecting to the base pin of a bipolar transistor, please do not exceed the rated current by taking countermeasure such as inserting a current limiting resistor.

4. Under Voltage Lock Out (UVLO) Circuit

To secure the lowest power supply voltage necessary to operate the internal circuit, and to prevent under voltage malfunctions, an UVLO circuit is built into the internal circuit. When the power supply voltage falls to V_{UVL} and below, the internal circuit forces output low. When the voltage rises to V_{UVH} and above, the UVLO circuit ends the lock out operation and returns to normal operation.

Absolute Maximum Ratings (Tj=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{CC}	7.0 ^(Note 1)	V
Input Voltage	V _{IN}	-0.3 to V _{CC}	V
Maximum Input Frequency	f _{INMAX}	10	kHz
Driver Outputs	I _{OMAX}	±5 ^(Note 1)	mA
Storage Temperature Range	T _{stg}	-55 to +125	°C
Maximum Junction Temperature	T _{jmax}	125	°C

(Note) All voltages are with respect to ground unless otherwise specified.

(Note 1) Do not exceed ASO.

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
SSOP5				
Junction to Ambient	θ _{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	40	30	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions (T_j=25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Junction Temperature	T _j	-40	-	+110	°C
Input Frequency Range	f _{IN}	5	-	5k	Hz
Input Signal Duty Range	F _{DUTY}	15	-	85	%

(Note) All voltages are with respect to ground unless otherwise specified.

Electrical Characteristics (Unless otherwise specified V_{CC}=5 V and T_j=25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply						
Quiescence Current	I _{CCQ}	0.3	0.46	1.0	mA	V _{IN} =0 V
Input						
Input Bias Current	I _{IN}	6	10	15	μA	V _{IN} =0 V
Input High Voltage	V _{INH}	2.0	-	V _{CC}	V	
Input Low Voltage	V _{INL}	0	-	0.8	V	
Output						
Output High Voltage	V _{OUTH}	V _{CC} -0.40	V _{CC} -0.08	V _{CC}	V	I _O =-2 mA
Output Low Voltage	V _{OUTL}	0	0.02	0.30	V	I _O =2 mA
Under Voltage Lock Out						
Release Voltage	V _{UVH}	3.3	3.6	3.9	V	
Lockout Voltage	V _{UVL}	2.7	3.0	3.3	V	

(Note) All voltages are with respect to ground unless otherwise specified.

Typical Performance Curves (Reference Data)

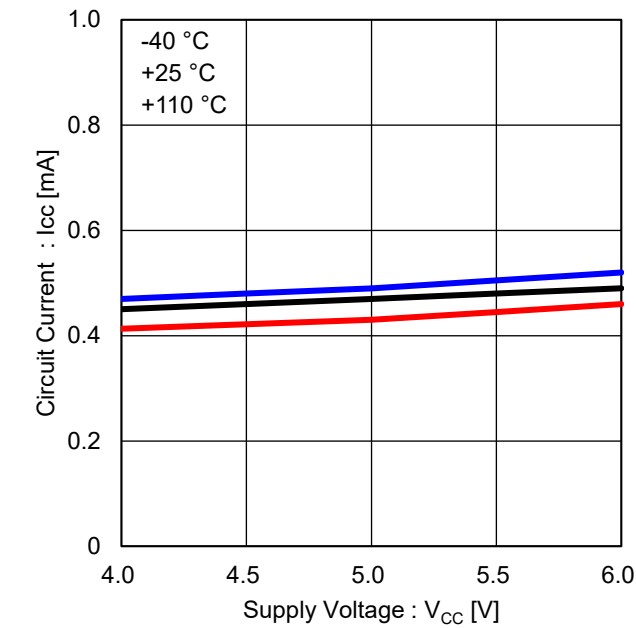


Figure 4. Operating Current
($I_N = 1\text{kHz}$)

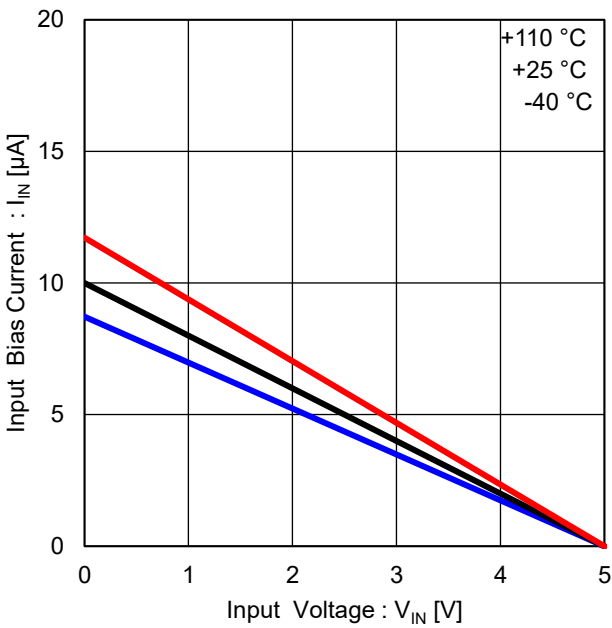


Figure 5. Input Bias Current

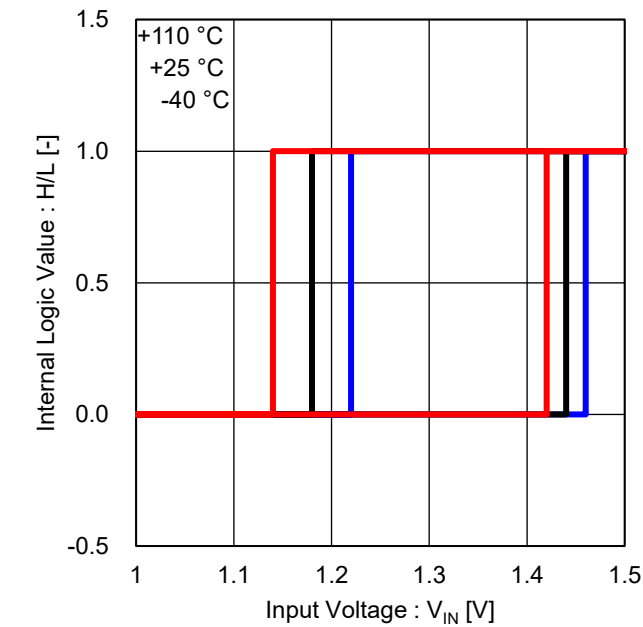


Figure 6. Input Threshold Voltage

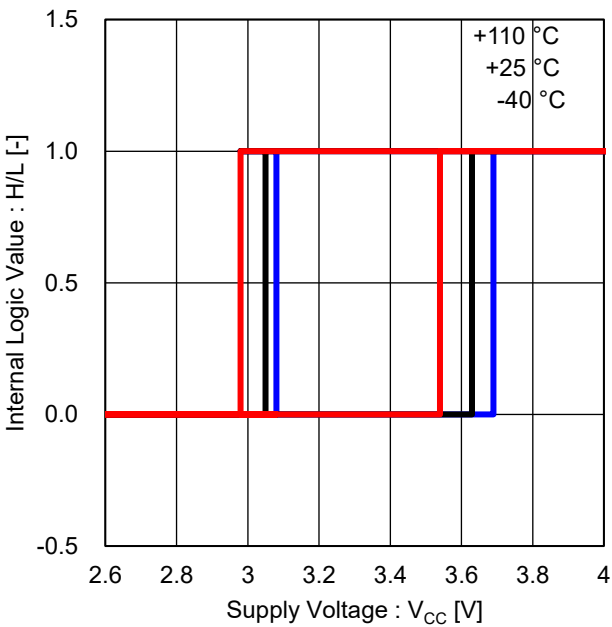


Figure 7. Under Voltage Lock Out

Typical Performance Curves (Reference Data) - continued

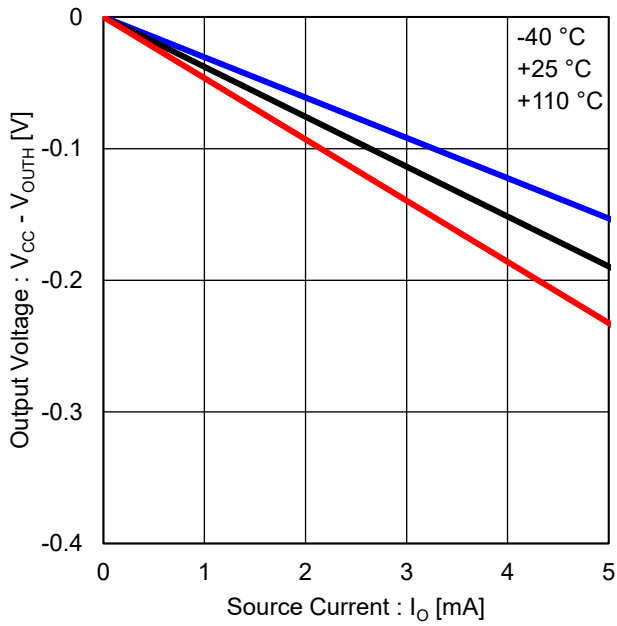


Figure 8. Output High Voltage

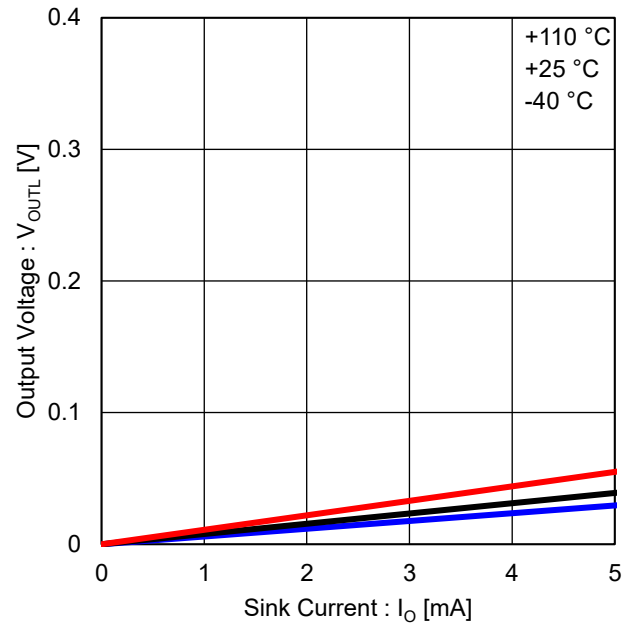


Figure 9. Output Low Voltage

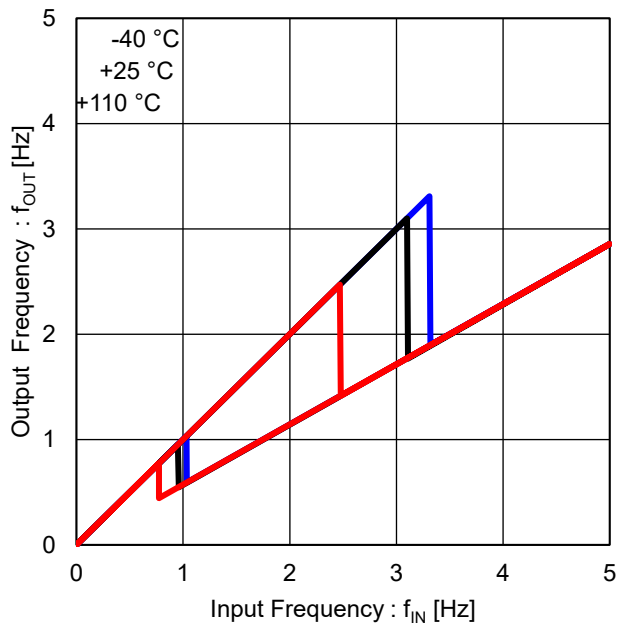


Figure 10. Output vs Input Frequency Characteristics (Low Frequency)

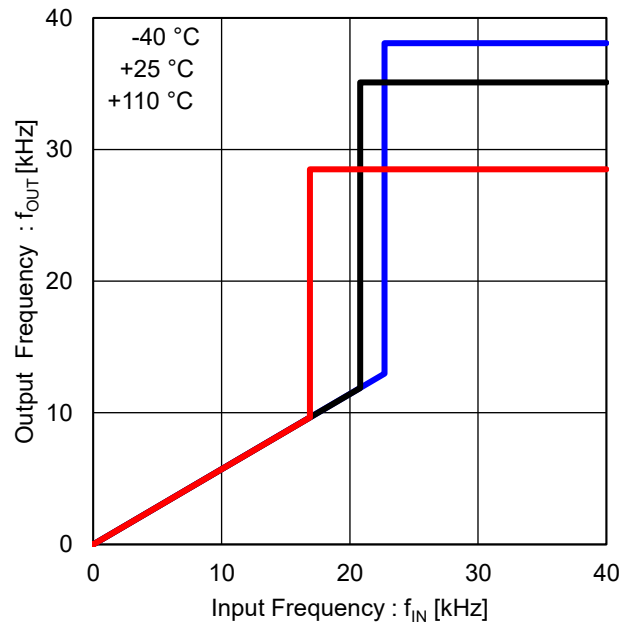


Figure 11. Output vs Input Frequency Characteristics

Timing Chart

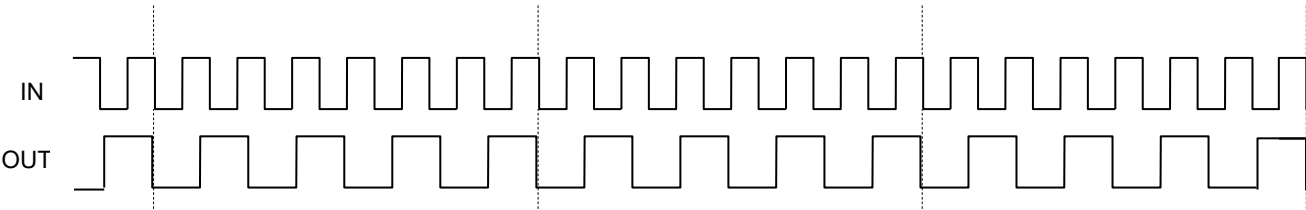


Figure 12. Timing Chart

I/O Equivalence Circuits

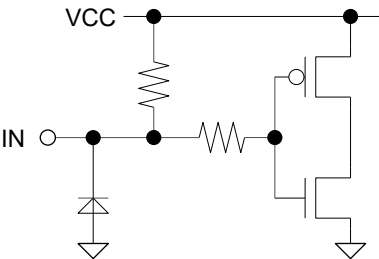


Figure 13. IN

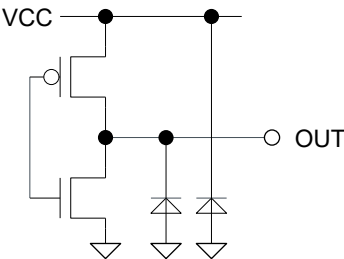


Figure 14. OUT, VCC

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

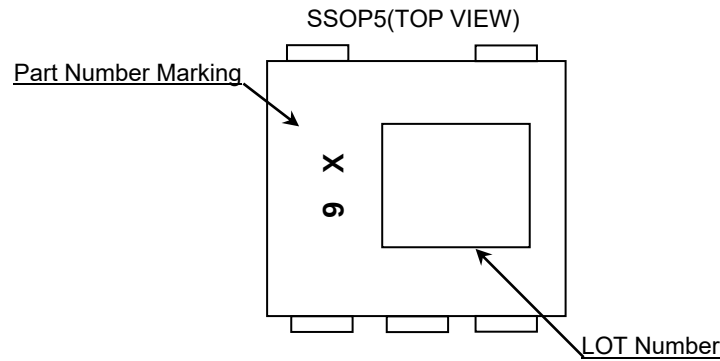
10. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

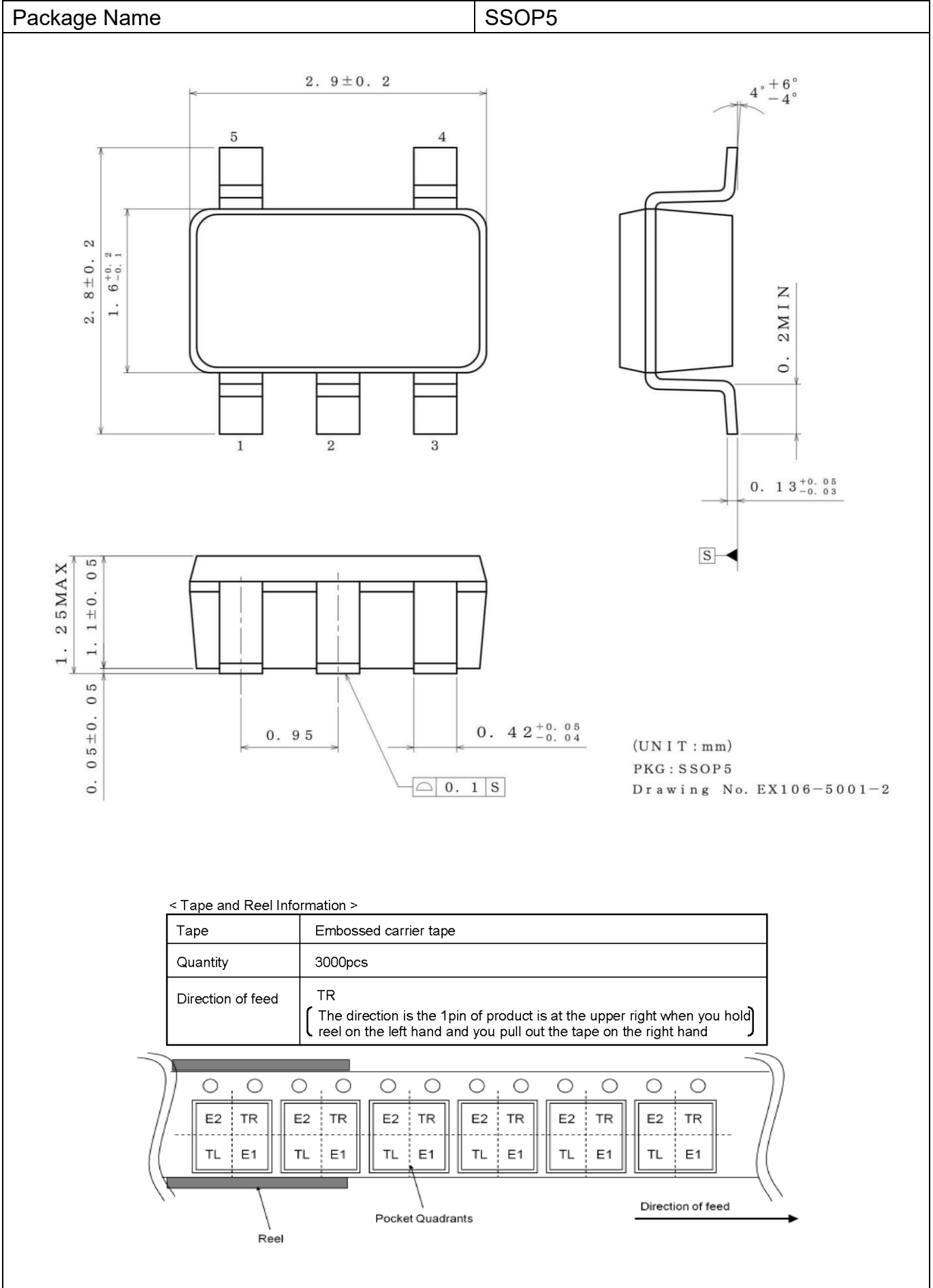
Ordering Information

B U 6 8 2 3 G							-	TR
Part Number							Package G: SSOP5	Packaging and forming specification TR: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
29.May.2018	001	New Release
30.Sep.2021	002	Page 1: Applications are added.

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of the Products in places subject to dew condensation
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