ISL28191, ISL28291

Single and Dual Single Supply Ultra-Low Noise, Low Distortion Rail-to-Rail Output, Op Amp

FN6156
Rev 10.00
July 22, 2014

The ISL28191 and ISL28291 are tiny single and dual ultra-low noise, ultra-low distortion operational amplifiers. They are fully specified to operate down to +3V single supply. These amplifiers have outputs that swing rail-to-rail and an input common mode voltage that extends to ground (ground sensing).

The ISL28191 and ISL28291 are unity gain stable with an input referred voltage noise of 1.7nV/√Hz. Both parts feature 0.00018% THD+N at 1kHz.

The ISL28191 is available in the space-saving 6 Ld UTDFN (1.6mmx1.6mm) and 6 Ld SOT-23 packages. The ISL28291 is available in the 8 Ld SOIC, 10 Ld 1.8mmx1.4mm UTQFN and 10 Ld MSOP packages. All devices are guaranteed over -40°C to +125°C.

Ordering Information

PART NUMBER (Note 5)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL28191FHZ-T7 (Notes 1, 2)	GABJ (Note 4)	6 Ld SOT-23	P6.064A
ISL28191FRUZ-T7 (Notes 1, 3)	M8	6 Ld UTDFN	L6.1.6x1.6A
ISL28291FUZ (Note 2)	8291Z	10 Ld MSOP	M10.118A
ISL28291FUZ-T7 (Notes 1, 2)	8291Z	10 Ld MSOP	M10.118A
ISL28291FBZ (Note 2)	28291 FBZ	8 Ld SOIC	M8.15E
ISL28291FBZ-T7 (Notes 1, 2)	28291 FBZ	8 Ld SOIC	M8.15E
ISL28291FRUZ-T7 (Notes 1, 3)	F	10 Ld UTQFN	L10.1.8x1.4A
ISL28191EVAL1Z	Evaluation Board		
ISL28291EVAL1Z	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. The part marking is located on the bottom of the part.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL28191, ISL28291. For more information on MSL please see techbrief TB363.

Features

- 1.7nV/√Hz input voltage noise at 1kHz
- 1kHz THD+N typical 0.00018% at $2V_{P-P}$ V_{OUT}
- Harmonic Distortion -76dBc, -70dBc, f_O = 1MHz
- 61MHz -3dB bandwidth
- 630µV maximum offset voltage
- 3µA input bias current
- 100dB typical CMRR
- 3V to 5.5V single supply voltage range
- Rail-to-rail output
- Ground Sensing
- Enable pin (not available in the 8 Ld SOIC package option)
- Pb-free (RoHS compliant)

Applications

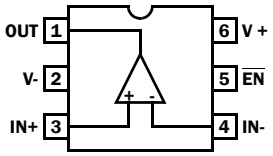
- Low noise signal processing
- Low noise microphones/preamplifiers
- ADC buffers
- DAC output amplifiers
- Digital scales
- Strain gauges/sensor amplifiers
- Radio systems
- Portable equipment
- Infrared detectors

Related Literature

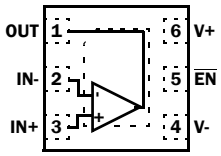
- AN1343: ISL2829xEVAL1Z, ISL5529xEVAL1Z Evaluation Board User's Guide

Pin Configurations

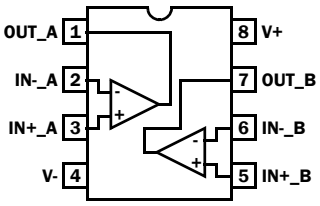
ISL28191
(6 LD SOT-23)
TOP VIEW



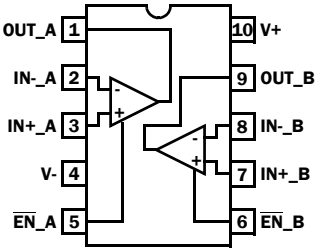
ISL28191
(6 LD 1.6X1.6X0.5 UTDFN)
TOP VIEW



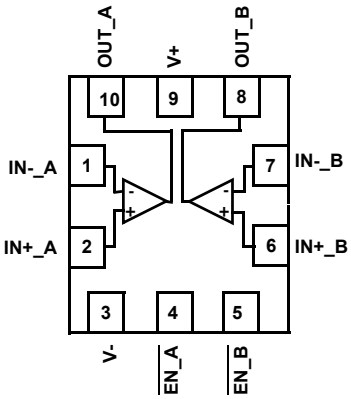
ISL28291
(8 LD SOIC)
TOP VIEW



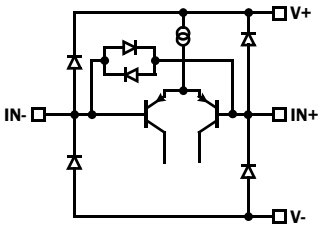
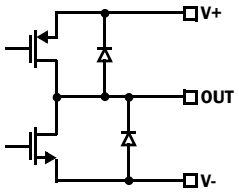
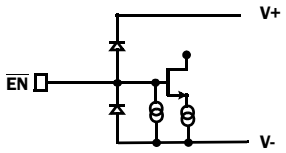
ISL28291
(10 LD MSOP)
TOP VIEW



ISL28291
(10 LD UTQFN)
TOP VIEW



Pin Descriptions

ISL28191 (6 Ld SOT-23)	ISL28191 (6 Ld UTDFN)	ISL28291 (8 Ld SOIC)	ISL28291 (10 Ld MSOP)	ISL28291 (10 Ld UTQFN)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
4	2	2 (A) 6 (B)	2 (A) 8 (B)	1 (A) 7 (B)	IN- IN-_A IN-_B	Inverting input	 Circuit 1
3	3	3 (A) 5 (B)	3 (A) 7 (B)	2 (A) 6 (B)	IN+ IN+_B IN+_B	Non-inverting input	(See circuit 1)
2	4	4	4	3	V-	Negative supply	
1	1	1 (A) 7 (B)	1 (A) 9 (B)	10 (A) 8 (B)	OUT OUT_A OUT_B	Output	 Circuit 2
6	6	8	10	9	V+	Positive supply	
5	5	N/A	5 (A) 6 (B)	4 (A) 5 (B)	$\overline{EN}$ $\overline{EN}$_A $\overline{EN}$_B	Enable BAR pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.	 Circuit 3

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Tolerance
Human Body Model 3kV
Machine Model 300V
Charged Device Model (CDM) 1200V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
6 Ld SOT-23 Package (Notes 6, 9)	170	105
6 Ld UTDFN Package (Notes 7, 8)	125	80
8 Ld SOIC Package (Notes 6, 9)	110	82
10 Ld MSOP Package (Notes 6, 9)	175	90
10 Ld UTQFN Package (Notes 6, 9)	190	140

Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage . . . . . 3V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
8. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
9. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V+ = 5.0V, V- = GND, R_L = Open, R_F = 1kΩ, A_V = -1 unless otherwise specified. Parameters are per amplifier. Typical values are at V+= 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage			270	630	µV
					840	
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature	Figure 21		3.1		µV/°C
I_{IO}	Input Offset Current			35	500	nA
					900	
I_B	Input Bias Current			3	6	µA
					7	
CMIR	Common-Mode Input Range		**0**		**3.8**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.8V	78	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 5V	74	80		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4V, R_L = 1kΩ	90	98		dB
			86			
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 1kΩ		20	50	mV
					80	
		Output high, R_L = 1kΩ, V+ = 5V	4.95	4.97		V
			4.92			
$I_{S,ON}$	Supply Current per Amplifier, Enabled			2.6	3.5	mA
					3.9	
$I_{S,OFF}$	Supply Current per Amplifier, Disabled			26	35	µA
					48	
I_O+	Short-Circuit Output Current	R_L = 10Ω	95	130		mA
			90			

Electrical Specifications V+ = 5.0V, V- = GND, R_L = Open, R_F = 1kΩ, A_V = -1 unless otherwise specified. Parameters are per amplifier. Typical values are at V+= 5V, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
I_{O-}	Short-Circuit Output Current	R_L = 10Ω	95	130		mA
			90			
V_{SUPPLY}	Supply Operating Range	V+ to V-	3		5.5	V
$V_{\overline{EN}H}$	$\overline{EN}$ High Level	Referred to V-	2			V
$V_{\overline{EN}L}$	$\overline{EN}$ Low Level	Referred to V-			0.8	V
$I_{\overline{EN}H}$	$\overline{EN}$ Pin Input High Current	$V_{\overline{EN}}$ = V+		0.8	1.1	µA
					1.3	
$I_{\overline{EN}L}$	$\overline{EN}$ Pin Input Low Current	$V_{\overline{EN}}$ = V-		20	80	nA
					100	
AC SPECIFICATIONS						
GBW	-3dB Unity Gain Bandwidth	R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		61		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1kHz. V_{OUT} + $2V_{P-P}$, A_V = +1, R_L = 10kΩ		0.0001		%
				8		
HD (1MHz)	2nd Harmonic Distortion	$2V_{P-P}$ output voltage, A_V = 1		-76		dBc
	3rd Harmonic Distortion			-70		dBc
ISO	Off-state Isolation f_O = 100kHz	A_V = +1, V_{IN} = 100mV_{P-P}, R_F = 0Ω C_L = 20pF, A_V = 1, R_L = 10kΩ		-38		dB
X-TALK ISL28291	Channel-to-Channel Crosstalk f_O = 100kHz	V_S = ±2.5V, A_V = +1, V_{IN} = $1V_{P-P}$, R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		-105		dB
PSRR	Power Supply Rejection Ratio f_O = 100kHz	V_S = ±2.5V, A_V = +1, V_{SOURCE} = $1V_{P-P}$, R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		-70		dB
CMRR	Common Mode Rejection Ratio f_O = 100kHz	V_S = ±2.5V, A_V = +1, V_{CM} = $1V_{P-P}$, R_F = 0Ω, C_L = 20pF, A_V = 1, R_L = 10kΩ		-65		dB
e_n	Input Referred Voltage Noise	f_O = 1kHz		1.7		nV/√Hz
i_n	Input Referred Current Noise	f_O = 1kHz		1.8		pA/√Hz
TRANSIENT RESPONSE						
SR	Slew Rate		12	17		V/µs
			12			
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	A_V = 1, V_{OUT} = $0.1V_{P-P}$, R_L = 10kΩ, C_L = 1.2pF		7		ns
	Fall Time, t_f 90% to 10%			12		ns
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	A_V = 2, V_{OUT} = $1V_{P-P}$; R_L = 10kΩ, R_F/R_G = 499Ω/499Ω, C_L = 1.2pF		44		ns
	Fall Time, t_f 90% to 10%			50		ns
	Rise Time, t_r 10% to 90%	A_V = 2, V_{OUT} = $4.7V_{P-P}$; R_L = 10kΩ, R_F/R_G = 499Ω/499Ω, C_L = 1.2pF		190		ns
	Fall Time, t_f 90% to 10%			190		ns
$t_{\overline{EN}}$	ENABLE to Output Turn-on Delay Time; 10% $\overline{EN}$ - 10% V_{OUT}	A_V = 1, V_{OUT} = 1VDC, R_L = 10kΩ, C_L = 1.2pF		330		ns
	ENABLE to Output Turn-off Delay Time; 10% $\overline{EN}$ - 10% V_{OUT}	A_V = 1, V_{OUT} = 0VDC, R_L = 10kΩ, C_L = 1.2pF		50		ns

NOTE:

10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

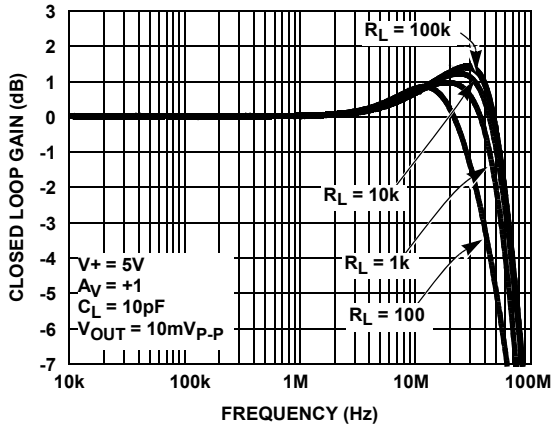


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

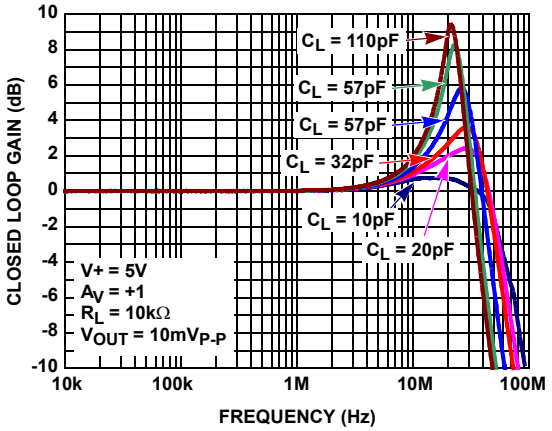


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

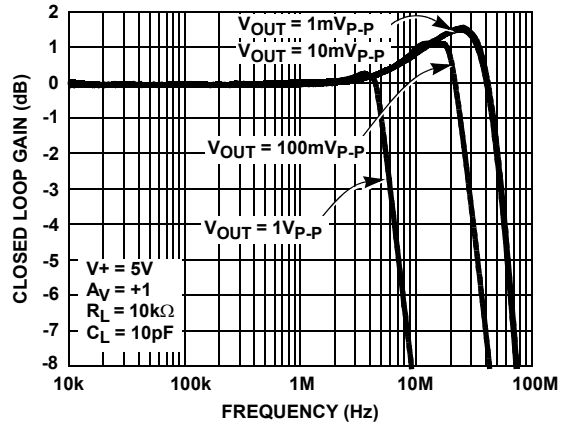


FIGURE 3. -3dB BANDWIDTH vs V_{OUT}

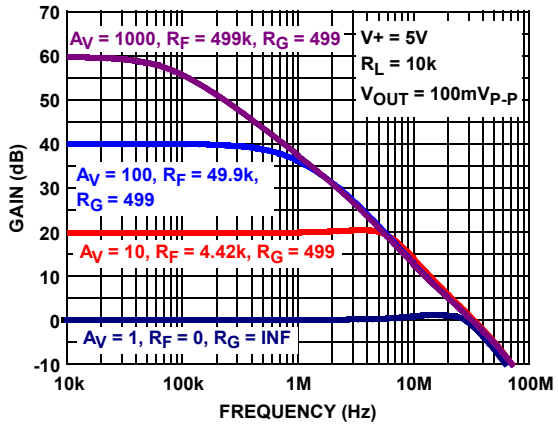


FIGURE 4. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

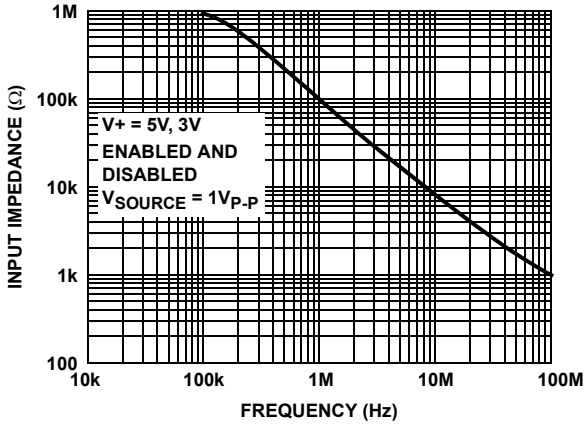


FIGURE 5. INPUT IMPEDANCE vs FREQUENCY

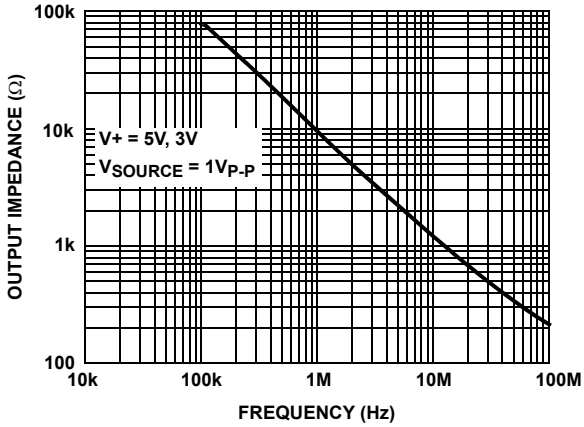


FIGURE 6. DISABLED OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

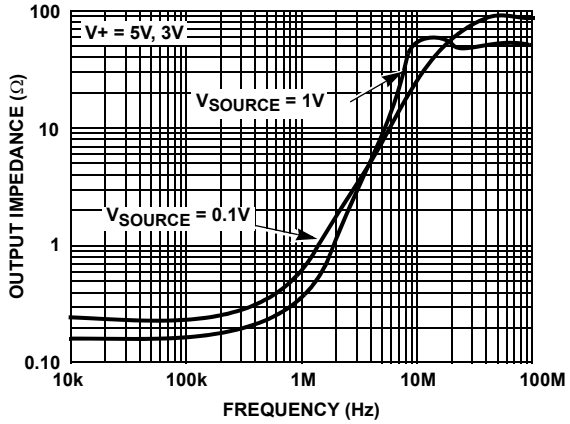


FIGURE 7. ENABLED OUTPUT IMPEDANCE vs FREQUENCY

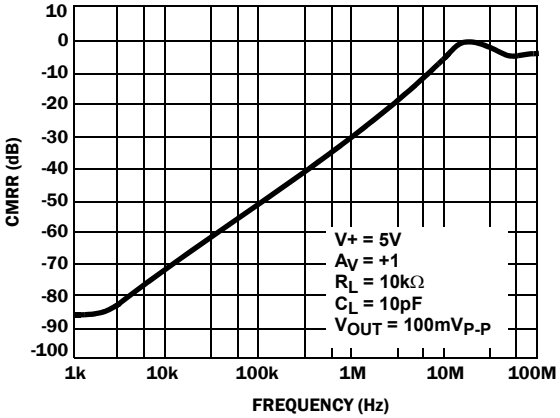


FIGURE 8. CMRR vs FREQUENCY

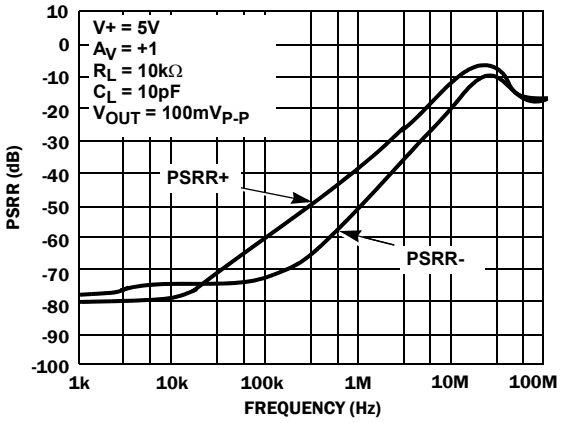


FIGURE 9. PSRR vs FREQUENCY

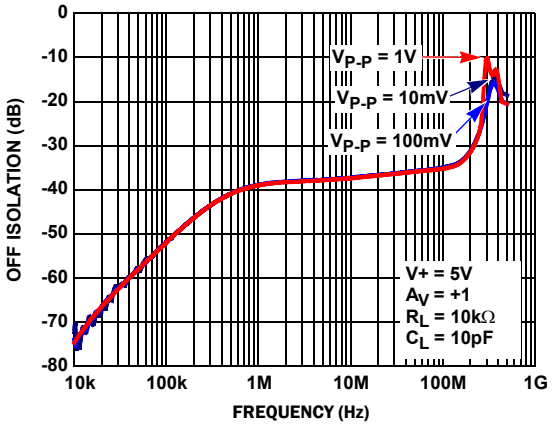


FIGURE 10. OFF ISOLATION vs FREQUENCY

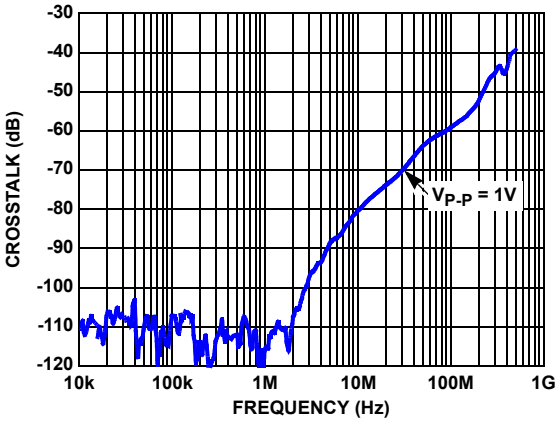


FIGURE 11. CHANNEL TO CHANNEL CROSSTALK vs FREQUENCY

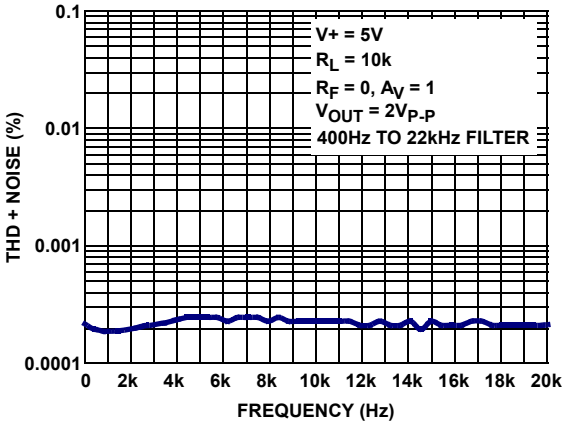


FIGURE 12. THD+N vs FREQUENCY

Typical Performance Curves (Continued)

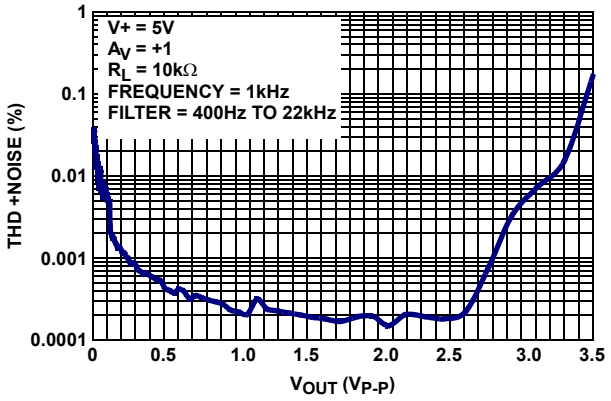


FIGURE 13. THD+N @ 1kHz vs V_{OUT}

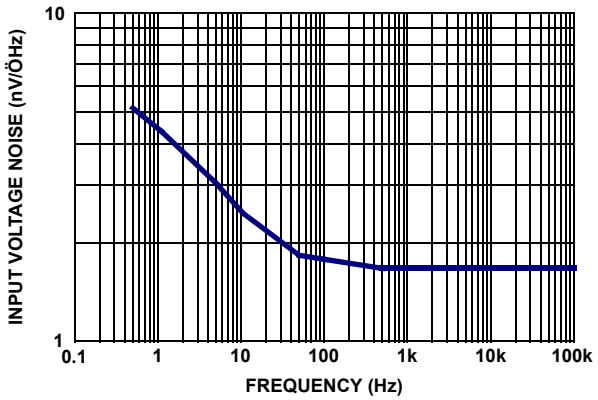


FIGURE 14. INPUT REFERRED NOISE VOLTAGE vs FREQUENCY

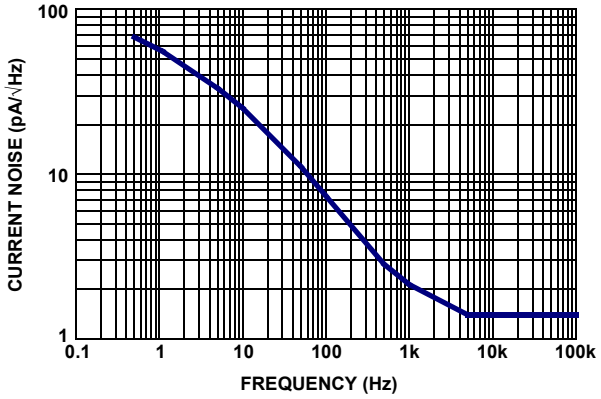


FIGURE 15. INPUT REFERRED NOISE CURRENT vs FREQUENCY

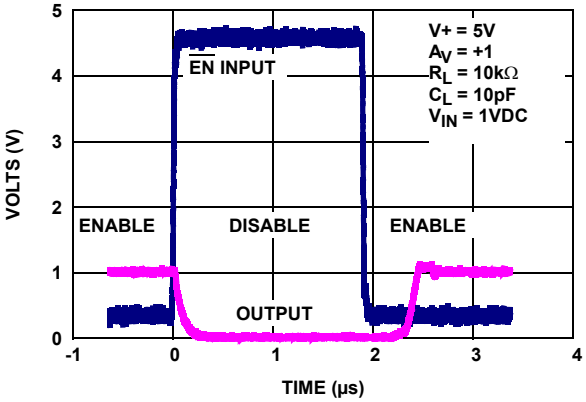


FIGURE 16. ENABLE/DISABLE TIMING

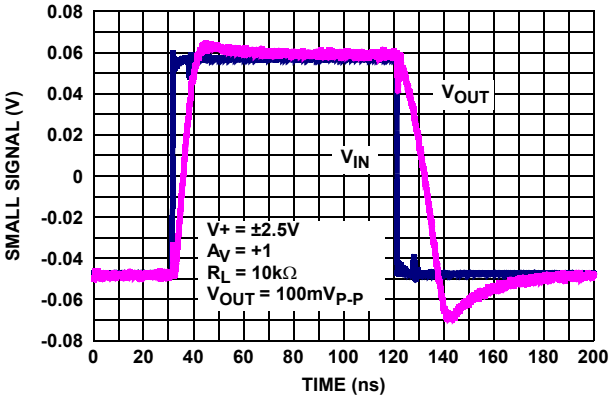


FIGURE 17. SMALL SIGNAL STEP RESPONSE

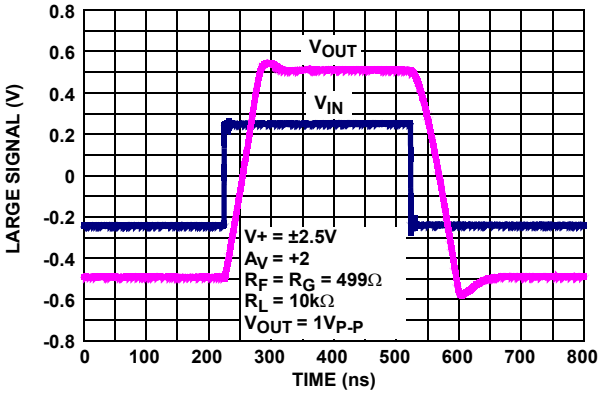


FIGURE 18. LARGE SIGNAL (1V) STEP RESPONSE

Typical Performance Curves (Continued)

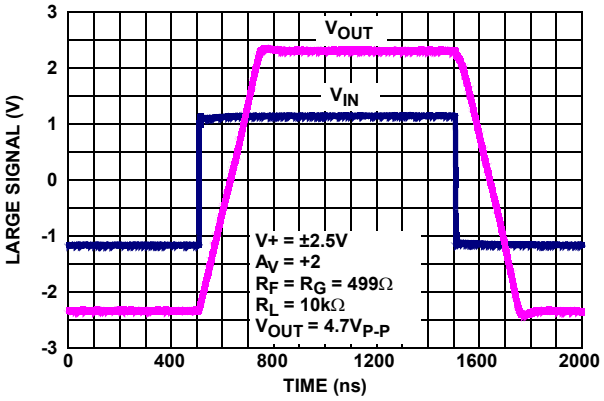


FIGURE 19. LARGE SIGNAL (4.7V) STEP RESPONSE

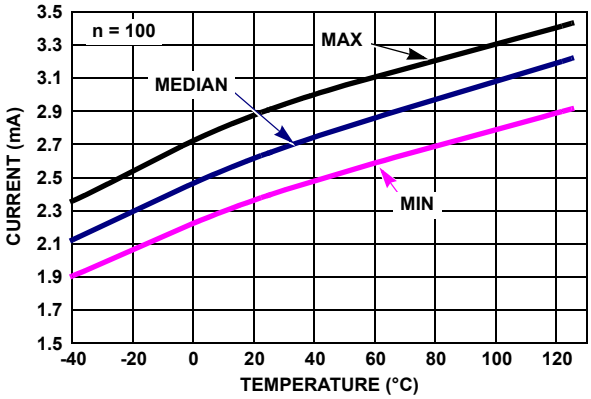


FIGURE 20. SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V ENABLED, R_L = INF

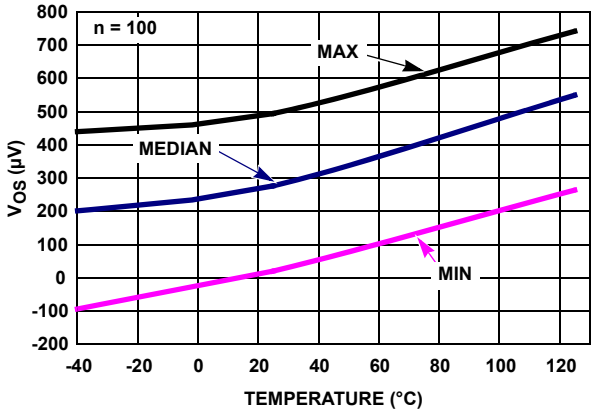


FIGURE 21. V_{OS} vs TEMPERATURE, V_S = ±2.5V

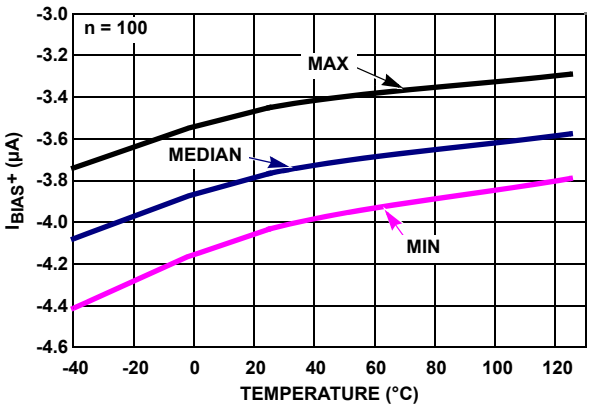


FIGURE 22. I_{BIAS+} vs TEMPERATURE, V_S = ±2.5V

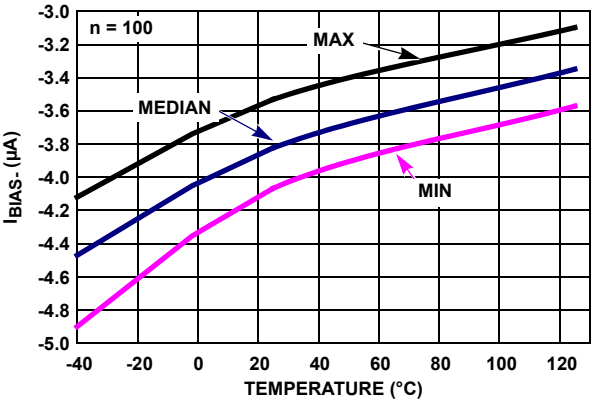


FIGURE 23. I_{BIAS-} vs TEMPERATURE, V_S = ±2.5V

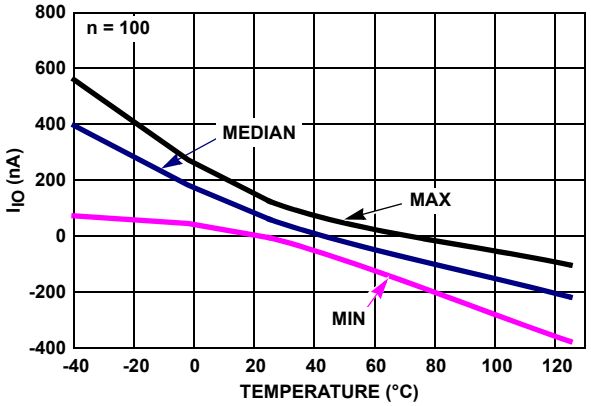


FIGURE 24. I_{IO} vs TEMPERATURE, V_S = ±2.5V

Typical Performance Curves (Continued)

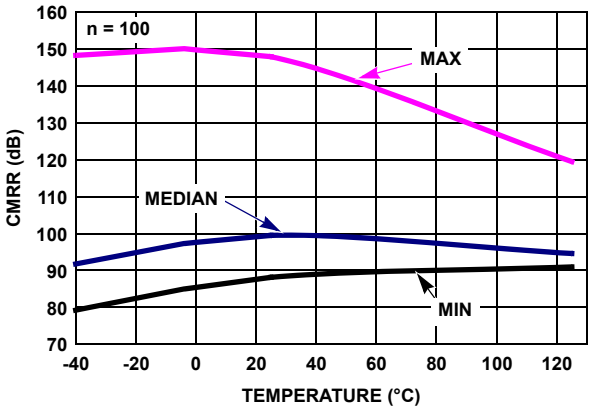


FIGURE 25. CMRR vs TEMPERATURE, VCM = 3.8V, V_S = ±2.5V

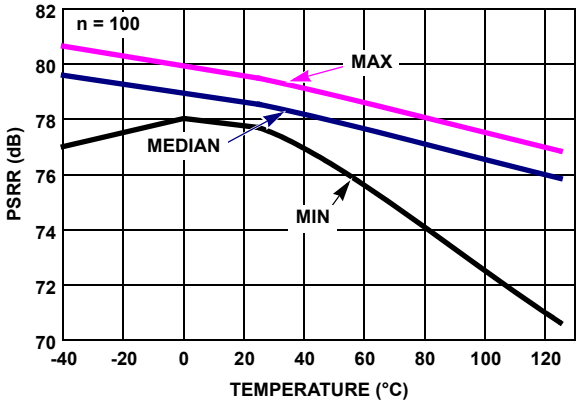


FIGURE 26. PSRR vs TEMPERATURE ±1.5V TO ±2.5V

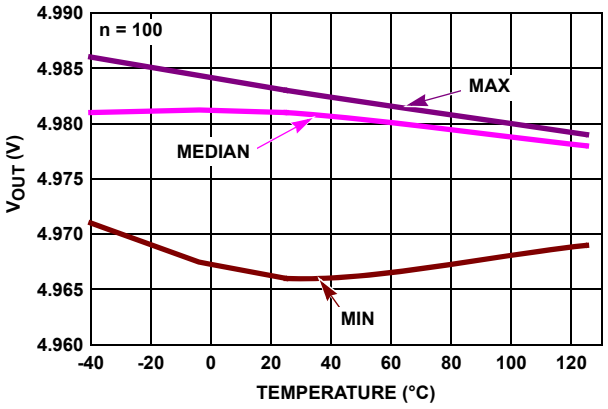


FIGURE 27. POSITIVE V_{OUT} vs TEMPERATURE, R_L = 1k V_S = ±2.5V

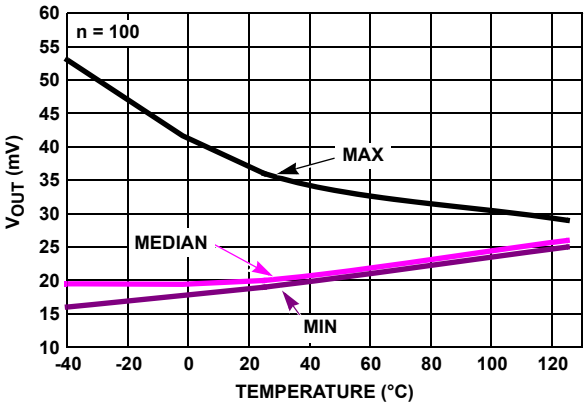


FIGURE 28. NEGATIVE V_{OUT} vs TEMPERATURE, R_L = 1k V_S = ±2.5V

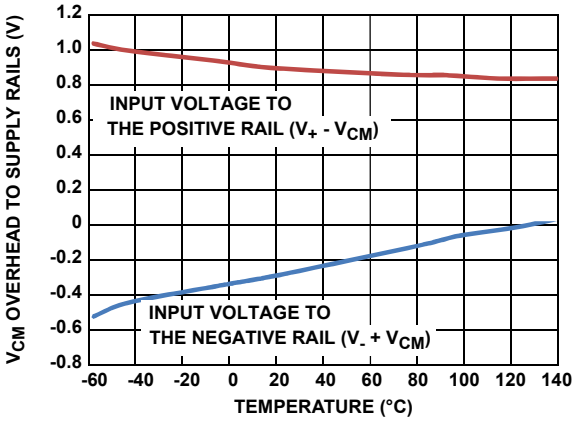


FIGURE 29. INPUT COMMON MODE VOLTAGE vs TEMPERATURE

Applications Information

Product Description

The ISL28191 and ISL28291 are voltage feedback operational amplifiers designed for communication and imaging applications requiring low distortion, very low voltage and current noise. Both parts feature high bandwidth while drawing moderately low supply current. They use a classical voltage-feedback topology, which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier.

Enable/Power-Down

The ISL28191 and ISL28291 amplifiers are disabled by applying a voltage greater than 2V to the $\overline{EN}$ pin, with respect to the V- pin. In this condition, the output(s) will be in a high impedance state and the amplifier(s) current will be reduced to 13µA/Amp. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. Both parts have additional back-to-back diodes across the input terminals (as shown in Figure 30). In pulse applications where the input Slew Rate exceeds the Slew Rate of the amplifier, the possibility exists for the input protection diodes to become forward biased. This can cause excessive input current and distortion at the outputs. If overdriving the inputs is necessary, the external input current must never exceed 5mA. An external series resistor may be used to limit the current, as shown in Figure 30.

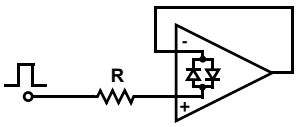


FIGURE 30. LIMITING THE INPUT CURRENT TO LESS THAN 5mA

Using Only One Channel

The ISL28291 is a dual channel op amp. If the application only requires one channel when using the ISL28291, the user must configure the unused channel to prevent it from oscillating. Oscillation can occur if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 31).

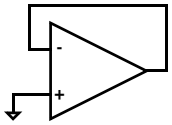


FIGURE 31. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the inverting input. When ground plane construction is used, it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of additional series inductance. Use of sockets, particularly for the SOIC package, should be avoided if possible. Sockets add parasitic inductance and capacitance, which will result in additional peaking and overshoot.

Current Limiting

The ISL28191 and ISL28291 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device. This is why the output short circuit current is specified and tested with $R_L = 10\Omega$.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated in Equation 2:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 22, 2014	FN6156.10	Updated location of note references. Updated Theta JA in the "Thermal Information" table on page 4 and added Theta JC to table.
January 18, 2012	FN6156.9	Page 1 - Ordering Information Update: Added Eval Board ISL28191EVAL1Z Changed micro TDFN and TQFN to Ultra matching POD Description Added SOT-23 Note Page 10 - Typical Performance Curves: Added Figure 29 - INPUT COMMON MODE VOLTAGE vs TEMPERATURE

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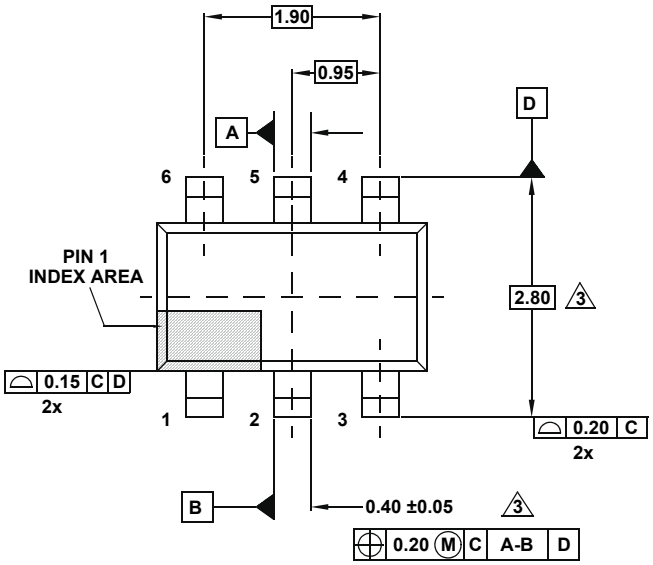
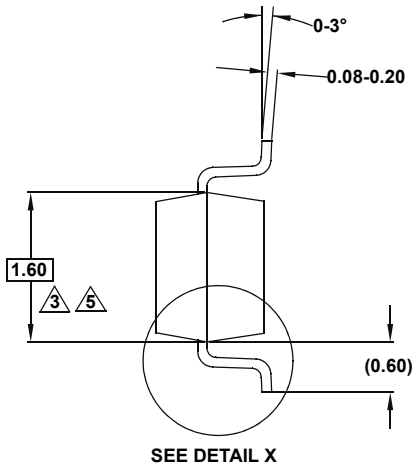
Package Outline Drawing

P6.064A

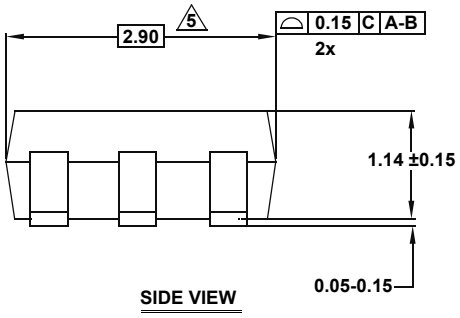
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



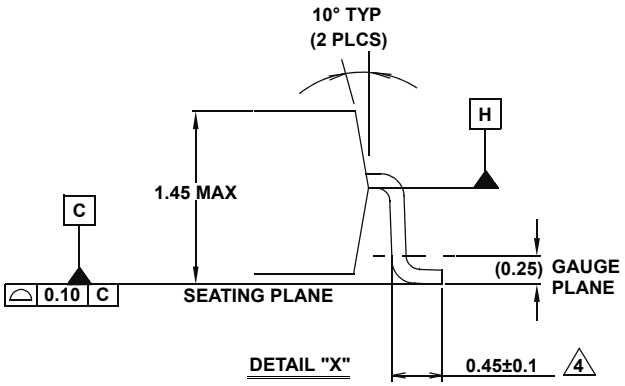
TOP VIEW



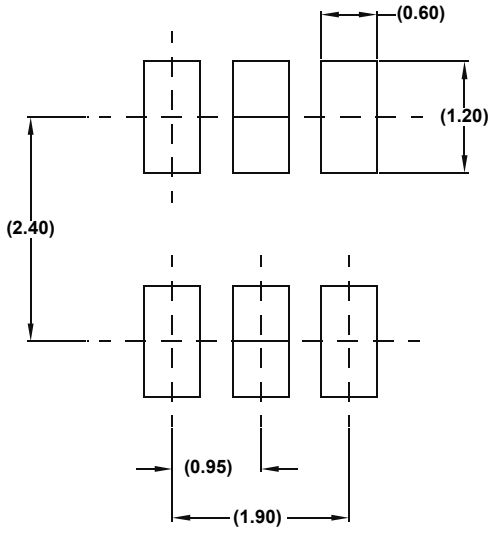
END VIEW



SIDE VIEW



DETAIL "X"

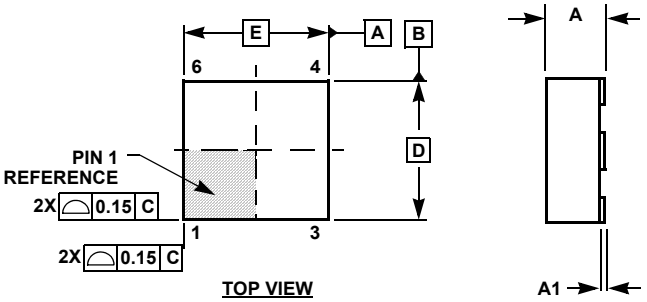


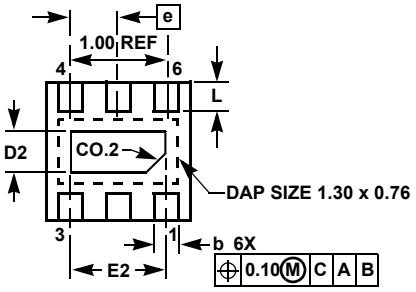
TYPICAL RECOMMENDED LAND PATTERN

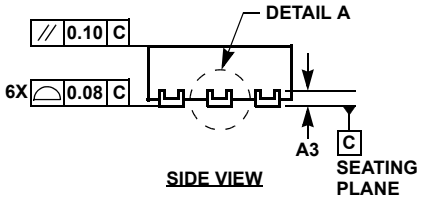
NOTES:

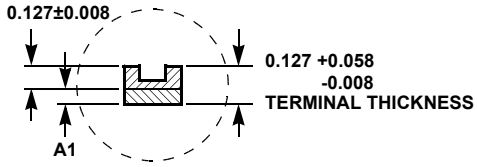
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

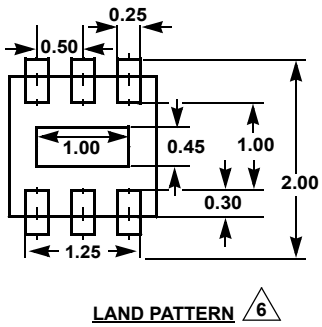
Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)











L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e		0.50 BSC		-
L	0.25	0.30	0.35	-

Rev. 1 6/06

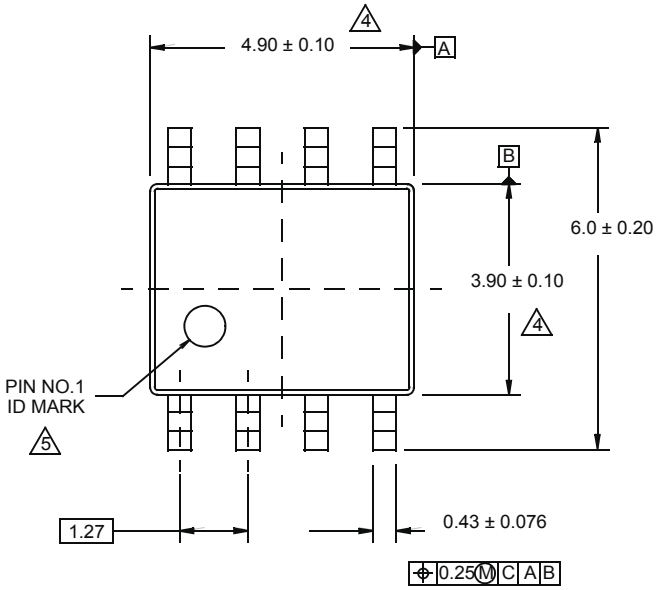
NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

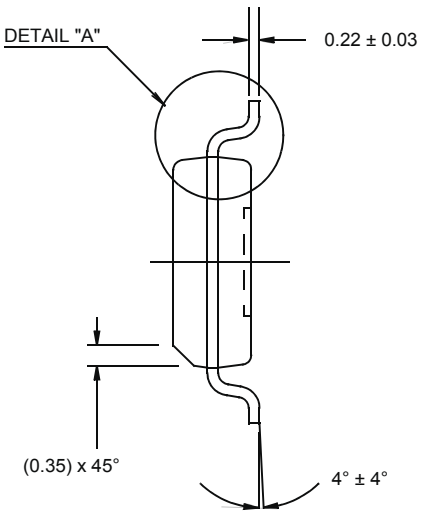
Package Outline Drawing

M8.15E

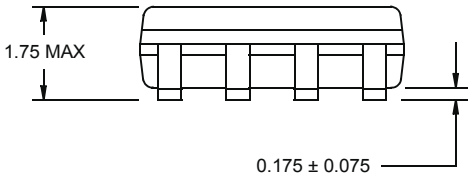
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



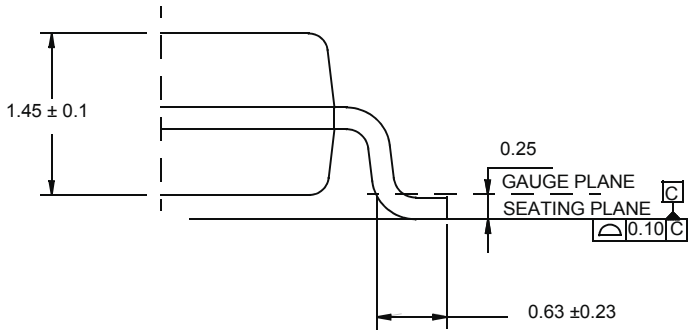
TOP VIEW



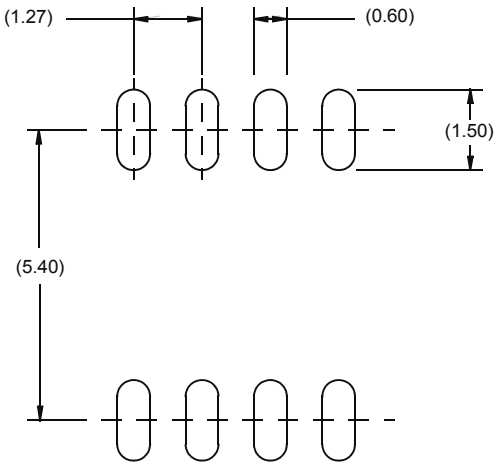
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

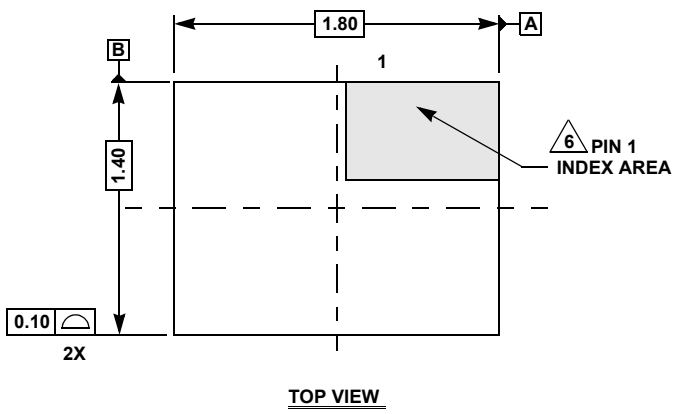
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

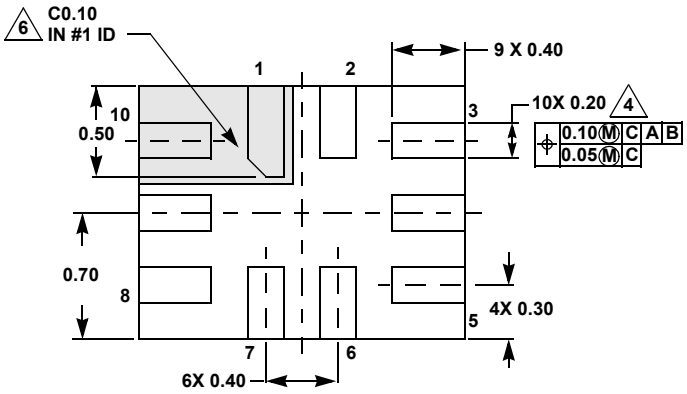
Package Outline Drawing

L10.1.8x1.4A

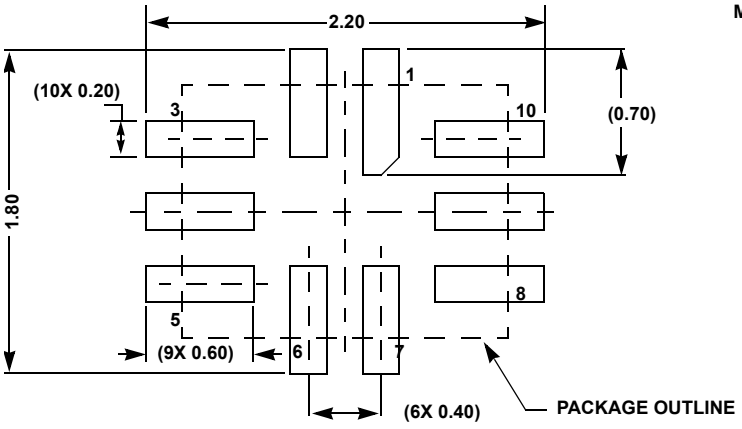
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 6, 8/13



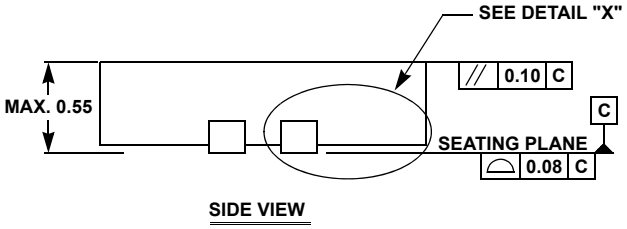
TOP VIEW



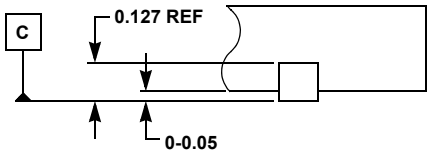
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

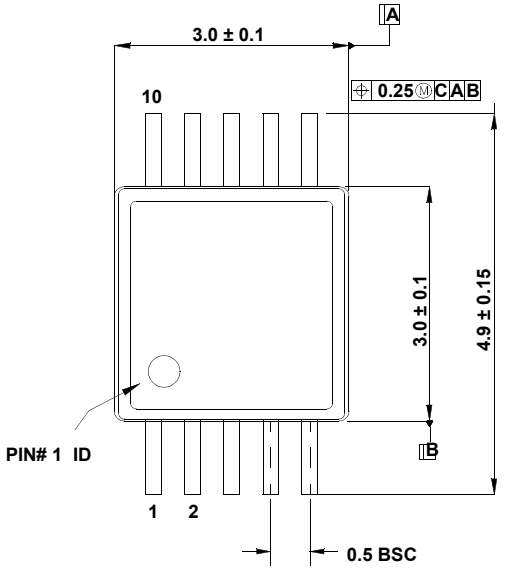
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. JEDEC reference MO-255.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

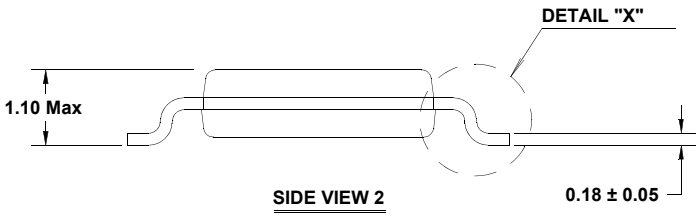
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

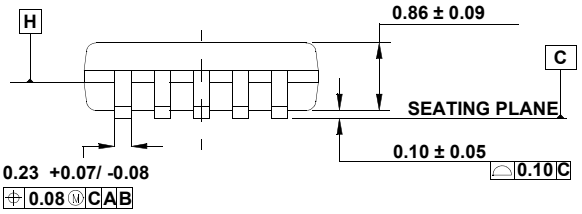
Rev 0, 9/09



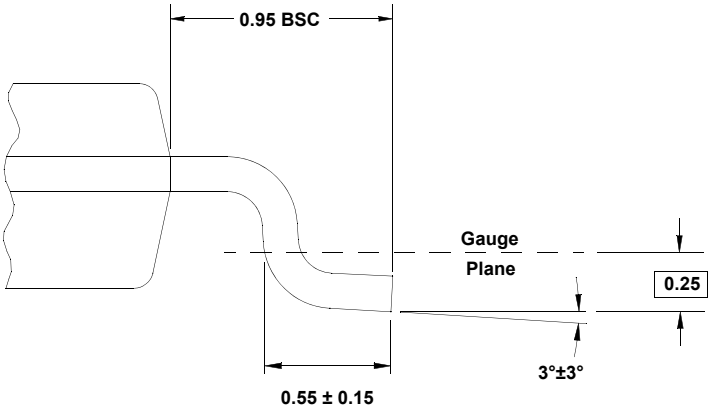
TOP VIEW



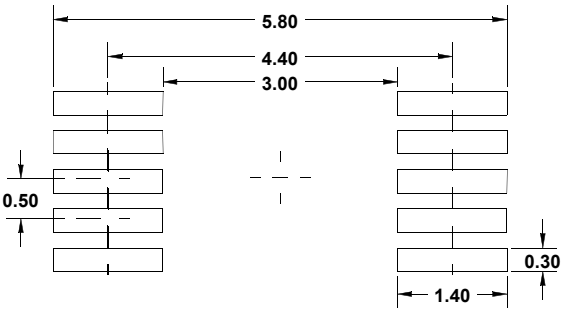
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.