

SN54LVC138A, SN74LVC138A 3-LINE TO 8-LINE DECODERS/DEMULPLEXERS

SCAS291I – MARCH 1993 – REVISED OCTOBER 1998

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flat (W) Package, and DIPs (J)

description

The SN54LVC138A 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation and the SN74LVC138A 3-line to 8-line decoder/demultiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

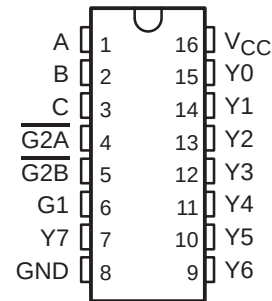
The 'LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

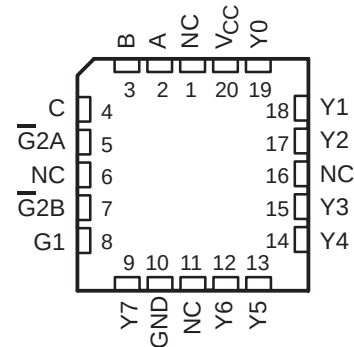
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN54LVC138A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVC138A is characterized for operation from -40°C to 85°C .

SN54LVC138A . . . J OR W PACKAGE
SN74LVC138A . . . D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVC138A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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**TEXAS
INSTRUMENTS**

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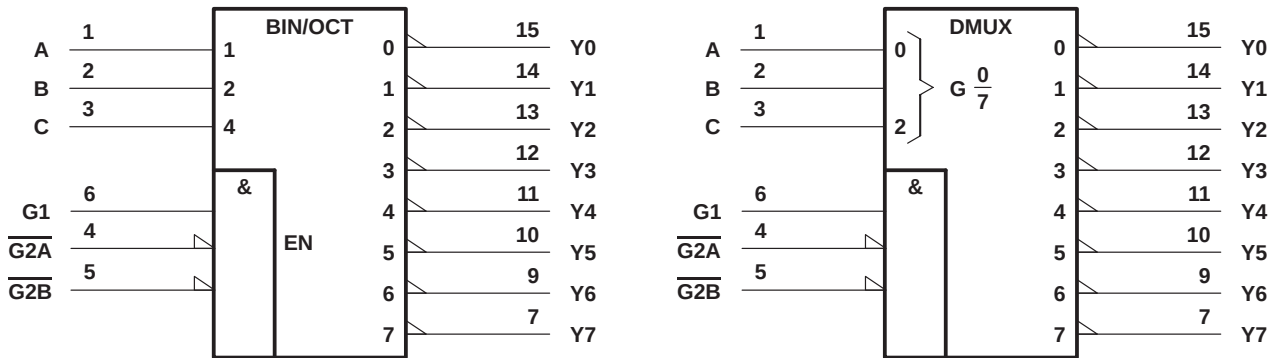
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FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

logic symbols (alternatives)[†]

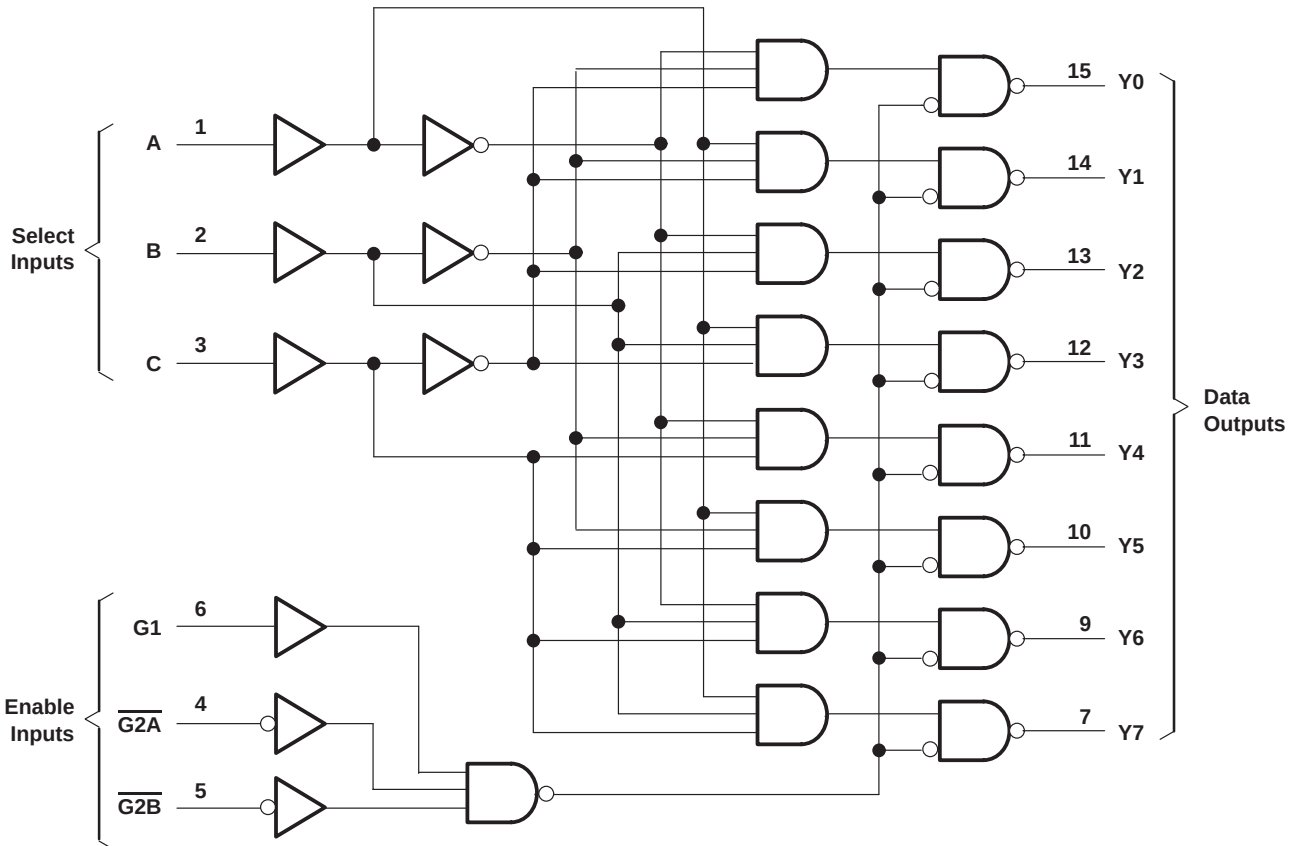


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	
D package	113°C/W
DB package	131°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

			SN54LVC138A		SN74LVC138A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V			0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V			0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8	0.8		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V			–4		mA
		V _{CC} = 2.3 V			–8		
		V _{CC} = 2.7 V		–12	–12		
		V _{CC} = 3 V		–24	–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V			4		mA
		V _{CC} = 2.3 V			8		
		V _{CC} = 2.7 V		12	12		
		V _{CC} = 3 V		24	24		
Δt/Δv	Input transition rise or fall rate		0	10	0	10	ns/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC138A			SN74LVC138A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V				V _{CC} –0.2			V
		2.7 V to 3.6 V	V _{CC} –0.2						
	I _{OH} = –4 mA	1.65 V				1.2			
	I _{OH} = –8 mA	2.3 V				1.7			
	I _{OH} = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
I _{OH} = –24 mA	3 V	2.2			2.2				
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC138A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B or C	Y	7.9		1	6.7	ns
	G2A or G2B		7.4		1	6.5	
	G1		6.4		1	5.8	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC138A						UNIT		
			V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V			V _{CC} = 3.3 V ± 0.3 V	
			TYP		MIN	MAX	MIN	MAX		MIN	MAX
t _{pd}	A or B or C	Y	15.9		1	9.9		7.9	1	6.7	ns
	G2A or G2B		15.4		1	9.4		7.4	1	6.5	
	G1		14.4		1	8.4		6.4	1	5.8	
t _{sk(o)} [‡]									1	ns	

[‡] Skew between any two outputs of the same package switching in the same direction

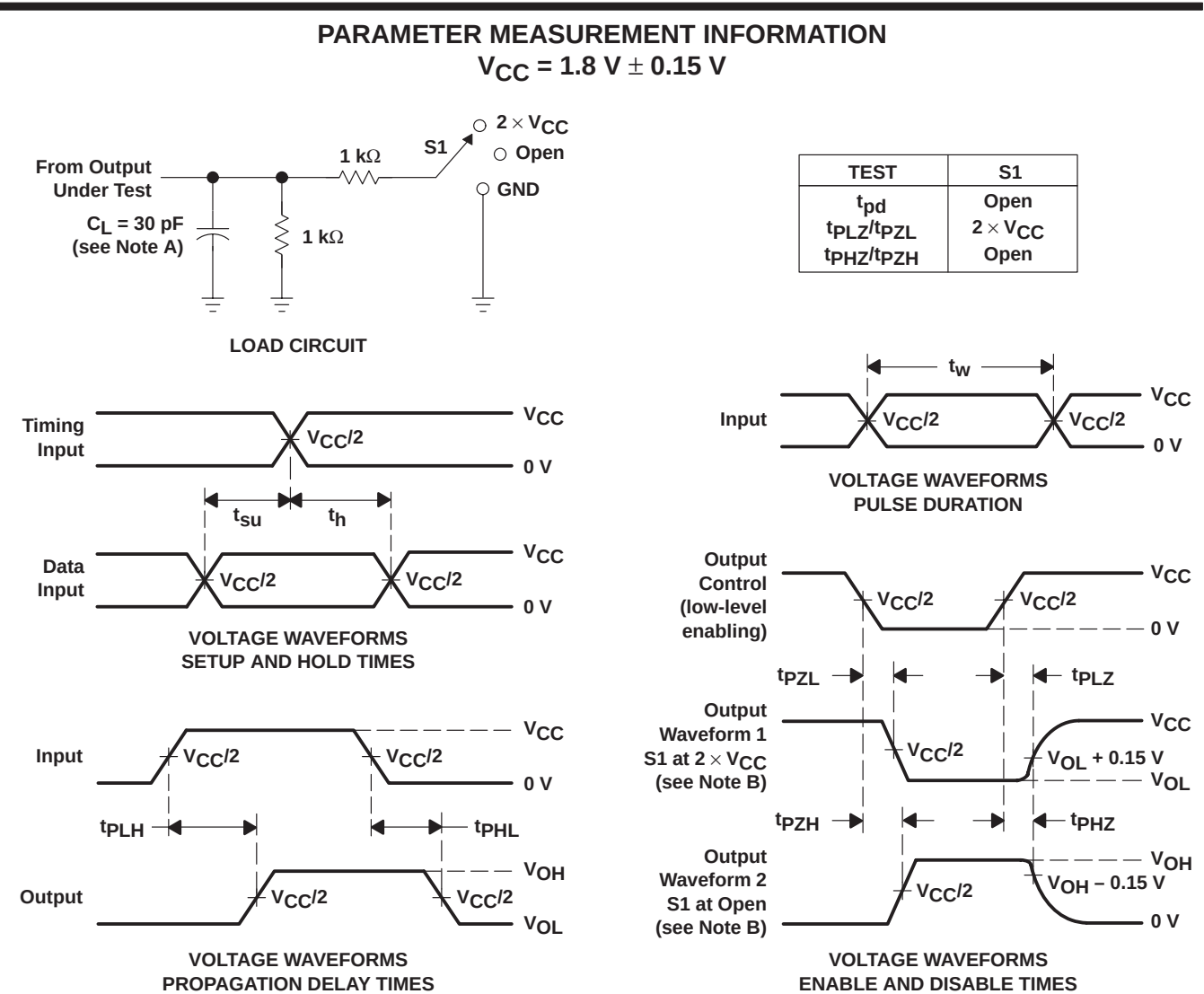


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operating characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	25	26	27	pF

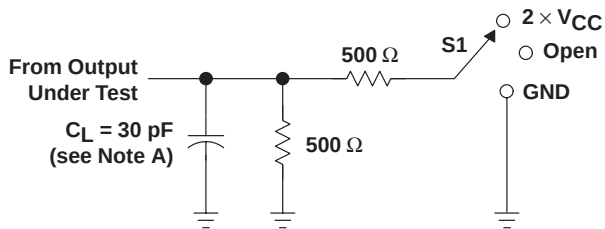


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

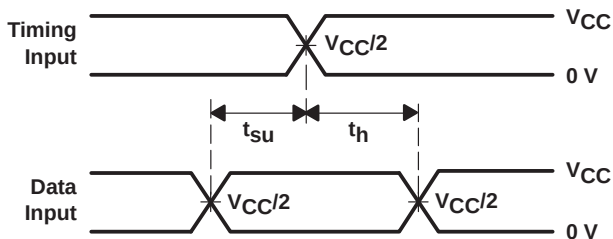
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

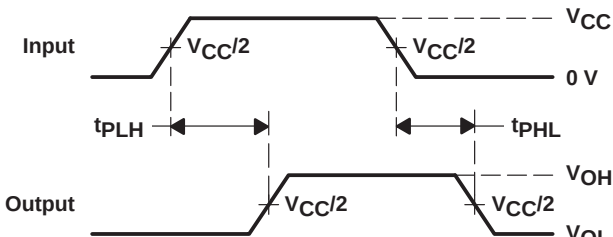


LOAD CIRCUIT

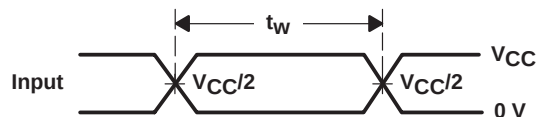
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



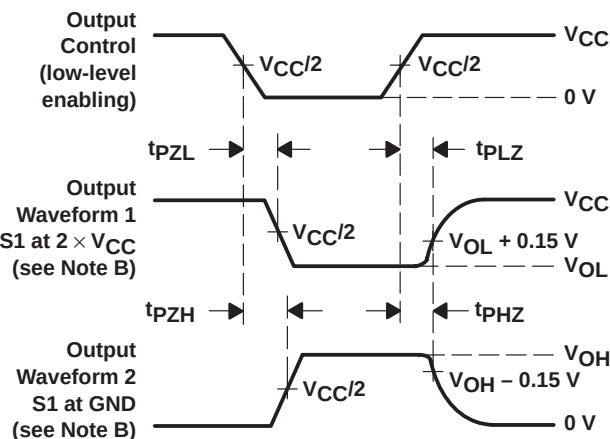
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

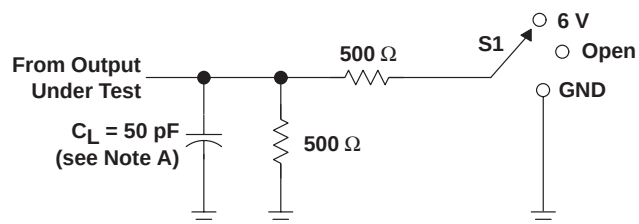
Figure 2. Load Circuit and Voltage Waveforms

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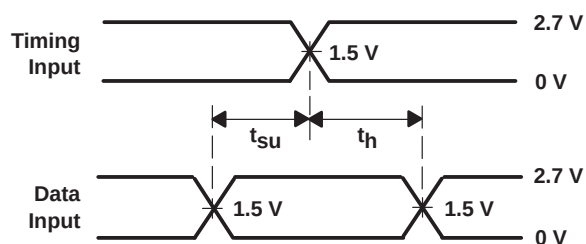
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

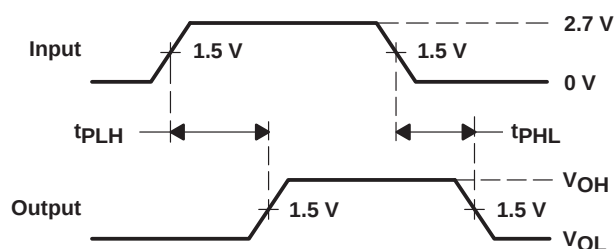


LOAD CIRCUIT

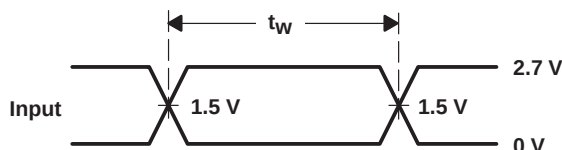
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



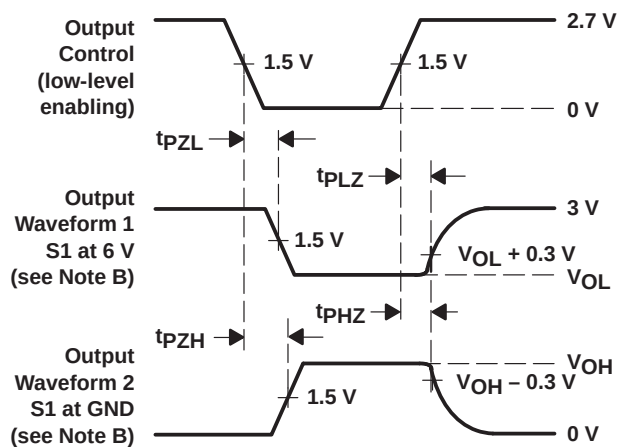
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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