

## High bandwidth (20 MHz) low offset (200 $\mu$ V) rail-to-rail 5 V op amp



### Features

- Gain bandwidth product 20 MHz, unity gain stable
- Low input offset voltage: 50  $\mu$ V typ., 200  $\mu$ V max.
- Low input bias current: 2 pA typ.
- Low noise: 7 nV/ $\sqrt{\text{Hz}}$
- Slew rate: 13 V/ $\mu$ s
- Wide supply voltage range: 2.0 V to 5.5 V
- Rail-to-rail input and output
- 4 kV HBM ESD tolerance
- Input common-mode range includes low rail
- Extended temperature range: -40  $^{\circ}$ C to +125  $^{\circ}$ C
- Automotive grade versions available
- Benefits:
  - Accuracy of measurement virtually unaffected by noise or input bias current
  - Signal conditioning for high frequencies

### Applications

- High bandwidth low-side and high-side current sensing
- Photodiode amplifiers
- A/D converters input buffers
- Power management in solar powered systems
- Automotive high bandwidth signal conditioning
- Active filters

### Description

The **TSV771**, **TSV772** and **TSV774** are single and dual 20 MHz-bandwidth unity-gain-stable amplifier. The rail-to-rail input stage and the slew rate of 10.5 V/ $\mu$ s make the **TSV771**, **TSV772** and **TSV774** ideal for low-side current measurement. The excellent accuracy provided by maximum input voltage of 200  $\mu$ V allows amplifying accurately small-amplitude input signal.

The **TSV771**, **TSV772** and **TSV774** can operate from a 2.0 V to 5.5 V single supply and are fully characterized for an output capacitor of 47 pF, therefore allowing easy usage as A/D converters input buffer.

| Maturity status link | Channel | Automotive | Package |
|----------------------|---------|------------|---------|
| TSV771               | 1       |            | SOT23-5 |
|                      | 1       | •          | SOT23-5 |
| TSV772               | 2       |            | DFN8    |
|                      | 2       |            | MiniSO8 |
|                      | 2       |            | SO8     |
|                      | 2       | •          | MiniSO8 |
|                      | 2       | •          | SO8     |
| TSV774               | 4       | •          | TSSOP14 |
|                      | 4       | •          | QFN16   |

| Related products             |                                               |
|------------------------------|-----------------------------------------------|
| TSV7721,<br>TSV7722          | Low rail 22 MHz amplifier                     |
| TSV791,<br>TSV792,<br>TSV794 | Rail-to-rail amplifier with higher GBW 50 MHz |

## 1 Pin description

### 1.1 TSV771 single operational amplifier

Figure 1. Pin connections (top view)

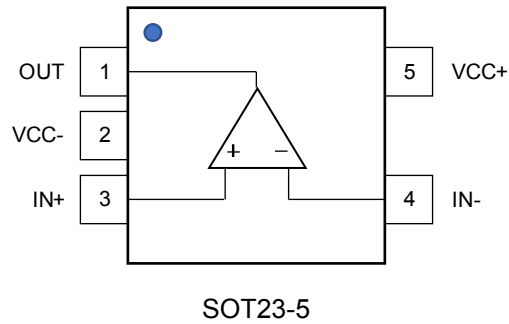
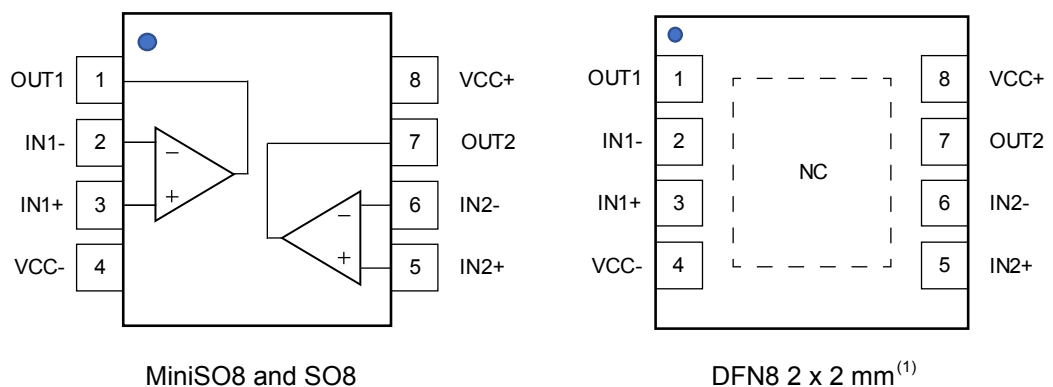


Table 1. Pin description

| Pin n° | Pin name | Description                 |
|--------|----------|-----------------------------|
| 1      | OUT      | Output channel              |
| 2      | VCC-     | Negative supply voltage     |
| 3      | IN+      | Non-inverting input channel |
| 4      | IN-      | Inverting input channel     |
| 5      | VCC+     | Positive supply voltage     |

### 1.2 TSV772 dual operational amplifier

Figure 2. Pin connections (top view)



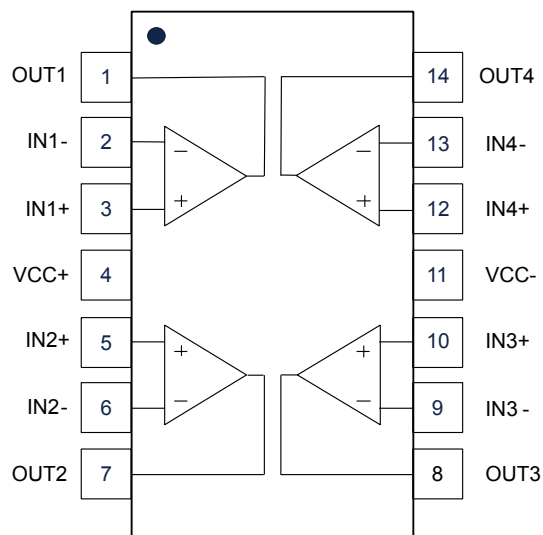
1. The exposed pad of the DFN8 2x2 can be connected to VCC- or left floating.

**Table 2. Pin description**

| Pin n° | Pin name | Description                   |
|--------|----------|-------------------------------|
| 1      | OUT1     | Output channel 1              |
| 2      | IN1-     | Inverting input channel 1     |
| 3      | IN1+     | Non-inverting input channel 1 |
| 4      | VCC-     | Negative supply voltage       |
| 5      | IN2+     | Non-inverting input channel 2 |
| 6      | IN2-     | Inverting input channel 2     |
| 7      | OUT2     | Output channel 2              |
| 8      | VCC+     | Positive supply voltage       |

### 1.3 TSV774 quad operational amplifier

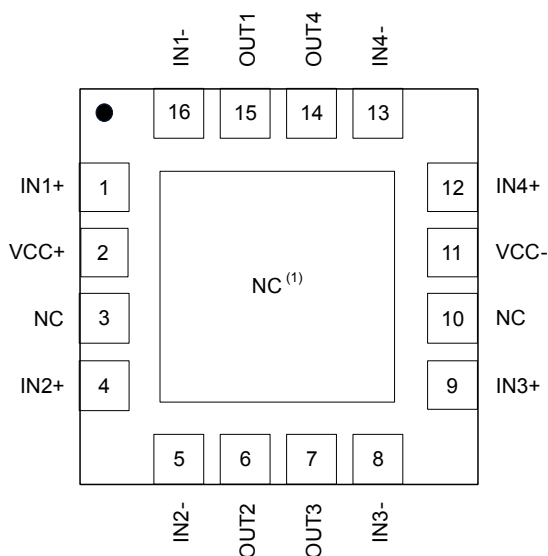
**Figure 3.** TSV774 pin connections for TSSOP14



**Table 3.** Pin description for TSSOP14

| Pin n° | Pin name | Description                   |
|--------|----------|-------------------------------|
| 1      | OUT1     | Output channel 1              |
| 2      | IN1-     | Inverting input channel 1     |
| 3      | IN1+     | Non-inverting input channel 1 |
| 4      | VCC+     | Positive supply voltage       |
| 5      | IN2+     | Non-inverting input channel 2 |
| 6      | IN2-     | Inverting input channel 2     |
| 7      | OUT2     | Output channel 2              |
| 8      | OUT3     | Output channel 3              |
| 9      | IN3-     | Inverting input channel 3     |
| 10     | IN3+     | Non-inverting input channel 3 |
| 11     | VCC-     | Negative supply voltage       |
| 12     | IN4+     | Non-inverting input channel 4 |
| 13     | IN4-     | Inverting input channel 4     |
| 14     | OUT4     | Output channel 4              |

**Figure 4. TSV774 pin connections for QFN16**



1. The exposed pad of the QFN16 3x3 WF can be connected to VCC- or left floating.

**Table 4. Pin description for QFN16**

| Pin n° | Pin name | Description                   |
|--------|----------|-------------------------------|
| 1      | IN1+     | Non-inverting input channel 1 |
| 2      | VCC+     | Positive supply voltage       |
| 3      | NC       | Not connected                 |
| 4      | IN2+     | Non-inverting input channel 2 |
| 5      | IN2-     | Inverting input channel 2     |
| 6      | OUT2     | Output channel 2              |
| 7      | OUT3     | Output channel 3              |
| 8      | IN3-     | Positive supply voltage       |
| 9      | IN3+     | Non-inverting input channel 3 |
| 10     | NC       | Not connected                 |
| 11     | VCC-     | Negative supply voltage       |
| 12     | IN4+     | Non-inverting input channel 4 |
| 13     | IN4-     | Inverting input channel 4     |
| 14     | OUT4     | Output channel 4              |
| 15     | OUT1     | Output channel 1              |
| 16     | IN1-     | Inverting input channel 1     |

## 2 Absolute maximum ratings and operating conditions

Table 5. Absolute maximum ratings

| Symbol            | Parameter <sup>(1)</sup>                           | Value                                         | Unit   |
|-------------------|----------------------------------------------------|-----------------------------------------------|--------|
| $V_{CC}$          | Supply voltage                                     | -0.3 to 6.0                                   | V      |
| $V_{id}$          | Input voltage differential ( $V_{IN+} - V_{IN-}$ ) | $\pm V_{CC}$                                  | V      |
| $V_{IN}^{(2)}$    | Input pins voltage                                 | $(V_{CC-}) - 0.3 \text{ V to } V_{CC+} + 0.3$ | V      |
| $I_{IN}$          | Input current                                      | $\pm 10$                                      | mA     |
| $T_{stg}$         | Storage temperature                                | 150                                           | °C     |
| $R_{th-ja}^{(3)}$ | Thermal resistance junction-to-ambient             | -                                             | °C / W |
|                   | DFN8 (2 mm x 2 mm)                                 | 76                                            |        |
|                   | SOT23-5                                            | 250                                           |        |
|                   | MiniSO8                                            | 127                                           |        |
|                   | SO8                                                | 113                                           |        |
|                   | TSSOP14                                            | 100                                           |        |
|                   | QFN16                                              | 39                                            |        |
| $T_j$             | Maximum junction temperature                       | 150                                           | °C     |
| ESD               | HBM: human body model <sup>(4)</sup>               | 4                                             | kV     |
|                   | CDM: charged device model <sup>(5)</sup>           | 1.5                                           | kV     |

1. All voltage values are with respect to VCC- pin, unless otherwise specified.
2. The maximum input voltage value may be extended to the condition that the input current is limited to  $\pm 10$  mA.
3.  $R_{th-ja}$  are typical values obtained with a PCB according to JEDEC 2s2p without vias.
4. Human Body Model: the test HBM is done in accordance with the standards ESDA-JS-001-2017 and Q100-002.
5. Charged device model: the test CDM is done in accordance with the standards ESDA-JS-002-2018 and Q100-011.

Table 6. Operating conditions

| Symbol     | Parameter                            | Value                                                 |
|------------|--------------------------------------|-------------------------------------------------------|
| $V_{CC}$   | Supply voltage                       | 2.0 to 5.5 V                                          |
| $V_{icm}$  | Common-mode input voltage range      | $V_{CC-} - 0.2 \text{ V to } V_{CC+} + 0.1 \text{ V}$ |
| $T_{oper}$ | Operating free air temperature range | -40 °C to +125 °C                                     |

### 3 Electrical characteristics

**Table 7. Electrical characteristics at  $V_{CC} = 5.0\text{ V}$ ,  $V_{icm} = V_{OUT} = V_{CC} / 2$ ,  $T = 25\text{ }^{\circ}\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_{CC} / 2$  and  $C_L = 47\text{ pF}$  (unless otherwise specified)**

| Symbol               | Parameter                                                         | Conditions                                                                                                            | Min.                                                                         | Typ. | Max. | Unit  |  |
|----------------------|-------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|------|------|-------|--|
| DC performance       |                                                                   |                                                                                                                       |                                                                              |      |      |       |  |
| V <sub>io</sub>      | Input offset voltage                                              | T = 25 °C                                                                                                             |                                                                              |      | ±200 | μV    |  |
|                      |                                                                   | -40 °C ≤ T ≤ 125 °C                                                                                                   |                                                                              |      | ±700 |       |  |
| ΔV <sub>io</sub> /ΔT | Input offset voltage drift                                        | -40 °C ≤ T ≤ 125 °C                                                                                                   |                                                                              |      | ±5   | μV/°C |  |
| I <sub>ib</sub>      | Input bias current <sup>(1)</sup>                                 | T = 25 °C                                                                                                             |                                                                              | 1    | 2    | pA    |  |
|                      |                                                                   | -40 °C ≤ T ≤ 85 °C                                                                                                    |                                                                              | 10   | 30   |       |  |
|                      |                                                                   | -40 °C ≤ T ≤ 125 °C                                                                                                   |                                                                              | 75   | 200  |       |  |
| I <sub>io</sub>      | Input offset current <sup>(1)</sup>                               | T = 25 °C                                                                                                             |                                                                              | 1    | 2    | pA    |  |
|                      |                                                                   | -40 °C ≤ T ≤ 85 °C                                                                                                    |                                                                              | 5    | 20   |       |  |
|                      |                                                                   | -40 °C ≤ T ≤ 125 °C                                                                                                   |                                                                              | 20   | 100  |       |  |
| A <sub>VD</sub>      | Open loop gain                                                    | V <sub>CC-</sub> +100 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -100 mV,<br>T = 25 °C                                  | 110                                                                          |      |      | dB    |  |
|                      |                                                                   | V <sub>CC-</sub> +100 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -100 mV,<br>-40 °C ≤ T ≤ 125 °C                        | 95                                                                           |      |      |       |  |
|                      |                                                                   | R <sub>L</sub> = 2 kΩ, V <sub>CC-</sub> + 200 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -200 mV,<br>T = 25 °C          | 105                                                                          |      |      |       |  |
|                      |                                                                   | R <sub>L</sub> = 2 kΩ, V <sub>CC-</sub> + 200 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -200 mV,<br>40 °C ≤ T ≤ 125 °C | 90                                                                           |      |      |       |  |
| CMR1                 | Common-mode rejection ratio                                       | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> -1.8 V,<br>T = 25 °C                                    | 98                                                                           | 120  |      | dB    |  |
|                      |                                                                   | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> -1.8 V,<br>-40 °C ≤ T ≤ 125 °C                          | 90                                                                           | 110  |      |       |  |
| CMR2                 |                                                                   | 20.log(ΔV <sub>io</sub> /ΔV <sub>icm</sub> )                                                                          | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> ,<br>T = 25 °C | 81   | 100  |       |  |
|                      |                                                                   | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> ,<br>-40 °C ≤ T ≤ 125 °C                                | 76                                                                           | 92   |      |       |  |
| SVR                  | Supply voltage rejection ratio                                    | 2.0 V ≤ V <sub>CC</sub> ≤ 5.5 V, T = 25 °C, V <sub>icm</sub> = 0 V                                                    | 90                                                                           | 110  |      | dB    |  |
|                      | 20.log(ΔV <sub>io</sub> /ΔV <sub>CC</sub> )                       | 2.0 V ≤ V <sub>CC</sub> ≤ 5.5 V, -40 °C ≤ T ≤ 125 °C,<br>V <sub>icm</sub> = 0 V                                       | 90                                                                           | 110  |      |       |  |
| V <sub>OH</sub>      | High level output voltage drop                                    | T = 25 °C                                                                                                             |                                                                              |      | 10   | mV    |  |
|                      | (V <sub>OH</sub> = V <sub>CC+</sub> - V <sub>OUT</sub> )          | -40 °C ≤ T ≤ 125 °C                                                                                                   |                                                                              |      | 20   |       |  |
| V <sub>OL</sub>      | Low level output voltage drop                                     | T = 25 °C                                                                                                             |                                                                              |      | 10   |       |  |
|                      | (V <sub>OL</sub> = V <sub>OUT</sub> )                             | -40 °C ≤ T ≤ 125 °C                                                                                                   |                                                                              |      | 20   |       |  |
| I <sub>OUT</sub>     | I <sub>sink</sub> (R <sub>L</sub> connected to V <sub>CC+</sub> ) | T = 25 °C                                                                                                             | 45                                                                           | 65   |      | mA    |  |
|                      |                                                                   | -40 °C ≤ T ≤ 125 °C                                                                                                   | 30                                                                           |      |      |       |  |

| Symbol           | Parameter                                                           | Conditions                                                                                          | Min. | Typ. | Max. | Unit    |
|------------------|---------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|------|------|------|---------|
| I <sub>OUT</sub> | I <sub>source</sub> (R <sub>L</sub> connected to V <sub>CC-</sub> ) | T = 25 °C                                                                                           | 45   | 65   |      | mA      |
|                  |                                                                     | -40 °C ≤ T ≤ 125 °C                                                                                 | 30   |      |      |         |
| I <sub>CC</sub>  | Supply current (per channel,<br>R <sub>L</sub> > 1 MΩ)              | T = 25 °C                                                                                           |      | 1.9  | 2.1  | mA      |
|                  |                                                                     | -40 °C ≤ T ≤ 125 °C                                                                                 |      |      | 2.1  |         |
| AC performance   |                                                                     |                                                                                                     |      |      |      |         |
| GBP              | Gain bandwidth product                                              |                                                                                                     | 17   | 20   |      | MHz     |
| SR               | Slew rate                                                           | A <sub>V</sub> = 1 V/V, 10% to 90% <sup>(2)</sup>                                                   | 11   | 13   |      | V/μs    |
| t <sub>s</sub>   | Settling time                                                       | R <sub>L</sub> = 4.7 kΩ, A <sub>V</sub> = -1 V/V, to 0.1%, V <sub>in</sub> = 1 Vp-p                 |      | 300  |      | ns      |
|                  |                                                                     | R <sub>L</sub> = 4.7 kΩ, A <sub>V</sub> = -1 V/V, to 0.01%, V <sub>in</sub> = 1 Vp-p <sup>(3)</sup> |      | 470  |      |         |
| t <sub>rec</sub> | Overload recovery time                                              | V <sub>OUT</sub> 100 mV from rail, A <sub>V</sub> = +1                                              |      | 235  |      | ns      |
| CR               | Cross talk                                                          | V <sub>OUT</sub> = 4 Vpp, A <sub>V</sub> = +101, f = 1 kHz                                          |      | 120  |      | dB      |
| Φ <sub>m</sub>   | Phase margin                                                        |                                                                                                     |      | 50   |      | degrees |
| GM               | Gain margin                                                         |                                                                                                     |      | 9    |      | dB      |
| C <sub>in</sub>  | Differential input capacitance                                      |                                                                                                     |      | 6.5  |      | pF      |
|                  | Common-mode input capacitance                                       |                                                                                                     |      | 2.5  |      |         |
| en               | Input voltage noise density                                         | f = 1 kHz                                                                                           |      | 13   |      | nV/√Hz  |
|                  |                                                                     | f = 10 kHz                                                                                          |      | 7    |      |         |
| en p-p           | Input noise voltage                                                 | 0.1 Hz ≤ f ≤ 10 Hz                                                                                  |      | 7    |      | μVpp    |

**Table 8. Electrical characteristics at  $V_{CC+} = 3.3\text{ V}$ ,  $V_{icm} = V_{OUT} = V_{CC} / 2$ ,  $T = 25\text{ }^{\circ}\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_{CC} / 2$  and  $C_L = 47\text{ pF}$  (unless otherwise specified)**

| Symbol               | Parameter                                                                                  | Conditions                                                                                                             | Min. | Typ. | Max. | Unit  |
|----------------------|--------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------|------|------|-------|
| DC performance       |                                                                                            |                                                                                                                        |      |      |      |       |
| V <sub>io</sub>      | Input offset voltage                                                                       | T = 25 °C                                                                                                              |      |      | ±200 | μV    |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    |      |      | ±700 |       |
| ΔV <sub>io</sub> /ΔT | Input offset voltage drift                                                                 | -40 °C ≤ T ≤ 125 °C                                                                                                    |      |      | ±5   | μV/°C |
| I <sub>ib</sub>      | Input bias current <sup>(1)</sup>                                                          | T = 25 °C                                                                                                              |      | 1    | 2    | pA    |
|                      |                                                                                            | -40 °C ≤ T ≤ 85 °C                                                                                                     |      | 10   | 30   |       |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    |      | 75   | 200  |       |
| I <sub>io</sub>      | Input offset current <sup>(1)</sup>                                                        | T = 25 °C                                                                                                              |      | 1    | 2    | pA    |
|                      |                                                                                            | -40 °C ≤ T ≤ 85 °C                                                                                                     |      | 5    | 20   |       |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    |      | 20   | 100  |       |
| A <sub>VD</sub>      | Open loop gain                                                                             | V <sub>CC-</sub> +100 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -100 mV, T = 25 °C                                      | 105  |      |      | dB    |
|                      |                                                                                            | V <sub>CC-</sub> +100 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -100 mV,<br>-40 °C ≤ T ≤ 125 °C                         | 90   |      |      |       |
|                      |                                                                                            | R <sub>L</sub> = 2 kΩ, V <sub>CC-</sub> + 200 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -200 mV,<br>T = 25 °C           | 100  |      |      |       |
|                      |                                                                                            | R <sub>L</sub> = 2 kΩ, V <sub>CC-</sub> + 200 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -200 mV,<br>-40 °C ≤ T ≤ 125 °C | 85   |      |      |       |
| CMR1                 | Common-mode rejection ratio<br>20.log(ΔV <sub>io</sub> /ΔV <sub>icm</sub> )                | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> -1.8 V,<br>T = 25 °C                                     | 93   | 115  |      | dB    |
|                      |                                                                                            | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> -1.8 V,<br>-40 °C ≤ T ≤ 125 °C                           | 85   | 108  |      |       |
| CMR2                 |                                                                                            | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> , T = 25 °C                                              | 77   | 98   |      |       |
|                      |                                                                                            | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> , -40 °C ≤ T ≤ 125 °C                                    | 70   | 90   |      |       |
| V <sub>OH</sub>      | High level output voltage drop<br>(V <sub>OH</sub> = V <sub>CC+</sub> - V <sub>OUT</sub> ) | T = 25 °C                                                                                                              |      |      | 10   | mV    |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    |      |      | 20   |       |
| V <sub>OL</sub>      | Low level output voltage drop<br>(V <sub>OL</sub> = V <sub>OUT</sub> )                     | T = 25 °C                                                                                                              |      |      | 10   |       |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    |      |      | 20   |       |
| I <sub>OUT</sub>     | I <sub>sink</sub> (R <sub>L</sub> connected to V <sub>CC+</sub> )                          | T = 25 °C                                                                                                              | 45   | 60   |      | mA    |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    | 30   |      |      |       |
|                      | I <sub>source</sub> (R <sub>L</sub> connected to V <sub>CC-</sub> )                        | T = 25 °C                                                                                                              | 45   | 65   |      |       |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    | 30   |      |      |       |
| I <sub>CC</sub>      | Supply current (per channel, R <sub>L</sub> > 1 MΩ)                                        | T = 25 °C                                                                                                              |      | 1.8  | 2.0  | mA    |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                    |      |      | 2.0  |       |
| AC performance       |                                                                                            |                                                                                                                        |      |      |      |       |
| GBP                  | Gain bandwidth product                                                                     |                                                                                                                        | 17   | 20   |      | MHz   |
| SR                   | Slew rate                                                                                  | A <sub>V</sub> = 1 V/V, 10% to 90% <sup>(2)</sup>                                                                      | 11   | 13   |      | V/μs  |
| t <sub>s</sub>       | Settling time                                                                              | R <sub>L</sub> = 4.7 kΩ, A <sub>V</sub> = -1 V/V, to 0.1%, V <sub>in</sub> = 1 Vp-p                                    |      | 310  |      | ns    |

| Symbol           | Parameter                      | Conditions                                                                                                | Min. | Typ. | Max. | Unit                   |
|------------------|--------------------------------|-----------------------------------------------------------------------------------------------------------|------|------|------|------------------------|
| $t_s$            | Settling time                  | $R_L = 4.7\text{ k}\Omega$ , $A_V = -1\text{ V/V}$ , to 0.01%, $V_{in} = 1\text{ V}_{p-p}$ <sup>(3)</sup> |      | 480  |      | ns                     |
| $t_{rec}$        | Overload recovery time         | $V_{OUT}$ 100 mV from rail, $A_V = +1$                                                                    |      | 260  |      | ns                     |
| $\Phi_m$         | Phase margin                   |                                                                                                           |      | 48   |      | degrees                |
| GM               | Gain margin                    |                                                                                                           |      | 9    |      | dB                     |
| $C_{in}$         | Differential input capacitance |                                                                                                           |      | 6.5  |      | pF                     |
|                  | Common-mode input capacitance  |                                                                                                           |      | 2.5  |      |                        |
| $e_n$            | Input voltage noise density    | $f = 1\text{ kHz}$                                                                                        |      | 13   |      | nV/ $\sqrt{\text{Hz}}$ |
|                  |                                | $f = 10\text{ kHz}$                                                                                       |      | 7    |      |                        |
| $e_n\text{ p-p}$ | Input noise voltage            | $0.1\text{ Hz} \leq f \leq 10\text{ Hz}$                                                                  |      | 7    |      | $\mu\text{V}_{pp}$     |

**Table 9. Electrical characteristics at  $V_{CC+} = 2.0\text{ V}$ ,  $V_{icm} = V_{OUT} = V_{CC}/2$ ,  $T = 25\text{ }^{\circ}\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_{CC}/2$  and  $C_L = 47\text{ pF}$  (unless otherwise specified)**

| Symbol               | Parameter                                                                                  | Conditions                                                                                                           | Min. | Typ. | Max. | Unit    |
|----------------------|--------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|------|------|------|---------|
| DC Performance       |                                                                                            |                                                                                                                      |      |      |      |         |
| V <sub>io</sub>      | Input offset voltage<br>(V <sub>icm</sub> = 0 V)                                           | T = 25 °C                                                                                                            |      |      | ±200 | μV      |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  |      |      | ±700 |         |
| ΔV <sub>io</sub> /ΔT | Input offset voltage drift                                                                 | -40 °C ≤ T ≤ 125 °C                                                                                                  |      |      | ±5   | μV/°C   |
| I <sub>ib</sub>      | Input bias current <sup>(1)</sup>                                                          | T = 25 °C                                                                                                            |      | 1    | 2    | pA      |
|                      |                                                                                            | -40 °C ≤ T ≤ 85 °C                                                                                                   |      | 10   | 30   |         |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  |      | 75   | 200  |         |
| I <sub>io</sub>      | Input offset current <sup>(1)</sup>                                                        | T = 25 °C                                                                                                            |      | 1    | 2    | pA      |
|                      |                                                                                            | -40 °C ≤ T ≤ 85 °C                                                                                                   |      | 5    | 20   |         |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  |      | 20   | 100  |         |
| A <sub>VD</sub>      | Open loop gain                                                                             | V <sub>CC-</sub> +100 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -100 mV, T = 25 °C                                    | 95   |      |      | dB      |
|                      |                                                                                            | V <sub>CC-</sub> +100 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -100 mV,<br>-40 °C ≤ T ≤ 125 °C                       | 80   |      |      |         |
|                      |                                                                                            | R <sub>L</sub> = 2 kΩ, V <sub>CC-</sub> + 200 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -200 mV,<br>T = 25 °C         | 90   |      |      |         |
|                      |                                                                                            | R <sub>L</sub> = 2 kΩ, V <sub>CC-</sub> + 200 mV ≤ V <sub>OUT</sub> ≤ V <sub>CC+</sub> -200 mV,<br>40 °C ≤ T ≤125 °C | 80   |      |      |         |
| CMR                  | Common-mode rejection ratio<br>20.log(ΔV <sub>io</sub> /ΔV <sub>icm</sub> )                | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> , T = 25 °C                                            | 73   | 94   |      | dB      |
|                      |                                                                                            | V <sub>CC-</sub> -0.1 V ≤ V <sub>icm</sub> ≤ V <sub>CC+</sub> , -40 °C ≤ T ≤ 125 °C                                  | 67   | 86   |      |         |
| V <sub>OH</sub>      | High level output voltage drop<br>(V <sub>OH</sub> = V <sub>CC+</sub> - V <sub>OUT</sub> ) | T = 25 °C                                                                                                            |      |      | 10   | mV      |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  |      |      | 20   |         |
| V <sub>OL</sub>      | Low level output voltage drop<br>(V <sub>OL</sub> = V <sub>OUT</sub> )                     | T = 25 °C                                                                                                            |      |      | 10   |         |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  |      |      | 20   |         |
| I <sub>OUT</sub>     | I <sub>sink</sub> (R <sub>L</sub> connected to V <sub>CC+</sub> )                          | T = 25 °C                                                                                                            | 45   | 60   |      | mA      |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  | 30   |      |      |         |
|                      | I <sub>source</sub> (R <sub>L</sub> connected to V <sub>CC-</sub> )                        | T = 25 °C                                                                                                            | 45   | 65   |      |         |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  | 30   |      |      |         |
| I <sub>CC</sub>      | Supply current (per channel, R <sub>L</sub> > 1 MΩ, V <sub>icm</sub> = 0 V)                | T = 25 °C                                                                                                            |      | 1.7  | 1.9  | mA      |
|                      |                                                                                            | -40 °C ≤ T ≤ 125 °C                                                                                                  |      |      | 1.9  |         |
| AC performance       |                                                                                            |                                                                                                                      |      |      |      |         |
| GBP                  | Gain bandwidth product                                                                     |                                                                                                                      | 17   | 20   |      | MHz     |
| SR                   | Slew rate                                                                                  | AV = 1 V/V, 10% to 90% <sup>(2)</sup>                                                                                | 9    | 11   |      | V/μs    |
| t <sub>s</sub>       | Settling time                                                                              | R <sub>L</sub> = 4.7 kΩ, AV = -1 V/V, to 0.1%, V <sub>in</sub> = 1 Vp-p                                              |      | 450  |      | ns      |
|                      |                                                                                            | R <sub>L</sub> = 4.7 kΩ, AV = -1 V/V, to 0.01%, V <sub>in</sub> = 1 Vp-p <sup>(3)</sup>                              |      | 570  |      |         |
| t <sub>rec</sub>     | Overload recovery time                                                                     | V <sub>OUT</sub> 50 mV from initial value, AV = +1                                                                   |      | 300  |      | ns      |
| Φ <sub>m</sub>       | Phase margin                                                                               |                                                                                                                      |      | 47   |      | degrees |

| Symbol   | Parameter                      | Conditions                                 | Min. | Typ. | Max. | Unit                         |
|----------|--------------------------------|--------------------------------------------|------|------|------|------------------------------|
| GM       | Gain margin                    |                                            |      | 8    |      | dB                           |
| $C_{in}$ | Differential input capacitance |                                            |      | 6.5  |      | pF                           |
|          | Common-mode input capacitance  |                                            |      | 2.5  |      |                              |
| $e_n$    | Input voltage noise density    | $f = 1 \text{ kHz}$                        |      | 30   |      | $\text{nV}/\sqrt{\text{Hz}}$ |
|          |                                | $f = 10 \text{ kHz}$                       |      | 14   |      |                              |
| en p-p   | Input noise voltage            | $0.1 \text{ Hz} \leq f \leq 10 \text{ Hz}$ |      | 10   |      | $\mu\text{Vpp}$              |

1. Guaranteed by design and characterization on a sample of parts, not tested in production
2. Slew rate value is the average of rising and falling values.
3. Settling time at 0.01% is guaranteed by design.

## 4 Typical performance characteristics

$R_L = 10\text{ k}\Omega$  connected to  $V_{CC} / 2$  and  $C_L = 47\text{ pF}$ , unless otherwise specified.

Figure 5. Supply current vs. supply voltage

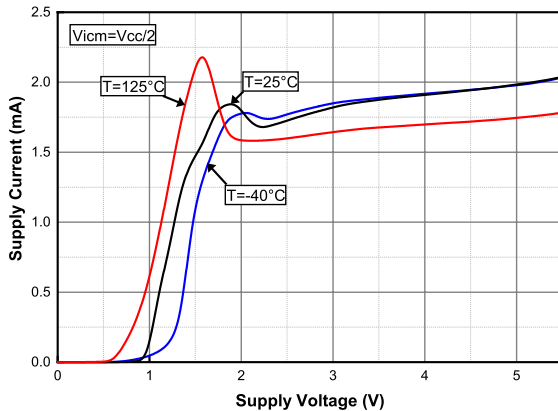


Figure 6. Input offset voltage distribution at  $V_{CC} = 5\text{ V}$

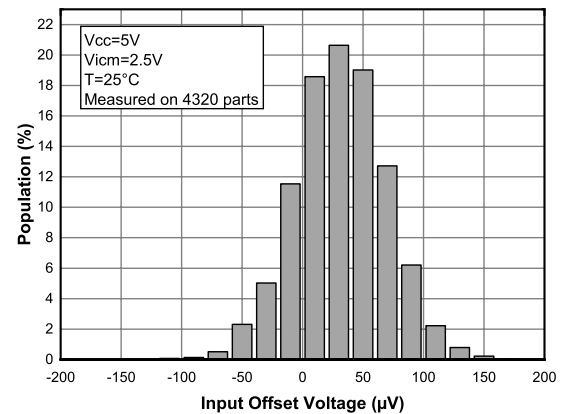


Figure 7. Input offset voltage distribution at  $V_{CC} = 2\text{ V}$

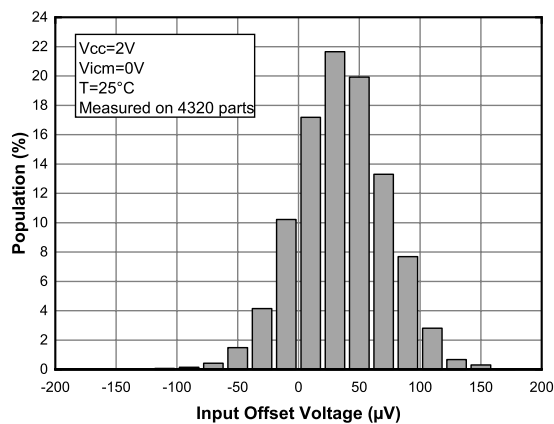


Figure 8. Input offset voltage vs. temperature at  $V_{CC} = 5\text{ V}$

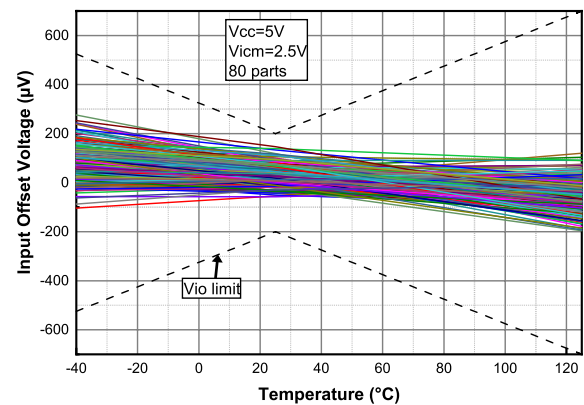


Figure 9. Input offset voltage vs. temperature at  $V_{CC} = 2\text{ V}$

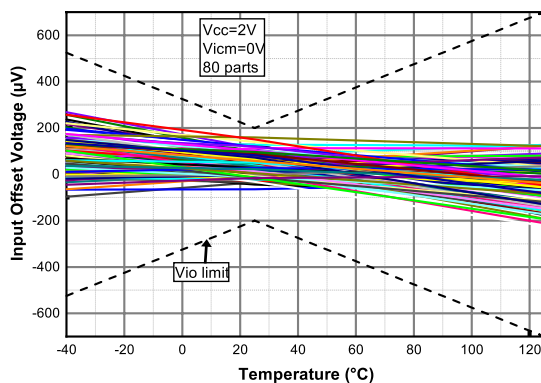
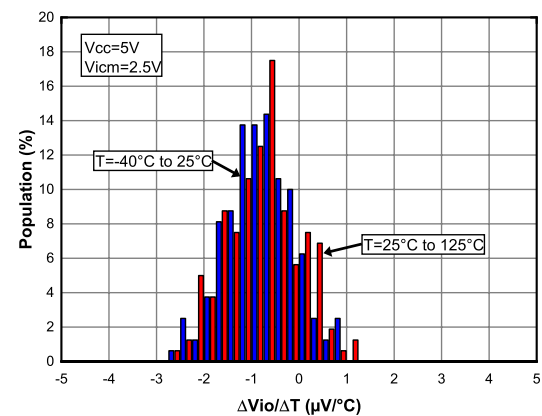
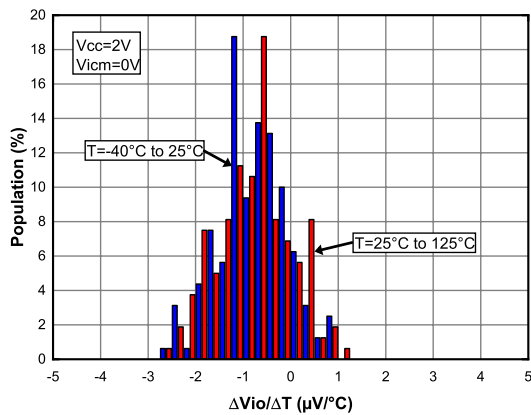


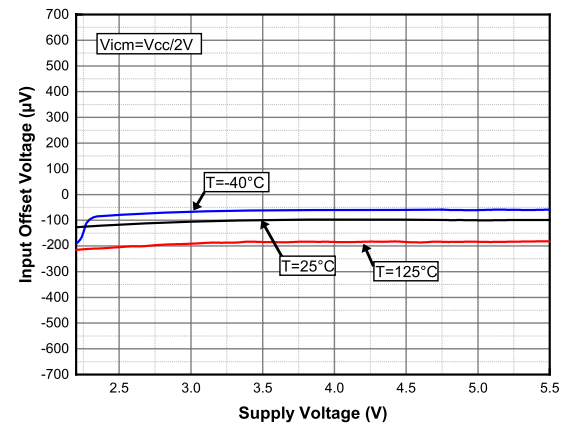
Figure 10. Input offset voltage thermal drift distribution at  $V_{CC} = 5\text{ V}$



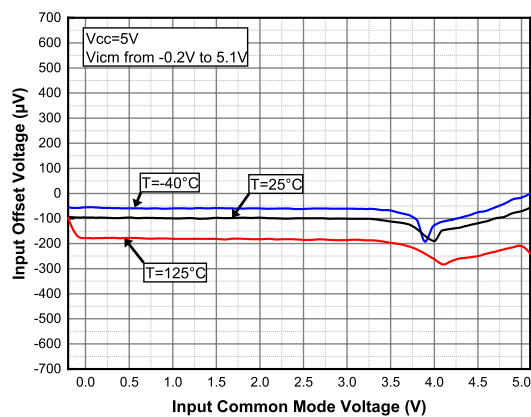
**Figure 11. Input offset voltage thermal drift distribution at  $V_{CC} = 2\text{ V}$**



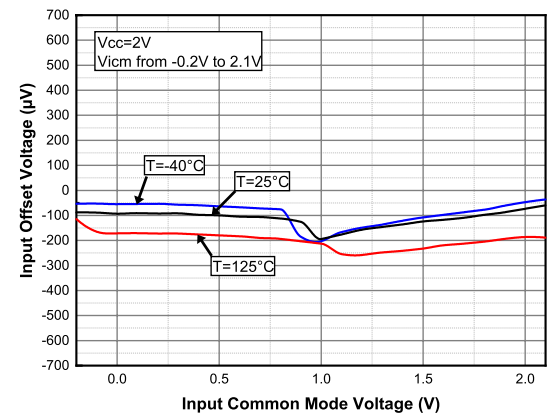
**Figure 12. Input offset voltage vs. supply voltage**



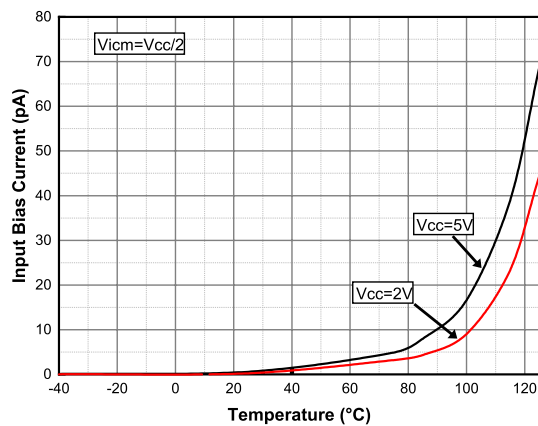
**Figure 13. Input offset voltage vs. common-mode voltage at  $V_{CC} = 5\text{ V}$**



**Figure 14. Input offset voltage vs. common-mode voltage at  $V_{CC} = 2\text{ V}$**



**Figure 15. Input bias current vs. temperature**



**Figure 16. Input bias current vs. common-mode voltage at  $V_{CC} = 5\text{ V}$**

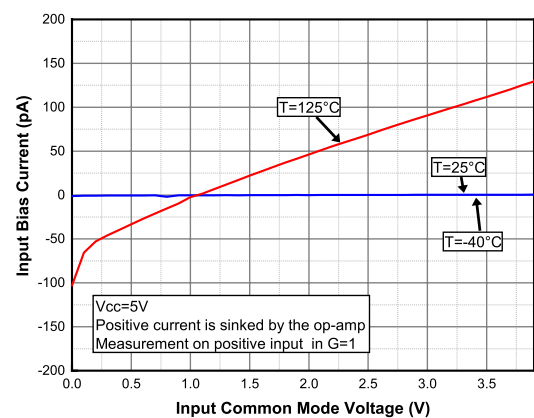


Figure 17. Output current vs. output voltage at  $V_{CC} = 5\text{ V}$

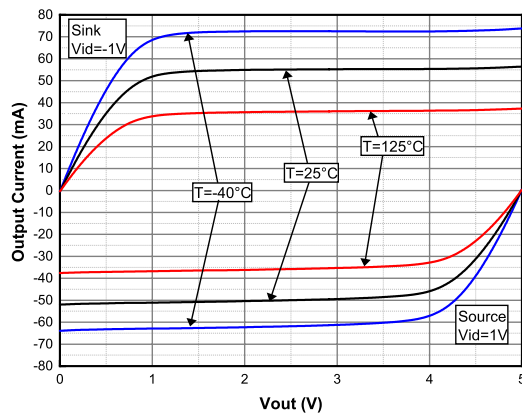


Figure 18. Output current versus output voltage at  $V_{CC} = 2\text{ V}$

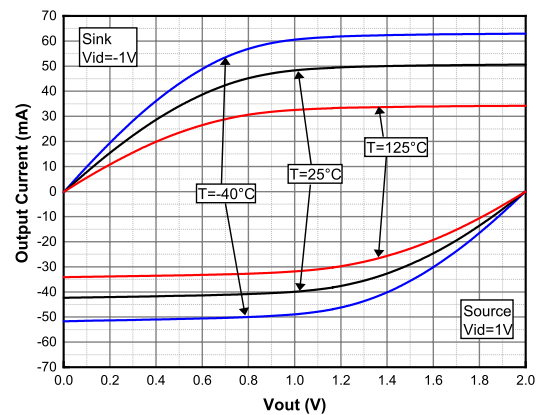


Figure 19. Output saturation voltage ( $V_{OL}$ ) vs. supply voltage

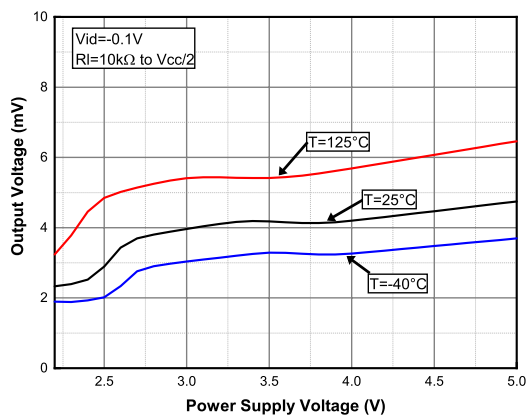


Figure 20. Output saturation voltage ( $V_{OH}$ ) vs. supply voltage

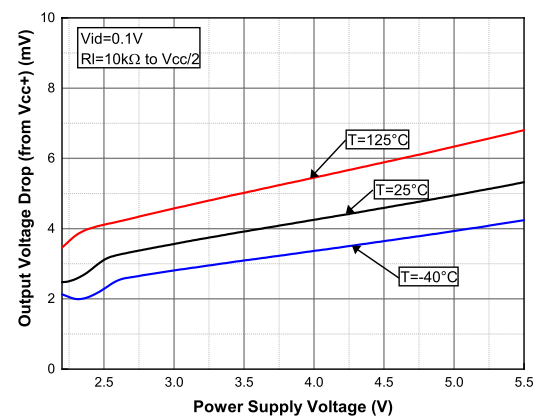


Figure 21. Positive slew rate at  $V_{CC} = 5\text{ V}$

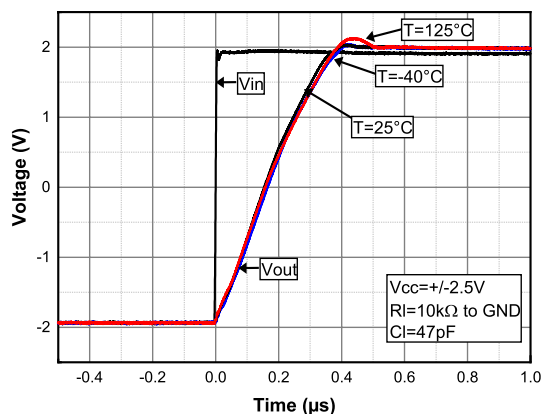


Figure 22. Negative slew rate at  $V_{CC} = 5\text{ V}$

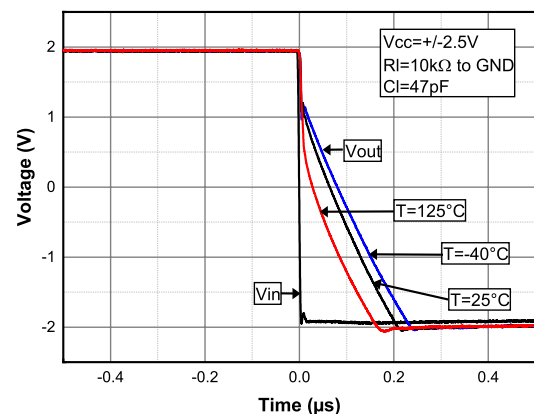


Figure 23. Slew rate vs.  $V_{CC}$

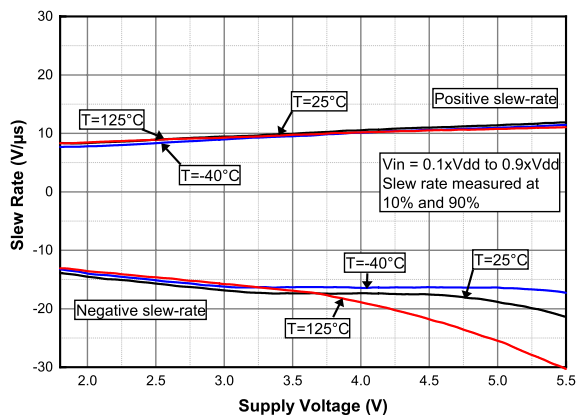


Figure 24. Open loop bode diagram at  $V_{CC} = 5\text{ V}$

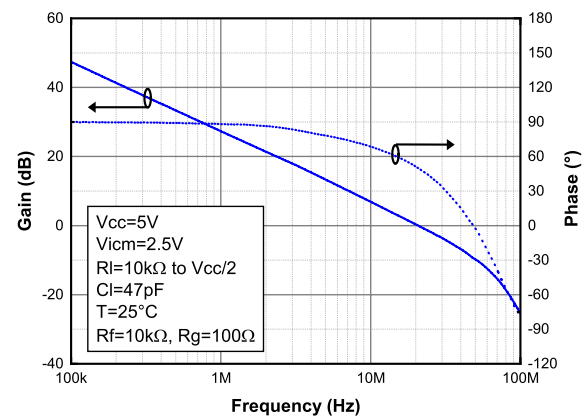


Figure 25. Open loop bode diagram at  $V_{CC} = 2\text{ V}$

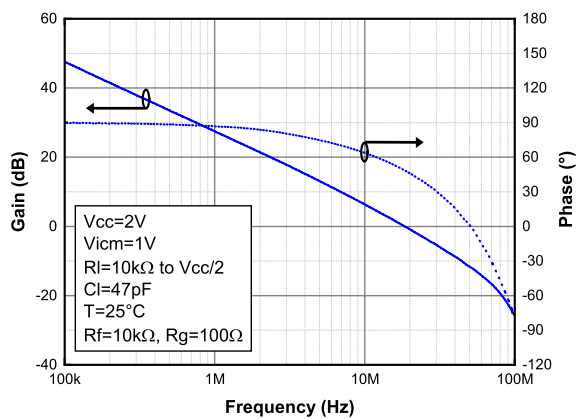


Figure 26. Closed loop bode diagram at  $V_{CC} = 5\text{ V}$

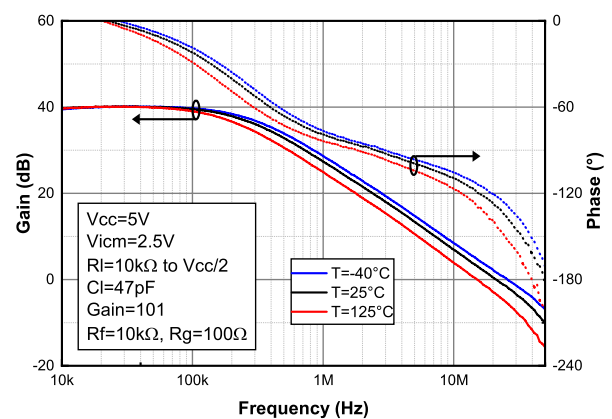


Figure 27. Closed loop bode diagram at  $V_{CC} = 2\text{ V}$

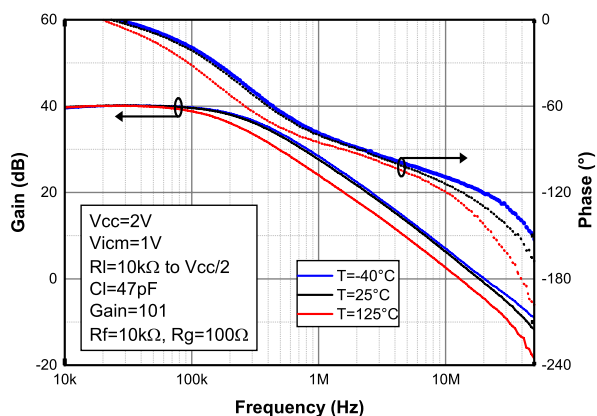


Figure 28. Phase margin vs. common-mode voltage and load current at  $V_{CC} = 5\text{ V}$

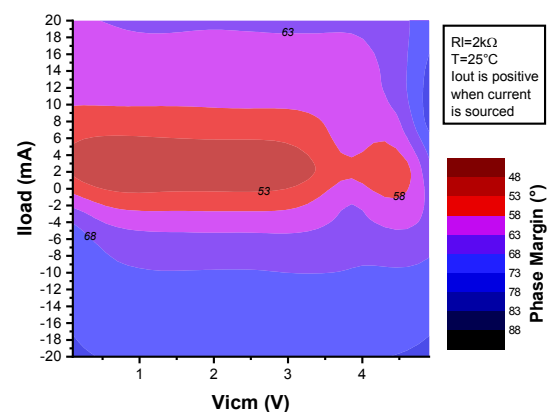


Figure 29. Phase margin vs. capacitive load

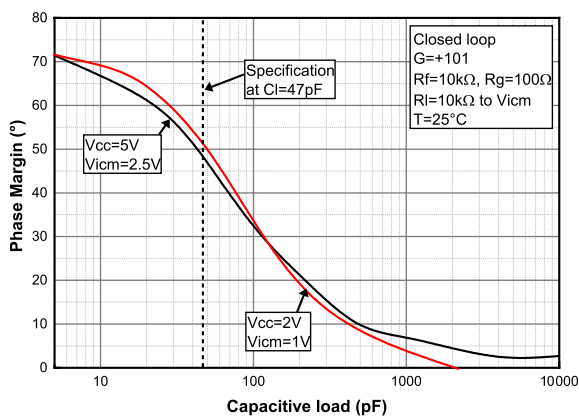


Figure 30. Small step response at  $V_{CC} = 5\text{ V}$

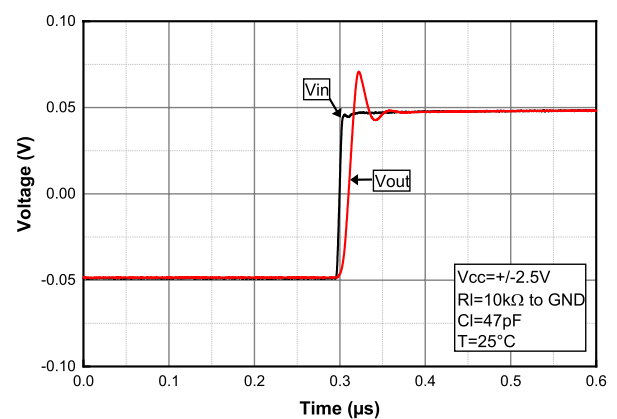


Figure 31. Small step response at  $V_{CC} = 2\text{ V}$

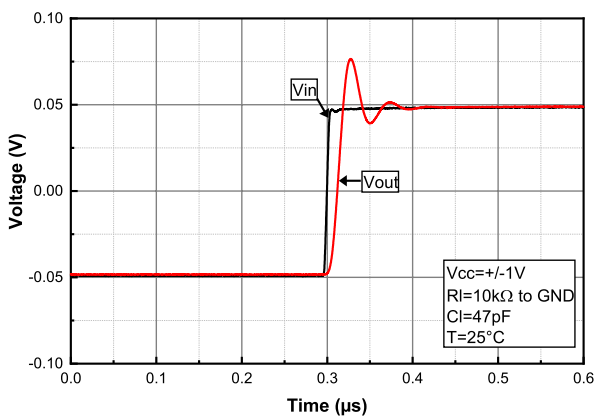


Figure 32. Desaturation from low rail at  $V_{CC} = 5\text{ V}$

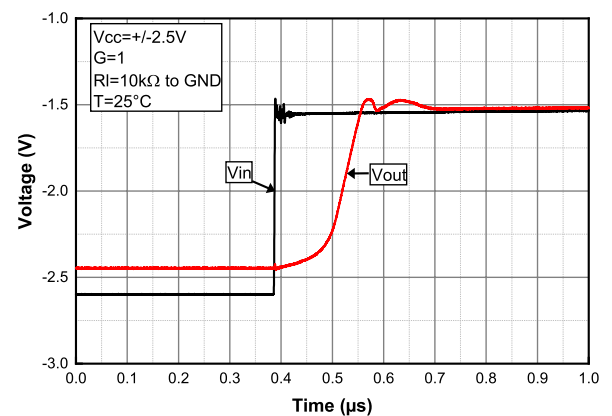


Figure 33. Desaturation from high rail at  $V_{CC} = 5\text{ V}$

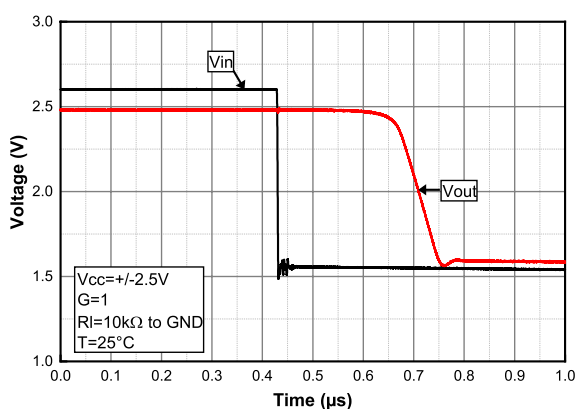


Figure 34. Settling time output high to low at  $V_{CC} = 5\text{ V}$

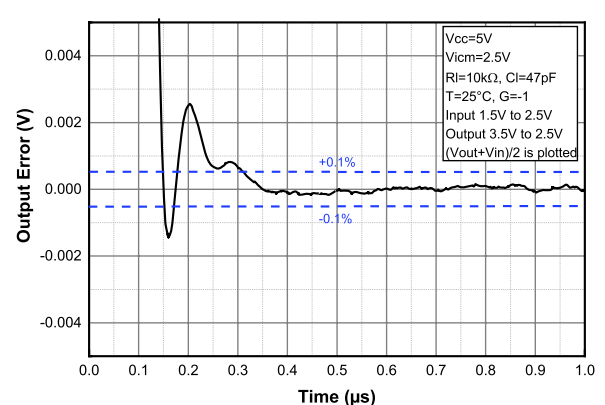


Figure 35. Settling time output low to high at  $V_{CC} = 5\text{ V}$

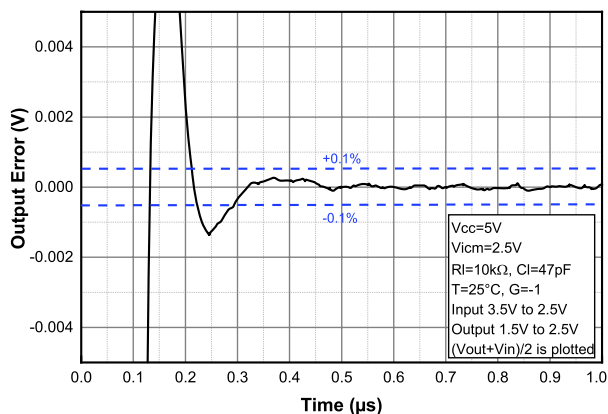


Figure 36. Small step overshoot vs. load capacitance

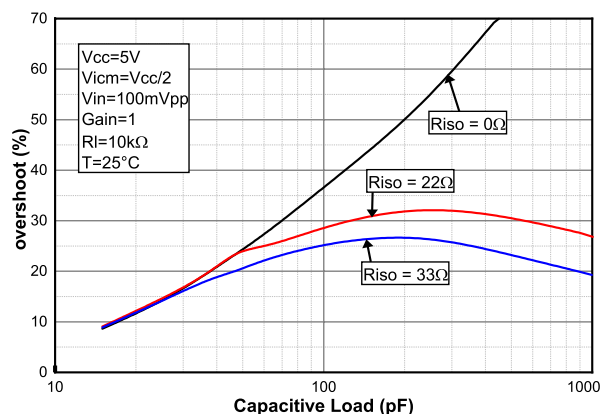


Figure 37. Linearity vs. load resistance at  $V_{CC} = 5\text{ V}$

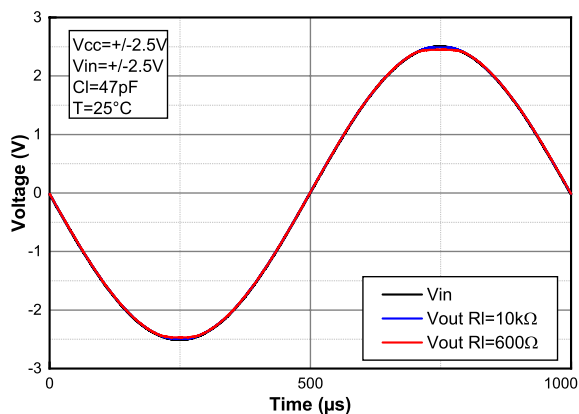


Figure 38. Noise vs. frequency

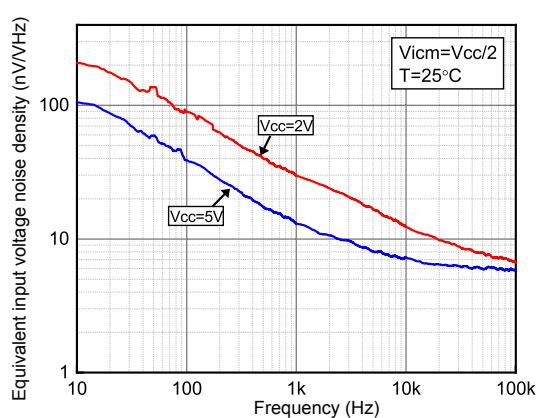


Figure 39. Noise vs. time at  $V_{CC} = 5\text{ V}$

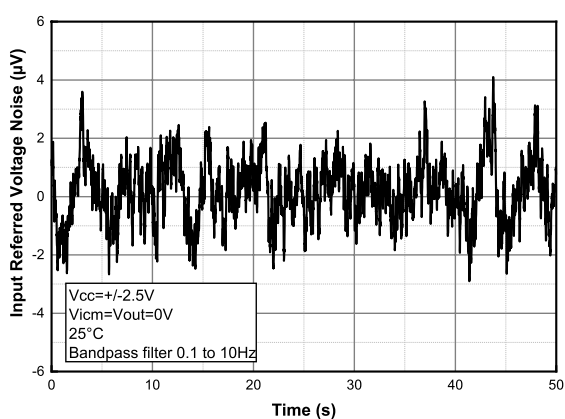


Figure 40. THD+N vs. frequency

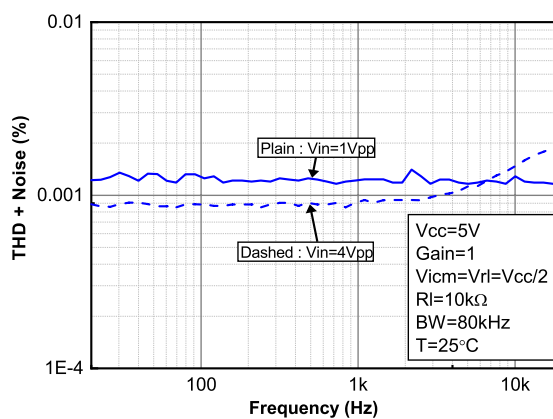


Figure 41. THD+N vs. output voltage

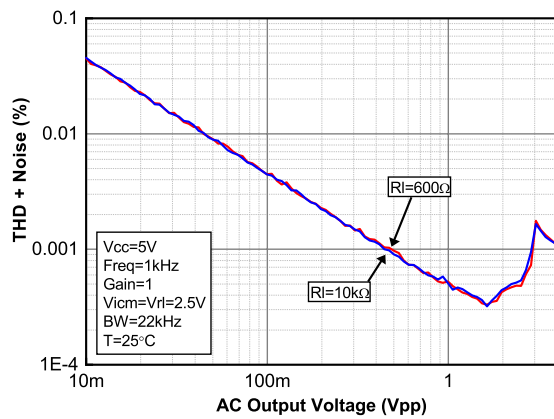


Figure 42. CMRR vs. frequency at  $V_{CC} = 5V$

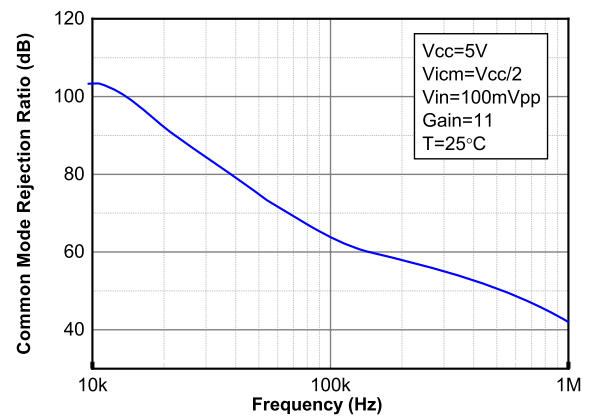


Figure 43. PSRR vs. frequency at  $V_{CC} = 5V$

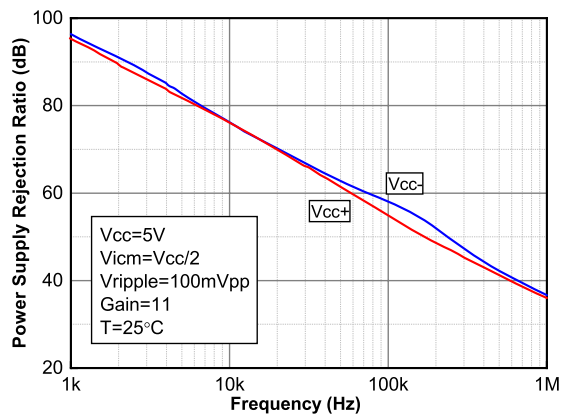


Figure 44. Turn-on time at  $V_{CC} = 5V$

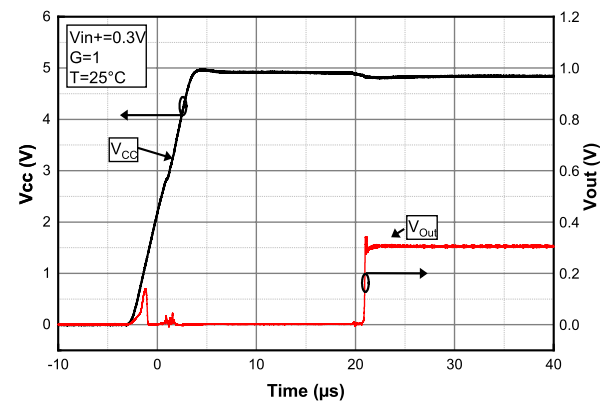
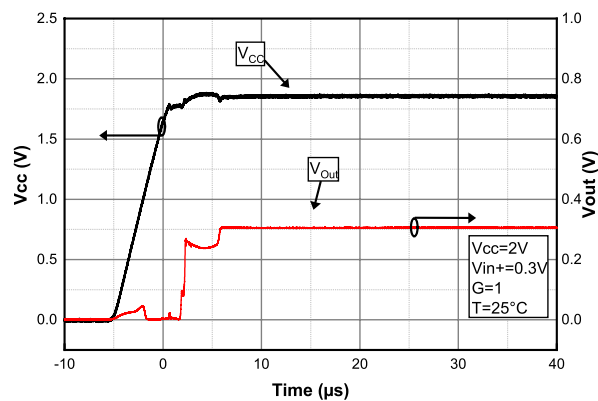


Figure 45. Turn-on time at  $V_{CC} = 2V$



## 5 Application information

### 5.1 Operating voltages

The TSV771, TSV772 and TSV774 devices can operate from 2.0 to 5.5 V. The parameters are fully specified at 2.0 V, 3.3 V and 5 V power supplies. However, the parameters are very stable over the full  $V_{CC}$  range and several characterization curves show the TSV771, TSV772 and TSV774 devices characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from -40 to 125 °C.

The TSV772 device is rail-to-rail input and output and features two input transistor pairs, allowing the op amp to operate over all the common mode range, from  $V_{CC-} - 0.2$  V, to  $V_{CC+} + 0.1$  V. The input pair transition typically occurs at  $V_{CC+} - 1$  V, as seen in Figure 13 and Figure 14. The precision and dynamic performances are particularly optimized on the low pair, from  $V_{CC-} - 0.1$  V to  $V_{CC+} - 1.8$  V, and operating in this  $V_{icm}$  range is advised for the best performance whenever possible. Besides, operating near the pair transition should be avoided when precision is a concern, as CMRR can be lower in these conditions.

### 5.2 Input offset voltage drift over the temperature

The input voltage drift variation over the temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset ( $V_{io}$ ) is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during the production at the application level. The maximum input voltage drift over the temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift overtemperature is computed using the following equation:

$$\frac{\Delta V_{io}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25^{\circ}\text{C})}{T - 25^{\circ}\text{C}} \right| \quad (1)$$

Where  $T = -40$  °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a  $C_{pk}$  (process capability index) greater than 1.3. The absolute worst case value between -40 °C and 125 °C is reported in the datasheet.

### 5.3 Unused channel

When one of the two channels of TSV771, TSV772 and TSV774 are not used, it must be properly connected in order to avoid internal oscillations that can negatively impact the signal integrity on the other channel, as well as the current consumption. Two different configurations can be used:

Gain or buffer configuration: the channel can be set in gain, the input can be set to any voltage within the  $V_{icm}$  operating range.

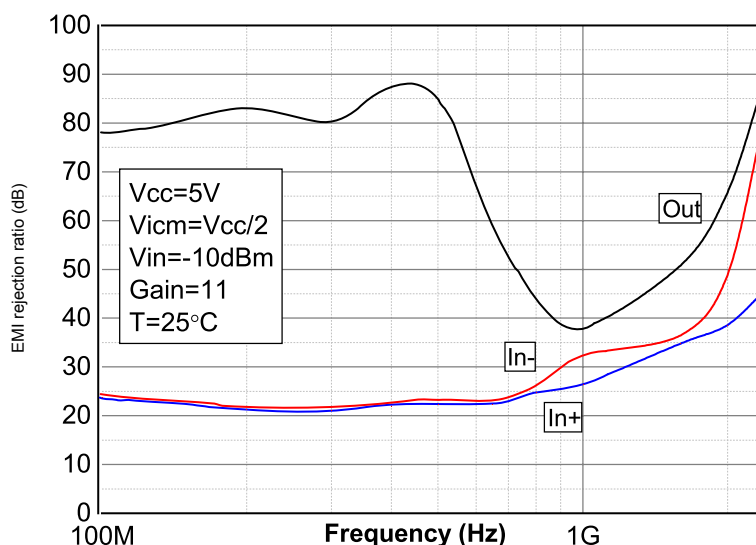
Comparator configuration: the channel can be set to a comparator configuration (without negative feedback). In this case, positive and negative inputs can be set to any value provided these values are significantly different (100 mV or more, to avoid oscillation between positive and negative state and within operating range) and the differential input is lower than the maximum specified in the operating range.

### 5.4 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined in Eq. (2):

$$EMIRR = 20 \cdot \log \left( \frac{V_{in\ pp}}{\Delta V_{io}} \right) \quad (2)$$

The TSV771, TSV772 and TSV774 have been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As can be seen in Figure 46, EMI rejection ratio has been measured on both inputs and output, from 400 MHz to 2.4 GHz.

**Figure 46. EMIRR on In+, In- and Out pins**


EMIRR performances might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins.

These capacitances help to minimize the impedance of these nodes at high frequencies.

## 5.5 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSV772 is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A \quad (3)$$

$T_J$  is the die junction temperature

$P_D$  is the power dissipated in the package

$\theta_{JA}$  is the junction-to-ambient thermal resistance of the package

$T_A$  is the ambient temperature

The power dissipated in the package  $P_D$  is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$P_D = (V_{CC} \times I_{CC}) + (V_{CC} + -V_{OUT}) \times I_{Load}$  when the op amp is sourcing the current.

$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times I_{Load}$  when the op amp is sinking the current.

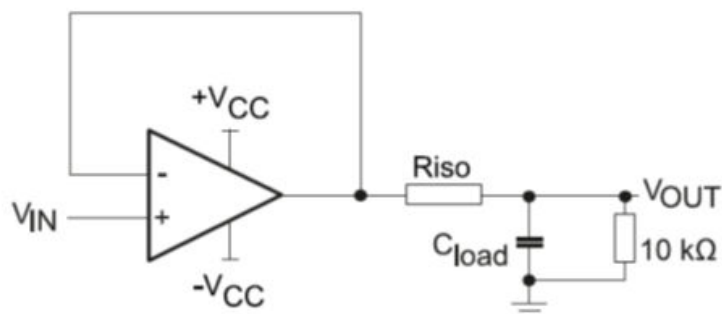
Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

## 5.6 Capacitive load and stability

Stability analysis must be performed for large capacitive loads over 47 pF; increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity-gain configuration, stability can be improved by inserting a small resistor  $R_{ISO}$  (10  $\Omega$  to 33  $\Omega$ ) in series with the output (see Figure 36). This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_{ISO} / R_L$ .  $R_{ISO}$  modifies the maximum capacitive load acceptable from a stability point of view, as described in Figure 47:

Figure 47. Test configuration for  $R_{ISO}$

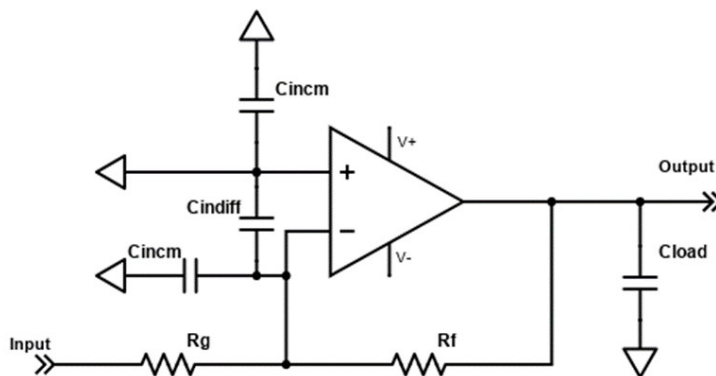


Please note that  $R_{ISO} = 33 \Omega$  is sufficient to make the TSV771 and TSV772 stable whatever the capacitive load.

## 5.7 Resistor values for high speed op amp design

Due to its high gain bandwidth product (GBP), this op amp is particularly sensitive to parasitic impedances. Board parasitics should be taken into account in any sensitive design. Indeed, excessive parasitic (both capacitive and inductive) in the op amp frequency range can alter performances and stability. These issues can often be mitigated by lowering the resistive impedances. More specifically, the RC network created by the schematic resistors ( $R_f$  and  $R_g$ ) and the parasitic capacitances of both the op amp (as documented in Table 1 to Table 7 and illustrated in Figure 48) and the PCB can generate a pole below or in the same order of magnitude than the closed-loop bandwidth of the circuit. In this case, the feedback circuit is not able to fully play its role at high frequency, and the application can be unstable. This issue can happen when the schematic gain is low (typically  $< 5$ ), or the device is used in follower mode with a resistor in the feedback. In these cases, it is advised to use a low value feedback resistor ( $R_f$ ), typically  $1 \text{ k}\Omega$ .

Figure 48. Inverting amplifier configuration with parasitic input capacitances

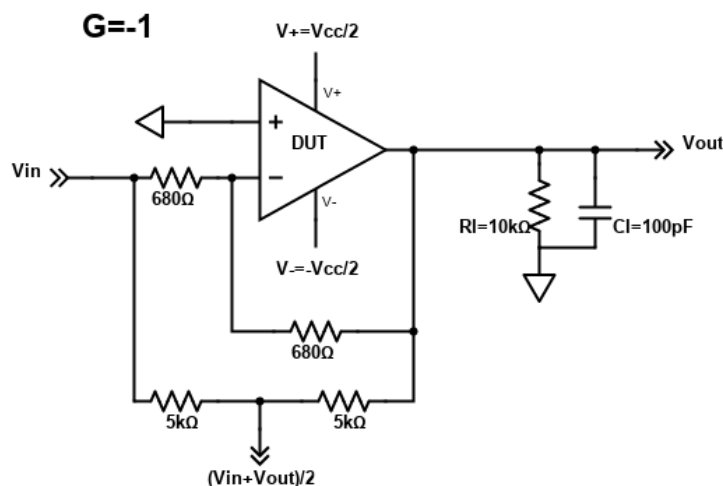


Also, some designs use an input resistor on the positive input, generally of the same value than the input resistance on the negative input. This resistor can be useful to balance the input currents on the positive and negative inputs, and reduce the impact of those input currents on precision. However, this is not useful on the TSV772 as the input currents are very low. Furthermore, this resistor can also interact with the input capacitances to generate a pole. The frequency of this pole should be kept higher than the closed-loop bandwidth frequency. The macromodel provided takes into account the circuit parasitic capacitors. Thus, a transient SPICE simulation (100 mV step) is an easy way to evaluate the stability of the application. However, this cannot replace a hardware evaluation of the application circuit.

## 5.8 Settling time

Settling time in an application can be defined as the amount of time between the input changes, and the output reaching its final value. It is usually defined with a given tolerance, so the output stability is reached when the output stays within the given range around the final value. In [Figure 30](#) and [Figure 31](#), the settling time is measured in an inverting configuration, using the so-called “false summing node” circuit.

**Figure 49. Settling time measurement configuration**



This circuit is used with a step input voltage from a positive or negative value, to 0 V. The measurement point being  $(V_{in} + V_{out}) / 2$ , and  $V_{out}$  being in an ideal circuit equal to  $V_{in}$ ; the measurement point gives half of the error on  $V_{out}$ , comparatively to  $V_{in}$ . This error is compared to the tolerance, 0.1% for this circuit, to deduce the settling time. This characteristic is particularly useful when driving an ADC. It is related to the slew rate, GBP and stability of the circuit. It also varies with the circuit gain, the circuit load, and the input voltage step value. However, computing the value of the settling time in a given configuration is not straightforward. The macromodel can give a good estimation, but prototyping can be needed for fine circuit optimization.

## 5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

## 5.10 Decoupling capacitor

In order to ensure op amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op amp supply pins. A good decoupling helps to reduce electromagnetic interference impact.

## 5.11 Macro model

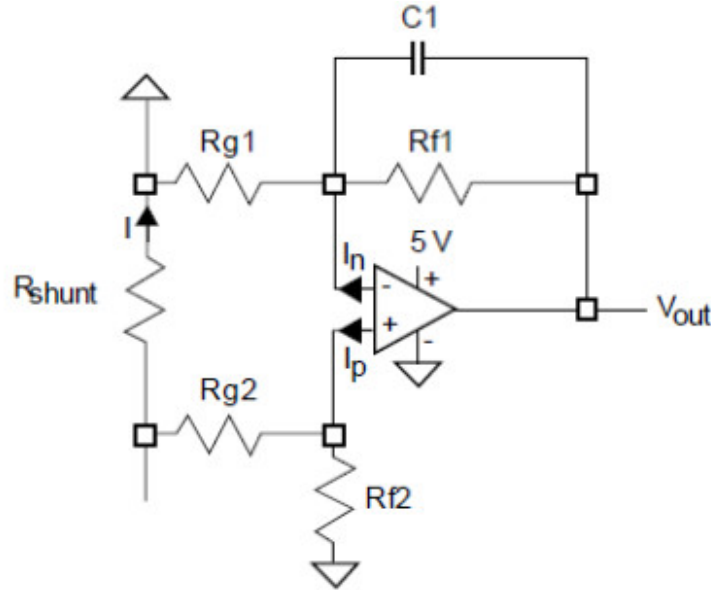
Accurate macromodels of the TSV771, TSV772 and TSV774 devices are available on the STMicroelectronics' website at: [www.st.com](http://www.st.com). These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV771, TSV772 and TSV774 operational amplifiers. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right operational amplifier, but they do not replace on-board measurements.

## 6 Typical applications

### 6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSV771, TSV772 and TSV774 (see Figure 50).

**Figure 50. Low-side current sensing schematic**



$V_{out}$  can be expressed as follows:

$$V_{Out} = R_{shunt} \cdot I \left( 1 - \frac{R_{g2}}{R_{g2} + R_{f2}} \right) \cdot \left( 1 + \frac{R_{f1}}{R_{g1}} \right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left( 1 + \frac{R_{f1}}{R_{g1}} \right) - I_n \cdot R_{f1} - V_{io} \cdot \left( 1 + \frac{R_{f1}}{R_{g1}} \right) \quad (4)$$

Assuming that  $R_{f2} = R_{f1} = R_f$  and  $R_{g2} = R_{g1} = R_g$ , this equation can be simplified as follows:

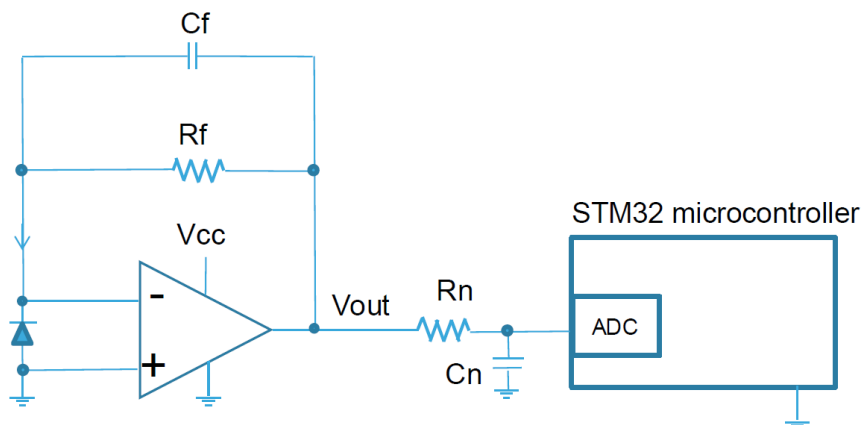
$$V_{Out} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{io} \cdot \left( 1 + \frac{R_f}{R_g} \right) + R_f \cdot I_{io} \quad (5)$$

The main advantage of using the TSV771, TSV772 and TSV774 for a low-side current sensing relies on its low  $V_{io}$ , compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of  $R_{g1}$ ,  $R_{g2}$ ,  $R_{f1}$ , and  $R_{f2}$ , to maximize the accuracy of the measurement.

### 6.2 Photodiode transimpedance amplification

The TSV7722, with high bandwidth and slew rate, is well suited for photodiode signal conditioning in a transimpedance amplifier circuit. This application is useful in high performance UV sensors, smoke detectors or particle sensors.

Figure 51. Photodiode transimpedance amplifier circuit



The transimpedance amplifier circuit converts the small photodiode output current in the nA range, into a voltage signal readable by an ADC following Eq. (6):

$$V_{out} = R_f \cdot I_{photodiode} \quad (6)$$

The feedback resistance is usually in the MΩ range, in order to get a large enough voltage output range. However, together with the diode parasitic capacitance, the op amp input capacitances and the PCB stray capacitance, this feedback network creates a pole that makes the circuit oscillate. Using a small (few pF) capacitor in parallel with the feedback resistor is mandatory to stabilize the circuit. The value of this capacitor can be tuned to optimize the application settling time with a SPICE simulation using the op amp macromodel, or by prototyping.

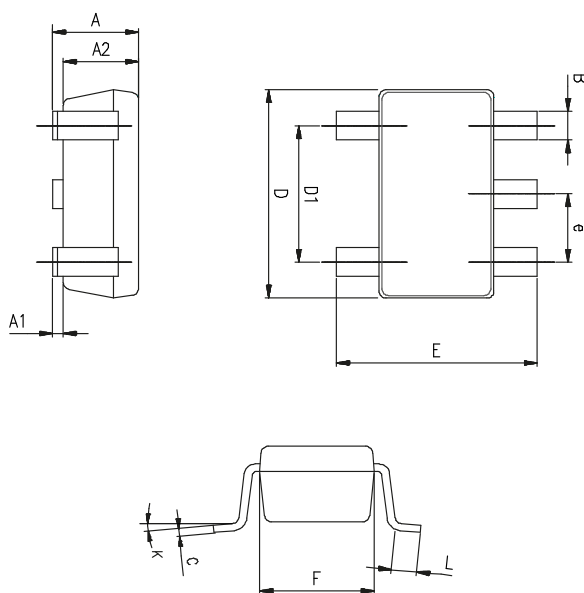
For more details on tuning this circuit, please read the application note AN4451.

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 7.1 SOT23-5 package information

**Figure 52. SOT23-5 package outline**

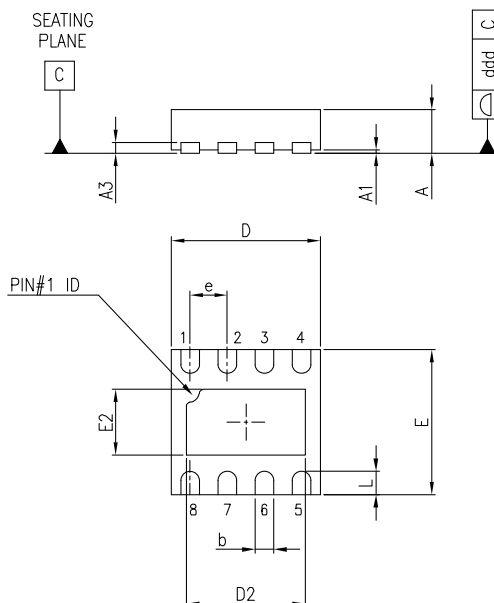


**Table 10. SOT23-5 mechanical data**

| Dimensions |             |      |      |        |       |       |
|------------|-------------|------|------|--------|-------|-------|
| Symbol     | Millimeters |      |      | Inches |       |       |
|            | Min.        | Typ. | Max. | Min.   | Typ.  | Max.  |
| A          | 0.90        | 1.20 | 1.45 | 0.035  | 0.047 | 0.057 |
| A1         |             |      | 0.15 |        |       | 0.006 |
| A2         | 0.90        | 1.05 | 1.30 | 0.035  | 0.041 | 0.051 |
| B          | 0.35        | 0.40 | 0.50 | 0.014  | 0.016 | 0.020 |
| C          | 0.09        | 0.15 | 0.20 | 0.004  | 0.006 | 0.008 |
| D          | 2.80        | 2.90 | 3.00 | 0.110  | 0.114 | 0.118 |
| D1         |             | 1.90 |      |        | 0.075 |       |
| e          |             | 0.95 |      |        | 0.037 |       |
| E          | 2.60        | 2.80 | 3.00 | 0.102  | 0.110 | 0.118 |
| F          | 1.50        | 1.60 | 1.75 | 0.059  | 0.063 | 0.069 |
| L          | 0.10        | 0.35 | 0.60 | 0.004  | 0.014 | 0.024 |
| K          | 0°          |      | 10°  | 0°     |       | 10°   |

## 7.2 DFN8 2x2 package information

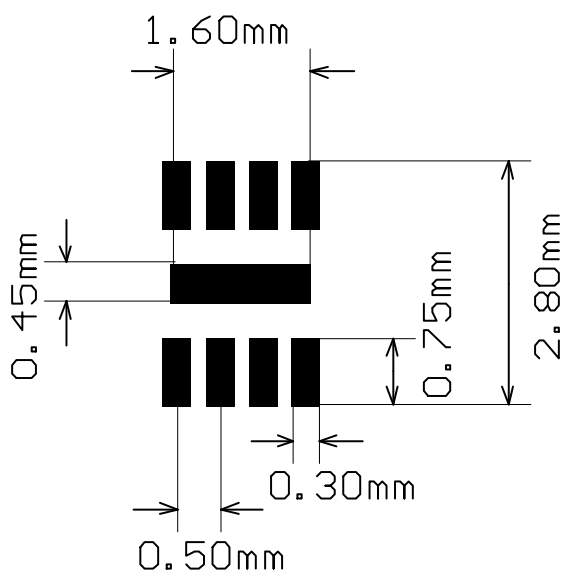
**Figure 53. DFN8 2x2 package outline**



**Table 11. DFN8 2x2 package mechanical data**

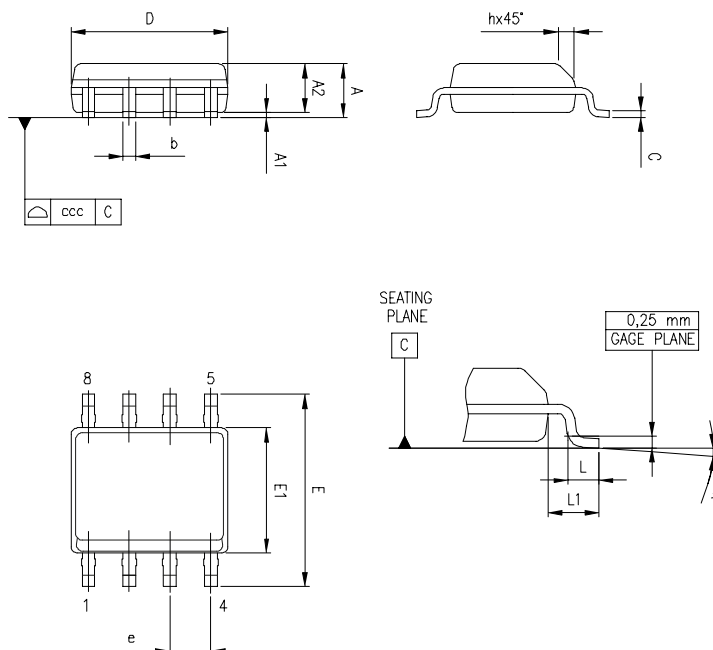
| Ref. | Dimensions  |       |       |        |       |       |
|------|-------------|-------|-------|--------|-------|-------|
|      | Millimeters |       |       | Inches |       |       |
|      | Min.        | Typ.  | Max.  | Min.   | Typ.  | Max.  |
| A    | 0.51        | 0.55  | 0.60  | 0.020  | 0.022 | 0.024 |
| A1   |             |       | 0.05  |        |       | 0.002 |
| A3   |             | 0.15  |       |        | 0.006 |       |
| b    | 0.18        | 0.25  | 0.30  | 0.007  | 0.010 | 0.012 |
| D    | 1.85        | 2.00  | 2.15  | 0.073  | 0.079 | 0.085 |
| D2   | 1.45        | 1.60  | 1.70  | 0.057  | 0.063 | 0.067 |
| E    | 1.85        | 2.00  | 2.15  | 0.073  | 0.079 | 0.085 |
| E2   | 0.75        | 0.90  | 1.00  | 0.030  | 0.035 | 0.039 |
| e    |             | 0.50  |       |        | 0.020 |       |
| L    | 0.225       | 0.325 | 0.425 | 0.009  | 0.013 | 0.017 |
| ddd  |             |       | 0.08  |        |       | 0.003 |

Figure 54. DFN8 2x2 recommended footprint



## 7.3 SO8 package information

**Figure 55. SO8 package outline**

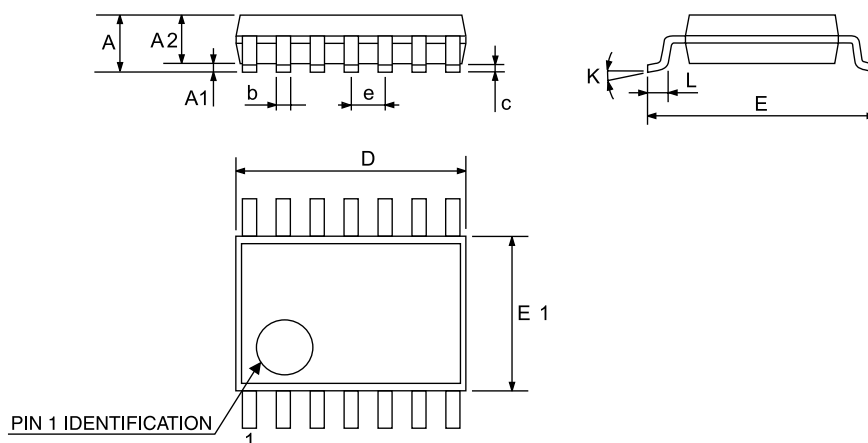


**Table 12. SO-8 mechanical data**

| Dim. | mm   |      |      | Inches |       |       |
|------|------|------|------|--------|-------|-------|
|      | Min. | Typ. | Max. | Min.   | Typ.  | Max.  |
| A    |      |      | 1.75 |        |       | 0.069 |
| A1   | 0.1  |      | 0.25 | 0.004  |       | 0.01  |
| A2   | 1.25 |      |      | 0.049  |       |       |
| b    | 0.28 |      | 0.48 | 0.011  |       | 0.019 |
| c    | 0.17 |      | 0.23 | 0.007  |       | 0.01  |
| D    | 4.8  | 4.9  | 5    | 0.189  | 0.193 | 0.197 |
| E    | 5.8  | 6    | 6.2  | 0.228  | 0.236 | 0.244 |
| E1   | 3.8  | 3.9  | 4    | 0.15   | 0.154 | 0.157 |
| e    |      | 1.27 |      |        | 0.05  |       |
| h    | 0.25 |      | 0.5  | 0.01   |       | 0.02  |
| L    | 0.4  |      | 1.27 | 0.016  |       | 0.05  |
| L1   |      | 1.04 |      |        | 0.04  |       |
| k    | 0    |      | 8 °  | 1 °    |       | 8 °   |
| ccc  |      |      | 0.1  |        |       | 0.004 |

## 7.4 TSSOP14 package information

**Figure 56.** TSSOP14 package outline



**Table 13.** TSSOP14 package mechanical data

| Symbol | Dimensions  |          |      |        |            |        |
|--------|-------------|----------|------|--------|------------|--------|
|        | Millimeters |          |      | Inches |            |        |
|        | Min.        | Typ.     | Max. | Min.   | Typ.       | Max.   |
| A      |             |          | 1.2  |        |            | 0.047  |
| A1     | 0.05        |          | 0.15 | 0.002  | 0.004      | 0.006  |
| A2     | 0.8         | 1        | 1.05 | 0.031  | 0.039      | 0.041  |
| b      | 0.19        |          | 0.30 | 0.007  |            | 0.012  |
| c      | 0.09        |          | 0.20 | 0.004  |            | 0.0089 |
| D      | 4.9         | 5        | 5.1  | 0.193  | 0.197      | 0.201  |
| E      | 6.2         | 6.4      | 6.6  | 0.244  | 0.252      | 0.260  |
| E1     | 4.3         | 4.4      | 4.48 | 0.169  | 0.173      | 0.176  |
| e      |             | 0.65 BSC |      |        | 0.0256 BSC |        |
| K      | 0°          |          | 8°   | 0°     |            | 8°     |
| L1     | 0.45        | 0.60     | 0.75 | 0.018  | 0.024      | 0.030  |

## 7.5 QFN16 3x3 wettable flank package information

Figure 57. QFN16 3x3 mm wettable flank drawing outline

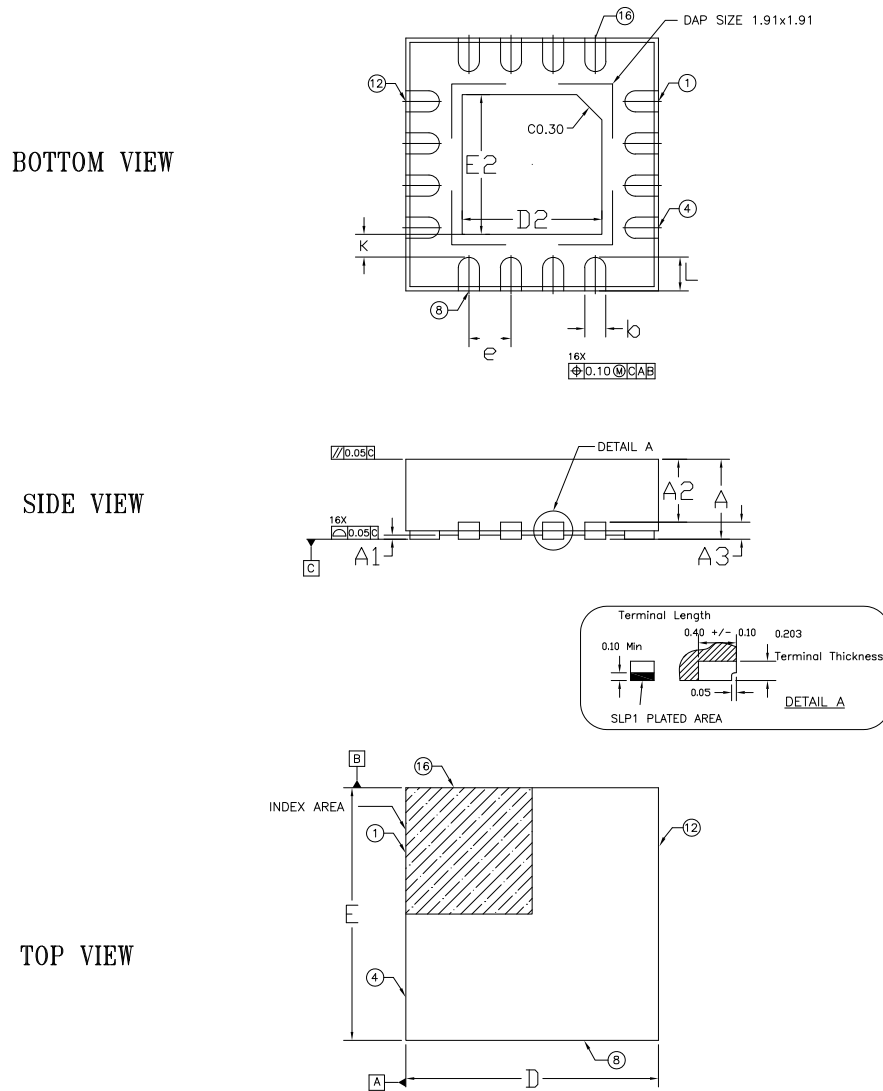
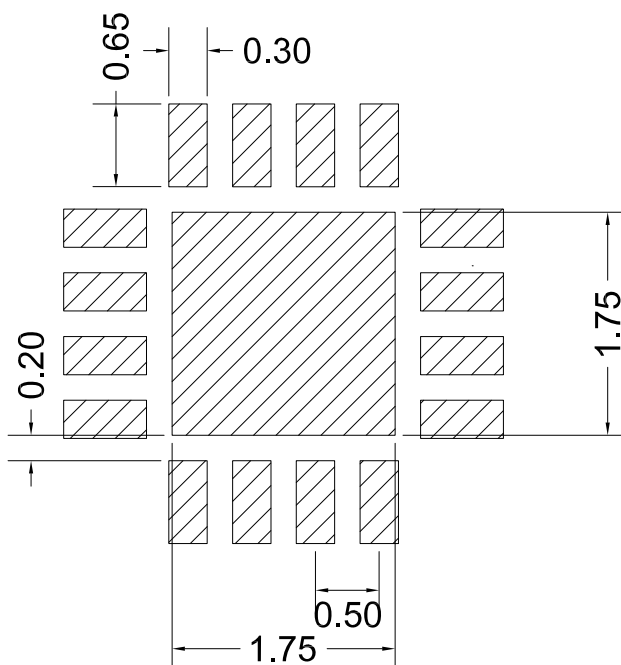


Table 14. QFN16 3x3 wettable flank mechanical data

| Ref. | Dimensions  |      |      |        |       |       |
|------|-------------|------|------|--------|-------|-------|
|      | Millimeters |      |      | Inches |       |       |
|      | Min.        | Typ. | Max. | Min.   | Typ.  | Max.  |
| A    | 0,90        | 0,95 | 1,00 | 0,035  | 0,037 | 0,039 |
| A1   | 0,00        |      | 0,05 | 0,000  |       | 0,002 |
| A2   |             | 0,75 |      |        | 0,030 |       |
| A3   |             | 0,20 |      |        | 0,008 |       |
| b    | 0,20        | 0,25 | 0,30 | 0,008  | 0,010 | 0,012 |
| D    |             | 3,00 |      |        | 0,118 |       |
| E    |             | 3,00 |      |        | 0,118 |       |
| e    |             | 0,50 |      |        | 0,020 |       |
| D2   | 1,56        | 1,66 | 1,76 | 0,061  | 0,065 | 0,069 |
| E2   | 1,56        | 1,66 | 1,76 | 0,061  | 0,065 | 0,069 |
| K    |             | 0,27 |      |        | 0,011 |       |
| L    | 0,30        | 0,40 | 0,50 | 0,012  | 0,016 | 0,020 |

Figure 58. QFN16 3x3 wettable flank recommended footprint



## 8 Ordering information

**Table 15. Order code**

| Order code  | Temperature range                              | Package  | Marking |
|-------------|------------------------------------------------|----------|---------|
| TSV771ILT   | -40 to +125 °C                                 | SOT23-5  | K236    |
| TSV772IQ2T  |                                                | DFN8 2x2 | K5R     |
| TSV772IST   |                                                | MiniSO8  | K5R     |
| TSV772IDT   |                                                | SO8      | TSV772I |
| TSV774IPT   |                                                | TSSOP14  | TSV774  |
| TSV774IQ5T  |                                                | QFN16    | K2R     |
| TSV771IYLT  | -40 to +125 °C Automotive grade <sup>(1)</sup> | SOT23-5  | K237    |
| TSV772IYST  |                                                | MiniSO8  | K231    |
| TSV772IYDT  |                                                | SO8      | TSV772Y |
| TSV774IYPT  |                                                | TSSOP14  | TSV774Y |
| TSV774IYQ5T |                                                | QFN16    | K2S     |

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent. For qualification status detail, check "Maturity Status Link" on the first page of the datasheet, then, the "Quality & Reliability" tab on [www.st.com](http://www.st.com).

## Revision history

**Table 16. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                               |
|-------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-Oct-2021 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                      |
| 25-Nov-2021 | 2        | Updated CDM value in Table 2 and Table 9. Order code.                                                                                                                                                                                                                                                                                                                 |
| 15-Jun-2022 | 3        | Added new part number TSV771, new SOT23-5 package, new Section 1.1 and new Section 7.1.<br>Updated Section 8.<br>Minor text changes.                                                                                                                                                                                                                                  |
| 19-Dec-2022 | 4        | Added lib and lio new values, $-40\text{ }^{\circ}\text{C} \leq T \leq 85\text{ }^{\circ}\text{C}$ conditions in Table 5 and Table 7.                                                                                                                                                                                                                                 |
| 05-Jun-2023 | 5        | Added new part number TSV774, new <a href="#">Section 1.3</a> , new <a href="#">Section 7.4 TSSOP14 package information</a> and <a href="#">Section 7.5 QFN16 3x3 wettable flank package information</a> .<br>Updated figure, maturity status link, related products and description on the cover page, <a href="#">Table 15. Order code</a> .<br>Minor text changes. |

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