

54ACT11241, 74ACT11241 OCTAL BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCAS011B - D2957, JULY 1987 - REVISED APRIL 1993

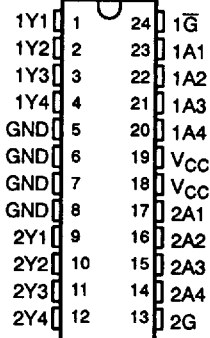
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Inputs Are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages, Plastic Shrink Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

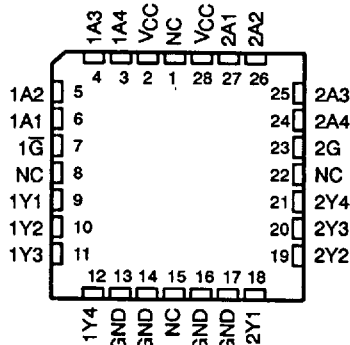
These octal buffers or line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the ACT11240 and ACT11244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\bar{G}$ (active-low output control) inputs, and complementary G and $\bar{G}$ inputs. These devices feature high fan-out.

The 54ACT11241 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11241 is characterized for operation from -40°C to 85°C.

54ACT11241 ... JT PACKAGE
74ACT11241 ... DB, DW OR NT PACKAGE
(TOP VIEW)



54ACT11241 ... FK PACKAGE
(TOP VIEW)



NC - No internal connection

FUNCTION TABLE

OUTPUT CONTROL $\bar{1G}$	DATA INPUT 1A	OUTPUT 1Y	OUTPUT CONTROL 2G	DATA INPUT 2A	OUTPUT 2Y
H	X	Z	L	X	Z
L	L	L	H	L	L
L	H	H	H	H	H

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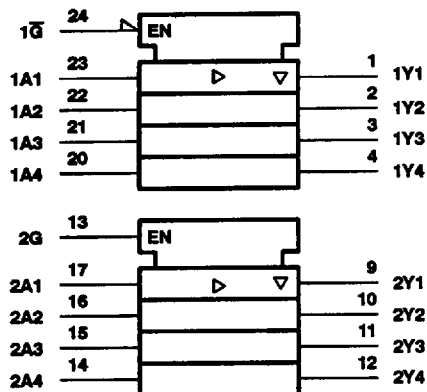
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WITH 3-STATE OUTPUTS

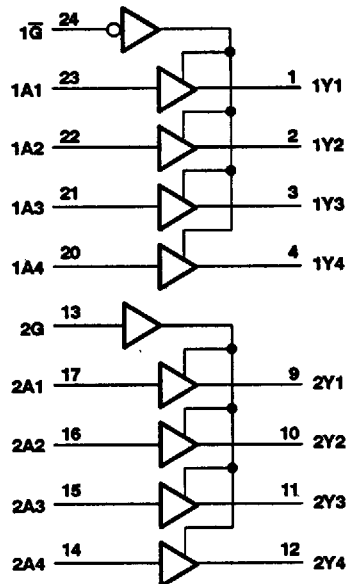
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

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recommended operating conditions

		54ACT11241		74ACT11241		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–24		–24	mA
I _{OL}	Low-level output current		24		24	mA
ΔI/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = – 50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I _{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = – 50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA†	5.5 V					1.65			
	I _{OL} = 75 mA†	5.5 V							1.65	
I _{OZ}	V _O = V _{CC} or GND	5.5 V			± 0.5		± 10		± 5	μA
I _I	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1		± 1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		160		80	μA
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1		1	mA
C _i	V _I = V _{CC} or GND	5 V			4					pF
C _o	V _O = V _{CC} or GND	5 V			10					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.



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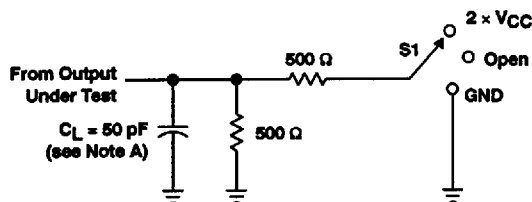
switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11241		74ACT11241		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6.6	9	1.5	10.7	1.5	10	ns
t_{PHL}			1.5	6.3	8.5	1.5	9.5	1.5	9.1	
t_{PZH}	G or $\bar{G}$	Y	1.5	7.5	11.3	1.5	13	1.5	12.3	
t_{PZL}			1.5	7.4	10.5	1.5	11.9	1.5	11.3	
t_{PHZ}	G or $\bar{G}$	Y	1.5	7.6	10.6	1.5	11.4	1.5	11	
t_{PLZ}			1.5	8.2	11.2	1.5	12	1.5	11.7	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

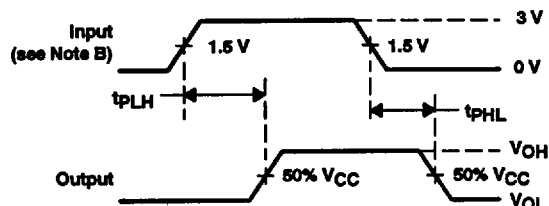
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	27	pF
		Outputs disabled		9	

PARAMETER MEASUREMENT INFORMATION

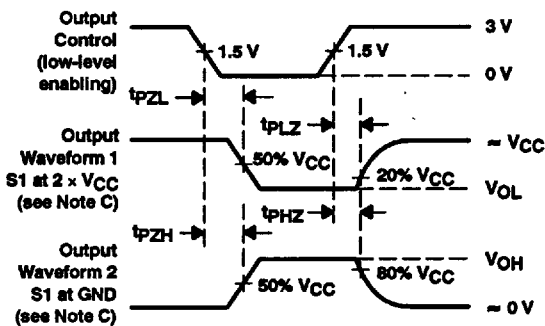


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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