

CBT16292

12-bit 1-of-2 multiplexer/demultiplexer

Rev. 02 — 18 April 2008

Product data sheet

1. General description

The CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible multiplexer/demultiplexer. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

When the select input (S) is LOW, port nA is connected to port nB1 and port nB2 is connected to GND via an internal pull-down resistor (500 Ω). When select input (S) is HIGH, port nA is connected to port nB2 and nB1 is connected to GND via an internal pull-down resistor (500 Ω).

The CBT16292 is characterized for operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

2. Features

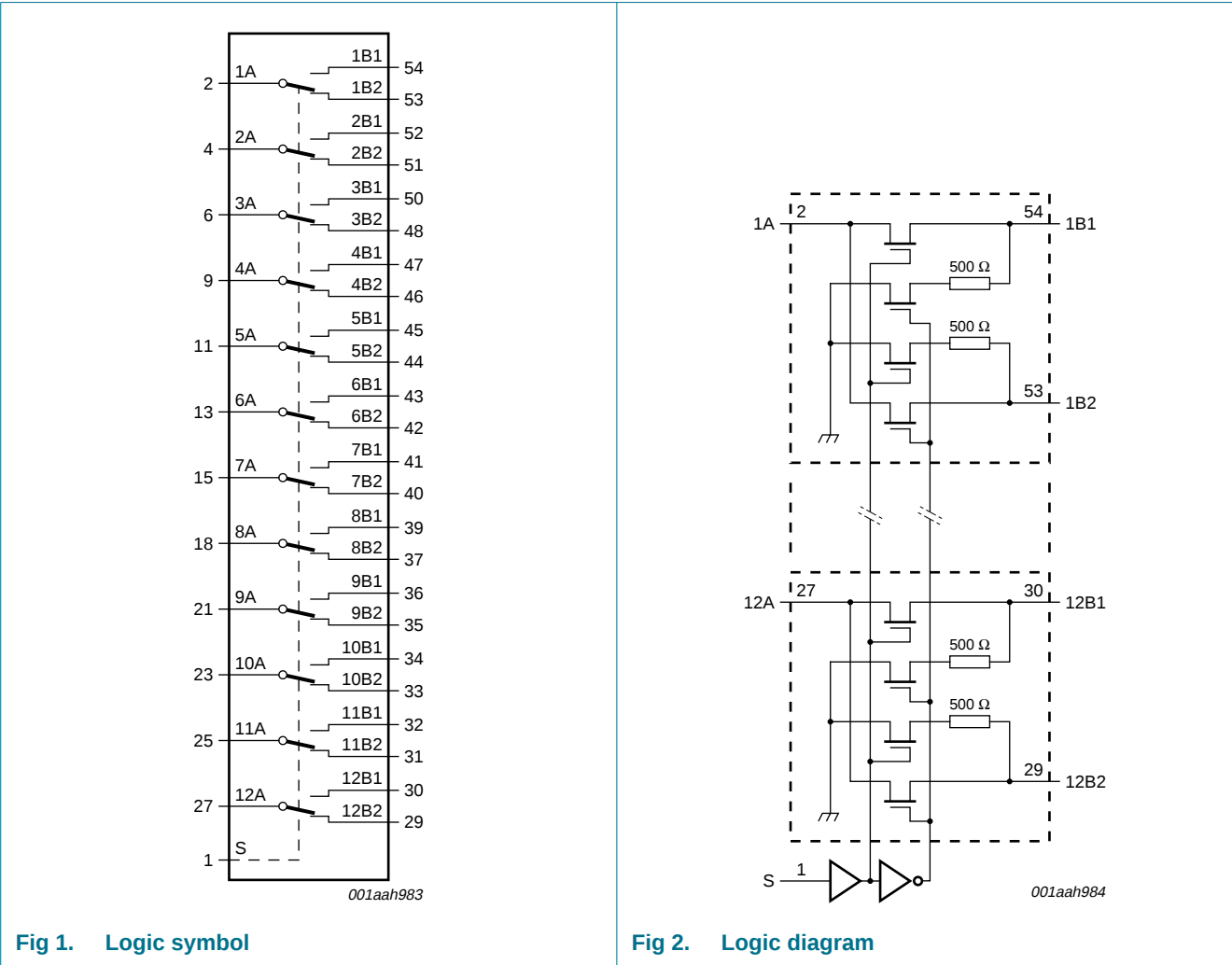
- 6 Ω switch connection between two ports
- TTL compatible input levels
- Break-before-make feature
- Internal 500 Ω pull-down resistors to ground
- ESD protection:
 - ◆ HBM JESD22-A114E Class 2 exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 500 mA per JESD 78

3. Ordering information

Table 1. Ordering information

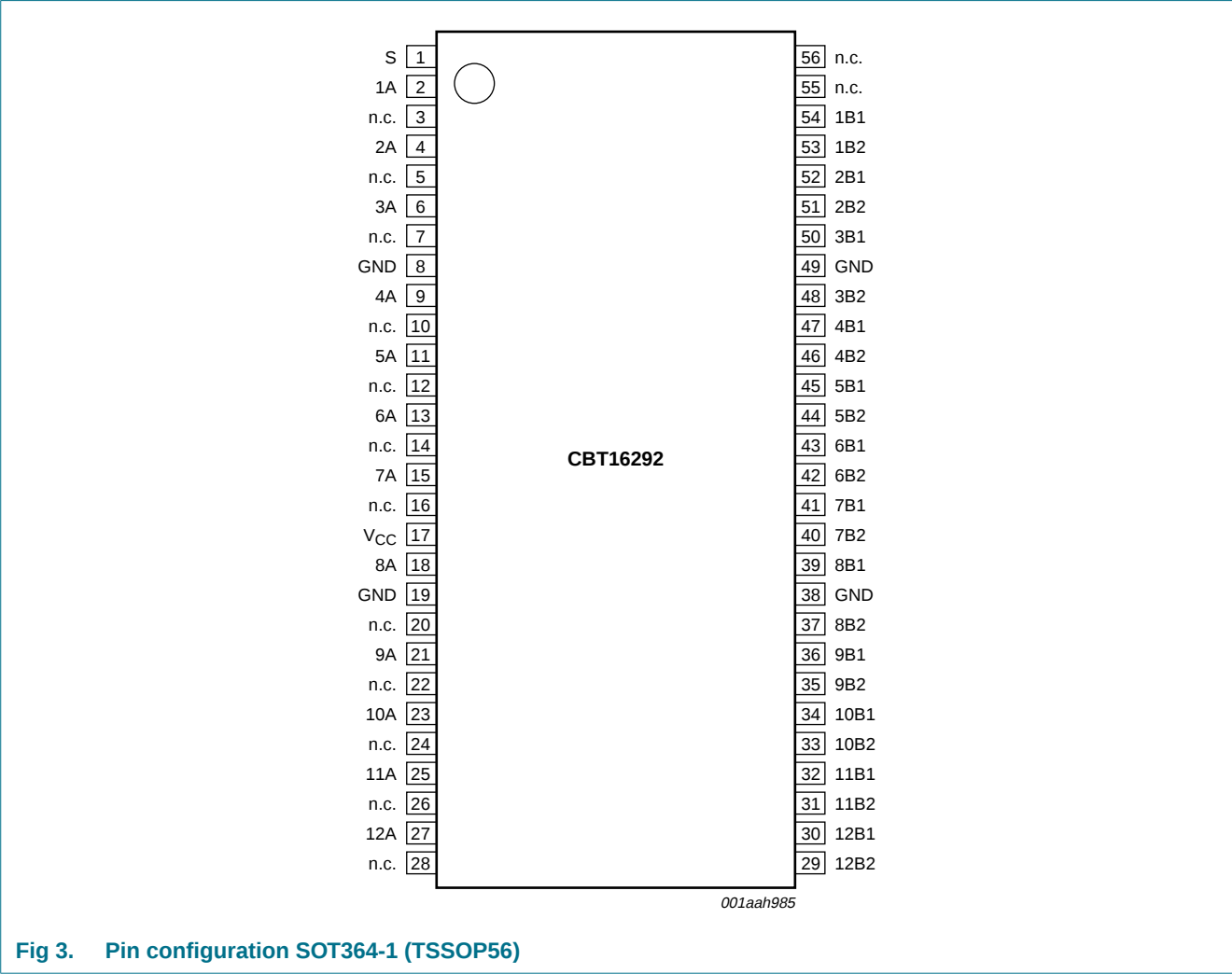
Type number	Package			
	Temperature range	Name	Description	Version
CBT16292DGG	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	select input
nA	2, 4, 6, 9, 11, 13, 15, 18, 21, 23, 25, 27	common input or output (1A to 12A)
n.c.	3, 5, 7, 10, 12, 14, 16, 20, 22, 24, 26, 28, 55, 56	not connected
GND	8, 19, 38, 49	ground (0 V)
V _{CC}	17	supply voltage
nB1	54, 52, 50, 47, 45, 43, 41, 39, 36, 34, 32, 30	independent input or output (1B1 to 12B1)
nB2	53, 51, 48, 46, 44, 42, 40, 37, 35, 33, 31, 29	independent input or output (1B2 to 12B2)

6. Functional description

Table 3. Function selection^[1]

S input	Channel on
L	nA to nB1 or nB1 to nA (nB2 connected to GND via internal resistor (500 Ω))
H	nA to nB2 or nB2 to nA (nB1 connected to GND via internal resistor (500 Ω))

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values ^{[1][2]}

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		^[3] -0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{SW}	switch current	continuous current through channel	-128	+128	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[4] -	600	mW

- [1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [4] P_{tot} derates linearly with 8 mW/K above 55 °C.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
T_{amb}	ambient temperature	operating in free-air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_I = -18\text{ mA}$	-	-	-1.2	V
I_I	input leakage current	$V_{CC} = 5.5\text{ V}$; $V_I = V_{CC}$ or GND	-	-	± 5	μA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}$; $I_O = 0\text{ mA}$; $V_I = V_{CC}$ or GND	-	-	3	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V, other inputs at V_{CC} or GND ^[2]	-	-	2.5	mA
C_I	input capacitance	select input S; $V_{CC} = 5.0\text{ V}$; $V_I = 3\text{ V}$ or 0 V	-	4	-	pF
$C_{IO(off)}$	off-state input/output capacitance	$V_O = 3\text{ V}$ or 0 V ; $V_{CC} = 0\text{ V}$	-	6	-	pF
R_{ON}	ON resistance	$V_{CC} = 4.5\text{ V}$ ^[3]				
		$V_I = 0\text{ V}$; $I_I = 64\text{ mA}$	-	8	12.5	Ω
		$V_I = 0\text{ V}$; $I_I = 30\text{ mA}$	-	8	11	Ω
		$V_I = 2.4\text{ V}$; $I_I = 15\text{ mA}$	-	13	16	Ω

[1] All typical values are measured at $T_{amb} = 25^{\circ}\text{C}$.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$; for test circuit see [Figure 6](#).

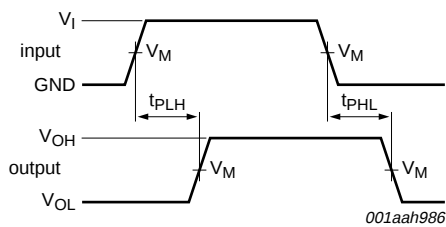
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{pd}	propagation delay	nA, nBn to nBn, nA; see Figure 4 ^{[1][2]}	-	-	0.4	ns
t_{en}	enable time	S to nA, nBn; see Figure 5 ^[2]	1.5	-	6.0	ns
t_{dis}	disable time	S to nA, nBn; see Figure 5 ^[2]	2.2	-	5.5	ns
t_{b-m}	break-before-make time	nA, nBn to nBn, nA ^[3]	0	-	2.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .

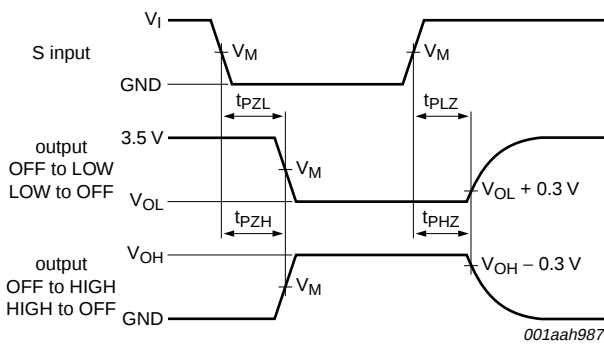
[3] Time interval between break and make measured at the same operating point (V_{CC} and temperature).

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Input (nA or nBn) to output (nBn or nA) propagation delays

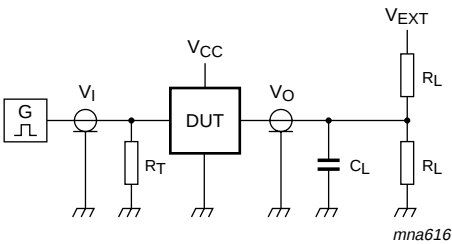


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_M
4.5 V to 5.5 V	1.5 V	GND to 3.0 V	1.5 V



Test data is given in [Table 9](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 6. Test circuit

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r = t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
4.5 V to 5.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

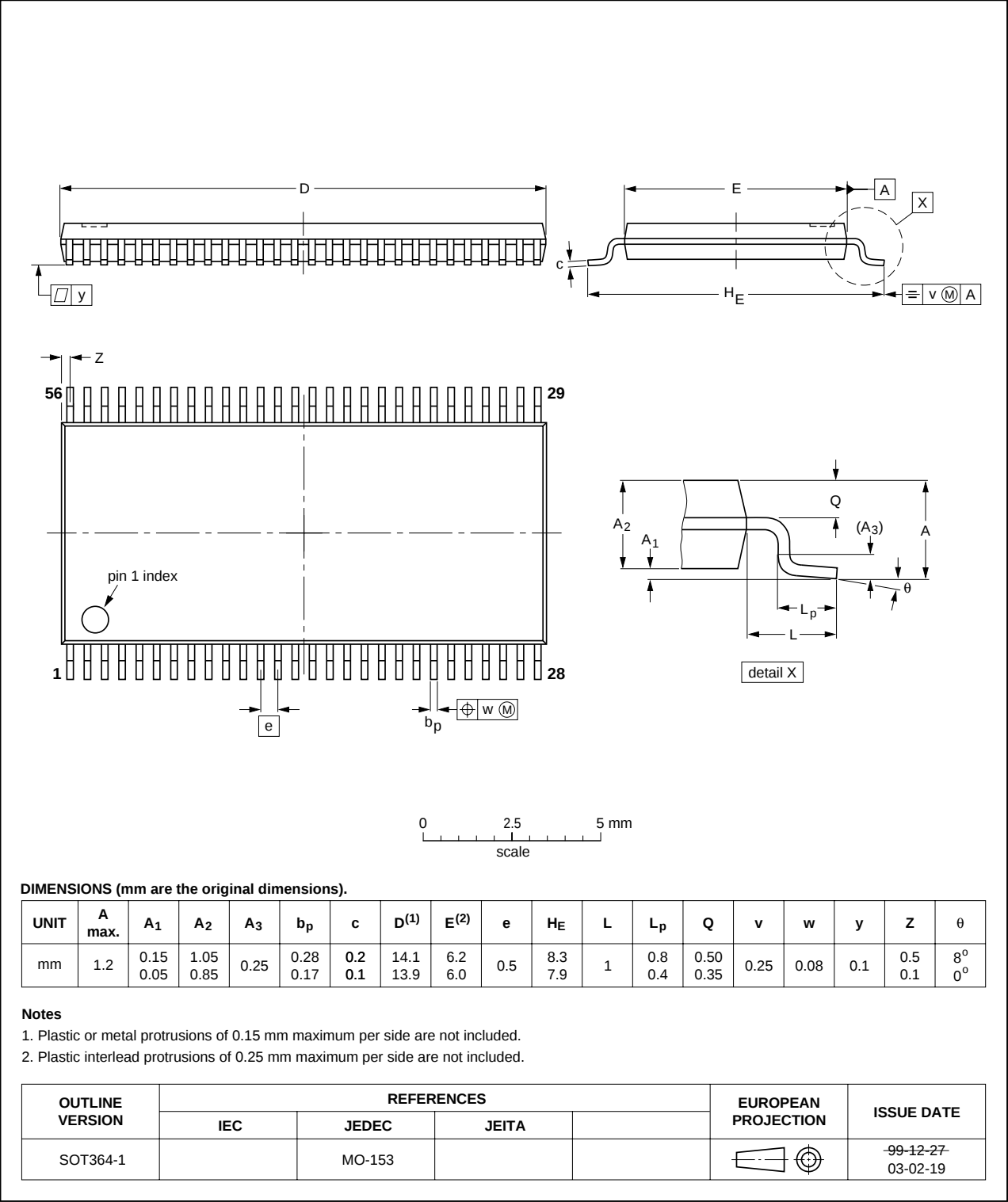


Fig 7. Package outline SOT364-1 (TSSOP56)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT16292_2	20080418	Product data sheet	-	CBT16292_1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Changed t_{en} from 5.8 ns to 6.0 ns in Table 7 "Dynamic characteristics".			
CBT16292_1	19990913	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1 General description 1

2 Features 1

3 Ordering information 1

4 Functional diagram 2

5 Pinning information 3

5.1 Pinning 3

5.2 Pin description 3

6 Functional description 4

7 Limiting values 4

8 Recommended operating conditions 4

9 Static characteristics 5

10 Dynamic characteristics 5

11 Waveforms 6

12 Package outline 8

13 Abbreviations 9

14 Revision history 9

15 Legal information 10

15.1 Data sheet status 10

15.2 Definitions 10

15.3 Disclaimers 10

15.4 Trademarks 10

16 Contact information 10

17 Contents 11



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.