

Analog Signal Input Monaural, Filter Less 3.0W Class-D Amplifier

■ FEATURES (Typical value, $T_a = 25^\circ\text{C}$)

- Supply Voltage 1.8V to 5.5V
- High Power ($V^+ = 5\text{V}$, THD+N = 10%)
 - $R_L = 8\Omega$ 1.7W
 - $R_L = 4\Omega$ 3.0W
- Output LC Filterless
- Built-in Pop Noise Reduction (Turn on / Turn off)
- Analog Differential Input / PWM Output
- Low Supply Current ($V^+ = 3.6\text{V}$) 2.7mA
 - Standby Current 1 μA max.
- Overcurrent Protection Circuit
- Thermal Shutdown Circuit
- Undervoltage Lock Out circuit (UVLO)
- Package HSOP8

■ APPLICATIONS

- Security Equipment
- Portable Equipment
- Portable Audio

■ MONAURAL POWER AMPLIFIER VARIATION

Part Number	Description
NJU72060	0.5W Class-AB Amplifier
NJU7089	1.2W Output 1.8V Operate Class-AB Amplifier
NJU8759/A	3.0W Output 1.8V Operate Filter-Less Class-D Amplifier

■ DESCRIPTION

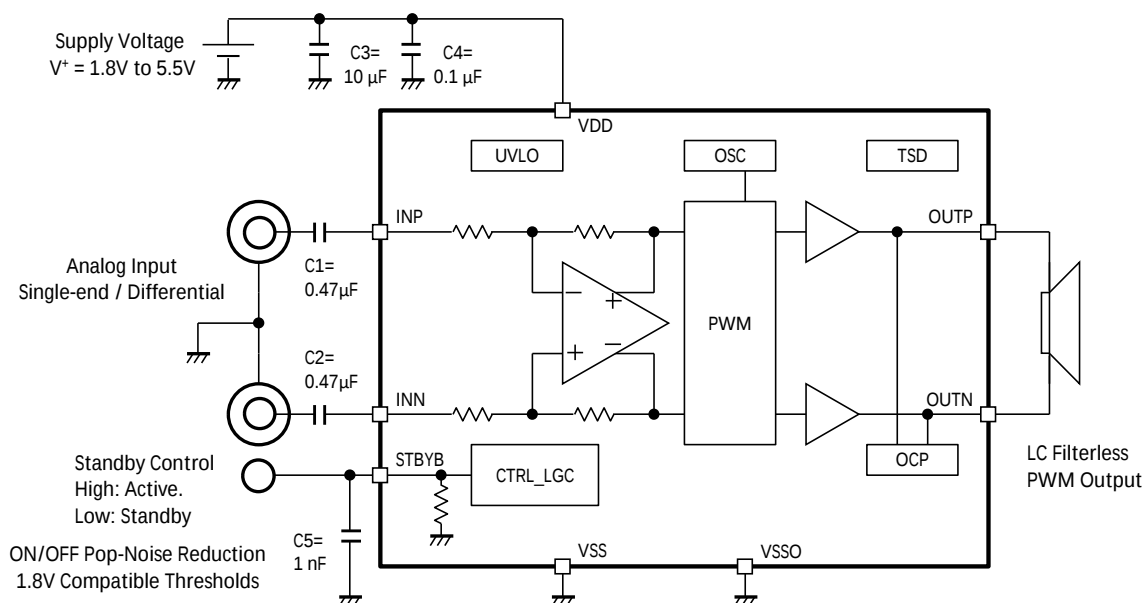
The NJU8759A is an analog signal input monaural filterless Class-D power amplifier. Operating voltage from 1.8V to 5.5V single supply can be used with 2-cell batteries.

NJU8759A features Class-D operation with high output capability, is 1.7W output (8 Ω load) and 3.0W output (4 Ω load). The BTL output configuration can reduce the coupling capacitor. Furthermore, the output LC filterless architecture, which was not available in conventional Class-D, reduces external parts and PCB size.

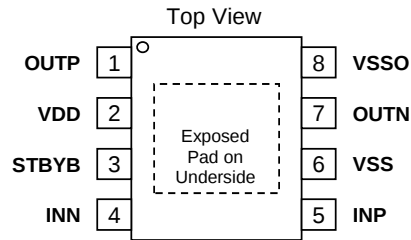
NJU8759A operates from a single power supply of 1.8 V and 1 μA maximum standby current, and is ideal for small portable devices and portable audio devices, as well as alarm devices and security devices that require low power and high output.

The NJU8759A is available in an 8-pin HSOP8 package with exposed pads for heat dissipation and a 1.45mm x 1.45mm wafer level package NJU8759WLC1 (see NJU8759 data sheet) for space saving devices.

■ APPLICATION CIRCUIT



■ PIN CONFIGURATION



PIN NO.	NAME	FUNCTION
1	OUTP	Positive output
2	VDD	Power supply
3	STBYB	Standby control
4	INN	Negative input
5	INP	Positive input
6	VSS	Analog GND
7	OUTN	Negative output
8	VSSO	Power GND

Connect exposed pad to the GND.

Exposed pad is electronically connected to the backside of the die, but cannot be function as GND.

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU8759AGM1 (TE1)	HSOP8	Yes	Yes	Pure Sn	8759A	81	3000

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	7	V
Input Voltage	V_{IN}	0 to V^+	V
Load Resistance	R_L	≥ 3.6	Ω
Power Dissipation ($T_a = 25^\circ\text{C}$) HSOP8	P_D	2-Layer / 4-Layer ⁽¹⁾ 620 / 1800	mW
Storage Temperature	T_{stg}	-40 to 125	$^\circ\text{C}$
Junction Temperature	T_j	125	$^\circ\text{C}$

(1) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-Layer FR-4).

4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-Layer FR-4).

(For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage	V^+	$V_{DD}=V^+$, $V_{SS} = V_{SSO} = \text{GND}$	1.8 to 5.5	V
Operating Temperature	T_{opr}		-40 to 105	$^\circ\text{C}$

■ **ELECTRICAL CHARACTERISTICS** ($V^+ = 3.6V$, $T_a = 25^\circ C$, unless otherwise noted.)

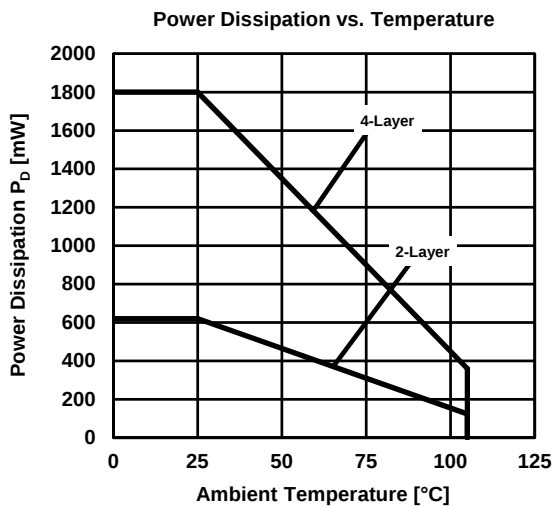
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
Standby Current	I_{ST}		-	-	1.0	μA
Supply Current	I_Q		-	2.7	5.4	mA
UVLO Detect Voltage	V_{DDDET}		1.1	1.4	1.7	V
UVLO Hysteresis Voltage	V_{DDHYS}		-	0.05	-	V
Digital Input Voltage	V_{IH}		1.5	-	VDD	V
	V_{IL}		0.0	-	0.3	V
Pull Down Resistance	R_{DOWN}	STBYB pin	-	100	-	k Ω
Input Resistance	R_{IN}	INP, INN pin	-	30	-	k Ω
Switching Frequency	F_{OSC}		100	250	395	kHz
Turn On Time	T_{ON}		10	16	40	ms
Turn Off Time	T_{OFF}		10	16	40	ms
Voltage Gain	A_v		17.5	18.0	18.5	dB
Output Leakage Current (Standby)	I_{OL}	$V_O = 3.6V$ or GND	-1	-	1	μA
Output Offset Voltage at Turn-On / Turn-Off	V_{OS}		-	1	-	mV
AC CHARACTERISTICS ($R_L = 8\Omega$, BW = 20Hz to 20kHz, $f_{in} = 1kHz$, unless otherwise noted.)						
Output Power	P_O	$V^+ = 5V$, THD+N = 10%, $R_L = 8\Omega$	-	1.7	-	W
		$V^+ = 5V$, THD+N = 10%, $R_L = 4\Omega$	-	3.0	-	W
Output Power Efficiency	η	$V^+ = 5V$, THD+N = 10%, $R_L = 8\Omega + 33\mu H$	-	93	-	%
Total Harmonic Distortion + Noise	THD+N	$P_O = 0.5W$	-	0.050	-	%
		$V^+ = 5V$, $P_O = 1.0W$	-	0.035	-	%
Supply Voltage Rejection Ratio	PSRR	$f_{in} = 217Hz$, ripple = 200mV _{PP}	-	-55	-	dB
Common-Mode Rejection Ratio	CMRR	$f_{in} = 217Hz$, $V_{inc} = 1V_{PP}$	-	-55	-	dB
Output Voltage Noise	V_{NO}	A-weighting	-	62	-	μV

■ THERMAL CHARACTERISTICS

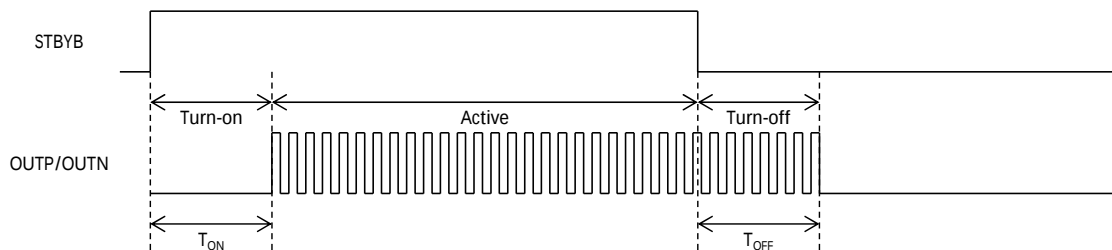
PACKAGE	SYMBOL	VALUE	UNIT
Junction-to-Ambient Thermal Resistance	θ_{ja}	2-Layer / 4-Layer ⁽¹⁾	°C/W
HSOP8		160 / 57	

- (1) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-Layer FR-4).
 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-Layer FR-4).
 (For 4-layer: Applying 74.2 mm × 74.2 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

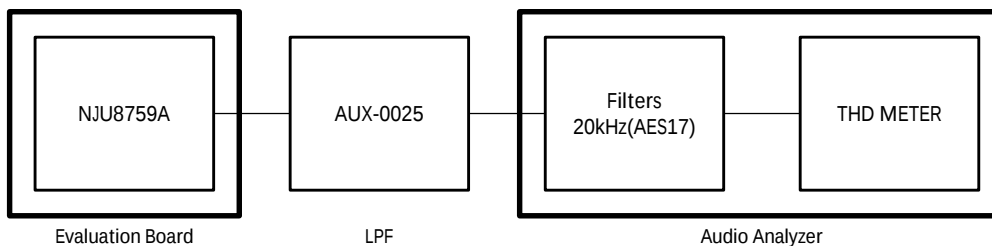


■ TURN ON / TURN OFF SEQUENCE

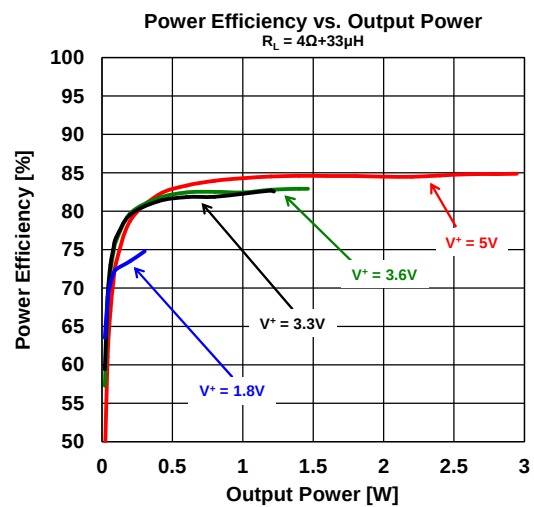
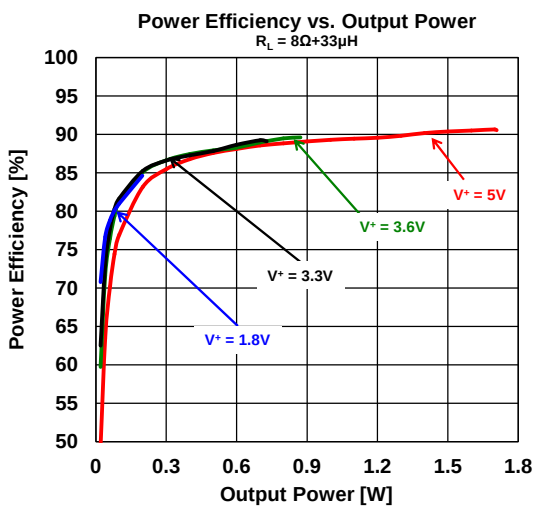
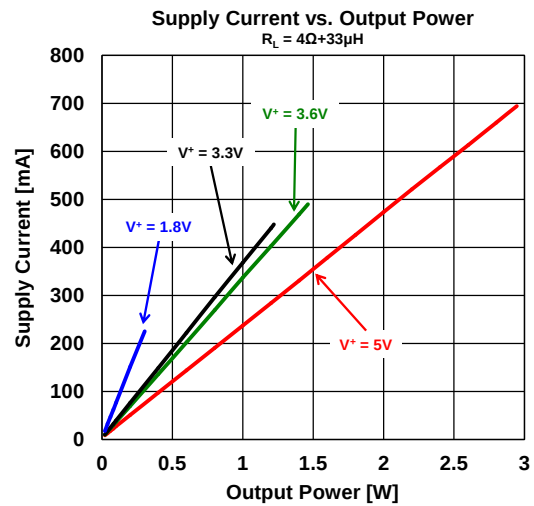
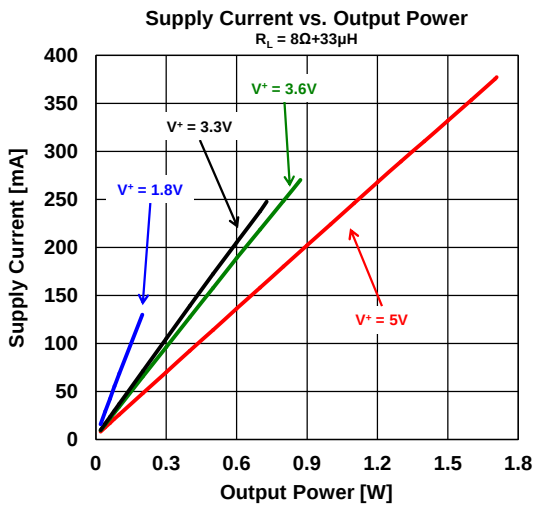
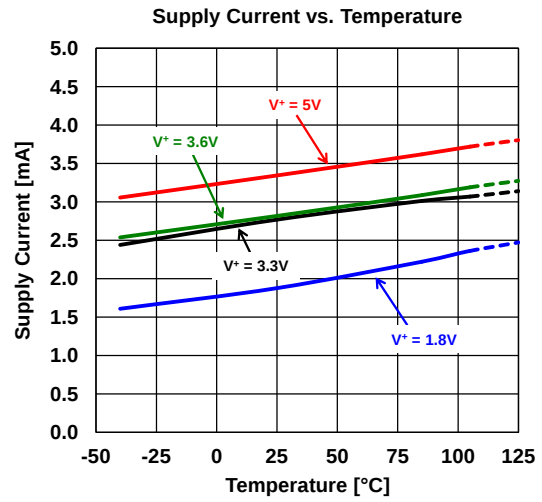
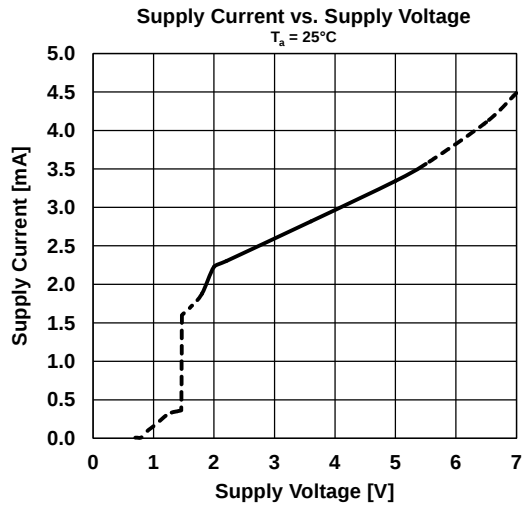


When STBYB is set to "High" in the T_{OFF}, it shifts to Active mode immediately.

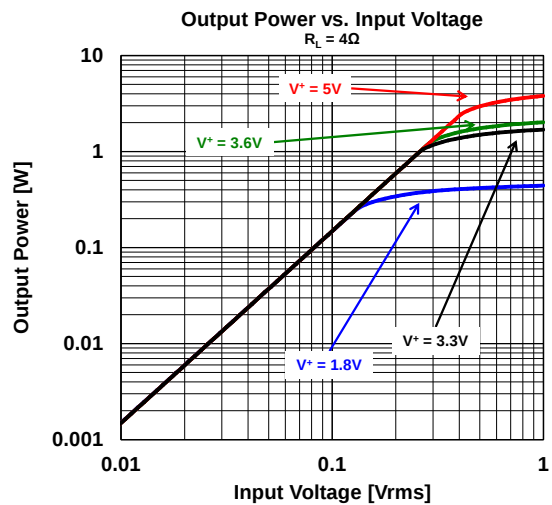
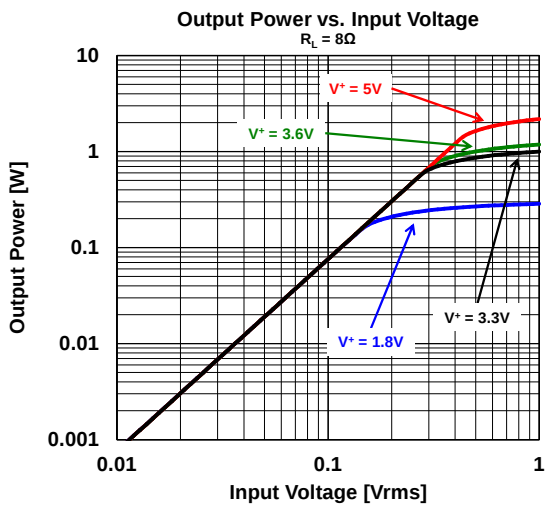
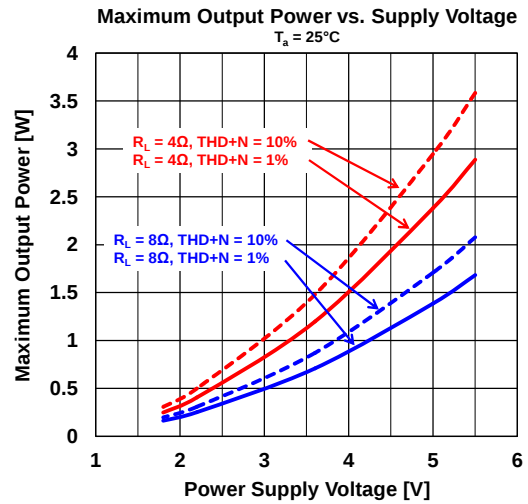
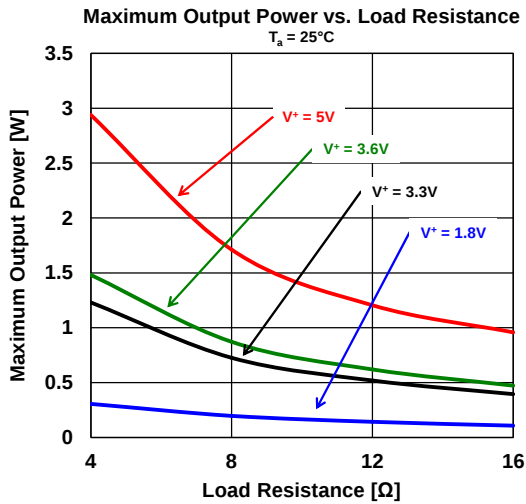
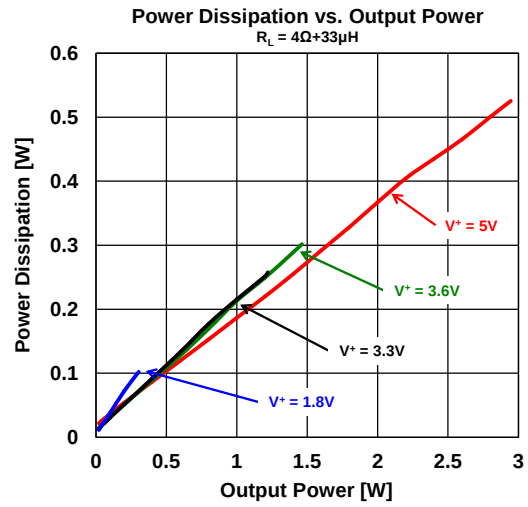
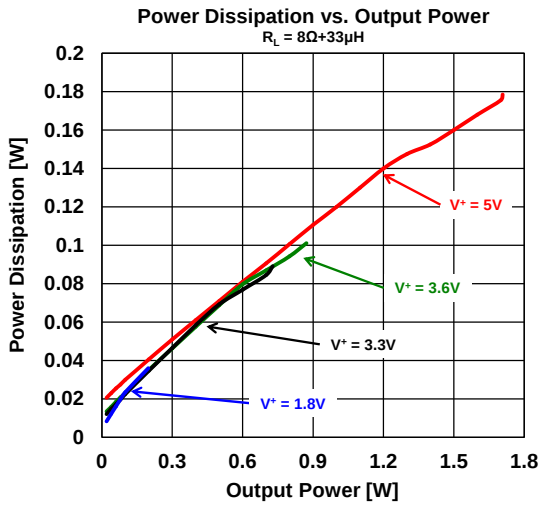
■ TEST SYSTEM OF THE OUTPUT THD+N

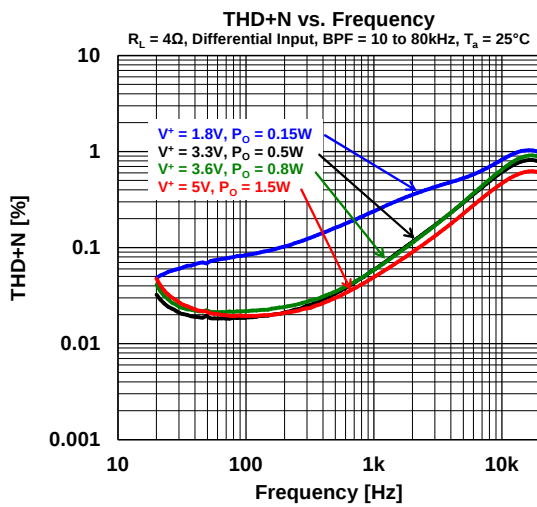
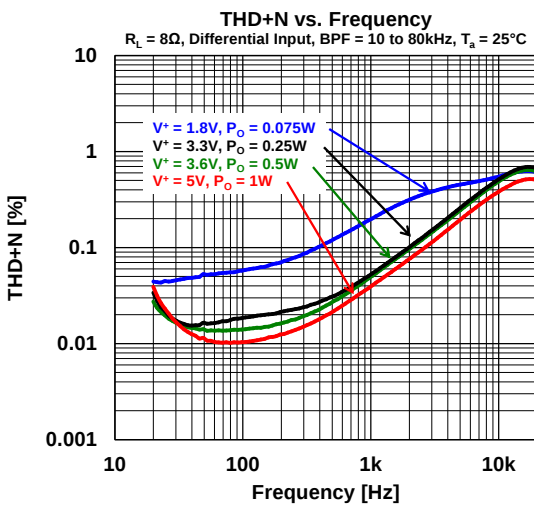
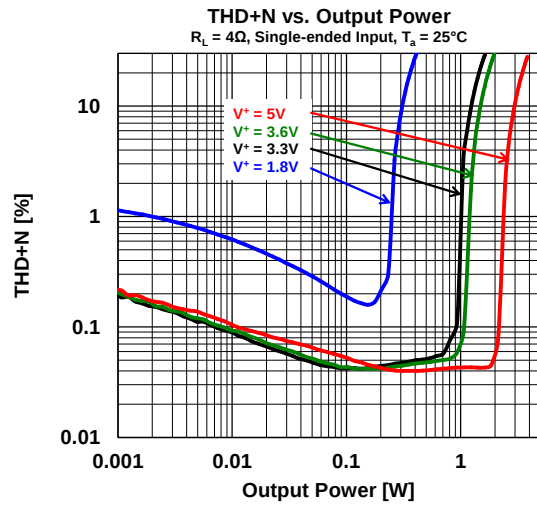
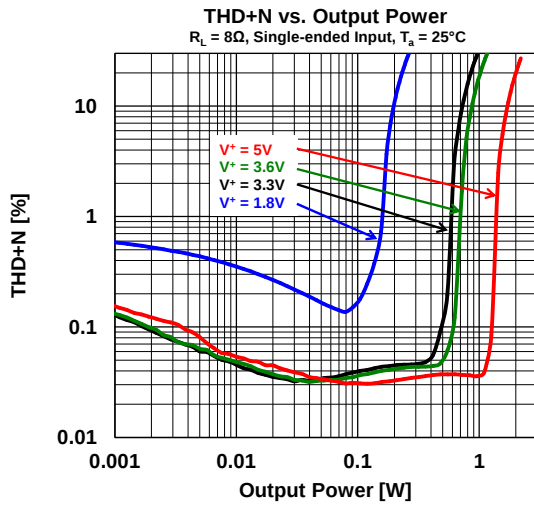
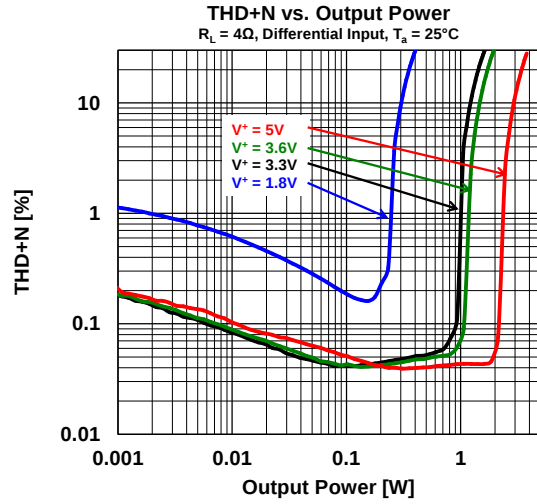
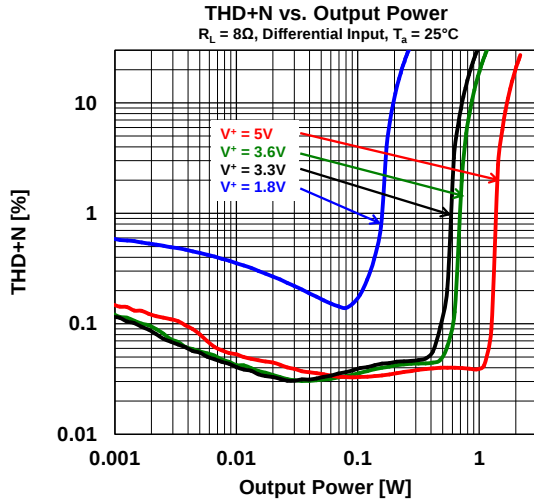


■ TYPICAL CHARACTERISTICS

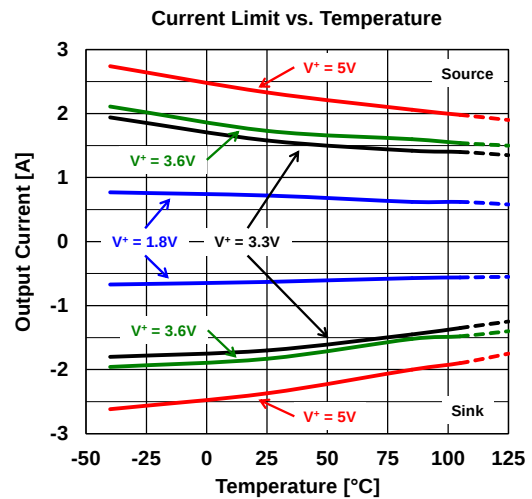
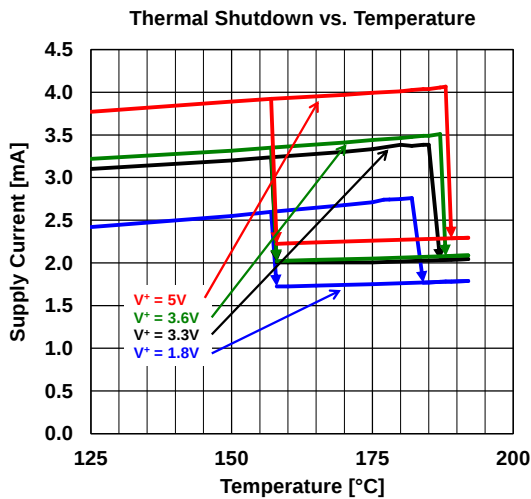
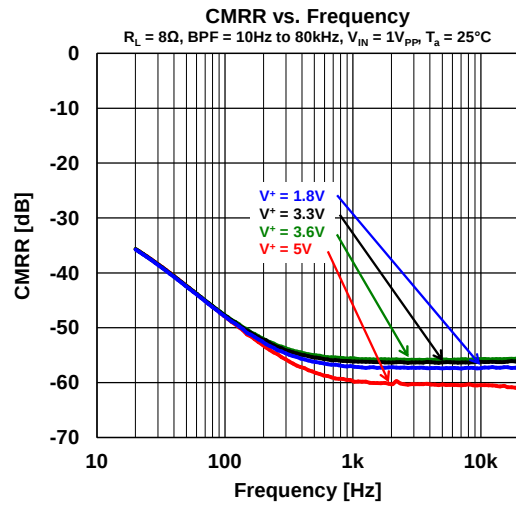
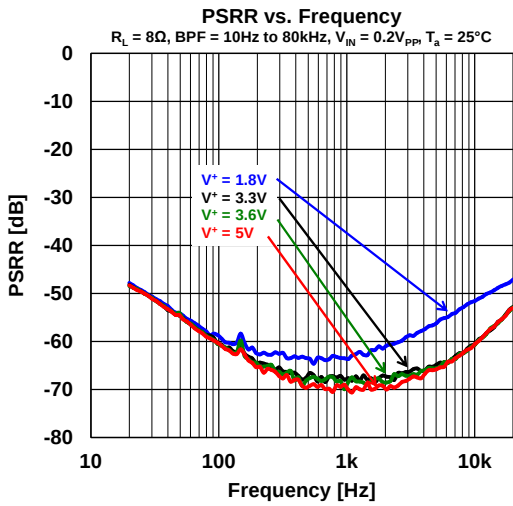
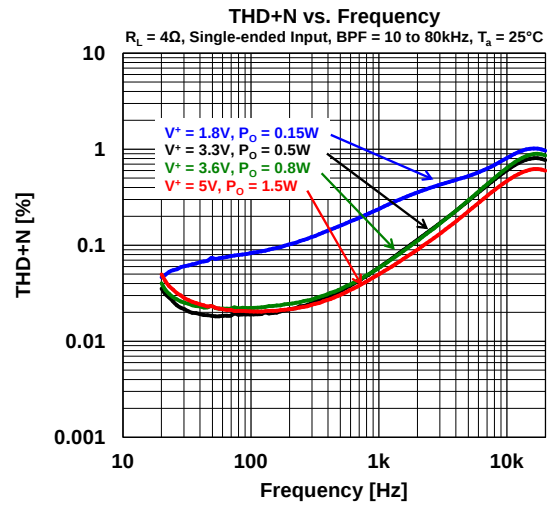
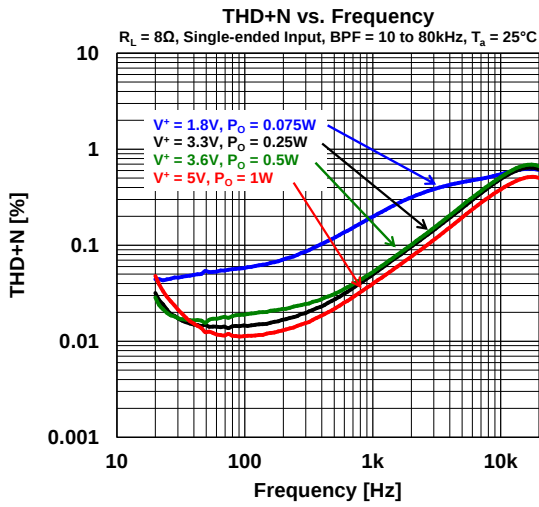


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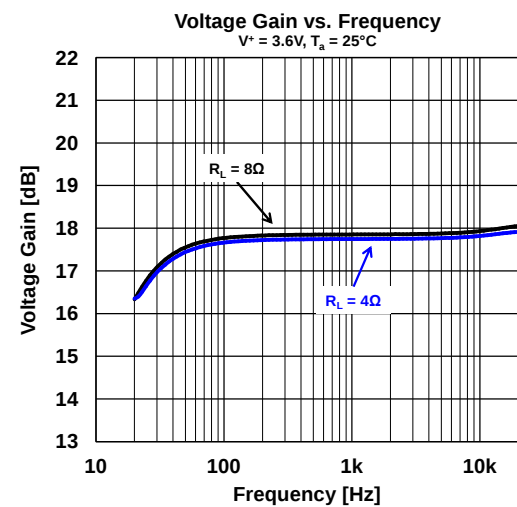
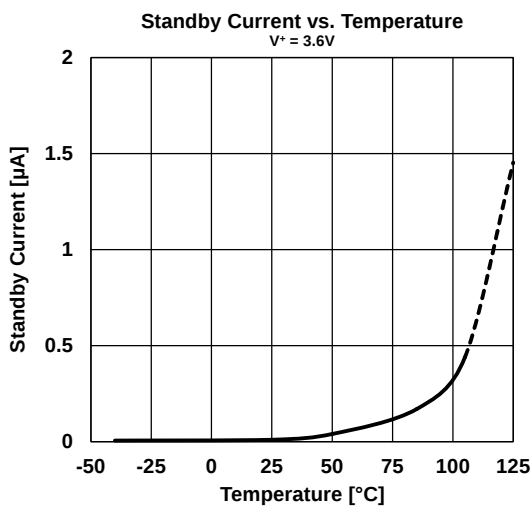
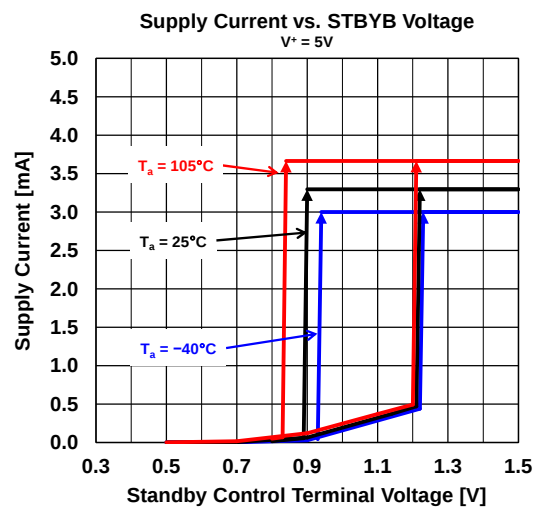
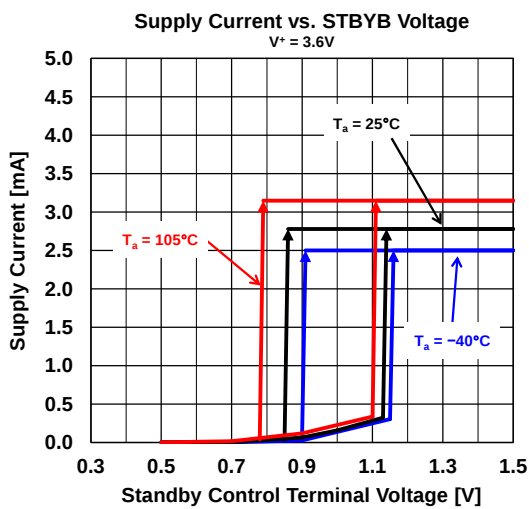
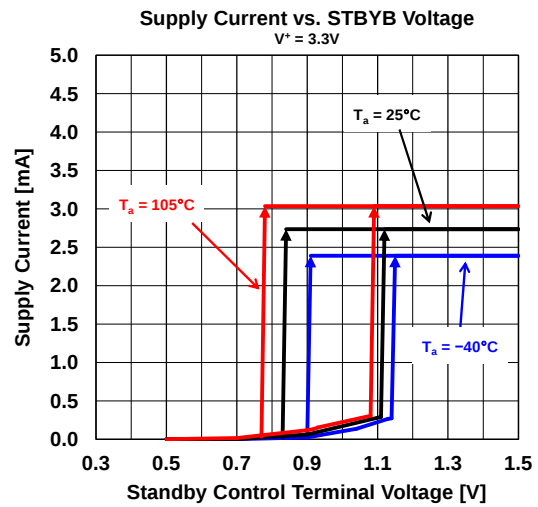
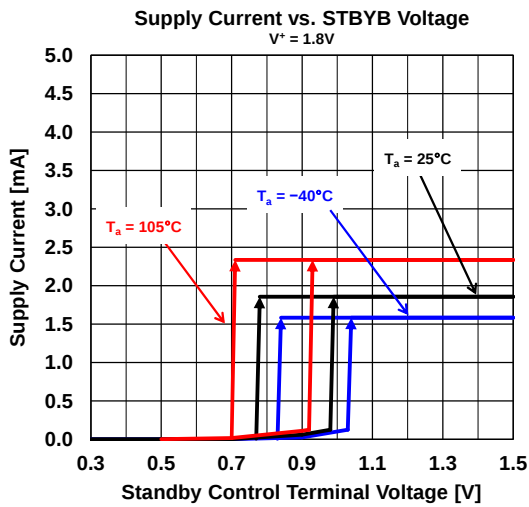


■ TYPICAL CHARACTERISTICS


■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■ APPLICATION NOTE

DESCRIPTION

The NJU8759A is an analog signal input monaural filterless Class-D power amplifier, features high output capability of 1.7W output (8Ω load) and 3.0W output (4Ω load). The BTL output configuration can reduce the coupling capacitor. Furthermore, the output LC filterless architecture reduces external parts and PCB size. Operating voltage is from 1.8V to 5.5V single supply, and can be used with 2-cell batteries.

Figure 1-1 shows the NJU8759A block diagram. The NJU8759A consists of a Class-D amplifier, an undervoltage lockout, a thermal shutdown and overcurrent protections.

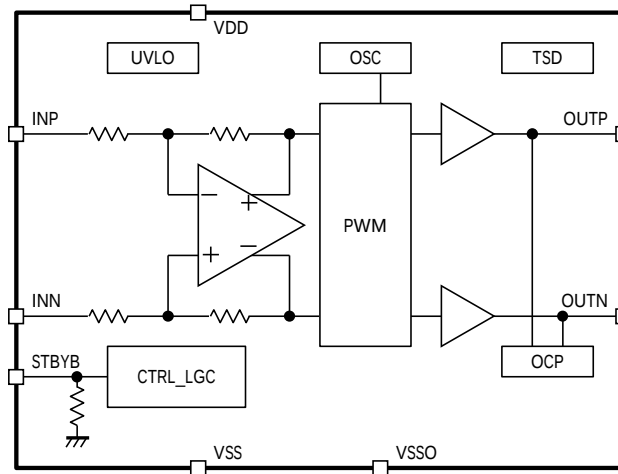


Figure 1-1 the NJU8759A block diagram

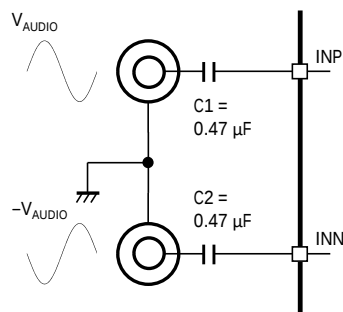
FUNCTIONAL DESCRIPTION

Audio Input Signals

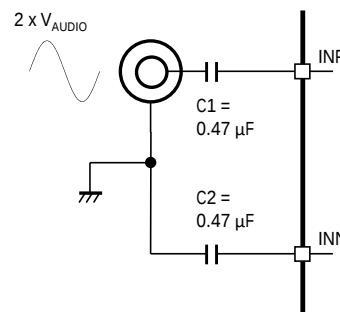
Differential analog signals are input into INP and INN as Figure 2-1 (a). The voltage gain is shown by

$$A_V = \frac{V_{OUTP} - V_{OUTN}}{V_{INP} - V_{INN}} = 18\text{dB}$$

In case of a single-ended input signal application, an analog signal is input into INP as Figure 2-1 (b). Input the INP signal with twice the amplitude of the differential application.



(a) Differential input signal application



(b) Single-ended input signal application

Figure 2-1 How to input audio signals

Input Signal Range

The input signal voltage may cause some troubles over power supply voltage. So design the input signal voltage under 600mVrms. Also, same troubles may be caused in case of floating input pins. For preventing floating input pins, design former audio IC active mode before releasing NJU8759A standby mode, or connect 1MΩ pull-down resistors shown as Figure 2-2.

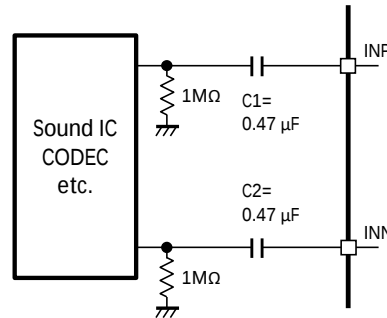


Figure 2-2 How to prevent floating input pins

Output Signals

PWM signals are output from OUTP and OUTN. Connect a dynamic speaker between OUTP and OUTN. The NJU8759A does not require OUTPUT LC filters which a traditional Class-D amplifier needed. The output power is shown below.

$$P_O = \frac{[A_V(V_{INP} - V_{INN})]^2}{R_L} \text{ [W]}$$

Input Coupling Capacitors

The input capacitors and input resistors set a high-pass filter. Its corner frequency is given by

$$f_c = \frac{1}{2\pi \times 30k\Omega(\text{typ.}) \times C1}$$

Although increasing the coupling capacitor constant improves low-frequency characteristics, pop noise tends to occur at startup. The recommended capacitor value is under 0.47μF. Sufficient evaluation is required when selecting 0.47μF or more.

The NJU8759A operates cancelling output offset voltage during turn-on and turn-off time. If an audio signal is input during offset voltage cancellation, offset voltage cancellation will not be performed properly and pop noise may occur. For applications in which audio signals are input even during turn-on/turn-off, perform pop noise audition evaluation sufficiently.

Thermal Design

The output power is restricted by maximum rating.

Maximum package power dissipation at any ambient temperature is given by

$$P_{D\text{MAX}} = \frac{125[^\circ\text{C}] - T_a[^\circ\text{C}]}{\theta_{ja}[^\circ\text{C}/\text{W}]}$$

Where $P_{D\text{MAX}}$: maximum power dissipation [W], T_a : ambient temperature [$^\circ\text{C}$], θ_{ja} : thermal resistance [$^\circ\text{C}/\text{W}$]

The IC power dissipation referred to Figure 2-3 is a difference between supply power and output power shown by

$$P_D = (V^+[\text{V}] \times I_Q[\text{A}]) - P_O[\text{W}]$$

Design so that the IC power dissipation P_D does not exceed the maximum package power dissipation $P_{D\text{MAX}}$.

For the power dissipation and thermal resistance of each package, refer to the absolute maximum ratings and thermal resistance in the data sheet.

Ex.) $T_a = 50^\circ\text{C}$, $V^+ = 5\text{V}$, $I_Q = 560\text{mA}$, $P_O = 2.5\text{W}$, HSOP8-M1 package, 4-layer PCB

$$\text{Power dissipation } P_D = (5[\text{V}] \times 560[\text{mA}]) - 2.5[\text{W}] = 300[\text{mW}]$$

Maximum package power dissipation $P_{D\text{MAX}}$ at $T_a = 50^\circ\text{C}$

$$P_{D\text{MAX}} = \frac{125[^\circ\text{C}] - 50[^\circ\text{C}]}{57[^\circ\text{C}/\text{W}]} = 1300[\text{mW}]$$

The power dissipation P_D is within the maximum package power dissipation $P_{D\text{MAX}}$.

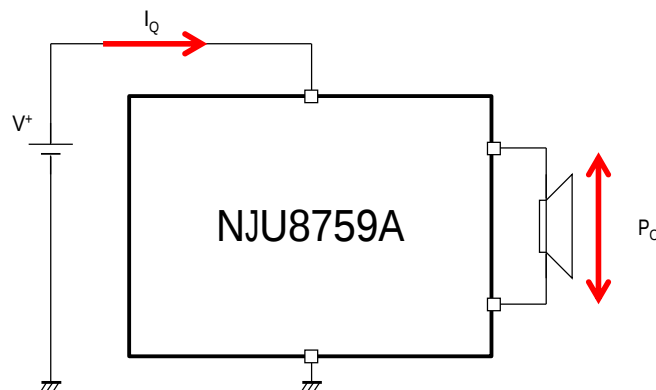


Figure 2-3 a power dissipation model

Standby Mode / Pop Noise Reduction at Turn-on/Turn-off

The NJU8759A has a standby function at 1 μ A (max). In addition, the output pin is in high impedance during standby mode. Input the standby control signal into "STBYB" pin with 100k Ω pull down resistor. Figure 2-4 shows the timing chart of standby control. Place a capacitor of 1nF or more near the standby pin to remove noise in the control signal.

The NJU8759A operates if "STBYB" voltage over High level digital voltage is applied and after turn-on time (16ms typ.), an audio signal is output. Even during turn-on, offset voltage cancel operation reduces pop noise.

The NJU8759A shuts down if "STBYB" voltage under Low level digital voltage is applied and after turn-off time (16ms typ.), it goes to the standby mode. Even during turn-off, offset voltage cancel operation reduces pop noise. If the STBYB pin goes high level during the turn-off time, the standby state is released immediately and the audio signal is output.

When the standby control is unnecessary, short the STBYB pin to VDD pin. However, since pop noise occurs at turn-on/turn-off, sufficient evaluation is required.

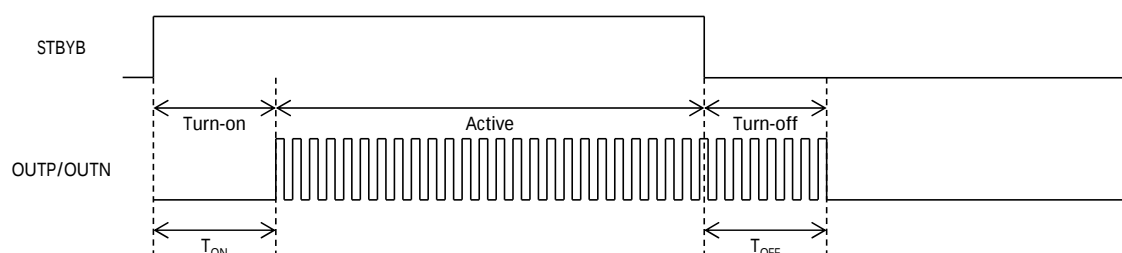


Figure 2-4 Timing chart

Undervoltage Lock Out (UVLO)

When the power-supply voltage drops down under UVLO detecting voltage, OUTP and OUTN become high impedance. When the power-supply voltage increases to over UVLO detecting voltage summing hysteresis voltage, it restarts after the turn-on time.

Overcurrent Protection

The overcurrent protection operates at the condition of the following, and when enables, the OUTP and OUTN become "high impedance".

- Short between OUTP and OUTN pin
- GND fault of OUTP pin
- GND fault of OUTN pin
- VDD fault of OUTP pin
- VDD fault of OUTN pin

Overcurrent protection status is not released automatically, it is released by applying a voltage below the Low level digital signal to the STBYB pin or turning off the power supply. To resume normal operation, apply a voltage below the Low level digital signal to the STBYB pin, check that it is not in an overcurrent state, and then restart the device.

The detectable current and the period for the protection depend on the power supply voltage and temperature. And the overcurrent protector is not effective for a long term overcurrent but for an instantaneous accident.

Continuous overcurrent may cause permanent damage to the NJU8759A.

Thermal Shutdown

When IC junction temperature is higher than detecting temperature, the OUTP and OUTN become high impedance. It restarts if IC junction temperature is lower than releasing temperature.

EMI Restriction

If it is necessary to restrict EMI, design the short traces from the amplifier to the speaker. If you need more restriction, design the short traces with ferrite beads shown as Figure 2-5. Figure 2-6 is the measurement result on equivalent VCCI CLASS-B 3m with 100mm traces from the amplifier to the speaker.

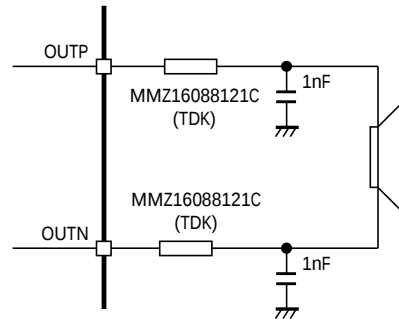
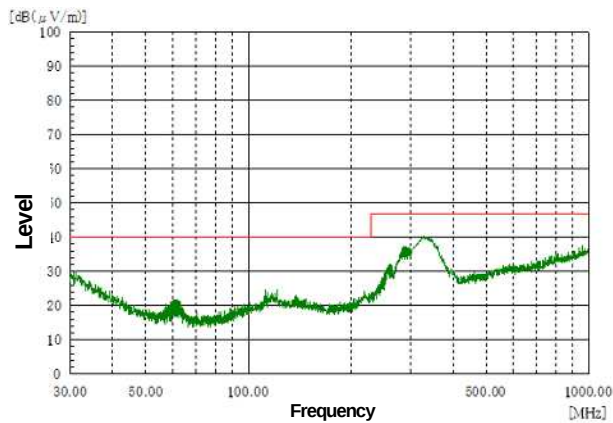
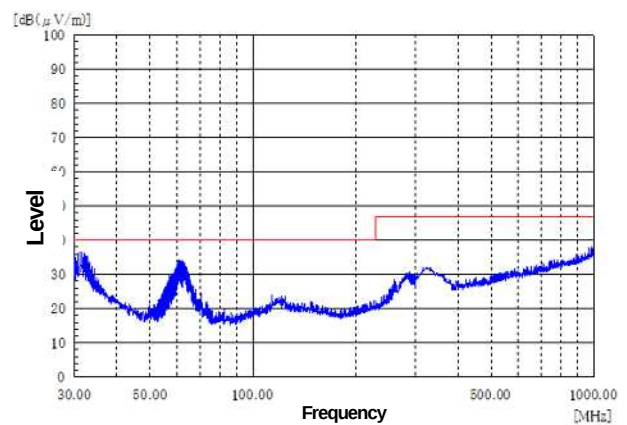


Figure 2-5 an EMI restriction model



(a) Horizontal



(b) Vertical

Figure 2-6 EMI result on equivalent VCCI CLASS-B 3m

PCB Layout

Figure 2-7 shows an example for 4-layer PCB Layout around the NJU8759A.

For VDD, VSSO, OUTP, and OUTN through which a large current flows, layout with the maximum width allowed by the wiring rules. The power supply of NJU8759A must operate stably against the sink or source current that is generated by the audio signal and the output stage. Chip ceramic capacitors are recommended for bypass capacitors between VDD and GND. It is recommended the 0.1 μ F capacitor sets near VDD, AGND and PGND pin for the restricting ripple.

If the standby control signal is noisy, the standby mode may not be controlled properly. In such cases, a capacitor of 1nF or more placed near the IC to eliminate then noise of standby control signal.

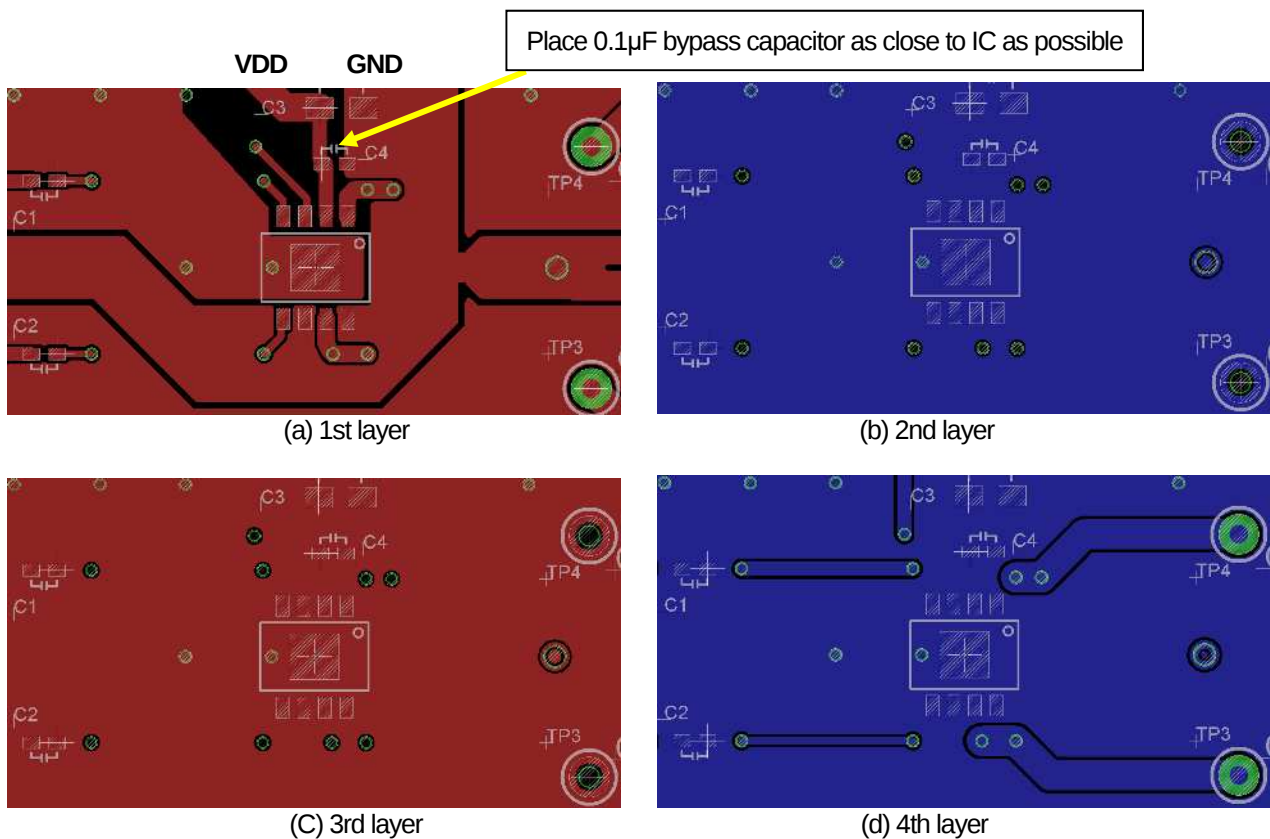


Figure 2-7 an example for 4-layer PCB Layout around the NJU8759A

Differential input application

Input reverse phase signals to INP and INN.

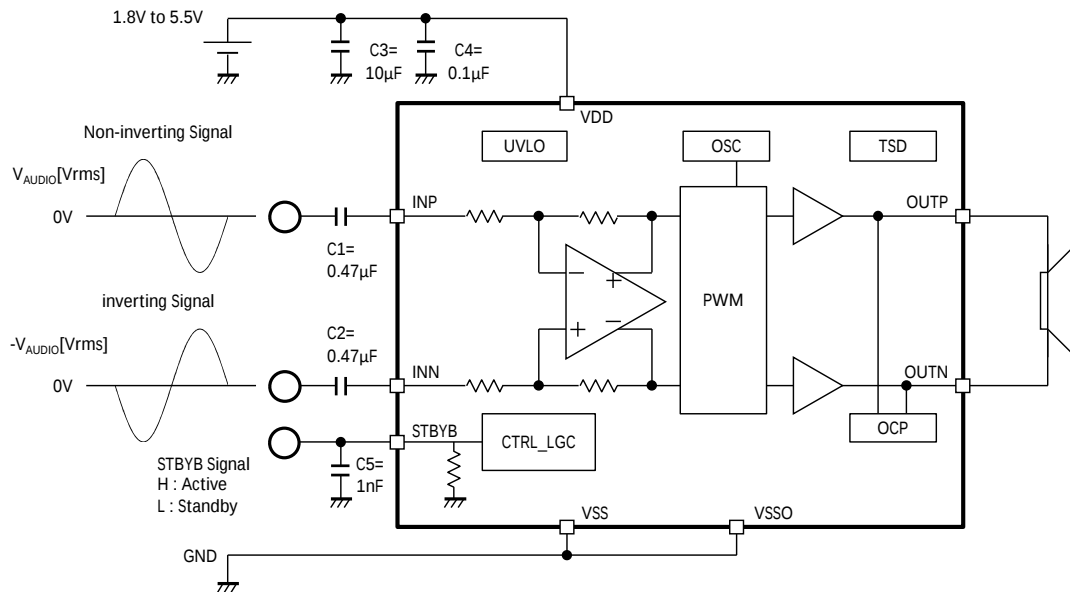


Figure 2-8 How to use Evaluation board (a differential input application)

Single-ended input application

Input the INP signal with twice the amplitude of the differential application. Connect INN to AGND.

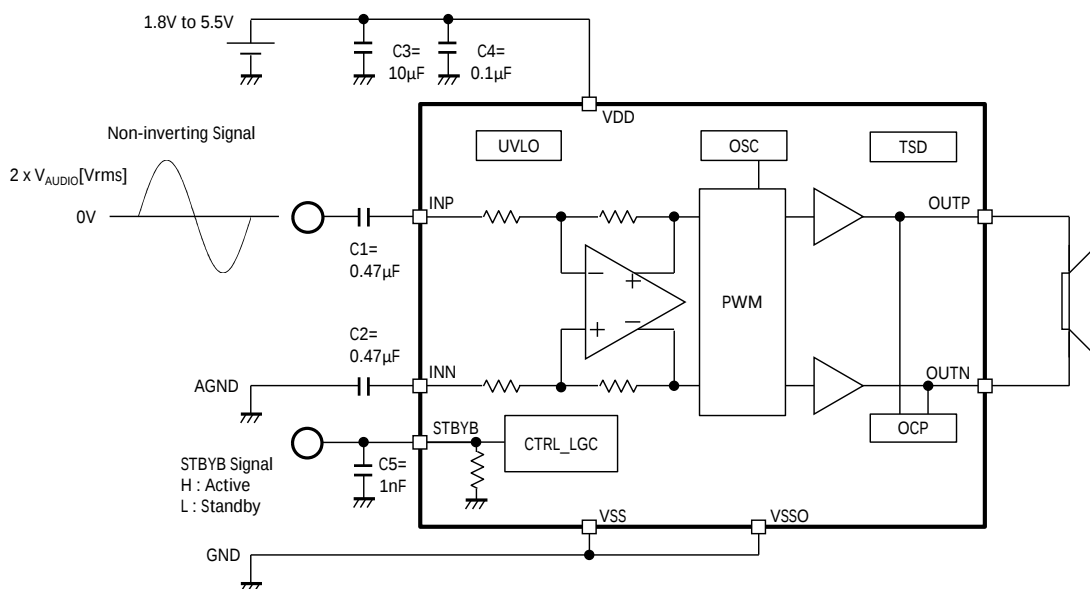


Figure 2-9 How to use Evaluation board (a single-ended input application)

Differences between NJU8759WLC1 and NJU8759AGM1

The NJU8759/A is available in the WCSP9 package, which has excellent space saving, and the HSOP8 package, which has excellent heat dissipation characteristics. Other than the package, there are the following differences, so please refer to the device selection according to the set specifications.

Package / Block Diagram

PRODUCT NAME	NJU8759WLC1	NJU8759AGM1
Package	WCSP9	HSOP8
Pin Function	Top View	Top View
Block Diagram		

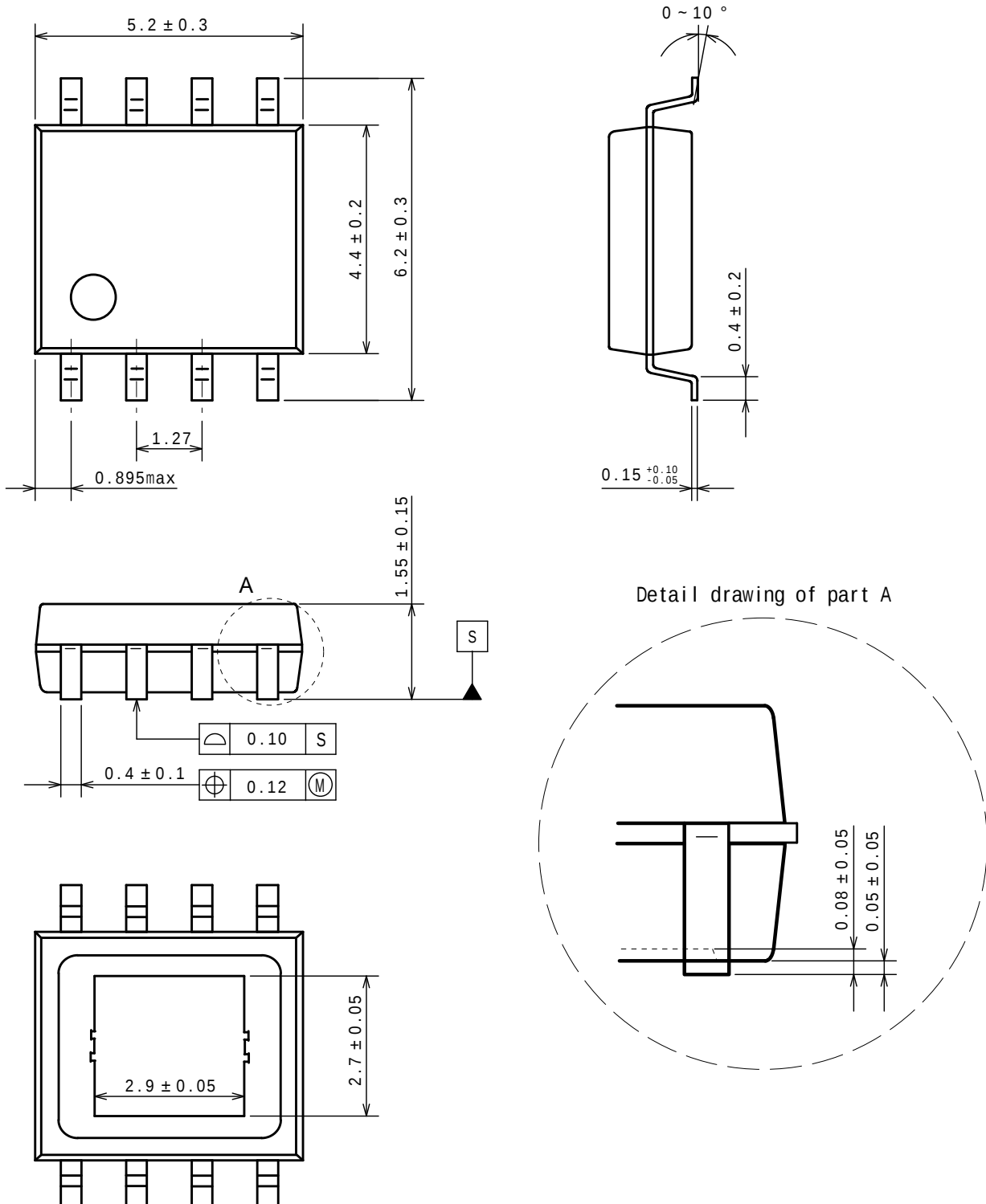
ABSOLUTE MAXIMUM RATINGS / ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NJU8759WLC1			NJU8759AGM1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power Dissipation ($T_a = 25^\circ\text{C}$)	P_D	2-Layer / 4-Layer	640 / 1200			620 / 1800			mW
Load Resistance	R_L		$R_L \geq 3.4\Omega$			$R_L \geq 3.6\Omega$			Ω
Supply Voltage	V^+	$R_L \geq 3.6\Omega$	1.8 to 5.5			1.8 to 5.5			V
		$R_L \geq 3.4\Omega$	2.0 to 5.5			-			V
Operating Temperature	T_{opr}	$R_L \geq 3.6\Omega$	-40 to 85			-40 to 105			$^\circ\text{C}$
		$R_L \geq 3.4\Omega$	-40 to 80			-			$^\circ\text{C}$
Output Offset Voltage at Turn-On / Turn-Off	V_{os}	$V^+ = 3.6\text{V}, T_a = 25^\circ\text{C}$	-20	-	20	-	1	-	mV

HSOP8

Unit: mm

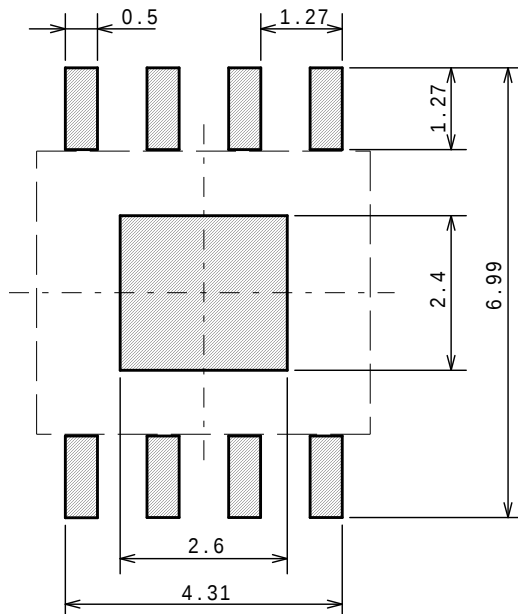
■ PACKAGE DIMENSIONS



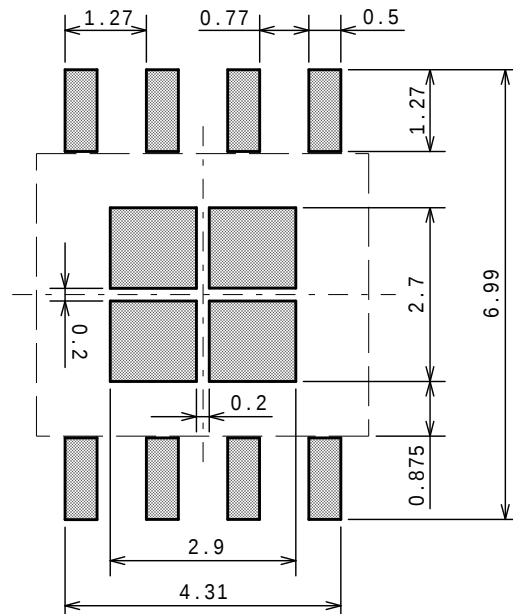
HSOP8

Unit: mm

■ EXAMPLE OF SOLDER PADS DIMENSIONS



<Solder pattern>



<Metal mask>

<Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.

Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.

We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

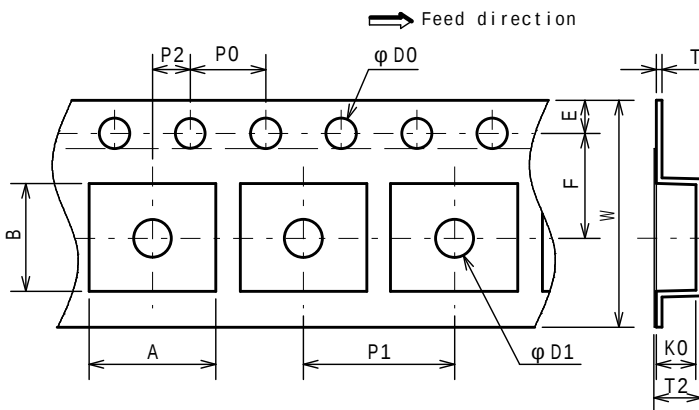
Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd:OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd:M705-GRN350-32-11)

HSOP8

PACKING SPEC

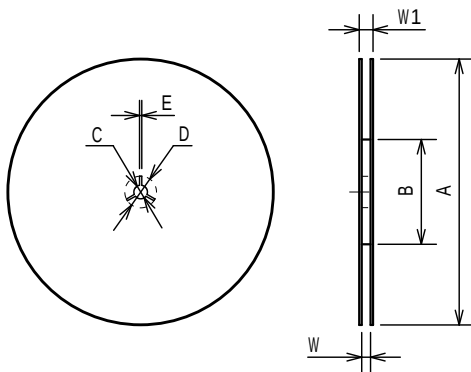
Unit: mm

TAPING DIMENSIONS



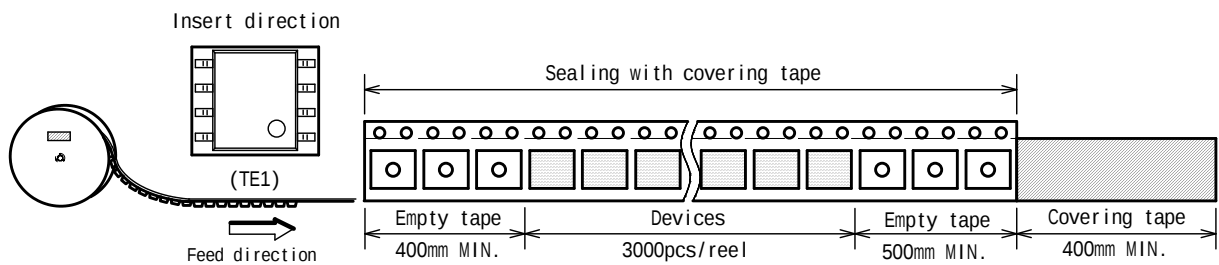
SYMBOL	DIMENSION	REMARKS
A	6.7 ± 0.1	
B	5.55 ± 0.1	
D0	1.55 ± 0.05	
D1	2.05 ± 0.05	
E	1.75 ± 0.1	
F	5.5 ± 0.05	
P0	4.0 ± 0.1	
P1	8.0 ± 0.1	
P2	2.0 ± 0.05	
T	0.3 ± 0.05	
T2	2.47	
K0	2.1 ± 0.1	
W	12.0 ± 0.2	

REEL DIMENSIONS

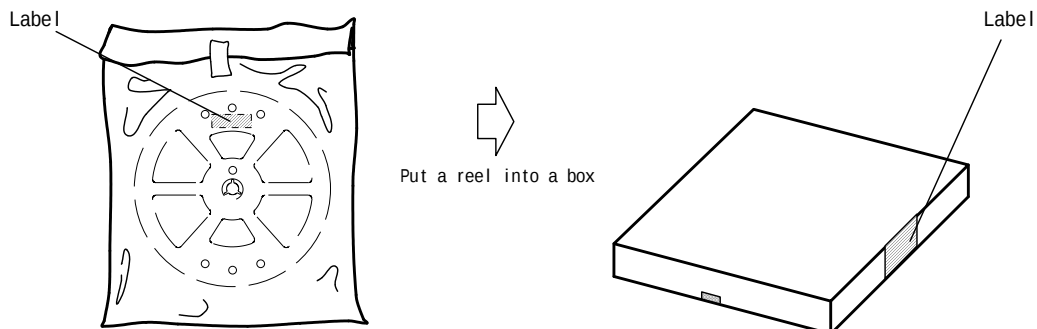


SYMBOL	DIMENSION
A	φ 330 ± 2
B	φ 80 ± 1
C	φ 13 ± 0.2
D	φ 21 ± 0.8
E	2 ± 0.5
W	13.5 ± 0.5
W1	17.5 ± 1

TAPING STATE

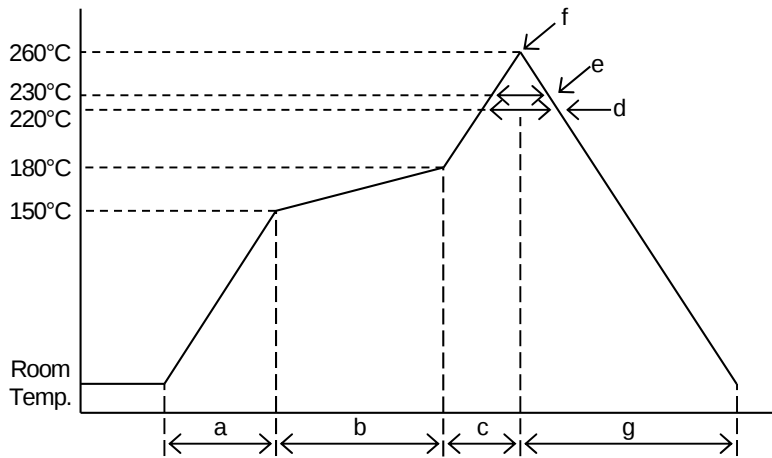


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature	150 to 180°C
	Pre-heating time	60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISION	CHANGES
August 31, 2020	Ver.1.0	Initial Release.

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