

100352

Low Power 8-Bit Buffer with Cut-Off Drivers

General Description

The 100352 contains an 8-bit buffer, individual inputs (Dn), outputs (Qn), and a data output enable pin ($\overline{\text{OEN}}$). A Q output follows its D input when the $\overline{\text{OEN}}$ pin is LOW. A HIGH on $\overline{\text{OEN}}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is -2.0V , presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

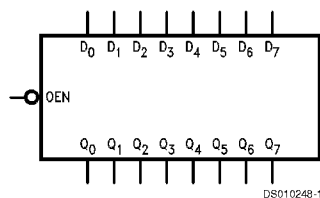
The 100352 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Ordering Code:

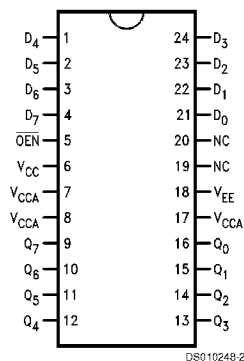
Logic Symbol



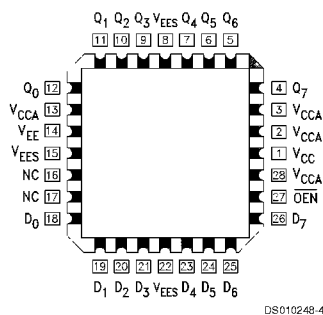
Pin Names	Description
D ₀ –D ₇	Data Inputs
$\overline{\text{OEN}}$	Output Enable Input
Q ₀ –Q ₇	Data Outputs
NC	No Connect

Connection Diagrams

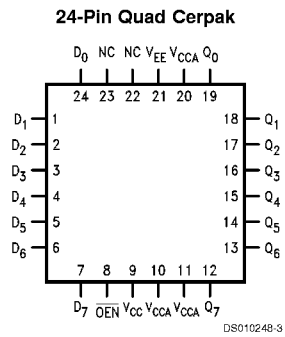
24-Pin DIP



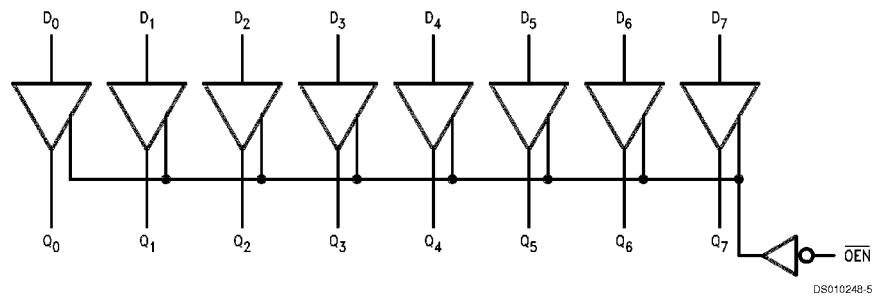
28-Pin PCC



Connection Diagrams (Continued)



Logic Diagram



Truth Table

Inputs		Outputs
Dn	$\overline{\text{OEN}}$	Qn
L	L	L
H	L	H
X	H	Cutoff

H = HIGH Voltage Level
 L = LOW Voltage Level
 Cutoff = Lower-than-LOW State
 X = Don't Care

Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired

Storage Temperature (T_{STG}) -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J)

Ceramic $+175^{\circ}\text{C}$

Plastic $+150^{\circ}\text{C}$

V_{EE} Pin Potential to

Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -100 mA

ESD (Note 2) $\geq 2000\text{V}$

Recommended Operating Conditions

Case Temperature (T_C)

Commercial 0°C to $+85^{\circ}\text{C}$

Industrial -40°C to $+85^{\circ}\text{C}$

Military -55°C to $+125^{\circ}\text{C}$

Supply Voltage (V_{EE}) -5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH(\text{Max})}$ or $V_{IL(\text{Min})}$ Loading with 25Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ Loading with 25Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610		
V_{OLZ}	Cut-Off LOW Voltage			-1950	mV	$V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ $\overline{\text{OEN}} = \text{HIGH}$
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL(\text{Min})}$
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH(\text{Max})}$
I_{EE}	Power Supply Current	-138 -143		-70 -70	mA	Inputs Open $V_{EE} = -4.2\text{V}$ to -4.8V $V_{EE} = -4.2\text{V}$ to -5.7V

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Parameter	$T_C = 0^{\circ}\text{C}$		$T_C = +25^{\circ}\text{C}$		$T_C = +85^{\circ}\text{C}$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.70	2.00	0.70	2.00	0.70	2.20	ns	Figures 1, 2 (Note 4)
t_{PHL}	Dn to Output								
t_{PZH}	Propagation Delay	1.60	4.20	1.60	4.20	1.60	4.20	ns	Figures 1, 2 (Note 4)
t_{PHZ}	$\overline{\text{OEN}}$ to Output	1.00	2.70	1.00	2.70	1.00	2.70		
t_{TLH}	Transition Time	0.45	2.00	0.45	2.00	0.45	2.00	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

$V_{EE} = 4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Dn to Output	0.70	1.80	0.70	1.80	0.70	2.00	ns	Figures 1, 2 (Note 6)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60	4.00	1.60	4.00	1.60	4.00	ns	Figures 1, 2 (Note 6)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	Figures 1, 2
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		230		230		230	ps	PCC only (Note 5)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		240		240		240	ps	PCC only (Note 5)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		350		350		350	ps	PCC only (Note 5)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		350		350		350	ps	PCC only (Note 5)

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 6: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version PCC DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$ (Note 7)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25 Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620			
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25 Ω to -2.0V
V_{OLC}	Output LOW Voltage		-1565		-1610			
V_{OLZ}	Cut-Off LOW Voltage		-1950		-1950	mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	$\overline{OEN} = HIGH$
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL(Min)}$	
I_{IH}	Input HIGH Current		340		240	μA	$V_{IN} = V_{IH(Max)}$	
I_{EE}	Power Supply Current	-138 -143	-60 -60	-138 -143	-70 -70	mA	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	

Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

$V_{EE} = 4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.60	1.80	0.70	1.80	0.70	2.00	ns	Figures 1, 2 (Note 8)
t_{PHL}	Dn to Output								
t_{PZH}	Propagation Delay	1.40	4.40	1.60	4.00	1.60	4.00	ns	Figures 1, 2 (Note 8)
t_{PHZ}	$\overline{OEN}$ to Output	1.00	2.50	1.00	2.50	1.00	2.50		
t_{TLH}	Transition Time	0.40	2.50	0.45	1.90	0.45	1.90	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

Note 8: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to $-2.0V$	(Notes 9, 10, 11)
		-1085	-870	mV	$-55^\circ C$			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to $-2.0V$	(Notes 9, 10, 11)
		-1830	-1555	mV	$-55^\circ C$			
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to $-2.0V$	(Notes 9, 10, 11)
		-1085		mV	$-55^\circ C$			
V_{OLC}	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH(Min)}$, or $V_{IL(Max)}$	$\overline{OEN}$ =HIGH	(Notes 9, 10, 11)
			-1555	mV	$-55^\circ C$			
V_{OLZ}	Cut-Off LOW Voltage		-1950	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH(Min)}$, or $V_{IL(Max)}$	$\overline{OEN}$ =HIGH	(Notes 9, 10, 11)
			-1850	mV	$-55^\circ C$			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH signal for All inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW signal for All inputs		(Notes 9, 10, 11, 12)
I_{IL}	Input LOW Current	0.50		μA	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = 4.2V$ $V_{IN} = V_{IL(Min)}$		(Notes 9, 10, 11)
I_{IH}	Input HIGH Current		240	μA	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$		(Notes 9, 10, 11)
			340	μA	$-55^\circ C$	$V_{IN} = V_{IH(Max)}$		
I_{EE}	Power Supply Current				$-55^\circ C$ to $+125^\circ C$	Inputs Open		(Notes 9, 10, 11)
		-145 -150	-55	mA		$V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$		

Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 11: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 12: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.30	2.60	0.50	2.40	0.50	2.70	ns	Figures 1, 2	(Notes 13, 14, 16, 17)
t_{PHL}	Dn to Output									

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

Note 13: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 14: Screen tested 100% on each device at $+25^{\circ}\text{C}$ temperature only, Subgroup A9.

Note 15: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^{\circ}\text{C}$, Subgroup A9, and at $+125^{\circ}\text{C}$ and -55°C temperatures, Subgroups A10 and A11.

Note 16: Not tested at $+25^{\circ}\text{C}$, $+125^{\circ}\text{C}$, and -55°C temperature (design characterization data).

Note 17: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1\mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 25Ω to GND
 C_L = Fixture and stray capacitance $\leq 3\text{ pF}$

The timing diagram illustrates the relationship between the DATA input, OUTPUT ENABLE, and OUTPUT signals. The DATA signal is a square wave. The OUTPUT ENABLE signal is a pulse. The OUTPUT signal is a square wave that follows the DATA signal when OUTPUT ENABLE is active. The propagation delay t_{PD} is the time from a DATA transition to the corresponding OUTPUT transition. The output delay times t_{PHZ} , t_{PLH} , t_{PHL} , and t_{PLZ} are shown relative to the OUTPUT ENABLE signal transitions. t_{PHZ} and t_{PLH} are the delays from the rising edge of OUTPUT ENABLE to the output reaching a high state. t_{PHL} and t_{PLZ} are the delays from the falling edge of OUTPUT ENABLE to the output reaching a low state. The 50% point of the output transition is marked.

Note:
The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active V_{OL} and V_{OH} .

6

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Technical drawing of a 24-pin D-sub connector showing top, side, and detail views with dimensions in inches and millimeters.

Top View Dimensions:

- Overall Width: 1.215 (30.86) MAX
- Pin 1 to Pin 12 Distance: 0.025 (0.64) RAD
- Pin 13 to Pin 24 Distance: 0.030 - 0.055 (0.76 - 1.40) RAD TYP
- Pin 1 to Pin 13 Distance: 0.390 (9.91) MAX
- Pin 1 to Pin 12 Distance: 0.005 (0.13) MIN TYP
- Pin 13 to Pin 24 Distance: 0.050 - 0.060 (1.27 - 1.52) TYP
- Pin 1 to Pin 12 Distance: 0.032 - 0.042 (0.81 - 1.07) TYP
- Pin 13 to Pin 24 Distance: 0.015 - 0.055 (0.38 - 1.40) TYP
- Pin 1 to Pin 12 Distance: 0.225 (5.72) MAX TYP
- Pin 13 to Pin 24 Distance: 0.400 - 0.430 (10.16 - 10.92) TYP
- Pin 1 to Pin 12 Distance: 0.180 (4.57) MAX
- Pin 13 to Pin 24 Distance: 0.008 - 0.012 (0.20 - 0.30) TYP

Side View Dimensions:

- Pin 1 to Pin 12 Distance: 0.005 (0.13) MIN TYP
- Pin 13 to Pin 24 Distance: 0.050 - 0.060 (1.27 - 1.52) TYP
- Pin 1 to Pin 12 Distance: 0.032 - 0.042 (0.81 - 1.07) TYP
- Pin 13 to Pin 24 Distance: 0.015 - 0.055 (0.38 - 1.40) TYP
- Pin 1 to Pin 12 Distance: 0.225 (5.72) MAX TYP
- Pin 13 to Pin 24 Distance: 0.400 - 0.430 (10.16 - 10.92) TYP
- Pin 1 to Pin 12 Distance: 0.180 (4.57) MAX
- Pin 13 to Pin 24 Distance: 0.008 - 0.012 (0.20 - 0.30) TYP

Detail View Dimensions:

- Pin 1 to Pin 12 Distance: 0.005 (0.13) MIN TYP
- Pin 13 to Pin 24 Distance: 0.050 - 0.060 (1.27 - 1.52) TYP
- Pin 1 to Pin 12 Distance: 0.032 - 0.042 (0.81 - 1.07) TYP
- Pin 13 to Pin 24 Distance: 0.015 - 0.055 (0.38 - 1.40) TYP
- Pin 1 to Pin 12 Distance: 0.225 (5.72) MAX TYP
- Pin 13 to Pin 24 Distance: 0.400 - 0.430 (10.16 - 10.92) TYP
- Pin 1 to Pin 12 Distance: 0.180 (4.57) MAX
- Pin 13 to Pin 24 Distance: 0.008 - 0.012 (0.20 - 0.30) TYP

Other Dimensions:

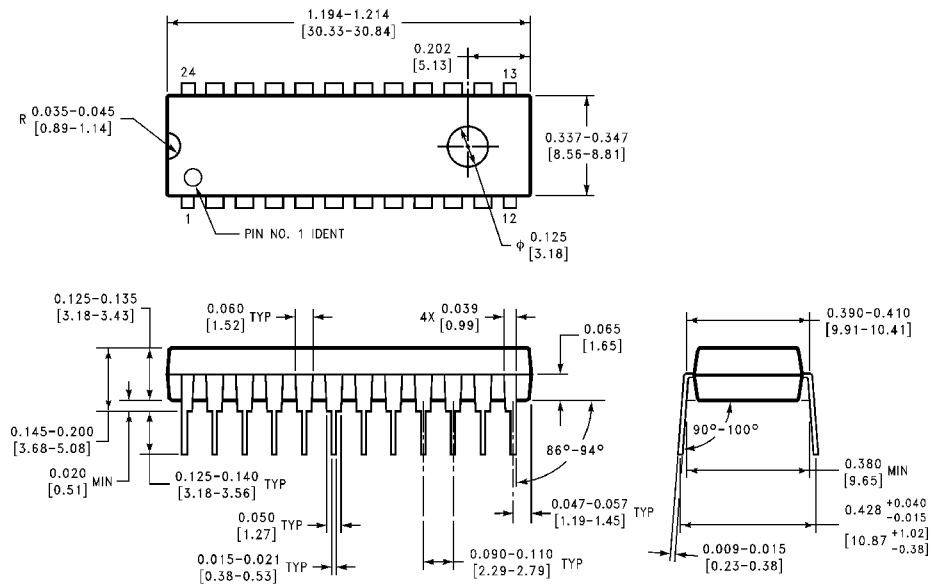
- Pin 1 to Pin 12 Distance: 0.005 (0.13) MIN TYP
- Pin 13 to Pin 24 Distance: 0.050 - 0.060 (1.27 - 1.52) TYP
- Pin 1 to Pin 12 Distance: 0.032 - 0.042 (0.81 - 1.07) TYP
- Pin 13 to Pin 24 Distance: 0.015 - 0.055 (0.38 - 1.40) TYP
- Pin 1 to Pin 12 Distance: 0.225 (5.72) MAX TYP
- Pin 13 to Pin 24 Distance: 0.400 - 0.430 (10.16 - 10.92) TYP
- Pin 1 to Pin 12 Distance: 0.180 (4.57) MAX
- Pin 13 to Pin 24 Distance: 0.008 - 0.012 (0.20 - 0.30) TYP

Notes:

- GLASS SEALANT
- 86° - 94° TYP
- 90° - 100° TYP
- BOTH ENDS

24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
Package Number J24E

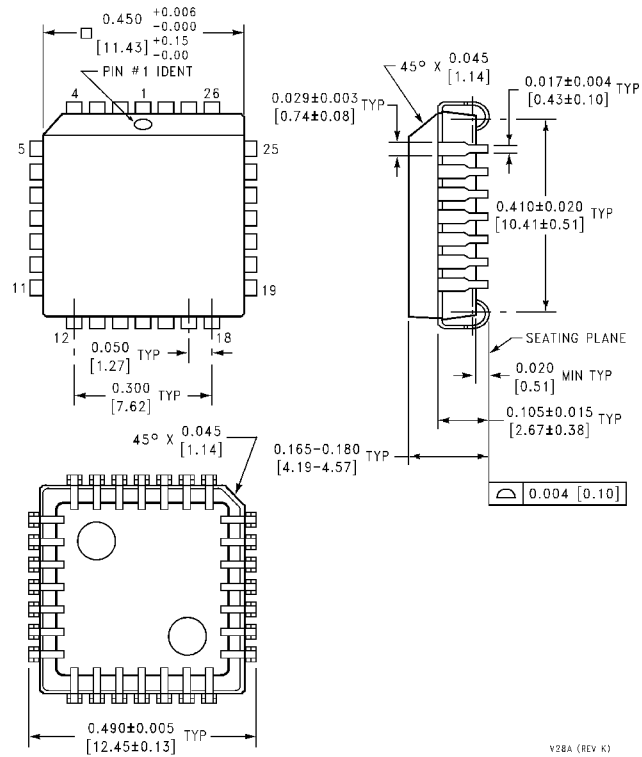
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N24E (REV A)

24-Lead Plastic Dual-In-Line Package (P)
Package Number N24E

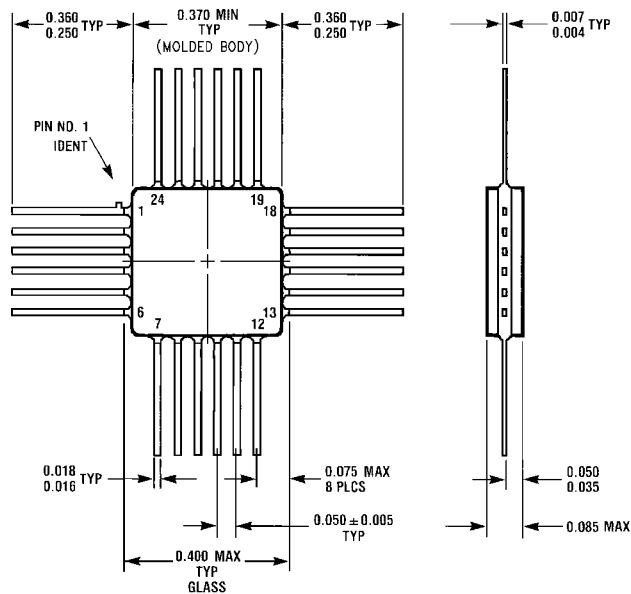
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



V28A (REV K)

**28-Lead Plastic Chip Carrier (Q)
Package Number V28A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Quad Cerpak (F)
Package Number W24B**

W24B (REV D)

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com