

SNx4LS24x, SNx4S24x Octal Buffers and Line Drivers With 3-State Outputs

1 Features

- Inputs Tolerant Down to 2 V, Compatible With 3.3-V or 2.5-V Logic Inputs
- Maximum t_{pd} of 15 ns at 5 V
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

The SNx4LS24x, SNx4S24x octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and non-inverting outputs, symmetrical, active-low output-control (\overline{G}) inputs, and complementary output-control (G and \overline{G}) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS24x and SN74S24x devices can be used to drive terminated lines down to 133 Ω .

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------------------|----------------|--------------------|
| SN54LS24x, SN54S24x | CDIP (20) – J | 24.20 mm × 6.92 mm |
| | CFP (20) – W | 7.02 mm × 13.72 mm |
| | LCCC (20) – FK | 8.89 mm × 8.89 mm |
| SN74LS240, SN74LS244 | SSOP (20) – DB | 7.20 mm × 5.30 mm |
| SN74LS24x, SN74S24x | SOIC (20) – DW | 12.80 mm × 7.50 mm |
| | PDIP (20) – N | 24.33 mm × 6.35 mm |
| SN74LS24x | SOP (20) – NS | 7.80 mm × 12.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

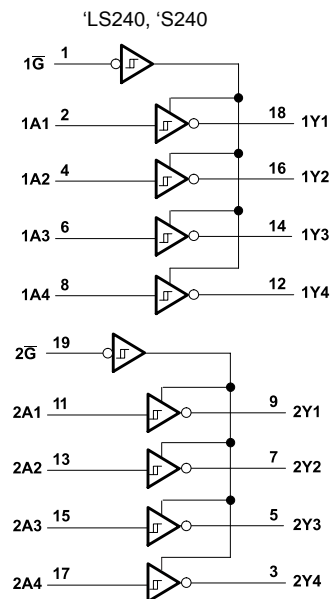


Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 8.2 Functional Block Diagrams | 11 |
| 2 Applications | 1 | 8.3 Feature Description | 12 |
| 3 Description | 1 | 8.4 Device Functional Modes | 12 |
| 4 Revision History | 2 | 9 Application and Implementation | 14 |
| 5 Pin Configuration and Functions | 3 | 9.1 Application Information | 14 |
| 6 Specifications | 4 | 9.2 Typical Application | 14 |
| 6.1 Absolute Maximum Ratings | 4 | 9.3 System Examples | 15 |
| 6.2 ESD Ratings | 4 | 10 Power Supply Recommendations | 17 |
| 6.3 Recommended Operating Conditions | 4 | 11 Layout | 17 |
| 6.4 Thermal Information | 5 | 11.1 Layout Guidelines | 17 |
| 6.5 Electrical Characteristics – SNx4LS24x | 5 | 11.2 Layout Example | 17 |
| 6.6 Electrical Characteristics – SNx4S24x | 5 | 12 Device and Documentation Support | 18 |
| 6.7 Switching Characteristics – SNx4LS24x | 6 | 12.1 Related Links | 18 |
| 6.8 Switching Characteristics – SNx4S24x | 6 | 12.2 Receiving Notification of Documentation Updates | 18 |
| 6.9 Typical Characteristics | 7 | 12.3 Community Resource | 18 |
| 7 Parameter Measurement Information | 7 | 12.4 Trademarks | 18 |
| 7.1 SN54LS24x and SN74LS24x Devices | 7 | 12.5 Electrostatic Discharge Caution | 18 |
| 7.2 SN54S24x and SN74S24x Devices | 9 | 12.6 Glossary | 18 |
| 8 Detailed Description | 11 | 13 Mechanical, Packaging, and Orderable Information | 19 |
| 8.1 Overview | 11 | | |

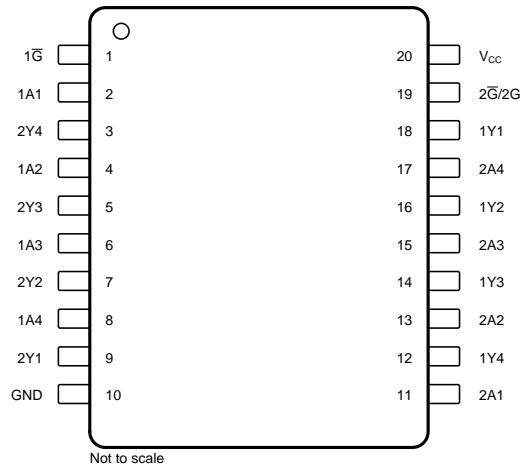
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

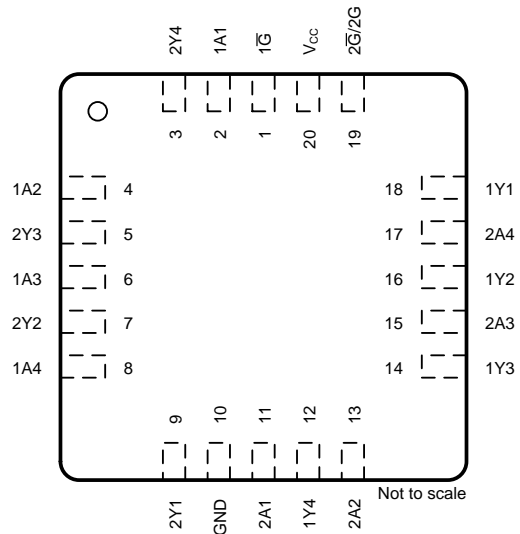
| Changes from Revision C (May 2010) to Revision D | Page |
|---|----------|
| • Added <i>Applications</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted Ordering Information table; see POA at the end of the data sheet | 1 |
| • Changed $R_{\theta_{JA}}$ values in the <i>Thermal Information</i> table from 70 to 94.3 (DB), from 58 to 90.3 (DW), from 69 to 50.6 (N), and from 60 to 76.6 (NS) | 5 |

5 Pin Configuration and Functions

DB, DW, J, N, NS, or W Package
20-Pin SSOP, SOIC, CDIP, PDIP, SOP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|--------------------------------|-----|-------------------------|
| NO. | NAME | | |
| 1 | 1 \bar{G} | I | Channel 1 output enable |
| 2 | 1A1 | I | Channel 1, A side 1 |
| 3 | 2Y4 | O | Channel 2, Y side 4 |
| 4 | 1A2 | I | Channel 1, A side 2 |
| 5 | 2Y3 | O | Channel 2, Y side 3 |
| 6 | 1A3 | I | Channel 1, A side 3 |
| 7 | 2Y2 | O | Channel 2, Y side 2 |
| 8 | 1A4 | I | Channel 1, A side 4 |
| 9 | 2Y1 | O | Channel 2, Y side 1 |
| 10 | GND | — | Ground |
| 11 | 2A1 | I | Channel 2, A side 1 |
| 12 | 1Y4 | O | Channel 1, Y side 4 |
| 13 | 2A2 | I | Channel 2, A side 2 |
| 14 | 1Y3 | O | Channel 1, Y side 3 |
| 15 | 2A3 | I | Channel 2, A side 3 |
| 16 | 1Y2 | O | Channel 1, Y side 2 |
| 17 | 2A4 | I | Channel 2, A side 4 |
| 18 | 1Y1 | O | Channel 1, Y side 1 |
| 19 | 2 \bar{G} /2G ⁽¹⁾ | I | Channel 2 output enable |
| 20 | V _{CC} | — | Power supply |

(1) 2G for SNx4LS241 and SNx4S241 or 2 \bar{G} for all other drivers.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|-----------|-----|-----|------|
| Supply voltage, V_{CC} ⁽²⁾ | | | 7 | V |
| Input voltage, V_I | SNx4LS24x | | 7 | V |
| | SNx4S24x | | 5.5 | |
| Off-state output voltage | | | 5.5 | V |
| Storage temperature, T_{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------------------------------|--|--|-------|------|
| ALL PACKAGES | | | | |
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | | 500 | V |
| N PACKAGE | | | | |
| $V_{(ESD)}$ Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | | 500 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|---------------------|------|-----|------|------------|
| V_{CC} Supply voltage ⁽¹⁾ | SN54xS24x | 4.5 | 5 | 5.5 | V |
| | SN74xS24x | 4.75 | 5 | 5.25 | |
| V_{IH} High-level input voltage | | 2 | | | V |
| V_{IL} Low-level input voltage | SN54LS24x | | | 0.7 | V |
| | SN54S24x, SN74xS24x | | | 0.8 | |
| I_{OH} High-level output current | SN54xS24x | | | -12 | mA |
| | SN74xS24x | | | -15 | |
| I_{OL} Low-level output current | SN54LS24x | | | 12 | mA |
| | SN54S24x | | | 48 | |
| | SN74LS24x | | | 24 | |
| | SN74S24x | | | 64 | |
| External resistance between any input and V_{CC} or ground (SNx4S24x only) | | | | 40 | k Ω |
| T_A Operating free-air temperature ⁽²⁾ | SN54xS24x | -55 | | 125 | °C |
| | SN74xS24x | 0 | | 70 | |

- (1) Voltage values are with respect to network ground terminal.
- (2) An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 40°C/W.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LS240, SN74LS244 | SN74LS24x, SN74S24x | | SN74LS24x | UNIT |
|-------------------------------|--|-------------------------|---------------------|----------|-----------|------|
| | | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽²⁾⁽³⁾ | 94.3 | 90.3 | 50.6 | 76.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 55.9 | 45.5 | 37.4 | 42.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 49.5 | 48.1 | 31.5 | 44.1 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 21.3 | 19.4 | 24 | 19.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 49.1 | 47.6 | 31.4 | 43.7 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Voltage values are with respect to network ground terminal.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics – SNx4LS24x

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT | |
|---|--|------------------|------------------------------------|--------------------|------|------|----|
| V _{IK} | V _{CC} = MIN, I _I = –18 mA | | | | –1.5 | V | |
| Hysteresis (V _{T+} – V _{T–}) | V _{CC} = MIN | | 0.2 | 0.4 | | V | |
| V _{OH} | V _{CC} = MIN, I _{OH} = –3 mA, V _{IH} = 2 V, V _{IL} = MAX | | 2.4 | 3.4 | | V | |
| | V _{CC} = MIN, I _{OH} = MAX, V _{IH} = 2 V, V _{IL} = 0.5 V | | 2 | | | | |
| V _{OL} | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V | | I _{OL} = 12 mA, SN54LS24x | | 0.4 | V | |
| | | | I _{OL} = 24 mA, SN74LS24x | | 0.5 | | |
| I _{OZH} | V _{CC} = MAX, V _{IL} = MAX, V _{IH} = 2 V, V _O = 2.7 V | | | | 20 | μA | |
| I _{OZL} | V _{CC} = MAX, V _{IL} = MAX, V _{IH} = 2 V, V _O = 0.4 V | | | | –20 | μA | |
| I _I | V _{CC} = MAX, V _I = 7 V | | | | 0.1 | mA | |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | | 20 | μA | |
| I _{IL} | V _{CC} = MAX, V _{IL} = 0.4 V | | | | –0.2 | mA | |
| I _{OS} ⁽³⁾ | V _{CC} = MAX | | –40 | | –225 | mA | |
| I _{CC} | V _{CC} = MAX, output open | Outputs high | All | | 17 | 27 | mA |
| | | Outputs low | SNx4LS240 | | 26 | 44 | |
| | | | SNx4LS241, SNx4LS244 | | 27 | 46 | |
| | | Outputs disabled | SNx4LS240 | | 29 | 50 | |
| SNx4LS241, SNx4LS244 | | | 32 | 54 | | | |

- (1) For conditions shown as minimum or maximum, use the appropriate value specified under recommended operating conditions.
- (2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
- (3) Not more than one output must be shorted at a time, and duration of the short-circuit must not exceed one second.

6.6 Electrical Characteristics – SNx4S24x

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|---|---|--|-----|--------------------|------|------|
| V _{IK} | V _{CC} = MIN, I _I = –18 mA | | | | –1.2 | V |
| Hysteresis (V _{T+} – V _{T–}) | V _{CC} = MIN | | 0.2 | 0.4 | | V |
| V _{OH} | V _{CC} = MIN, I _{OH} = –1 mA, V _{IH} = 2 V, V _{IL} = 0.8 V, SN74S24x only | | 2.7 | | | V |
| | V _{CC} = MIN, I _{OH} = –3 mA, V _{IH} = 2 V, V _{IL} = 0.8 V | | 2.4 | 3.4 | | |
| | V _{CC} = MIN, I _{OH} = MAX, V _{IH} = 2 V, V _{IL} = 0.5 V | | 2 | | | |
| V _{OL} | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 0.8 V | | | | 0.55 | V |

- (1) For conditions shown as minimum or maximum, use the appropriate value specified under recommended operating conditions.
- (2) All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics – SNx4S24x (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT | |
|--------------------------------|---|------------------|--------------------|--------------------|------|------|----|
| I _{OZH} | V _{CC} = MAX, V _{IL} = 0.8 V, V _{IH} = 2 V, V _O = 2.4 V | | | | 50 | μA | |
| I _{OZL} | V _{CC} = MAX, V _{IL} = MAX, V _{IH} = 2 V, V _O = 0.5 V | | | | –50 | μA | |
| I _I | V _{CC} = MAX, V _I = 5.5 V | | | | 1 | mA | |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | | | 50 | μA | |
| I _{IL} | V _{CC} = MAX, V _{IL} = 0.5 V | Any A | | | –400 | μA | |
| | | Any G | | | –2 | mA | |
| I _{OS} ⁽³⁾ | V _{CC} = MAX | | –50 | | –225 | mA | |
| I _{CC} | V _{CC} = MAX, output open | Outputs high | SN54S240 | | 80 | 123 | mA |
| | | | SN74S240 | | 80 | 135 | |
| | | | SN54S241, SN54S244 | | 95 | 147 | |
| | | | SN74S241, SN74S244 | | 95 | 160 | |
| | | Outputs low | SN54S240 | | 100 | 145 | |
| | | | SN74S240 | | 100 | 150 | |
| | | | SN54S241, SN54S244 | | 120 | 170 | |
| | | | SN74S241, SN74S244 | | 120 | 180 | |
| | | Outputs disabled | SN54S240 | | 100 | 145 | |
| | | | SN74S240 | | 100 | 150 | |
| | | | SN54S241, SN54S244 | | 120 | 170 | |
| | | | SN74S241, SN74S244 | | 120 | 180 | |

(3) Not more than one output must be shorted at a time, and duration of the short-circuit must not exceed one second.

6.7 Switching Characteristics – SNx4LS24x

V_{CC} = 5 V, T_A = 25°C (see [SN54LS24x](#) and [SN74LS24x](#) Devices)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|--|----------------------|-----|-----|-----|------|
| t _{PLH} | R _L = 667 Ω, C _L = 45 pF | SNx4LS240 | | 9 | 14 | ns |
| | | SNx4LS241, SNx4LS244 | | 12 | 18 | |
| t _{PHL} | R _L = 667 Ω, C _L = 45 pF | | | 12 | 18 | ns |
| t _{PZL} | R _L = 667 Ω, C _L = 45 pF | | | 20 | 30 | ns |
| t _{PZH} | R _L = 667 Ω, C _L = 45 pF | | | 15 | 23 | ns |
| t _{PLZ} | R _L = 667 Ω, C _L = 5 pF | | | 10 | 20 | ns |
| t _{PHZ} | R _L = 667 Ω, C _L = 5 pF | | | 15 | 25 | ns |

6.8 Switching Characteristics – SNx4S24x

V_{CC} = 5 V and T_A = 25°C (see [SN54S24x](#) and [SN74S24x](#) Devices)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|---|--------------------|-----|-----|-----|------|
| t _{PLH} | R _L = 90 Ω, C _L = 50 pF | SNx4S240 | | 4.5 | 7 | ns |
| | | SNx4S241, SNx4S244 | | 6 | 9 | |
| t _{PHL} | R _L = 90 Ω, C _L = 50 pF | SNx4S240 | | 4.5 | 7 | ns |
| | | SNx4S241, SNx4S244 | | 6 | 9 | |
| t _{PZL} | R _L = 90 Ω, C _L = 50 pF | | | 10 | 15 | ns |
| t _{PZH} | R _L = 90 Ω, C _L = 50 pF | SNx4S240 | | 6.5 | 10 | ns |
| | | SNx4S241, SNx4S244 | | 8 | 12 | |
| t _{PLZ} | R _L = 90 Ω, C _L = 5 pF | | | 10 | 15 | ns |
| t _{PHZ} | R _L = 90 Ω, C _L = 5 pF | | | 6 | 9 | ns |

6.9 Typical Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$, and $R_L = 667\ \Omega$ (unless otherwise noted)

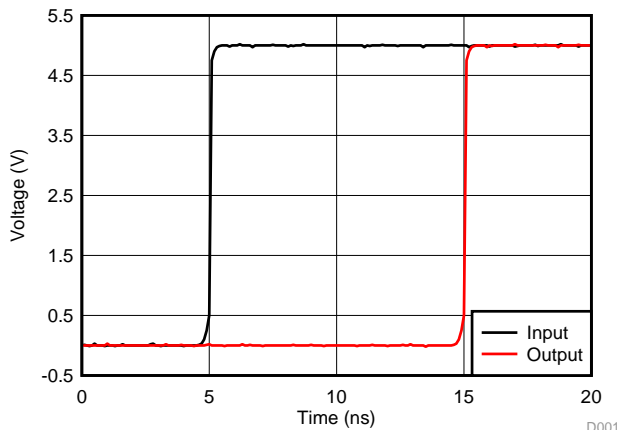


Figure 1. Simulated Propagation Delay From Input to Output

7 Parameter Measurement Information

7.1 SN54LS24x and SN74LS24x Devices

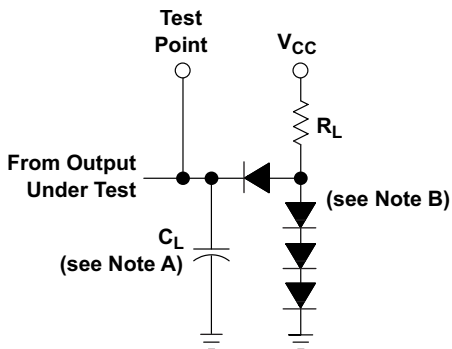


Figure 2. Load Circuit, For 2-State Totem-Pole Outputs

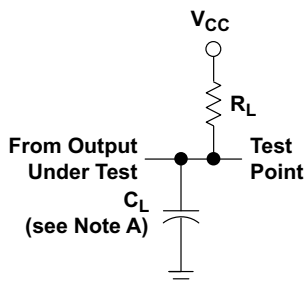


Figure 3. Load Circuit, For Open-Collector Outputs

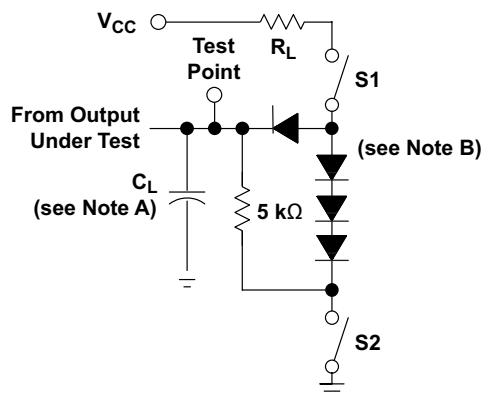


Figure 4. Load Circuit, For 3-State Outputs

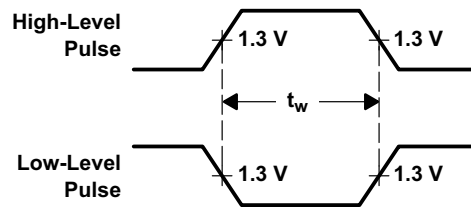


Figure 5. Voltage Waveforms, Pulse Durations

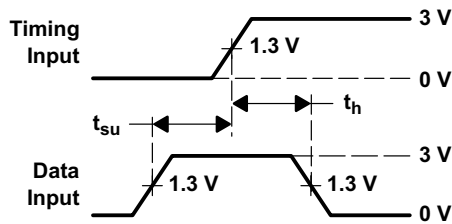


Figure 6. Voltage Waveforms, Setup and Hold Times

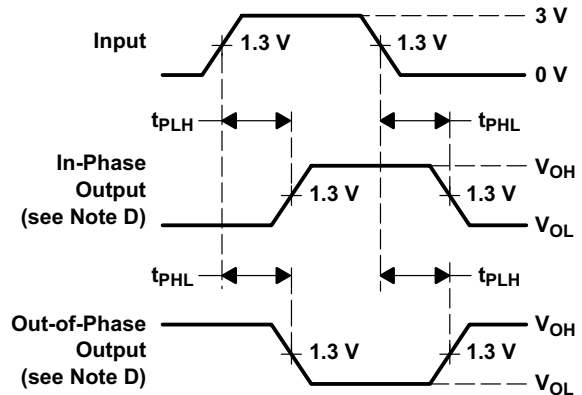
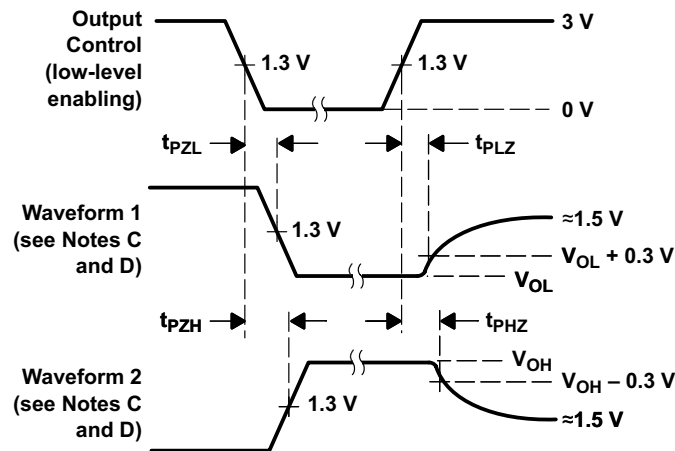


Figure 7. Voltage Waveforms, Propagation Delay Times



- C_L includes probe and jig capacitance.
- All diodes are 1N3064 or equivalent.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
- Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, Z_O is approximately 50Ω , $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- The outputs are measured one at a time with one input transition per measurement.

Figure 8. Voltage Waveforms, Enable and Disable Times, 3-State Outputs

7.2 SN54S24x and SN74S24x Devices

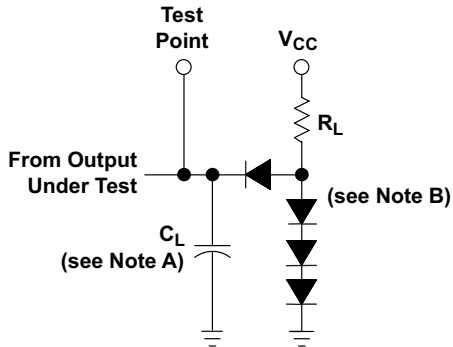


Figure 9. Load Circuit, For 2-State Totem-Pole Outputs

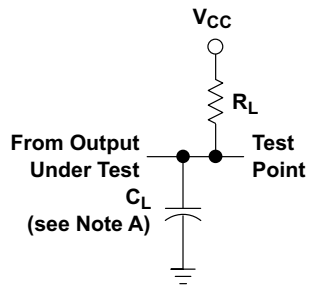


Figure 10. Load Circuit, For Open-Collector Outputs

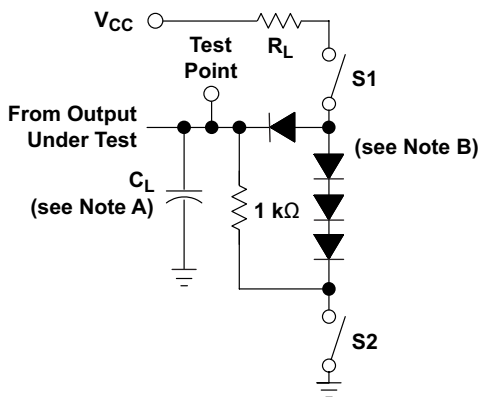


Figure 11. Load Circuit, For 3-State Outputs

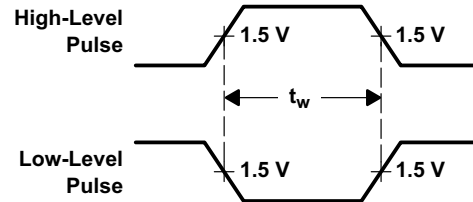


Figure 12. Voltage Waveforms, Pulse Durations

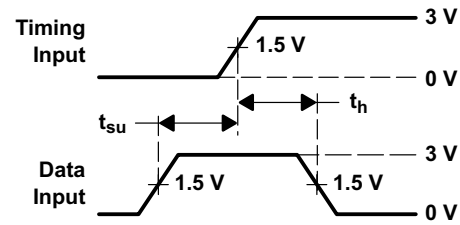


Figure 13. Voltage Waveforms, Setup and Hold Times

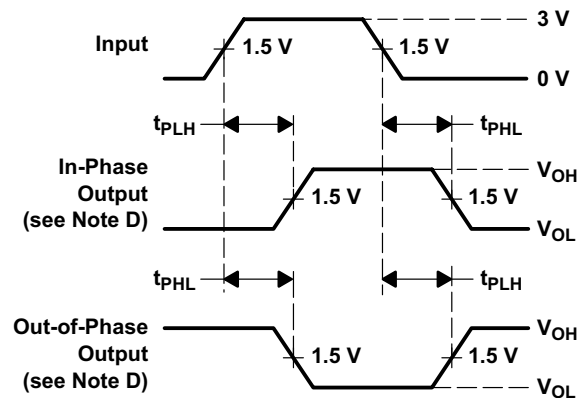
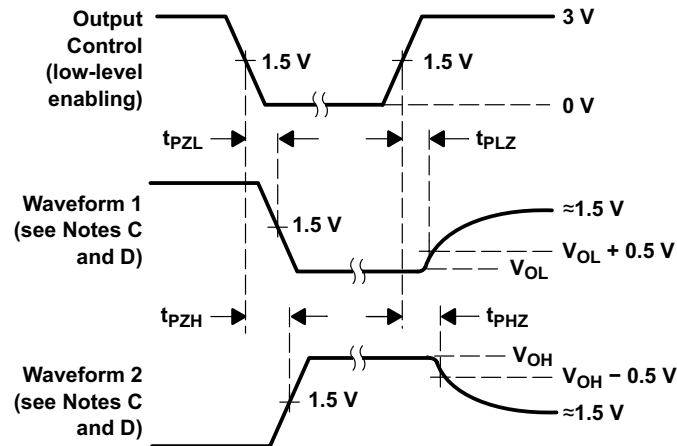


Figure 14. Voltage Waveforms, Propagation Delay Times



- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N3064 or equivalent.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
- E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O is approximately 50 Ω ; t_r and $t_f \leq$ 7 ns for SN54LS24x and SN74LS24x devices, and t_r and $t_f \leq$ 2.5 ns for SN54S24x and SN74S24x devices.
- F. The outputs are measured one at a time with one input transition per measurement.

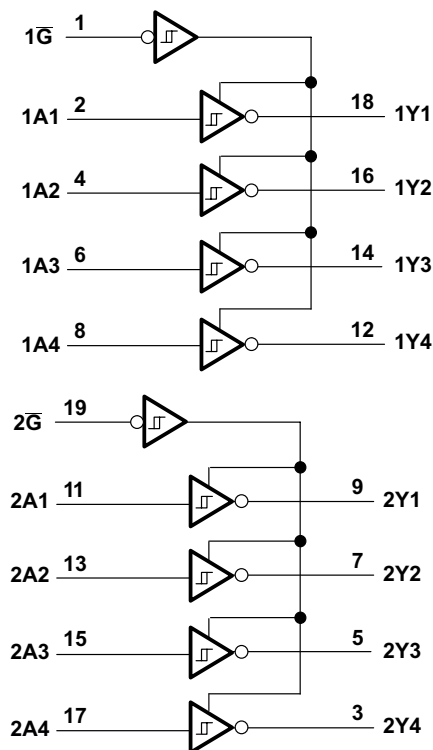
Figure 15. Voltage Waveforms, Enable and Disable Times, 3-State Outputs

8 Detailed Description

8.1 Overview

This device is organized as two 4-bit buffers and drivers with separate output-enable (\overline{G}) inputs. When \overline{G} is low, the device passes data from the A inputs to the Y outputs. When \overline{G} is high, the outputs are in the high impedance state. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V and 5-V system environment. To ensure the high-impedance state during power up or power down, \overline{G} must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

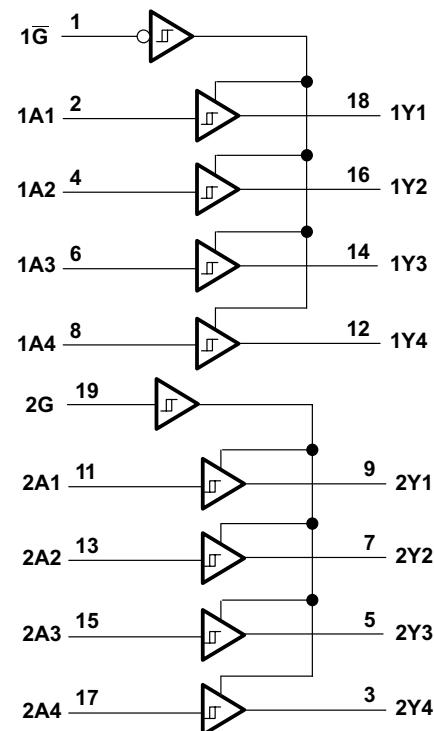
8.2 Functional Block Diagrams



Copyright © 2016, Texas Instruments Incorporated

Pin numbers shown are for DB, DW, J, N, NS, and W packages

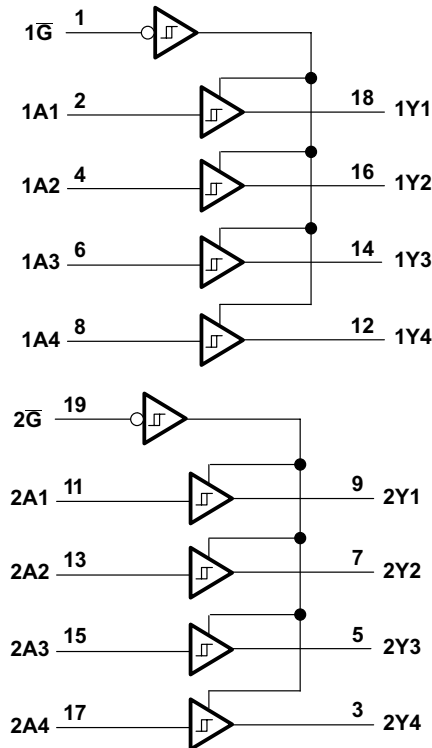
Figure 16. SNx4LS240 and SNx4S240 Logic Diagram



Copyright © 2016, Texas Instruments Incorporated

Pin numbers shown are for DB, DW, J, N, NS, and W packages

Figure 17. SNx4LS241 and SNx4S241 Logic Diagram



Copyright © 2016, Texas Instruments Incorporated

Pin numbers shown are for DB, DW, J, N, NS, and W packages

**Figure 18. SNx4LS244 and SNx4S244
 Logic Diagram**

8.3 Feature Description

8.3.1 3-State Outputs

The 3-state outputs can drive bus lines directly. All outputs can be put into high impedance mode through the \overline{G} pin.

8.3.2 PNP Inputs

This device has PNP inputs which reduce dc loading on bus lines.

8.3.3 Hysteresis on Bus Inputs

The bus inputs have built-in hysteresis that improves noise margins.

8.4 Device Functional Modes

The SNx4LS24x and SNx4S24x devices can be used as inverting and non-inverting bus buffers for data line transmission and can isolate input to output by setting the \overline{G} pin HIGH. [Table 1](#), [Table 2](#), and [Table 3](#) list the function tables for all devices.

**Table 1. SNx4LS240 and SNx4S240
 Function Table**

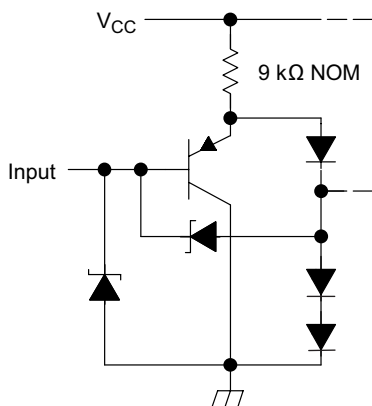
| INPUTS | | OUTPUTS |
|----------------|---|---------|
| \overline{G} | A | Y |
| L | L | H |
| L | H | L |
| H | X | Z |

Table 2. SNx4LS241 and SNx4S241
Function Table

| CHANNEL 1 | | | CHANNEL 2 | | |
|-------------|----|--------|-----------|----|--------|
| INPUTS | | OUTPUT | INPUTS | | OUTPUT |
| 1 \bar{G} | 1A | 1Y | 2G | 2A | 2Y |
| L | L | L | H | L | L |
| L | H | H | H | H | H |
| H | X | Z | L | X | Z |

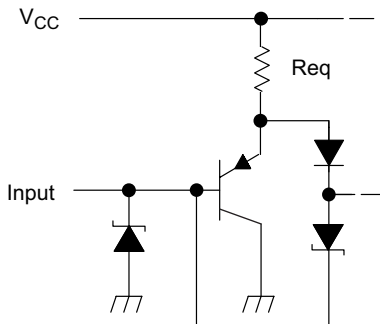
Table 3. SNx4LS244 and SNx4S244
Function Table

| INPUTS | | OUTPUTS |
|-----------|---|---------|
| \bar{G} | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |



Copyright © 2016, Texas Instruments Incorporated

Figure 19. SNx4LS240, SNx4LS241, SNx4LS244
Equivalent of Each Input

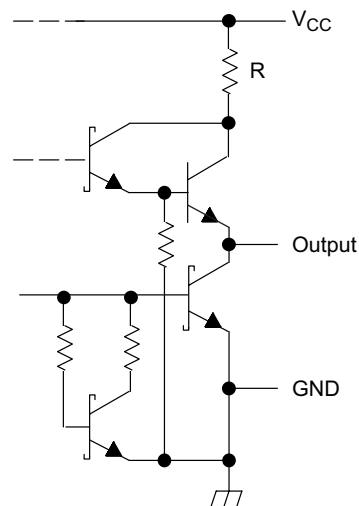


Copyright © 2016, Texas Instruments Incorporated

G and \bar{G} inputs: $R_{eq} = 2 \text{ k}\Omega \text{ NOM}$

A inputs: $R_{eq} = 2.8 \text{ k}\Omega \text{ NOM}$

Figure 20. SNx4S240, SNx4S241, SNx4S244
Equivalent of Each Input



Copyright © 2016, Texas Instruments Incorporated

SNx4LS240, SNx4LS241, SNx4LS244:

$R = 50 \Omega \text{ NOM}$

SNx4S240, SNx4S241, SNx4S244:

$R = 25 \Omega \text{ NOM}$

Figure 21. Typical of All Outputs

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4LS24x, SNx4S24x octal buffers and line drivers are designed to be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

9.2 Typical Application

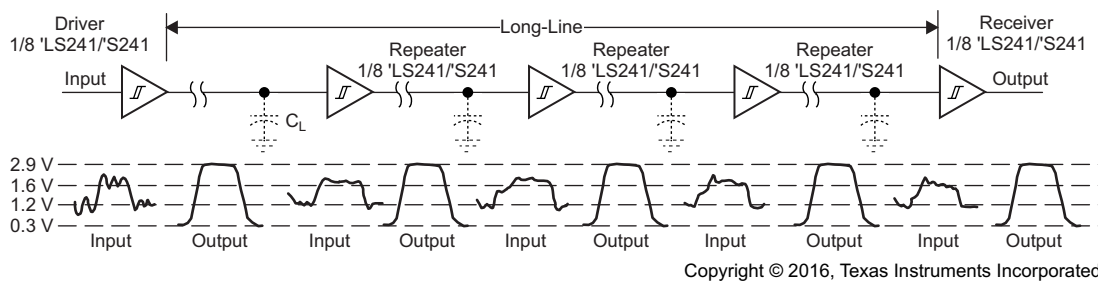


Figure 22. SNx4LS241 and SNx4S241 Used as Repeater or Level Restorer

9.2.1 Design Requirements

This device uses Schottky transistor logic technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Power Supply
 - Each device must maintain a supply voltage between 4.5 V and 5.5 V.
- Inputs
 - Input signals must meet the V_{IH} and V_{IL} specifications in [Electrical Characteristics – SNx4LS24x](#).
 - Inputs leakage values (I_I , I_{IH} , I_{IL}) from [Electrical Characteristics – SNx4LS24x](#) must be considered.
- Outputs
 - Output signals are specified to meet the V_{OH} and V_{OL} specifications in [Electrical Characteristics – SNx4LS24x](#) as a minimum (the values could be closer to V_{CC} for high signals or GND for low signals).
 - TI recommends maintaining output currents as specified in [Recommended Operating Conditions](#).
 - The part can be damaged by sourcing or sinking too much current (see [Electrical Characteristics – SNx4LS24x](#) for details).

Typical Application (continued)

9.2.3 Application Curve

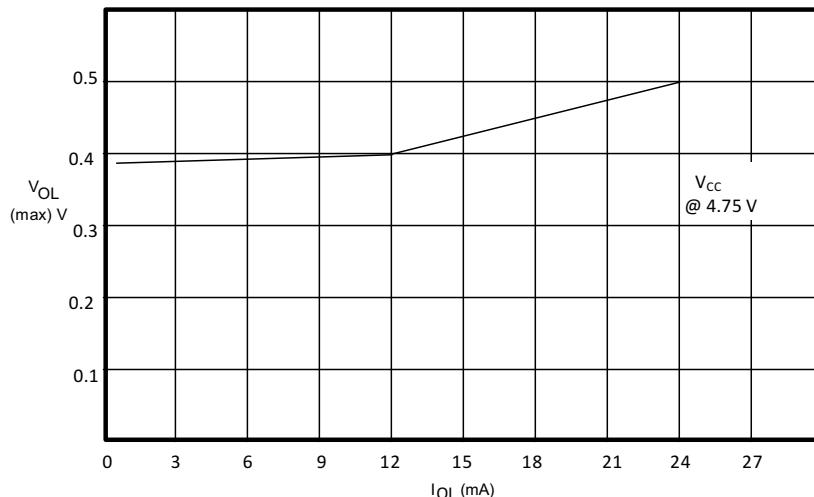
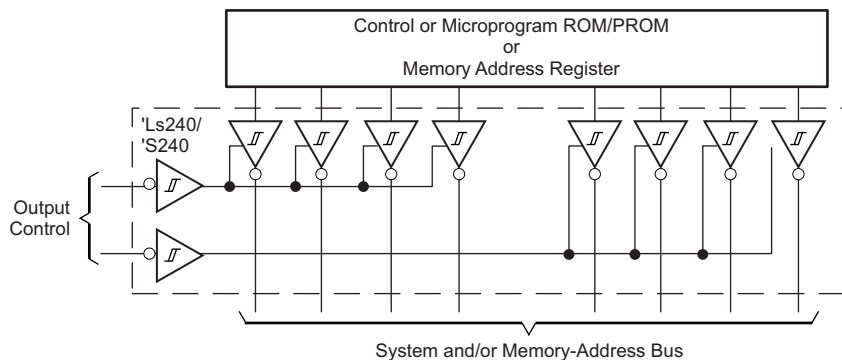


Figure 23. V_{OL} vs I_{OL}

9.3 System Examples

The SNx4LS240 and SNx4S240 devices can be used to buffer signals along a memory bus. The increased output drive helps data transmission reliability. Figure 24 shows a schematic of this example.



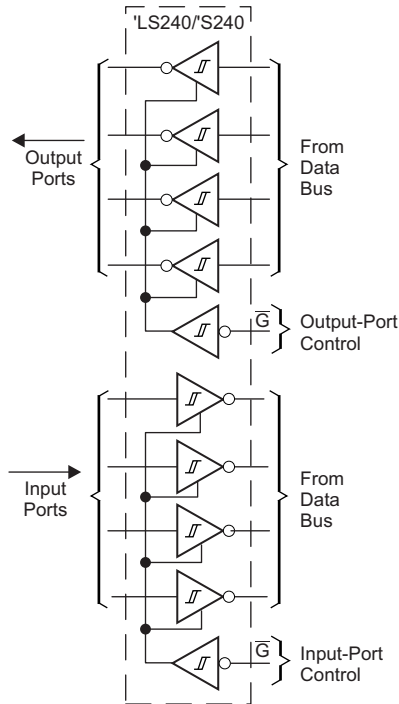
Copyright © 2016, Texas Instruments Incorporated

4-bit organization can be applied to handle binary or BCD

Figure 24. SNx4LS240 and SNx4S240 Used as System or Memory Bus Driver

The SNx4LS240 and SNx4S240 devices have two independently controlled 4-bit drivers, and can be used to buffer signals in a bidirectional manner along a data bus. Figure 25 shows the SNx4LS240 or SNx4S240 used in this manner.

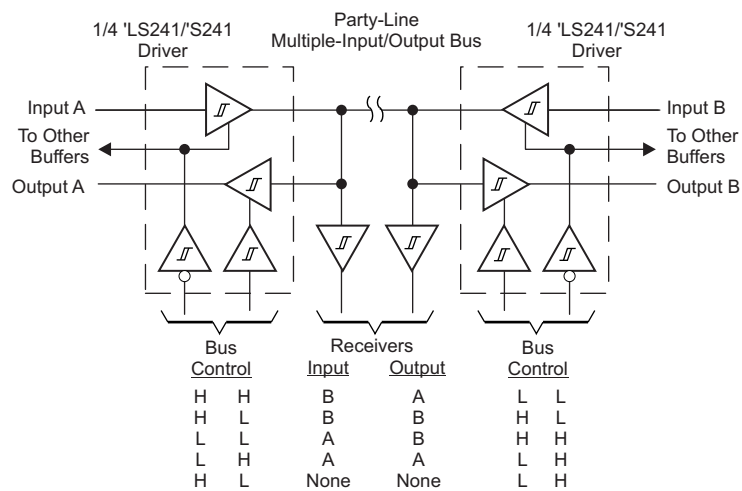
System Examples (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 25. Independent 4-Bit But Drivers/Receivers in a Single Package

The enable pins on the SNx4LS241 and SNx4S241 devices can be used to help direct signals along a shared party-line bus. Figure 26 shows a general configuration of how to implement this structure. Take care to ensure that bus contention does not occur.



Copyright © 2016, Texas Instruments Incorporated

Figure 26. Party-Line Bus System With Multiple Inputs, Outputs, and Receivers

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#). Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF bypass capacitor. If there are multiple V_{CC} pins, TI recommends a 0.01- μF or 0.022- μF bypass capacitors for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. Two bypass capacitors of value 0.1 μF and 1 μF are commonly used in parallel. For best results, install the bypass capacitor(s) as close to the power pin as possible.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not be left floating. In many applications, some channels of the SNx4LS24x, SNx4S24x are unused, and thus must be terminated properly. Because each transceiver channel pin can be either an input or an output, they must be treated as both when being terminated. Ground or V_{CC} (whichever is more convenient) can be used to terminate unused inputs; however, each unused channel should be terminated to the same logic level on both the A and Y side. For example, in [Figure 27](#) unused channels are terminated correctly with both sides connected to the same voltage, while channel 8 is terminated incorrectly with each side being tied to a different voltage. The \bar{G} input is also unused in this example, and is terminated directly to ground to permanently enable all outputs.

11.2 Layout Example

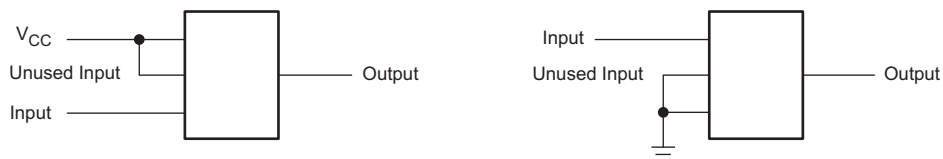


Figure 27. Example Demonstrating How to Terminate Unused Inputs and Channels of a Transceiver

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LS240 | Click here | Click here | Click here | Click here |
| SN74LS241 | Click here | Click here | Click here | Click here |
| SN74LS244 | Click here | Click here | Click here | Click here |
| SN54S240 | Click here | Click here | Click here | Click here |
| SN54S241 | Click here | Click here | Click here | Click here |
| SN54S244 | Click here | Click here | Click here | Click here |
| SN74LS240 | Click here | Click here | Click here | Click here |
| SN74LS241 | Click here | Click here | Click here | Click here |
| SN74LS244 | Click here | Click here | Click here | Click here |
| SN74S240 | Click here | Click here | Click here | Click here |
| SN74S241 | Click here | Click here | Click here | Click here |
| SN74S241 | Click here | Click here | Click here | Click here |

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-7801201VSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-7801201VS A SNV54LS240W | Samples |
| 7705701RA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7705701RA SNJ54LS244J | Samples |
| 7705701SA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7705701SA SNJ54LS244W | Samples |
| 78012012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 78012012A SNJ54LS 240FK | Samples |
| 7801201RA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7801201RA SNJ54LS240J | Samples |
| 7801201SA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7801201SA SNJ54LS240W | Samples |
| JM38510/32401B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32401B2A | Samples |
| JM38510/32401BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32401BRA | Samples |
| JM38510/32401BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32401BSA | Samples |
| JM38510/32402B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32402B2A | Samples |
| JM38510/32402BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32402BRA | Samples |
| JM38510/32402BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32402BSA | Samples |
| JM38510/32403B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403B2A | Samples |
| JM38510/32403BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403BRA | Samples |
| JM38510/32403BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403BSA | Samples |
| JM38510/32403SRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403SRA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/32403SSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403SSA | Samples |
| M38510/32401B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32401B2A | Samples |
| M38510/32401BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32401BRA | Samples |
| M38510/32401BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32401BSA | Samples |
| M38510/32402B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32402B2A | Samples |
| M38510/32402BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32402BRA | Samples |
| M38510/32402BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32402BSA | Samples |
| M38510/32403B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403B2A | Samples |
| M38510/32403BRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403BRA | Samples |
| M38510/32403BSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403BSA | Samples |
| M38510/32403SRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403SRA | Samples |
| M38510/32403SSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 32403SSA | Samples |
| SN54LS240J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS240J | Samples |
| SN54LS241J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS241J | Samples |
| SN54LS244J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS244J | Samples |
| SN54S240J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54S240J | Samples |
| SN54S241J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54S241J | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN54S244J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54S244J | Samples |
| SN74LS240DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | LS240 | Samples |
| SN74LS240DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS240 | Samples |
| SN74LS240DWG4 | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS240 | Samples |
| SN74LS240DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS240 | Samples |
| SN74LS240N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS240N | Samples |
| SN74LS240NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS240N | Samples |
| SN74LS240NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS240 | Samples |
| SN74LS241DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS241 | Samples |
| SN74LS241DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS241 | Samples |
| SN74LS241N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS241N | Samples |
| SN74LS241NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS241 | Samples |
| SN74LS244DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS244 | Samples |
| SN74LS244DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS244 | Samples |
| SN74LS244DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS244 | Samples |
| SN74LS244N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS244N | Samples |
| SN74LS244NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS244N | Samples |
| SN74LS244NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS244 | Samples |
| SN74LS244NSRG4 | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS244 | Samples |
| SN74S240DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S240 | Samples |
| SN74S240N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S240N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------------|-------------------------|
| SN74S240NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S240N | Samples |
| SN74S241DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S241 | Samples |
| SN74S241N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S241N | Samples |
| SN74S244DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S244 | Samples |
| SN74S244DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | S244 | Samples |
| SN74S244N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74S244N | Samples |
| SNJ54LS240FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 78012012A SNJ54LS 240FK | Samples |
| SNJ54LS240J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7801201RA SNJ54LS240J | Samples |
| SNJ54LS240W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7801201SA SNJ54LS240W | Samples |
| SNJ54LS241FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS 241FK | Samples |
| SNJ54LS241J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS241J | Samples |
| SNJ54LS241W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS241W | Samples |
| SNJ54LS244FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS 244FK | Samples |
| SNJ54LS244J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7705701RA SNJ54LS244J | Samples |
| SNJ54LS244W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7705701SA SNJ54LS244W | Samples |
| SNJ54S240FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S 240FK | Samples |
| SNJ54S240J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S240J | Samples |
| SNJ54S240W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S240W | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SNJ54S241FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S 241FK | Samples |
| SNJ54S241J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S241J | Samples |
| SNJ54S244J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S244J | Samples |
| SNJ54S244W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54S244W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS240, SN54LS240-SP, SN54LS241, SN54LS244, SN54LS244-SP, SN54S240, SN54S241, SN54S244, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 :

- Catalog : [SN74LS240](#), [SN54LS240](#), [SN74LS241](#), [SN74LS244](#), [SN54LS244](#), [SN74S240](#), [SN74S241](#), [SN74S244](#)
- Military : [SN54LS240](#), [SN54LS241](#), [SN54LS244](#), [SN54S240](#), [SN54S241](#), [SN54S244](#)
- Space : [SN54LS240-SP](#), [SN54LS244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

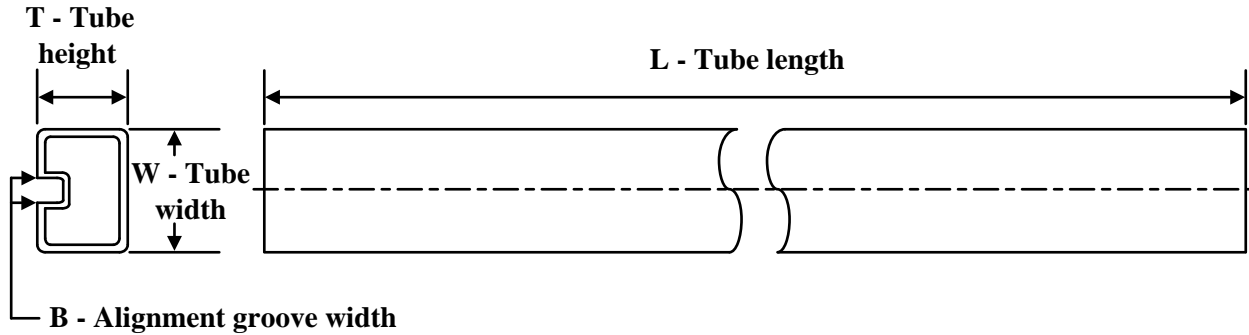

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS240DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS240DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS240NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS241DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS241NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LS244DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LS244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LS244NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74S244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS240DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS240DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS240NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS241DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS241NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS244DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LS244DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LS244NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74S244DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-7801201VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 7705701SA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| 78012012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 7801201SA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32401B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/32401BSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32402B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/32402BSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32403B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/32403BSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/32403SSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/32401B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/32401BSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/32402B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/32402BSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/32403B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/32403BSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| M38510/32403SSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74LS240DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LS240DWG4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LS240N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS240NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS241DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LS241N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS244DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LS244N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS244NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74S240DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74S240N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74S240NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74S241DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74S241N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74S244DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74S244N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54LS240FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS240W | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS241FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS241W | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SNJ54LS244FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS244W | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SNJ54S240FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54S241FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

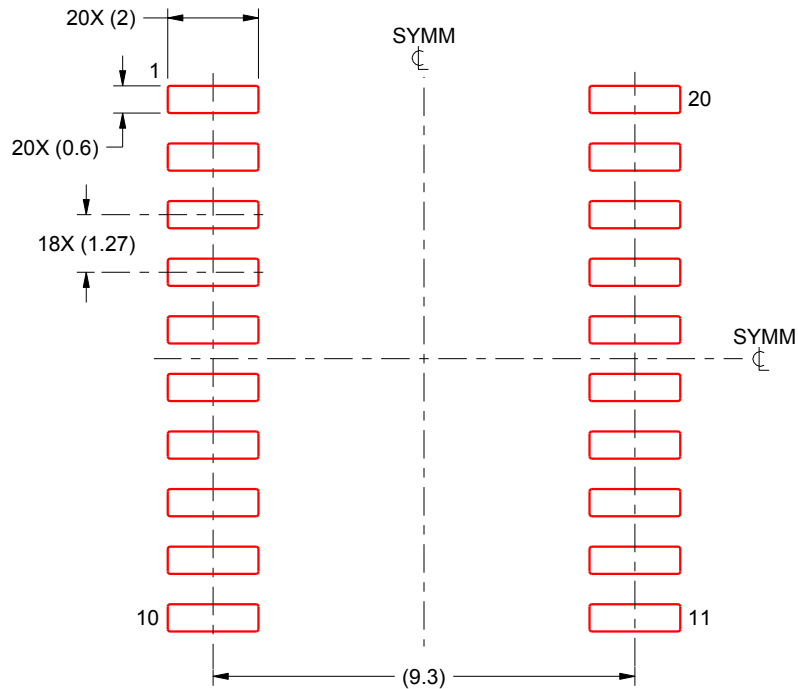
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

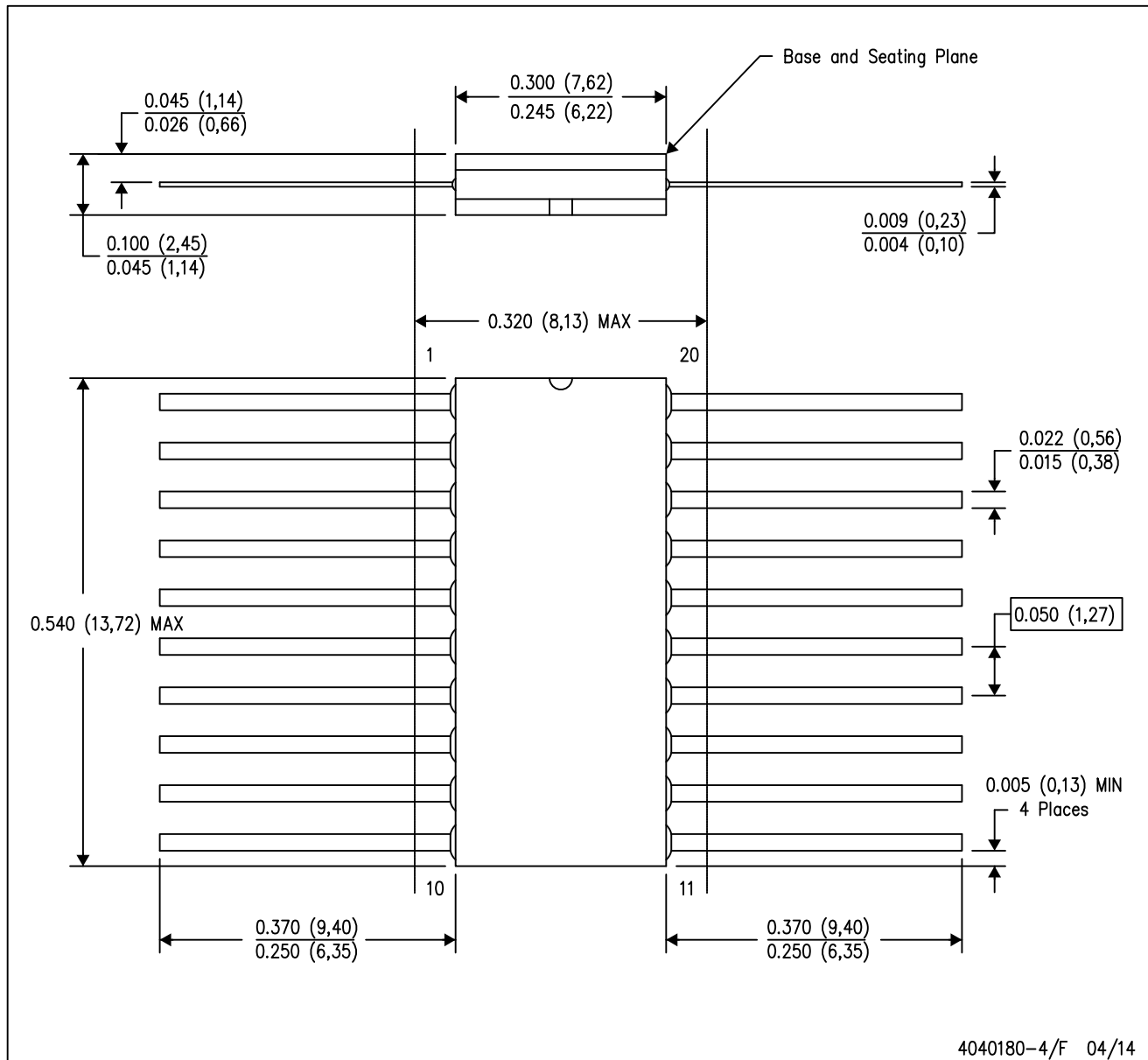
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

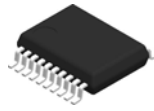
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

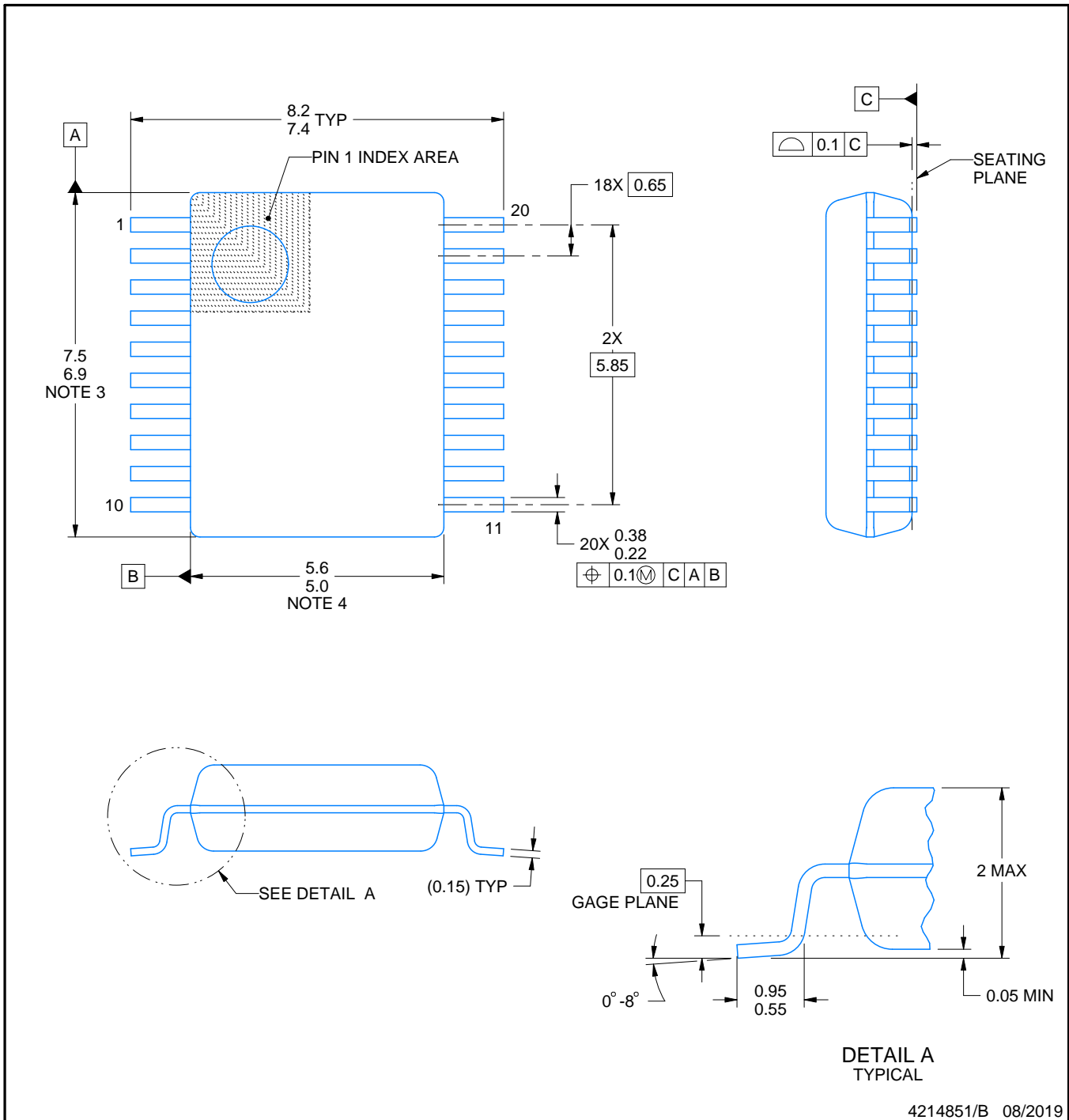
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

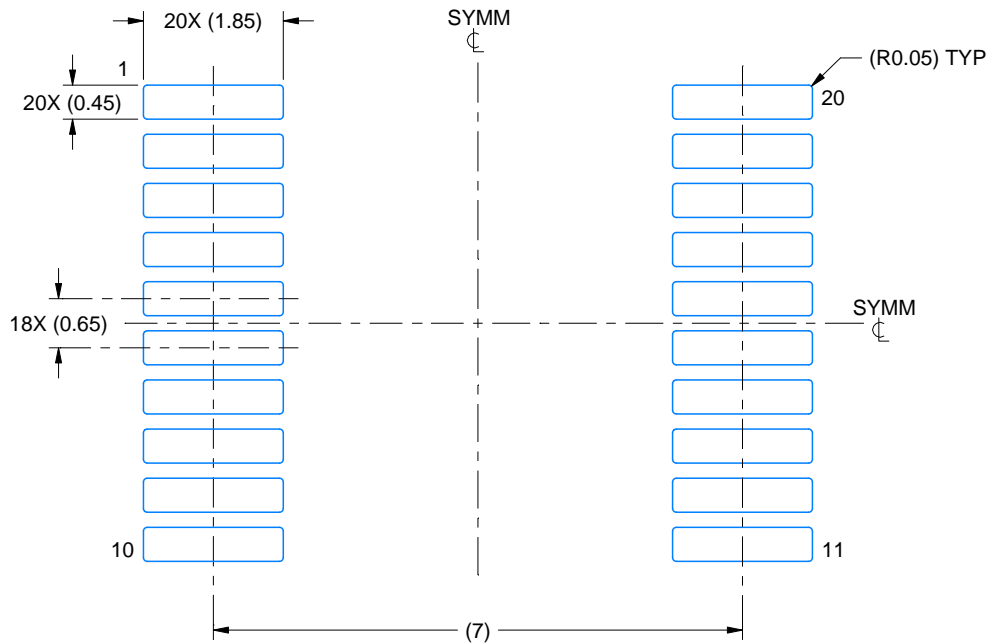
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

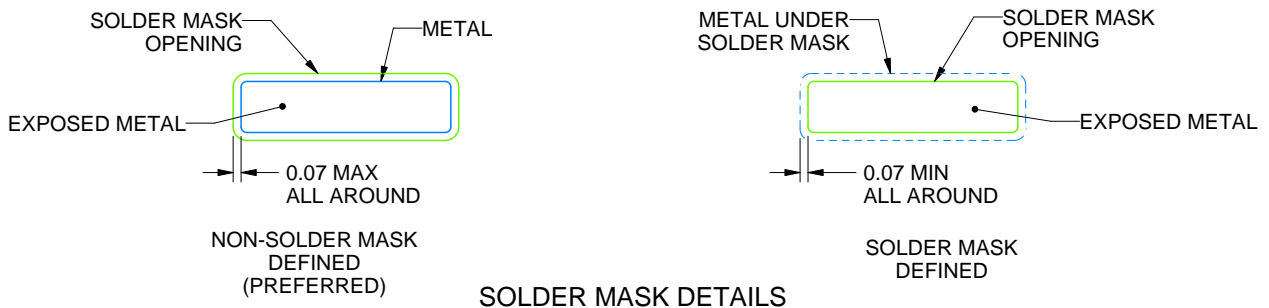
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

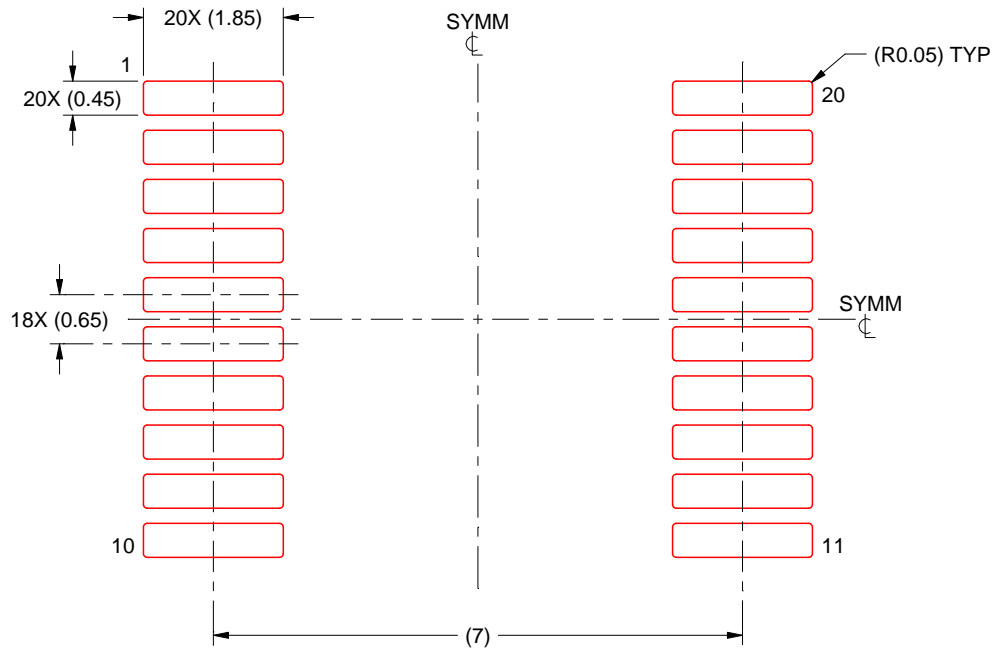
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated