Description

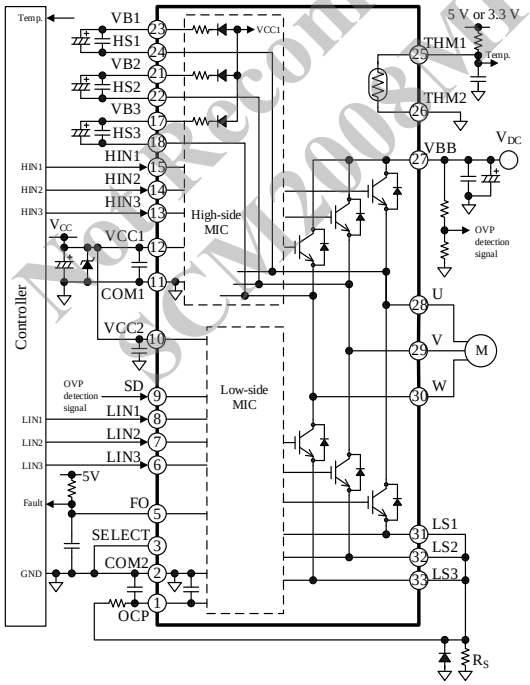
The SCM2000MKF series are 3-phase brushless motor drivers in which output transistors, pre-drive circuits, bootstrap diodes with current-limiting resistors, and a temperature-sensing thermistor are highly integrated.

These products can run on a 3-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards.

Features

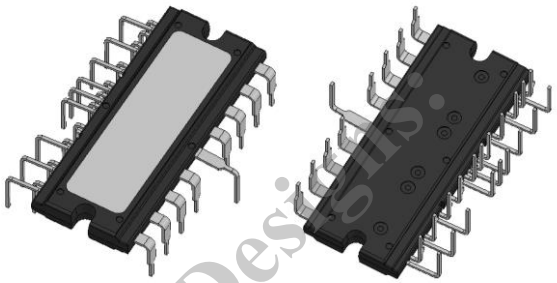
- Pb-free (RoHS Compliant)
- Isolation Voltage: 2500 V (for 1 min)
  (UL Recognition Pending)
- Built-in Thermistor
- Built-in Bootstrap Diodes
- CMOS-compatible Input (3.3 V or 5 V)
- Fault Signal Output at Protection Activation
- Shutdown Signal Input
- Selectable OCP Hold Time
  (SELECT Pin: 34 µs, 8 ms)
- Protections Include:
  Undervoltage Lockout for Power Supply
  VBx Pin (UVLO_VB): Auto-restart
  VCCx Pin (UVLO_VCCx): Auto-restart
  Overcurrent Protection (OCP): Auto-restart
  Overvoltage Protection (OVP): Auto-restart

Typical Application



Package

DIP33
Pin Pitch: 1.27 mm
Mold Dimensions: 47 mm × 19 mm × 4.4 mm



Not to scale

Selection Guide

- Power Device: IGBT + FRD (600 V)

Part Number	I_O
SCM2007MKF	20 A
SCM2008MKF	30 A

Applications

For motor drives such as:

- Refrigerator Compressor Motor
- Air Conditioner Compressor Motor
- Washing Machine Main Motor
- Fan Motor
- Pump Motor

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1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Main Supply Voltage (DC)	V_{DC}	VBB–LSx	450	V	
Main Supply Voltage (Surge)	$V_{DC(SURGE)}$	VBB–LSx	500	V	
IGBT Breakdown Voltage	V_{CES}	V_{CC} = 15 Vm, I_C = 1 mA, V_{IN} = 0 V	600	V	
Logic Supply Voltage	V_{CC}	VCCx–COM	20	V	
	V_{BS}	VBx–HSx	20	V	
Output Current[1]	I_O	T_C = 25 °C, T_J < 150 °C	20	A	SCM2007MKF
			30		SCM2008MKF
Output Current (Pulse)	I_{OP}	T_C = 25 °C, pulse width ≤ 1 ms, single pulse	40	A	SCM2007MKF
			60		SCM2008MKF
Input Voltage	V_{IN}	HINx–COM, LINx–COM	−0.5 to 7	V	
FO Pin Voltage	V_{FO}	FO–COM	−0.5 to 7	V	
SELECT Pin Voltage	V_{SEL}	SELECT–COM	−0.5 to 7	V	
SD Pin Voltage	V_{SD}	SD–COM	−0.5 to 7	V	
OCP Pin Voltage	V_{OCP}	OCP–COM	−10 to 7	V	
Operating Case Temperature[2]	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature[3]	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	
Isolation Voltage[4]	$V_{ISO(RMS)}$	Between surface of heatsink side and each pin; AC, 60 Hz, 1 min	2500	V	

[1] Should be derated depending on an actual case temperature. See Section 15.4.
[2] Refers to a case temperature measured during IC operation.
[3] Refers to the junction temperature of each chip built in the IC, including the control MICs, transistors, and freewheeling diodes.
[4] Refers to voltage conditions to be applied between all of the pins and the case. All the pins have to be shorted.

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2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–LSx	—	300	400	V	
Logic Supply Voltage	V_{CC}	VCCx–COM	13.5	—	16.5	V	
	V_{BS}	VB1–U, VB2–V, VB3–W	13.5	—	16.5	V	
Input Voltage (HINx, LINx, FO, SELECT, SD)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	µs	
	$t_{IN(MIN)OFF}$		0.5	—	—	µs	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	µs	
FO Pin Pull-up Resistor	R_{FO}		1	—	22	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF	
SELECT Pin Pull-up Resistor	R_{SEL}		1	—	22	kΩ	
SELECT Pin Pull-up Voltage	V_{SEL}		3.0	—	5.5	V	
SELECT Pin Noise Filter Capacitor	C_{SEL}		0.001	—	0.01	µF	
SD Pin Pull-up Resistor	R_{SD_U}	VBB = 500 V(1)	465.3	470.0	474.3	kΩ	
SD Pin Pull-donw Resistor	R_{SD_D}		1.782	1.800	1.818	kΩ	
THM Pin Pull-up Resistor	R_{THM}		4.4	—	—	kΩ	
THM Pin Noise Filter Capacitor	C_{THM}		0.1	—	—	µF	
Bootstrap Capacitor	C_{BOOT}		10	—	220	µF	
Shunt Resistor(2)	R_S	$I_{OP} \leq 40$ A	13.5	—	—	mΩ	SCM2007MKF
		$I_{OP} \leq 60$ A	9	—	—		SCM2008MKF
RC Filter Resistor(3)	R_O		—	100	—	Ω	
RC Filter Capacitor(2)	C_O		—	0.01	—	µF	
PWM Carrier Frequency	f_C		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

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(1) Refers to the application where overvoltage detection takes place when the VBB pin voltage is 500 V.
(2) Should be a low-inductance resistor.
(3) Requires the time constants that satisfy the following equation (see also Section 12.3.4): $R_O \times C_O < 1.0$ µs .

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3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM.

3.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.		Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCCx–COM	9.5	10.5	11.5	V	
	$V_{BS(ON)}$	VBx–HSx	9.5	10.5	11.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCCx–COM	9	10	11	V	
	$V_{BS(OFF)}$	VBx–HSx	9	10	11	V	
Logic Supply Current	I_{CC}	VCC1 = VCC2	—	2.85	—	mA	Total sink current of the VCC1 and VCC2 pins
	I_{BS}	VBx–HSx = 15 V, HINx = 5 V; VBx pin current in 1-phase operation	—	140	—	µA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, FO, SELECT)	V_{IH}		1.5	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx, FO, SELECT)	V_{IL}		1.0	1.5	2.0	V	
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	µA	
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	µA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	—	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V	
Protection							
OCP Threshold Voltage	V_{TRIP}		0.475	0.500	0.525	V	
OCP Hold Time 1	t_{P1}	V_{SELECT} = 5 V	20	34	—	µs	
OCP Hold Time 2	t_{P2}	V_{SELECT} = 0 V	5	8	—	ms	
OCP Blanking Time	t_{BK}	V_{TRIP} = 1 V	—	0.5	—	µs	
SD Pin OVP Operating Voltage	V_{SDH}		1.86	1.90	1.94	V	
SD Pin OVP Release Voltage	V_{SDL}		—	1.78	—	V	
SD Pin Input Current	I_{SD}	V_{SD} = 5 V	—	16.6	36.0	µA	
SD Pin Filtering Time	t_{SD}		—	2.0	—	µs	
OVP Hold Time	t_{P_SD}		20	31	—	µs	

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3.2. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 600 V	—	—	10	μA	
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	3.0	—	V	

3.3. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance[1]	$R_{(J-C)Q}$[2]	1 element operating (IGBT)	—	—	3		SCM2007MKF SCM2008MKF
	$R_{(J-C)F}$[3]	1 element operating (freewheeling diode)	—	—	4		SCM2007MKF SCM2008MKF

(1) Refers to a case temperature at the measurement point described in Figure 3-1, below.
(2) Refers to steady-state thermal resistance between the junction of the built-in transistors and the case. For transient thermal characteristics, see Section 15.1.
(3) Refers to steady-state thermal resistance between the junction of the built-in freewheeling diodes and the case.

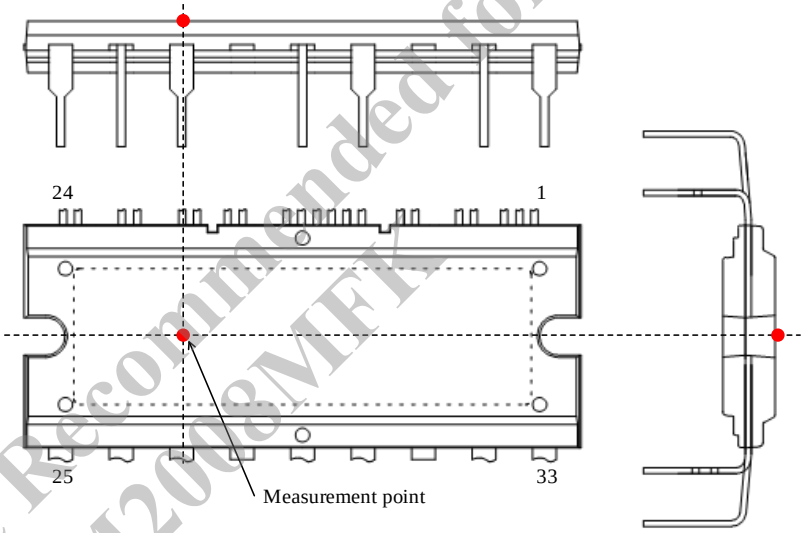

Figure 3-1. Case Temperature Measurement Point

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3.4. Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

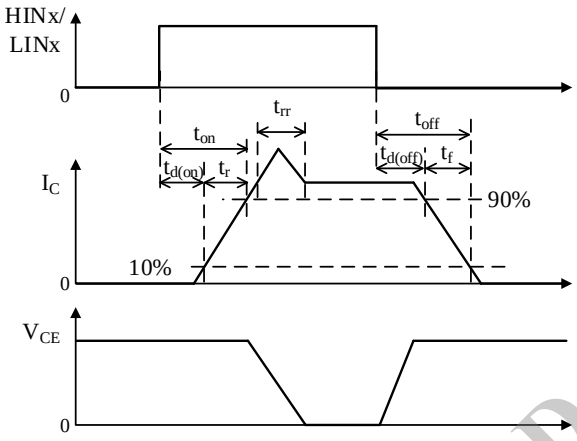

Figure 3-2. Switching Characteristics Definitions

3.4.1. SCM2007MKF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 20 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 20 A, V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	75	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	900	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	840		ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 20 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	85	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	900	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	840		ns
Fall Time	t_f		—	90	—	ns

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3.4.2. SCM2008MKF

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Collector-to-Emitter Leakage Current	I_{CES}	V_{CE} = 600 V, V_{IN} = 0 V	—	—	1	mA
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 A, V_{IN} = 5 V	—	1.7	2.2	V
Diode Forward Voltage	V_F	I_F = 30 A, V_{IN} = 0 V	—	1.9	2.4	V
High-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	65	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	960	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	950		ns
Fall Time	t_f		—	90	—	ns
Low-side Switching						
Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_C = 30 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	75	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	960	—	ns
Rise Time	t_r		—	150	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	960		ns
Fall Time	t_f		—	90	—	ns

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4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Heatsink Mounting Screw Torque	*	0.588	—	0.784	N·m	
Flatness of Heatsink Attachment Area	See Figure 4-1.	0	—	100	μm	
Package Weight		—	7.6	—	g	

* Requires using a metric screw of M3 and a plain washer of 7.0 mm (φ). For more on screw tightening, see Section 13.2.

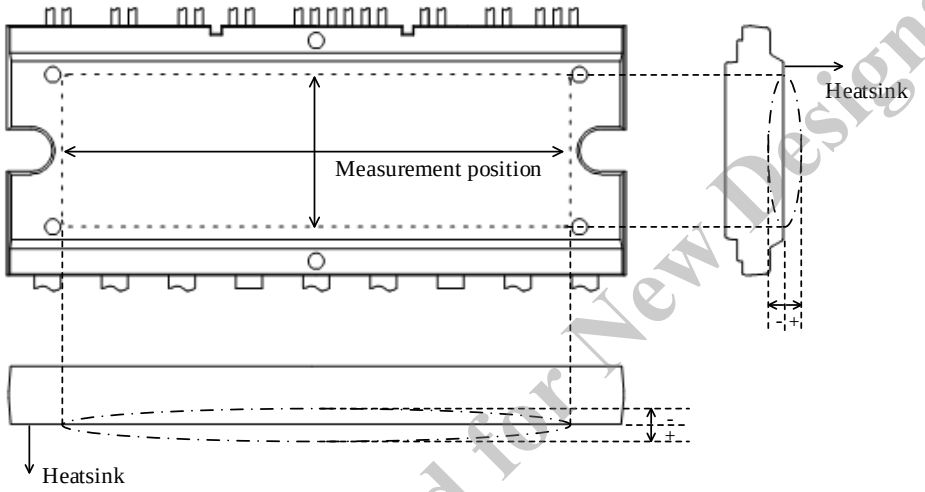

Figure 4-1. Flatness Measurement Position

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5. Insulation Distance

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Clearance	Between heatsink* and leads. See Figure 5-1.	2.0	—	2.5	mm	
Creepage		3.86	—	4.26	mm	

* Refers to when a heatsink to be mounted is flat. If your application requires a clearance exceeding the maximum distance given above, use an alternative (e.g., a convex heatsink) that will meet the target requirement.

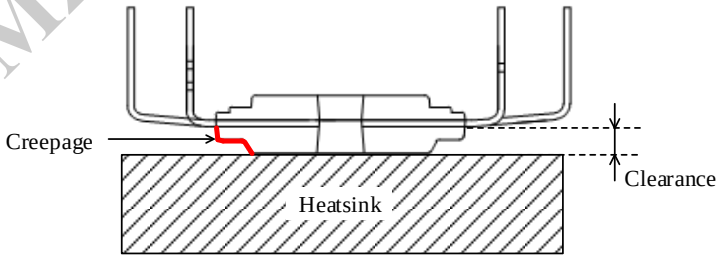

Figure 5-1. Insulation Distance Definitions

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6. Truth Table

Table 6-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx pin signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state). Therefore, HINx and LINx signals, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state events can be avoided.

After the IC recovers from a UVLO_VCCx condition, the high- and low-side transistors resume switching, according to the input logic levels of the HINx and LINx signals (level-triggered).

After the IC recovers from a UVLO_VB condition, the high-de transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

Table 6-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
External Shutdown Signal Input FO = L	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
VBx Pin Undervoltage Lockout (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
VCC1 Pin Undervoltage Lockout (UVLO_VCC1)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
VCC2 Pin Undervoltage Lockout (UVLO_VCC2)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overvoltage Protection (OVP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

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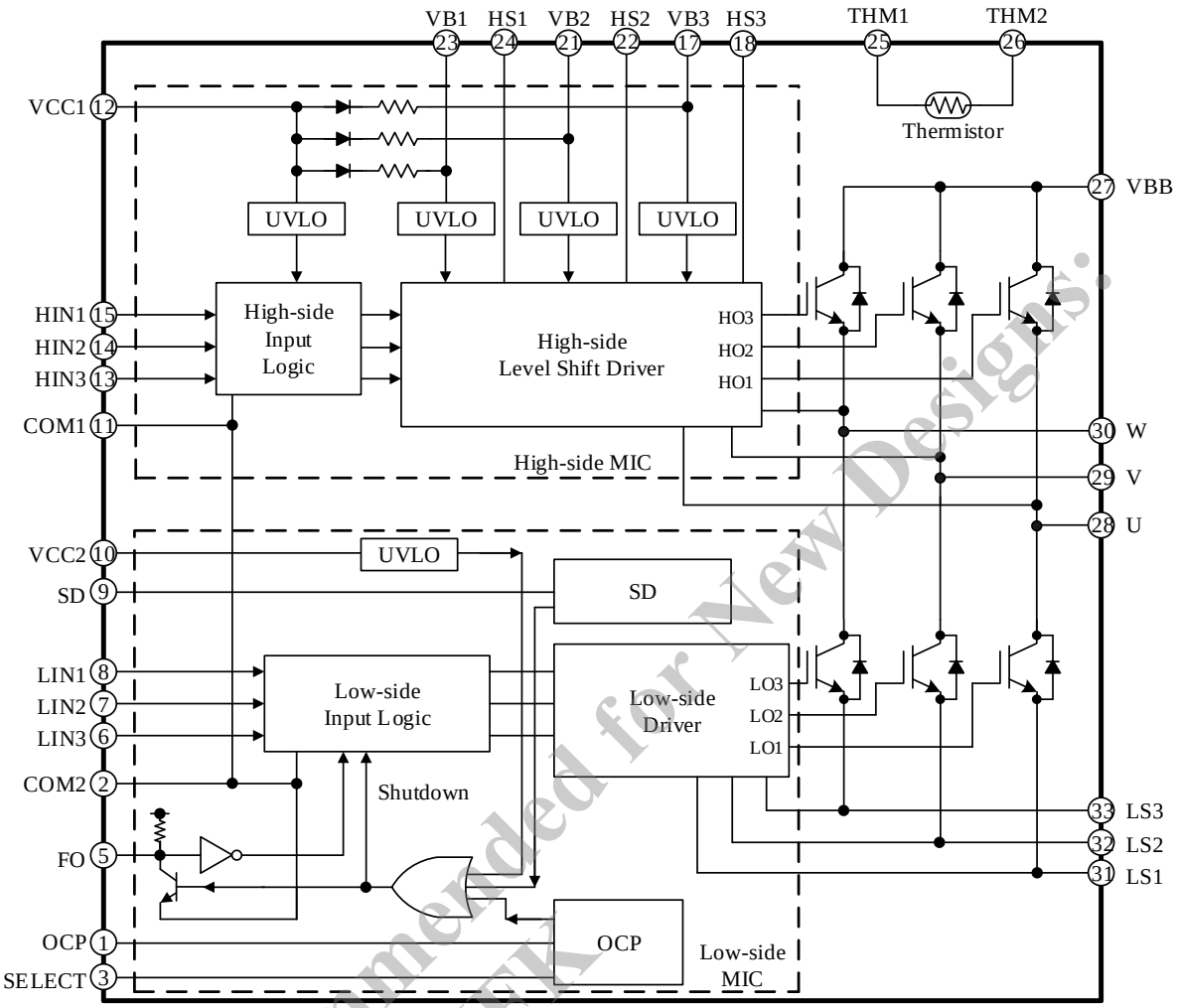
7. Block Diagram



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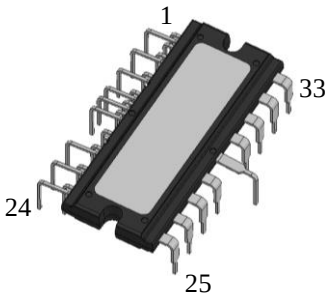
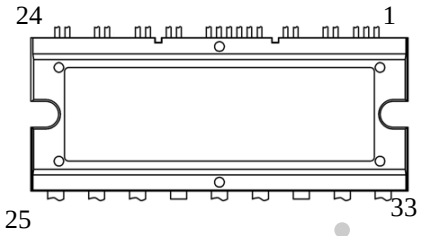
8. Pin Configuration Definitions



Top View



Pin Number	Pin Name	Description
1	OCP	Overcurrent protection signal input
2	COM2	Logic ground 2
3	SELECT	OCP hold time setting
4	—	(Pin removed)
5	FO	Fault signal output and shutdown signal input
6	LIN3	Logic input for W-phase low-side gate driver
7	LIN2	Logic input for V-phase low-side gate driver
8	LIN1	Logic input for U-phase low-side gate driver
9	SD	Overvoltage protection signal input
10	VCC2	Low-side logic supply voltage input
11	COM1	Logic ground 1
12	VCC1	High-side logic supply voltage input
13	HIN3	Logic input for W-phase high-side gate driver
14	HIN2	Logic input for V-phase high-side gate driver
15	HIN1	Logic input for U-phase high-side gate driver
16	COM1	(Pin trimmed) logic ground 1
17	VB3	W-phase high-side floating supply voltage input
18	HS3	W-phase high-side floating supply ground
19	—	(Pin removed)
20	—	(Pin removed)
21	VB2	V-phase high-side floating supply voltage input
22	HS2	V-phase high-side floating supply ground
23	VB1	U-phase high-side floating supply voltage input
24	HS1	U-phase high-side floating supply ground
25	THM1	Thermistor output 1
26	THM2	Thermistor output 2
27	VBB	Positive DC bus supply voltage
28	U	U-phase output
29	V	V-phase output
30	W	W-phase output
31	LS1	U-phase IGBT emitter
32	LS2	V-phase IGBT emitter
33	LS3	W-phase IGBT emitter

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9. Typical Applications

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

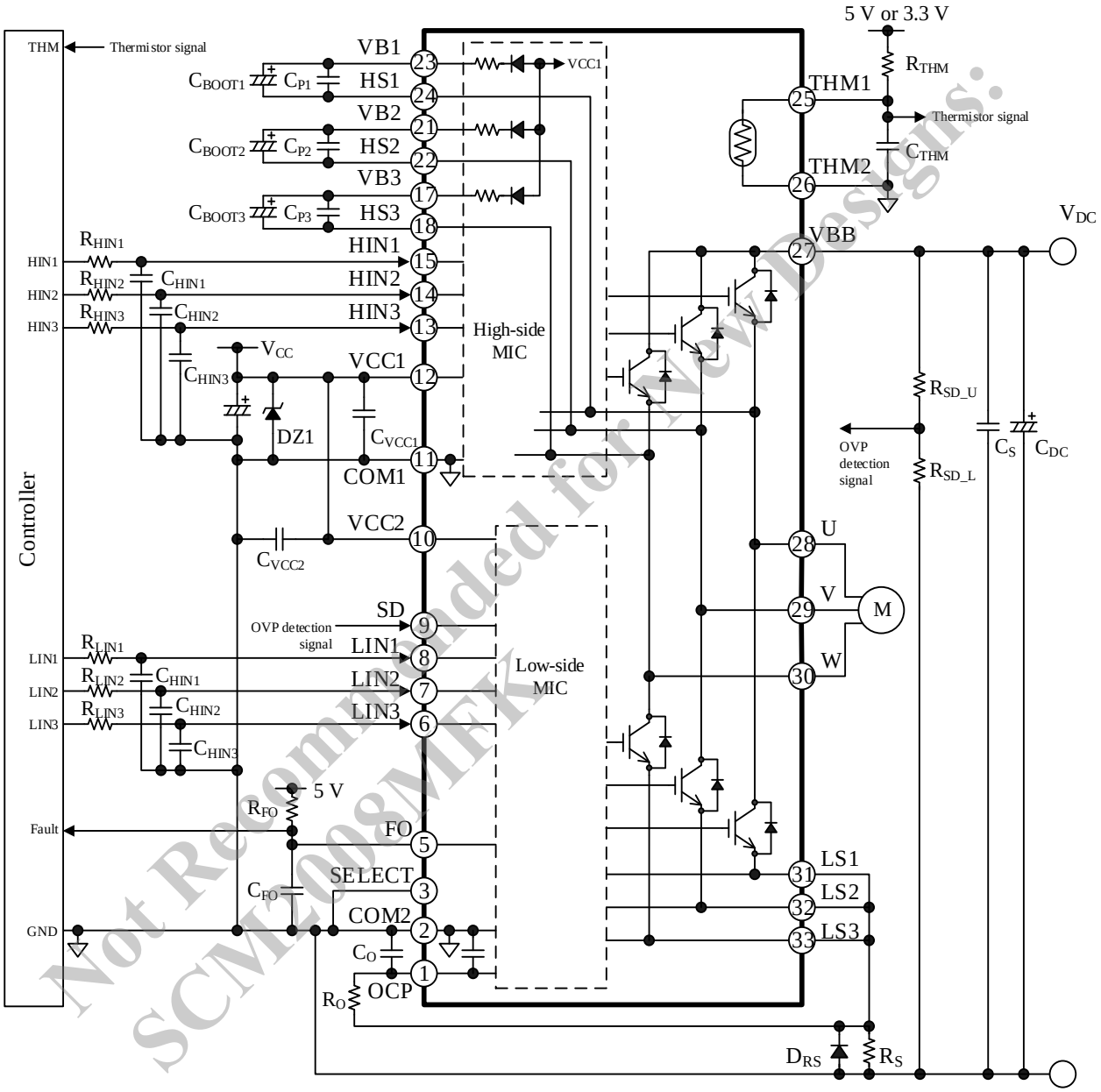

Figure 9-1. Typical Application (OCP Hold Time: 8 ms)

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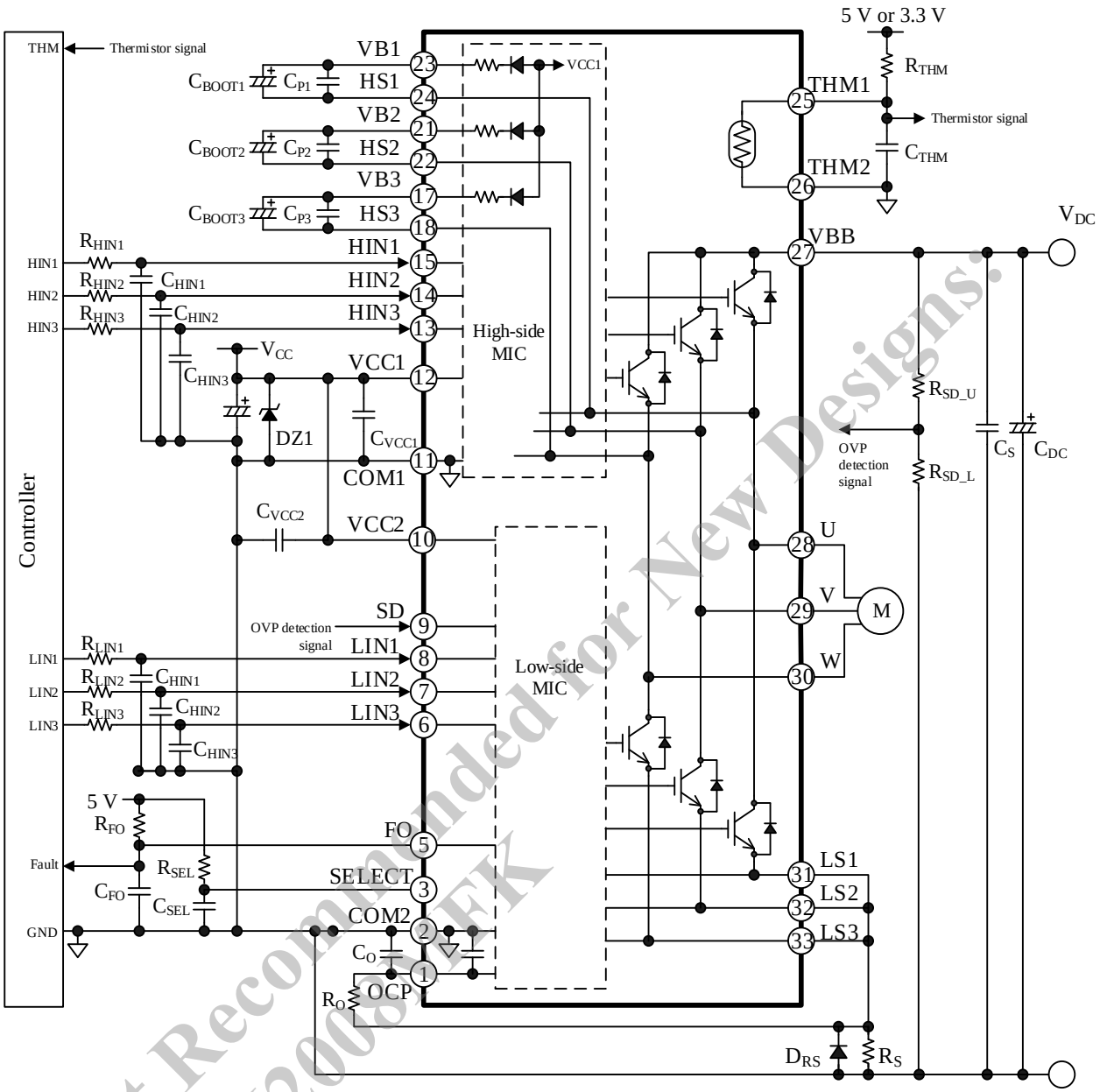

Figure 9-2. Typical Application (OCP Hold Time: 34 µs)

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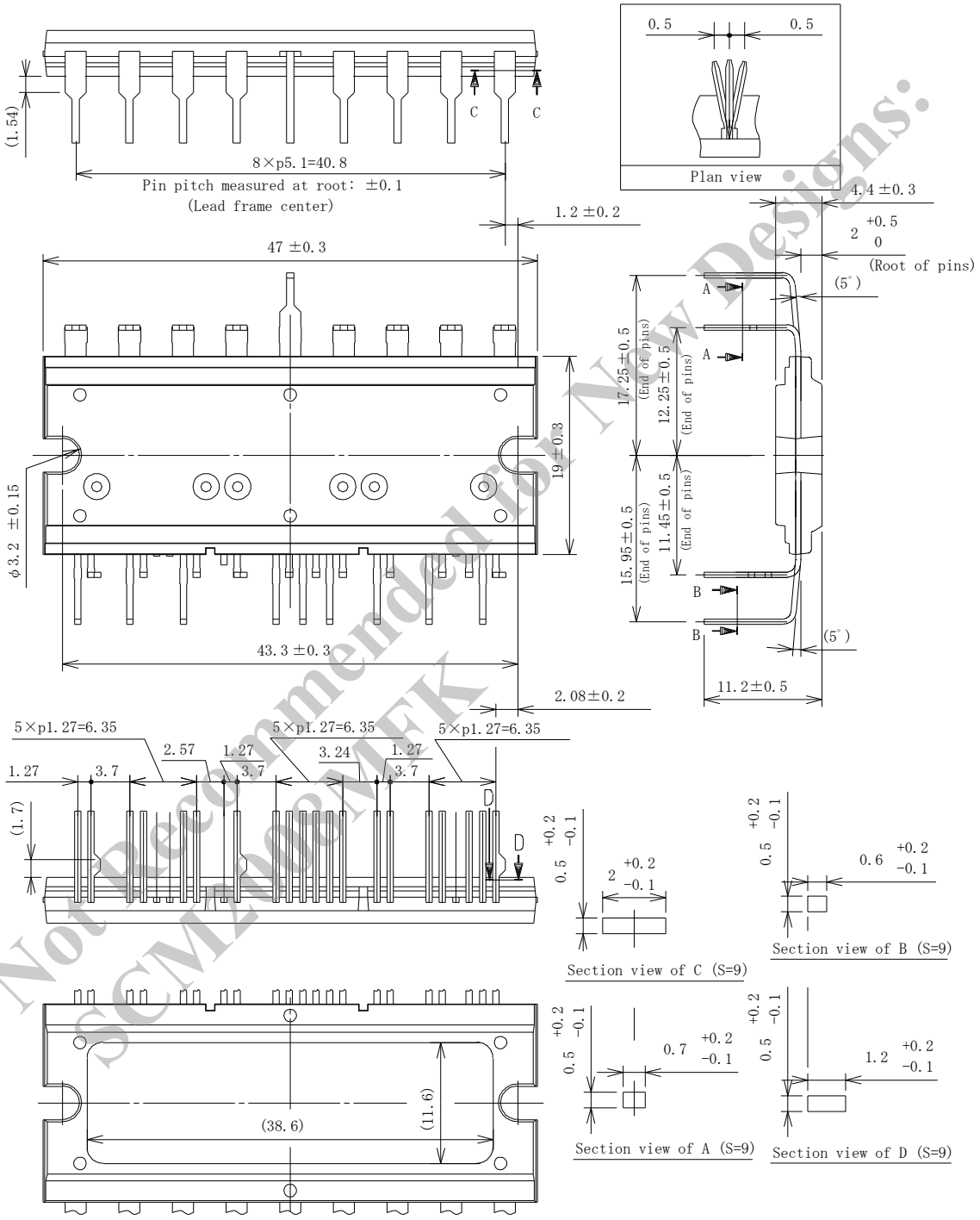
10. Physical Dimensions

10.1. DIP33

● **Leadform 2563**



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NOTES:

- Dimensions in millimeters
- Pb-free (RoHS compliant)

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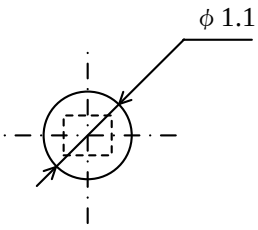
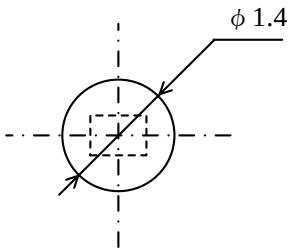
10.2. Reference PCB Hole Sizes

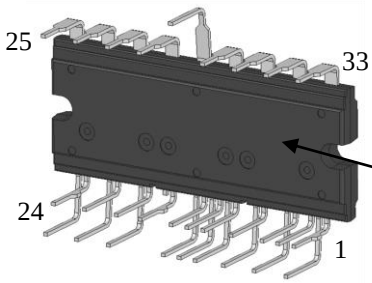


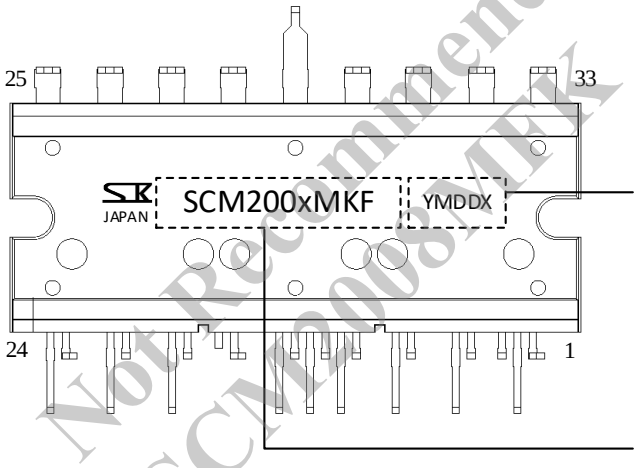
Pins 1 to 24



Pins 25 to 33

11. Marking Diagram





Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
X is the control number

Part Number

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12. Functional Descriptions

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. The COM1 and COM2 pins must be externally connected on a PCB; an electric potential across the two pins that are shorted is represented as "COM".

For pin descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. The U-, V-, and W-phases are represented as the pin numbers 1, 2, and 3, respectively. Thus, "the VBx pin" is used when referring to either of the VB1, VB2, or VB3 pin. Also, when different pin names are mentioned as a pair (e.g., "the VBx and HSx pins"), they are meant to be the pins in the same phase.

12.1. Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBB, HINx, and LINx pins until the logic power supply, VCC, has reached a stable state ($V_{CC(ON)} \geq 11.5$ V).

It is required to fully charge bootstrap capacitors, C_{BOOTx}, at startup (see Section 12.2.3).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

12.2. Pin Descriptions

12.2.1. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the IGBT collectors of the high-side are connected to this pin. Voltages between the VBB pin and the ground (COM) should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

12.2.2. U, V, and W

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The U, V, and W pins are internally connected to the HS1, HS2, and HS3 pins, respectively.

12.2.3. VB1, VB2, and VB3

These are the inputs of the high-side floating power supplies for the individual phases.

Voltages across the VBx and HSx pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

In each phase, a bootstrap capacitor, C_{BOOTx}, should be connected between the VBx and HSx pins. For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor, C_{BOOTx}. For the capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{BOOTx}.

$$C_{BOOT}\ (\mu F) > 800 \times t_{L(OFF)}\ (s) \quad (1)$$

$$10\ \mu F \leq C_{BOOT} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Even while the high-side transistor is off, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the VBx pin undervoltage lockout (UVLO_VB) starts operating (see Section 12.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 12-1 shows, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are internally placed in series between the VCCx and VBx pins.

When turning on the IC, be sure to turn on the low-side transistor first, then fully charge the bootstrap capacitor, C_{BOOTx}. Table 12-1 provides reference charging times according to C_{BOOTx} capacities.

Table 12-1. C_{BOOTx} Charging Time (Reference)

C_{BOOTx} Capacitance (µF)	Charging Time, Duty = 100% (s)
10	0.5
22	0.5
47	0.5
100	1.0
220	1.0

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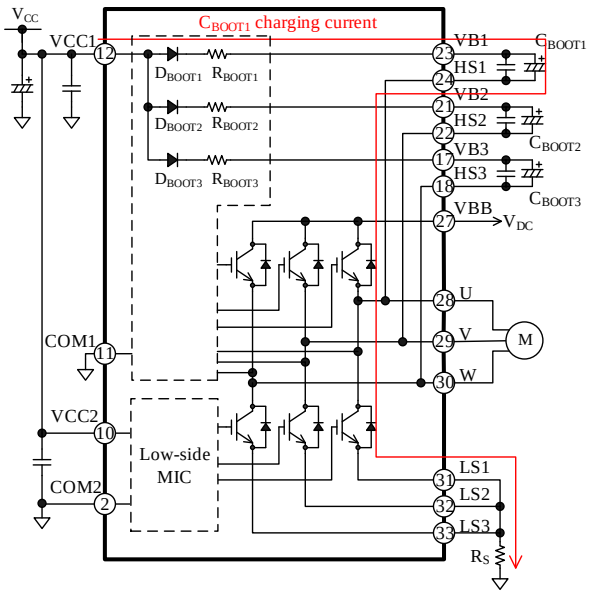

Figure 12-1. Bootstrap Circuit

Figure 12-2 shows an internal level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input signal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

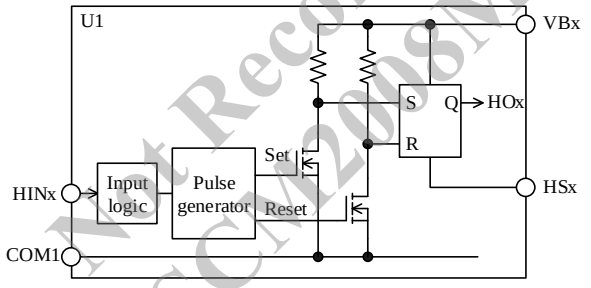

Figure 12-2. Internal Level-shifting Circuit

Figure 12-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and HSx pins ("VBx–HSx") occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HOx signal stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high (i.e., the high-side transistor is in an on-state), the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC and be connected between the VBx and HSx pins with a minimal length of traces.

If C_{BOOTx} requires an electrolytic capacitor, connect a 0.01 µF to 0.1 µF bypass capacitor, C_{Px}, parallelly to C_{BOOTx}. Then, place the bypass capacitor, C_{Px}, as close as possible to the VBx and HSx pins.

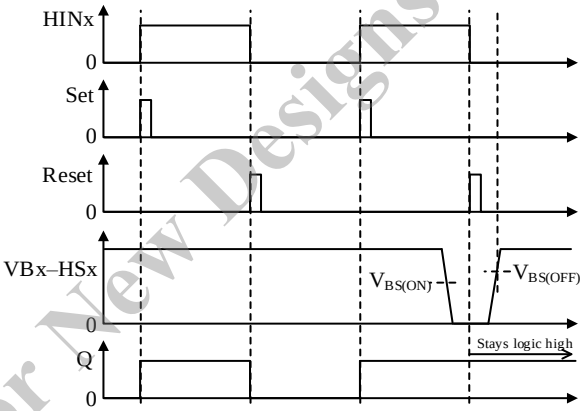

Figure 12-3. Waveforms at VBx–HSx Voltage Drop

12.2.4. HS1, HS2, and HS3

These pins are the grounds of the high-side floating power supplies for each phase, and are connected to the negative nodes of bootstrap capacitors, C_{BOOTx}. The HS1, HS2, and HS3 pins are internally connected to the U, V, and W pins, respectively.

12.2.5. LS1, LS2, and LS3

These are the emitter pins of the low-side IGBTs. For current detection, the LS1, LS2, and LS3 pins should be externally connected to a shunt resistor, R_S.

When connecting a shunt resistor, use a resistor with low inductance (required), and place it as near as possible to the IC with a minimum length of traces to the LSx and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LSx pin and the ground (COM) in order to prevent the IC from malfunctioning.

12.2.6. VCC1 and VCC2

These are the logic supply pins for the built-in control

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ICs. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCCx}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

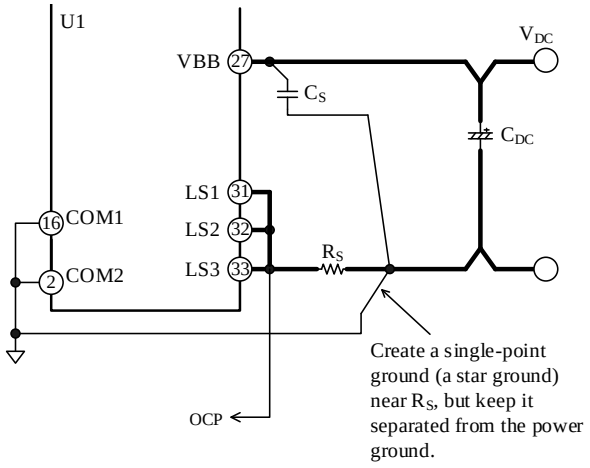

Figure 12-4. Connections to Logic Ground

12.2.7. HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller. Figure 12-5 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 22 kΩ pull-down resistor, and its input logic is active high.

Input signals across the HINx–COM and the LINx–COM in each phase should be set within the ranges provided in Table 12-2, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid such malfunctions, set the microcontroller output line not to have high-impedance outputs.

Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 12-6).

Here are filter circuit constants for reference:

- R_{IN1x}: 33 Ω to 500 Ω
- R_{IN2x}: 5 kΩ to 10 kΩ
- C_{INx}: 100 pF to 200 pF

Care should be taken in adding R_{IN1x} and R_{IN2x} to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 12-2. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.5 µs	

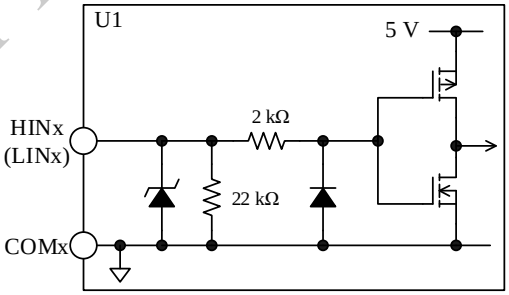

Figure 12-5. Internal Circuit Diagram of HINx or LINx Pin

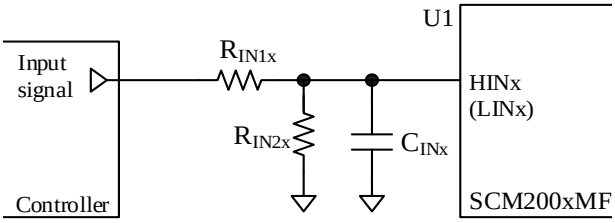

Figure 12-6. Filter Circuit for HINx or LINx Pin

12.2.8. OCP

This pin serves as the input of the overcurrent protection (OCP) for monitoring the currents going through the output transistors. Section 12.3.4 provides further information about the OCP circuit configuration and its mechanism.

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12.2.9. SELECT

The SCM2000MKF series is designed to select an OCP hold time, t_P, from 34 µm or 8 ms, based on the SELECT pin connection. (For more details on the OCP, see Section 12.3.4.)

When connecting the SELECT pin to the ground (COM) as in Figure 9-1, select an OCP hold time of 8 ms. When pulling up the SELECT pin to the external power supply (3.0 V to 5.5 V) as in Figure 9-2, select an OCP hold time of 34 µs. A pull-up resistor, R_{SEL}, and a noise filter capacitor, C_{SEL}, should be maintained within the recommended range given in Section 2.

12.2.10. SD

The SD pin serves as the input for the overvoltage protection which monitors voltages across the VBB and LSx pins. Section 12.3.5 provides details on the SD pin peripheral circuit and the OVP operation.

12.2.11. FO

This pin operates as the fault signal output and the shutdown signal input. Sections 12.3.1 and 12.3.2 explain the two functions in detail, respectively.

Figure 12-7 illustrates an internal circuit diagram of the FO pin and its peripheral circuit. Because of its open-drain nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage, V_{FO}) should range from 3.0 V to 5.5 V. Figure 12-9 shows a relation between the FO pin voltage and the pull-up resistor, R_{FO}. When the pull-up resistor, R_{FO}, has a too small resistance, the FO pin voltage at fault signal output becomes high due to the on-resistance of a built-in MOSFET, Q_{FO} (Figure 12-7). Therefore, it is recommended to use a 1 kΩ to 22 kΩ pull-up resistor when the Low Level Input Threshold Voltage of the microcontroller, V_{IL}, is set to 1.0 V. To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COMx pins.

Note that, however, this additional filtering allows a delay time, $t_{D(FO)}$, to occur, as seen in Figure 12-8. The delay time, $t_{D(FO)}$, is a period of time which starts when the IC receives a fault flag turning on the internal MOSFET, Q_{FO}, and continues until when the FO pin reaches its threshold voltage (V_{IL}) of 1.0 V or below (put simply, until the time when the IC detects a low state, "L"). Figure 12-10 shows how the delay time, $t_{D(FO)}$, and the noise filter capacitor, C_{FO}, are related.

When V_{IL} is set to 1.0 V, it is recommended to use a 0.001 µF to 0.01 µF noise filter capacitor, C_{FO}, allowing a sufficient margin to deal with variations in characteristics. For avoiding repeated OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, after the internal MOSFET (Q_{FO}) turn-on. t_P is 20 µs where the thermal characteristics (SELECT = logic high) are taken into account. (For more details, see Section 12.3.4.) To resume the motor operation thereafter, set the motor to be resumed after a lapse of ≥2 seconds.

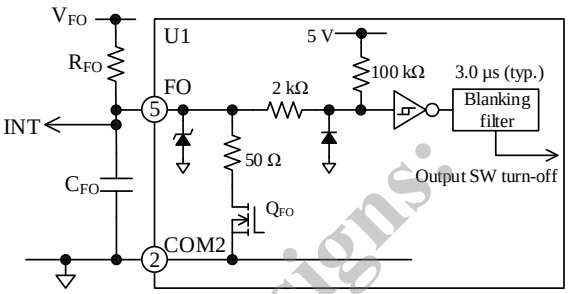

Figure 12-7. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

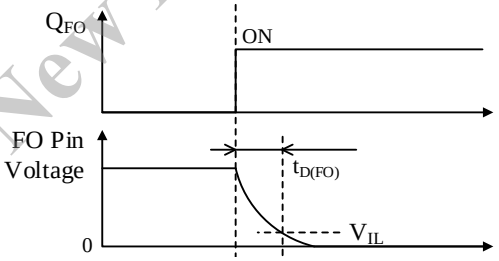

Figure 12-8. FO Pin Delay Time, $t_{D(FO)}$

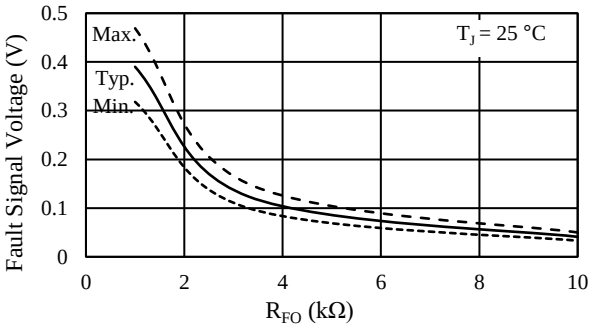

Figure 12-9. Fault Signal Voltage vs. Pull-up Resistor, R_{FO}

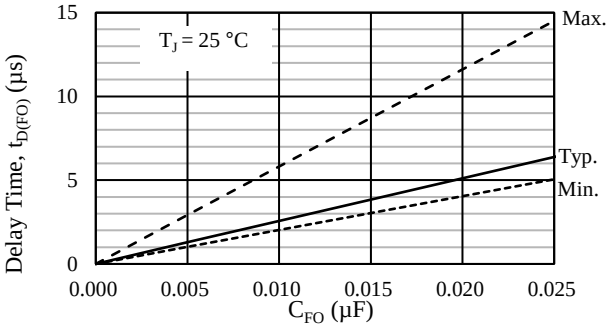

Figure 12-10. Delay Time, $t_{D(FO)}$ vs. Filter Capacitor, C_{FO}

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12.2.12. THM1 and THM2

The SCM2000MKF series incorporates a thermistor which monitors the case temperatures of the IC. The both ends of the internal thermistor are connected to the THM1 and THM2 pins, respectively.

Thermistor connections depend on which type of output characteristics to use: positive temperature coefficient or negative temperature coefficient. When building a positive temperature coefficient circuit, connect it as shown in Figure 12-11.

When building a negative temperature coefficient circuit, connect the THM1 pin to the external power supply and a resistor, R_{THM}, as shown in Figure 12-12.

In addition, connect a noise filter capacitor, C_{THM}, to the THMx pin which is connected to the external microcontroller.

The external power supply voltage, V_{THM}, should range from 3.0 V to 5.5 V. Use R_{THM} with a resistance of ≥4.4 kΩ, and C_{THM} with a capacitance of ≥0.1 nF. Then, place C_{THM} as close as possible to the IC, and connect it to the THMx pin connected to the microcontroller and the ground (COM) with minimizing respective trace lengths.

Figure 12-13 depicts a typical thermistor resistance vs. temperature curve; Figure 12-14 plots a typical performance curve of the THM1 pin.

The SCM2000MKF series does not have any protection against overtemperature; therefore, the motor must be externally controlled when a temperature rise occurs, or be controlled with such protective measures. Moreover, note that the thermistor output does not provide the temperature followability, especially when a rapid temperature rise in the output transistors occurs during motor lock and short circuit conditions.

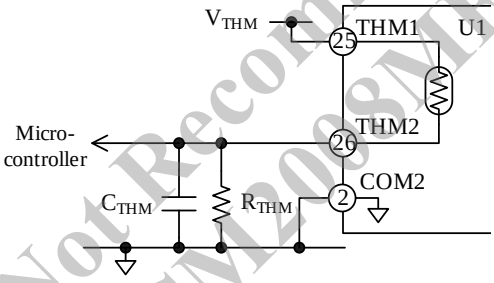

Figure 12-11. Circuit Using a Positive Temperature Coefficient

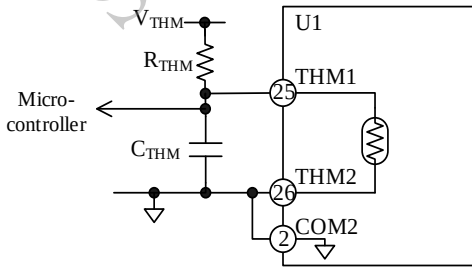

Figure 12-12. Circuit Using a Negative Temperature Coefficient

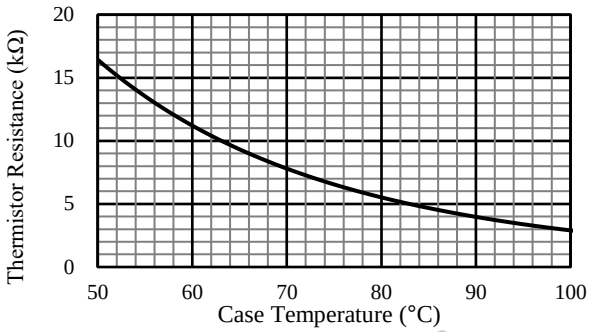

Figure 12-13. Typical Thermistor Resistance vs. Temperature Curve

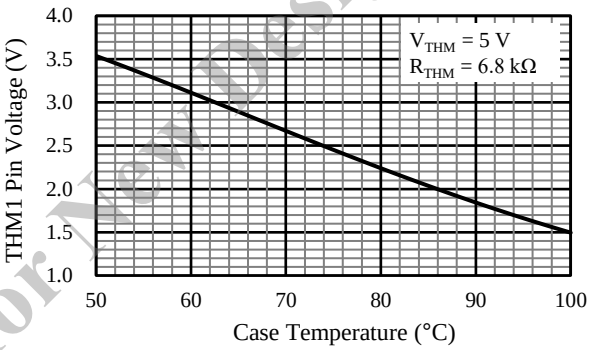

Figure 12-14. THM1 Pin Typical Performance Curve

12.2.13. COM1 and COM2

These are the logic ground pins for the IC. The COM1 and COM2 pins are internally connected. For proper control, the control parts used in the IC must be connected to the logic ground pin. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to a shunt resistor, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 12-4). Moreover, extreme care should be taken in designing a PCB trace layout so that currents from the power ground do not affect the COMx pin.

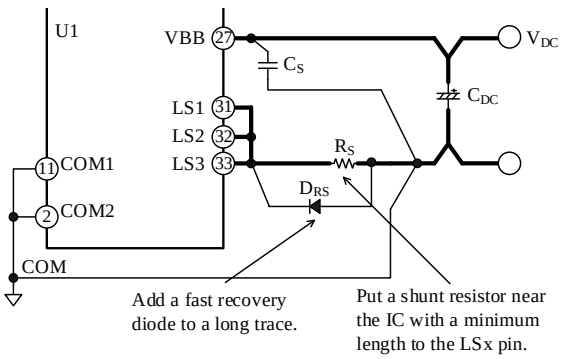

Figure 12-15. Connections to LSx Pin

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12.3. Protection Functions

This section describes the various protection circuits provided in the SCM2000MKF series. The protection circuits include the undervoltage lockout for power supplies (UVLO), the overvoltage protection (OVP), and the overcurrent protection (OCP).

In case one or more of these protection circuits are activated, the IC outputs a fault signal. In addition, the external microcontroller can input a shutdown signal to the IC.

In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor (see also the diagram in Section 7). "VBx–HSx" refers to the voltages between the VBx and HSx pins.

12.3.1. Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on, then the FO pin becomes logic low (≤0.5 V). By receiving a fault signal from the FO pin, the external microcontroller can stop the operations of the three phases.

1) VCC2 pin undervoltage lockout (UVLO_VCC2)
2) Overcurrent protection (OCP)
3) Overvoltage protection (OVP)

While the FO pin is in the low state, all the low-side transistors turn off. In normal operation, the FO pin outputs a high signal of about 5 V. The fault signal output time of the FO pin at OCP activation is defined as the OCP Hold Time, t_P, fixed by a built-in feature of the IC itself (see Section 12.3.4). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P.

If you need to resume the motor operation thereafter, set the motor to be resumed after a lapse of ≥2 seconds.

12.3.2. Shutdown Signal Input

The FO pin also acts as the input pin of shutdown signals. When the FO pin becomes logic low, all the low-side transistors turn off. The voltages and pulse widths of shutdown signals should be set as listed in Table 12-3.

Table 12-3. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥3.0 µs	≥3.0 µs

12.3.3. Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SCM2000MKF series has the undervoltage lockout (UVLO) circuits for each of the VBx, VCC1, and VCC2 pins.

12.3.3.1. VBx Pin Undervoltage Lockout (UVLO_BV)

Figure 12-16 shows operational waveforms of the VBx pin undervoltage lockout (i.e., UVLO_VB).

When the voltage between the VBx and output pins (VBx−HSx) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$ = 10 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low. When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VB operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release. Any fault signals are not output from the FO pin during the UVLO_VB operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

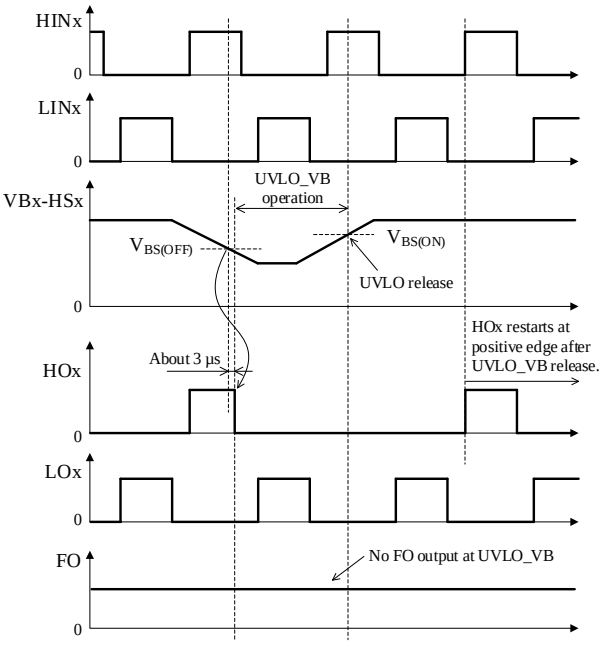

Figure 12-16. UVLO_VB Operational Waveforms

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12.3.3.2. VCC1 Pin Undervoltage Lockout (UVLO_VCC1)

As Figure 12-17 depicts, when the VCC1 pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 10 V) or less, the VCC1 pin undervoltage lockout (i.e., UVLO_VCC1) circuit gets activated and sets an HOx signal to logic low. When the VCC1 pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VCC1 operation. Then it resumes transmitting the HOx signal according to an input command on the HINx pin. Any fault signals are not output from the FO pin during the UVLO_VCC1 operation. In addition, the VCC1 pin has an internal UVLO_VCC1 filter of about 3 µs, in order to prevent noise-induced malfunctions.

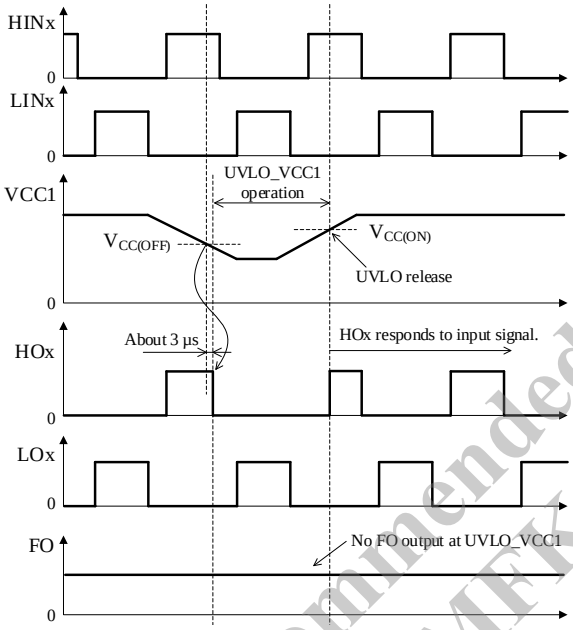

Figure 12-17. UVLO_VCC1 Operational Waveforms

12.3.3.3. VCC Pin Undervoltage Lockout (UVLO_VCC2)

Figure 12-18 shows operational waveforms of the VCC1 pin undervoltage lockout (i.e., UVLO_VCC2).

When the VCC2 pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 10 V) or less, the UVLO_VCC2 circuit gets activated and sets an LOx signal to logic low. When the VCC2 pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VCC2 condition. Then it resumes transmitting the LOx signal according to an input command on the LINx pin. During the UVLO_VCC2 operation, the FO pin becomes logic low and sends fault signals. In addition, the VCC2 pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

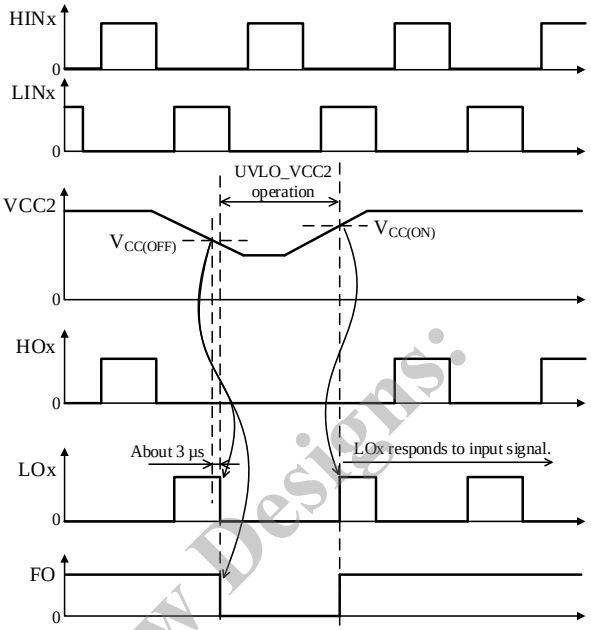

Figure 12-18. UVLO_VCC2 Operational Waveforms

12.3.4. Overcurrent Protection (OCP)

Figure 12-19 is an internal circuit diagram describing the OCP pin and its peripheral circuit. The OCP pin detects overcurrents with voltage across an external shunt resistor, R_S. Because the OCP pin is internally pulled down, the OCP pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

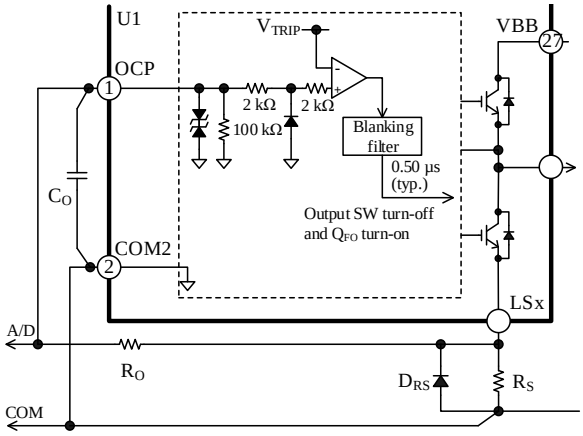

Figure 12-19. Internal Circuit Diagram of OCP Pin and Its Peripheral Circuit

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Figure 12-20 is a timing chart that represents operation waveforms during OCP operation. When the OCP pin voltage increases to the OCP Threshold Voltage (V_{TRIP} = 0.500 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK} = 0.5 µs) or longer, the OCP circuit is activated. When the OCP is activated, the IC puts both an LOx signal and the FO pin to logic low.

The output transistors turn off as the LOx signal becomes logic low; as a result, output current decreases. Even if the OCP pin voltage falls below V_{TRIP}, the IC holds the FO pin in the low state for a fixed OCP hold time (t_P). Then, the output transistors operate according to input signals.

You can select a suitable OCP hold time (t_P), 34 µs or 8 ms, based on the SELECT pin connection (see Section 12.2.9).

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. For this reason, motor operations must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. If you need to resume the motor operation thereafter, set the motor to be resumed after a lapse of ≥2 seconds.

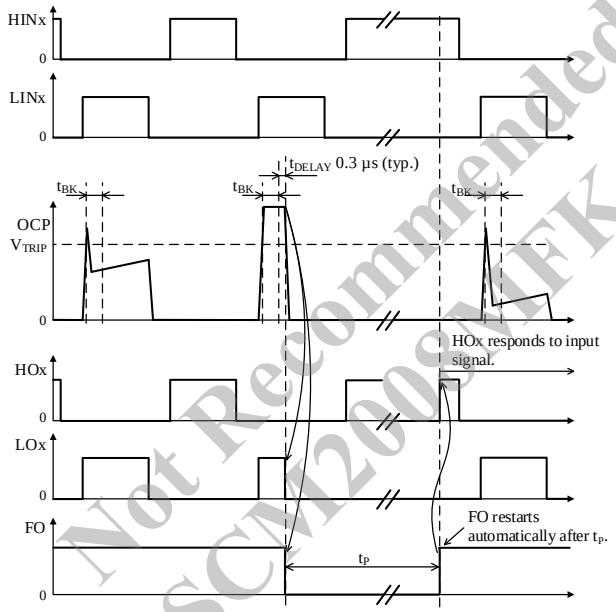

Figure 12-20. OCP Operational Waveforms

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the OCP pin input voltage to vary within the rated OCP pin voltages, V_{OCP} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

When you connect a CR filter (i.e., a pair of a filter resistor, R_O, and a filter capacitor, C_O) to the OCP pin, care should be taken in setting the time constants of R_O and C_O. The larger the time constant, the longer the time that the OCP pin voltage rises to V_{TRIP}. And this may cause permanent damage to the transistors. Consequently, a propagation delay of the IC must be taken into account when you determine the time constants. For R_O and C_O, their time constants must be set to ≤1 µs. And place C_O as close as possible to the IC with minimizing a trace length between the OCP and COMx pins.

Note that overcurrents are undetectable when one or more of the U, V, and W pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

12.3.5. Overvoltage Protection (OVP)

Figure 12-21 is a circuit diagram of the SD pin and its peripheral circuit; Figure 12-22 is a timing chart representing OVP operational waveforms.

The VBB pin voltage split by a resistive voltage divider, R_{SD_U} and R_{SD_D}, is applied to the SD pin. The SD pin is designed with an error tolerance of ±2%, allowing a high degree of voltage detection accuracy.

The higher the VBB pin voltage, the higher the SD pin voltage. When the SD pin voltage increases to the OVP Operating Voltage (V_{SDH} = 1.90 V) or more, then remains in this condition for a period of the SD Pin Filtering Time (t_{SD} = 2.0 µs), the OVP operation starts.

When the OVP is activated, the IC puts both an LOx signal and the FO pin to logic low. Even if the SD pin voltage decreases to the OVP Release Voltage (V_{DSL} = 1.78 V) or less, the IC keeps the FO pin to logic low for a certain period, i.e., the OVP Hold Time (t_{P_SD} = 31 µs). Then, the IC operates according to input signals after a lapse of t_{P_SD}.

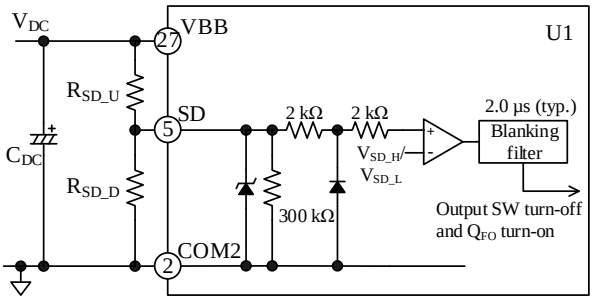

Figure 12-21. Internal Circuit Diagram of SD Pin and Its Peripheral Circuit

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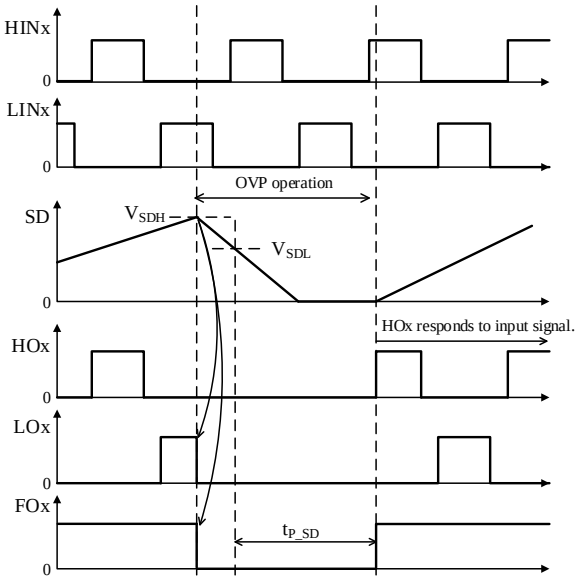

Figure 12-22. OVP Operational Waveforms

13. Design Notes

This section also employs the notation system described in the beginning of the previous section.

13.1. PCB Pattern Layout

Figure 13-1 shows a schematic diagram of a motor driver circuit.

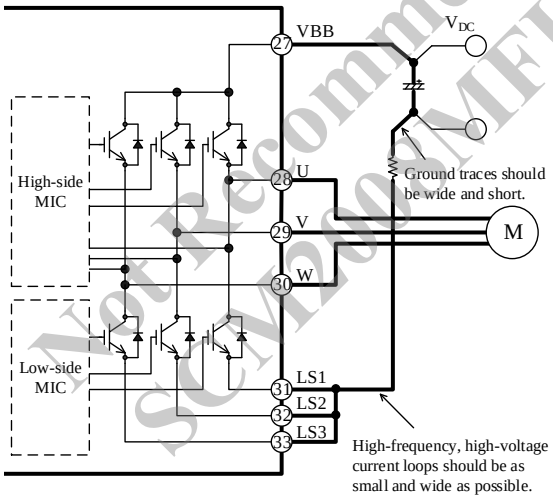

Figure 13-1. High-frequency, High-voltage Current Paths

The motor driver circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

13.2. Considerations in Heatsink Mounting

The following are the key considerations and the guidelines for mounting a heatsink:

- Be sure to use a metric screw of M3 and a plain washer of 7.0 mm (φ). To tighten the screws, use a torque screwdriver. Tighten the two screws firstly up to about 30% of the maximum screw torque, then finally up to 100% of the prescribed maximum screw torque. Perform appropriate tightening within the range of screw torque defined in Section 4.
- When mounting a heatsink, it is recommended to use silicone greases. If a thermally conductive sheet or an electrically insulating sheet is used, package cracks may be occurred due to creases at screw tightening. Therefore, you should conduct thorough evaluations before using these materials.
- When applying a silicone grease, make sure that there are no foreign substances between the IC and a heatsink. Extreme care should be taken not to apply a silicone grease onto any device pins as much as possible. The following requirements must be met for proper grease application:
  - Grease thickness: 100 μm
  - Heatsink flatness: ±100 μm
  - Apply a silicone grease within the area indicated in Figure 13-2, below.

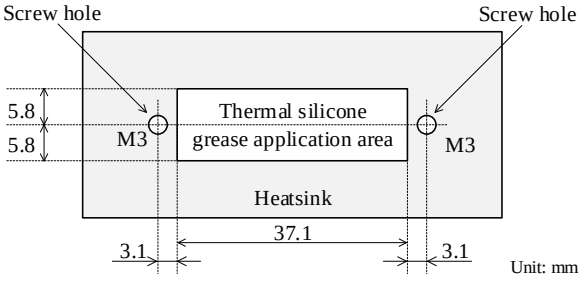

Figure 13-2. Reference Application Area for Thermal Silicone Grease

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13.3. Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that all of the output (U, V, and W), LSx, and COMx pins must be appropriately connected. Otherwise, the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 13-3 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 13-4 shows the low-side transistor (Q_{1L}) in the U-phase. When measuring the high-side transistors, leave all the non-measuring pins open. When measuring the low-side transistors, connect only the measuring LSx pin to the COM2 pin and leave the other pins open.

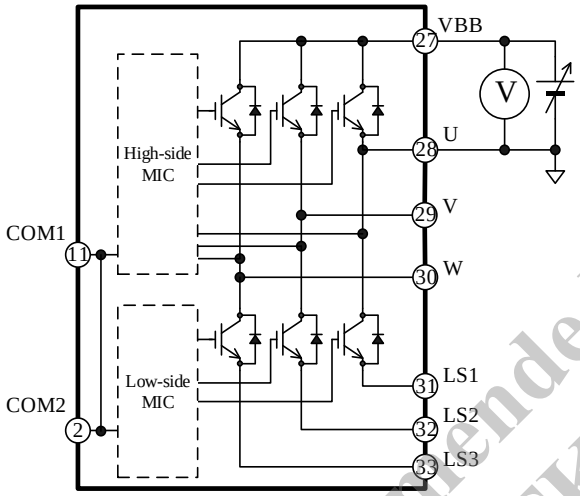

Figure 13-3. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

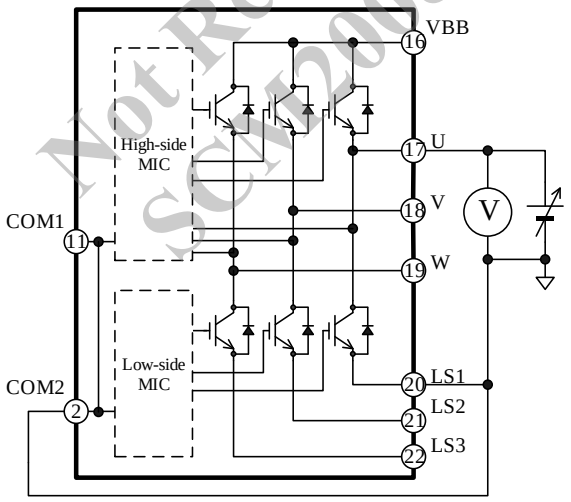

Figure 13-4. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

14. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in a switching transistor, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SCM2000MKF series, which is controlled by a 3-phase sine-wave PWM driving strategy.

Total power loss in an IGBT can be obtained by taking the sum of steady-state loss, P_{ON}, and switching loss, P_{SW}. The following subsections contain the mathematical procedures to calculate the power losses in an IGBT and its junction temperature. For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0051: SCM2000MKF Series Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/igbt1_caltool_en.html

14.1. IGBT Steady-state Loss, P_{ON}

Steady-state loss in an IGBT can be computed by using the $V_{CE(SAT)}$ vs. I_C curves, listed in Section 15.3.1. As expressed by the curves in Figure 14-1, a linear approximation at a range the IC is actually used is obtained by: $V_{CE(SAT)} = \alpha \times I_C + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (3), below. Hence, the equation to obtain the IGBT steady-state loss, P_{ON}, is:

$$P_{ON} = \frac{1}{2\pi}\int_0^{\pi} V_{CE(SAT)}(\varphi) \times I_C(\varphi) \times DT \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} + \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} + \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (3)$$

Where:

$V_{CE(SAT)}$ is the collector-to-emitter saturation voltage of the IGBT (V),
I_C is the collector current of the IGBT (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve, and
β is the intercept of the linear approximation in the $V_{CE(SAT)}$ vs. I_C curve.

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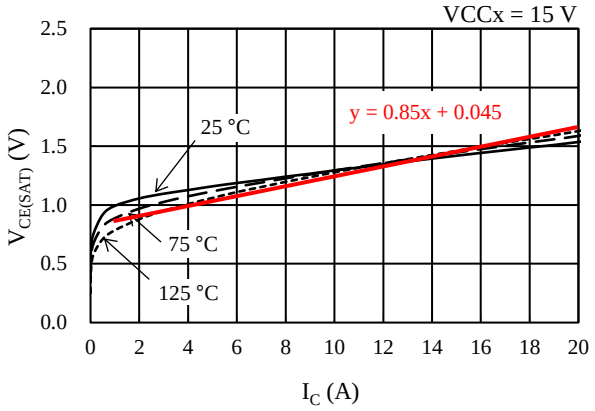

Figure 14-1. Linear Approximate Equation of $V_{CE(SAT)}$ vs. I_C

14.2. IGBT Switching Loss, P_{SW}

Switching loss in an IGBT, P_{SW}, can be calculated by Equation (4), letting I_M be the effective current value of the motor:

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (4)$$

Where:

f_C is the PWM carrier frequency (Hz),

V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and

α_E is the slope of the switching loss curve (see Section 15.3.2).

14.3. Estimating Junction Temperature of IGBT

The junction temperature of an IGBT, T_J, can be estimated with Equation (5):

$$T_J = R_{(J-C)Q} \times (P_{ON} + P_{SW}) + T_C. \quad (5)$$

Where:

$R_{(J-C)Q}$ is the junction-to-case thermal resistance per IGBT (°C/W), and

T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

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15. Performance Curves

15.1. Transient Thermal Resistance Curves

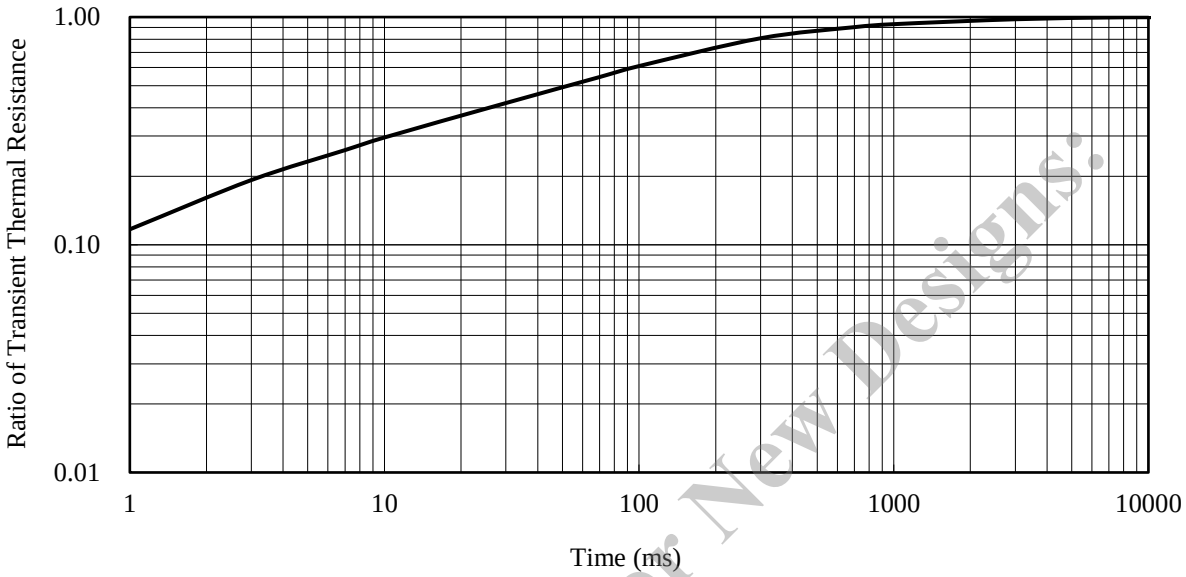

Figure 15-1. Transient Thermal Resistance: SCM2007MKF, SCM2008MKF

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15.2. Performance Curves of Control Parts

Figure 15-2 to Figure 15-27 provide performance curves of the control parts integrated in the SCM2000MKF series, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 15-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 15-2	Logic Supply Current, I_{CC} (I_{CC1} + I_{CC2}) vs. T_C
Figure 15-3	Logic Supply Current, I_{CC} (I_{CC1} + I_{CC2}) vs. VCCx Pin Voltage, V_{CC}
Figure 15-4	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 15-5	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 15-6	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B
Figure 15-7	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 15-8	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 15-9	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 15-10	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 15-11	UVLO_VB Filtering Time vs. T_C
Figure 15-12	UVLO_VCC Filtering Time vs. T_C
Figure 15-13	Input Current at High Level (HINx or LINx), I_{IH} vs. T_C
Figure 15-14	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 15-15	Low Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 15-16	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 15-17	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 15-18	FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_C
Figure 15-19	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 15-20	Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C
Figure 15-21	OCP Hold Time, t_{P1} vs. T_C
Figure 15-22	OCP Hold Time, t_{P2} vs. T_C
Figure 15-23	SD Pin OVP Operating Voltage, V_{SDH} vs. T_C
Figure 15-24	SD Pin OVP Release Voltage, V_{SDL} vs. T_C
Figure 15-25	SD Pin Input Current, I_{SD} vs. T_C
Figure 15-26	SD Pin Filtering Time, t_{SD} vs. T_C
Figure 15-27	OVP Hold Time, t_{P_SD} vs. T_C

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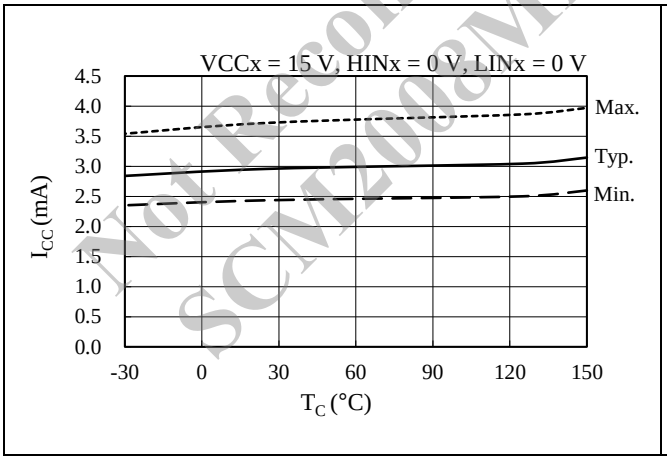

Figure 15-2. Logic Supply Current, I_{CC} (I_{CC1} + I_{CC2}) vs. T_C

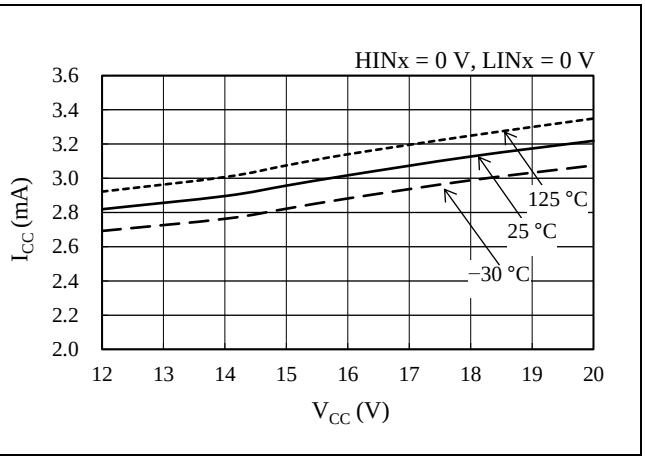

Figure 15-3. Logic Supply Current, I_{CC} (I_{CC1} + I_{CC2}) vs. VCCx Pin Voltage, V_{CC}

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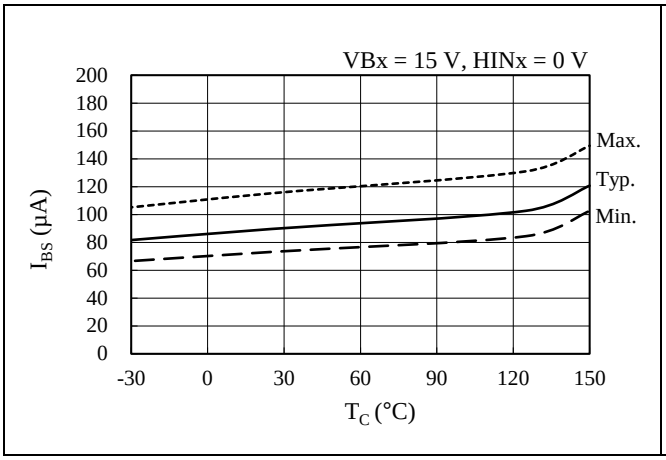

Figure 15-4. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

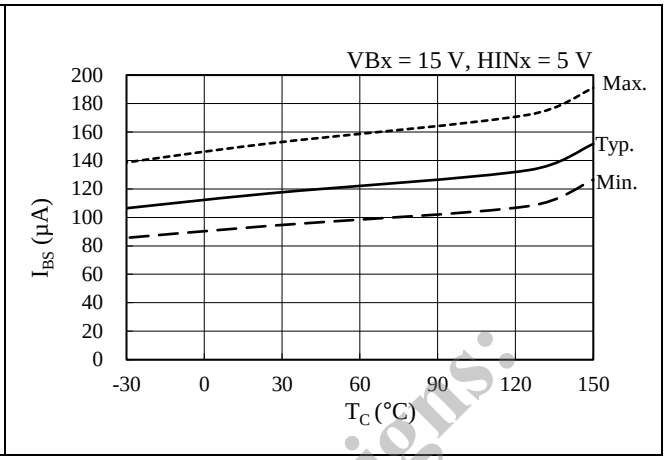

Figure 15-5. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

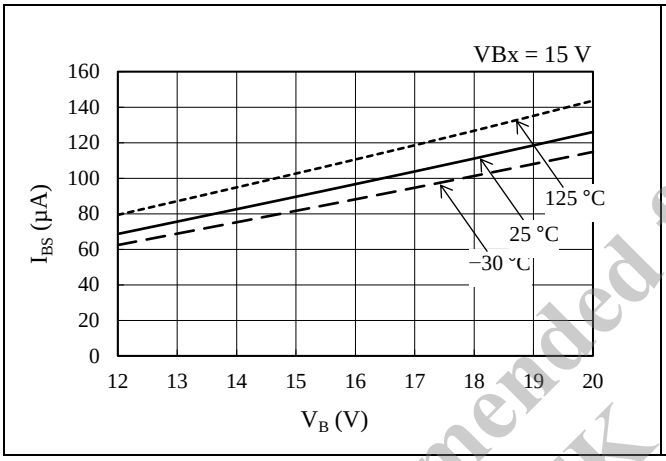

Figure 15-6. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. VBx Pin Voltage, V_B

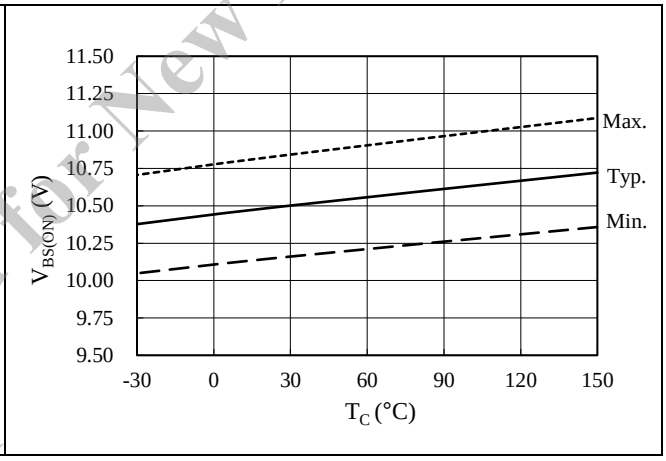

Figure 15-7. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

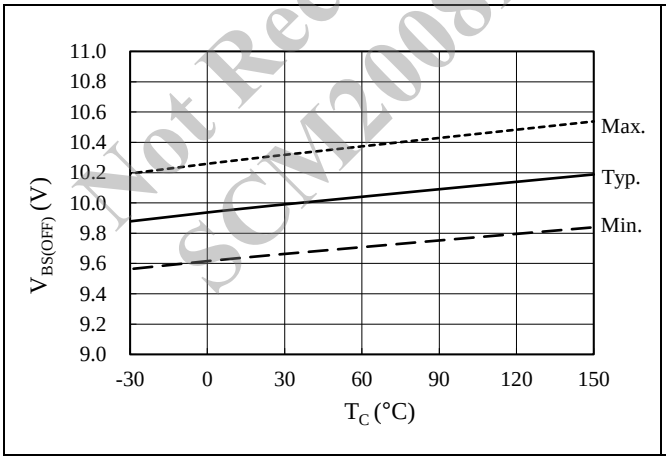

Figure 15-8. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

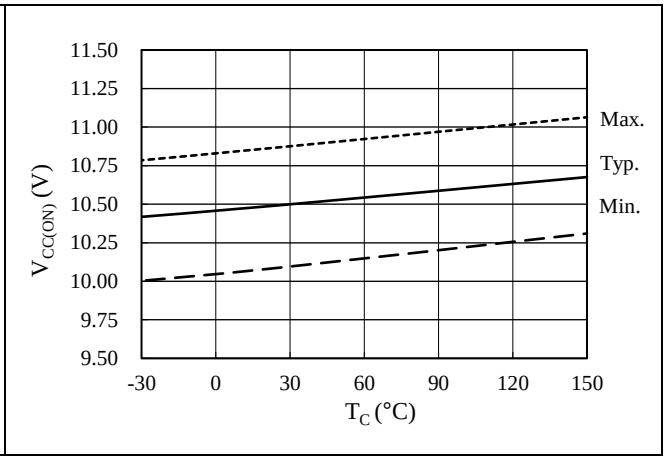

Figure 15-9. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

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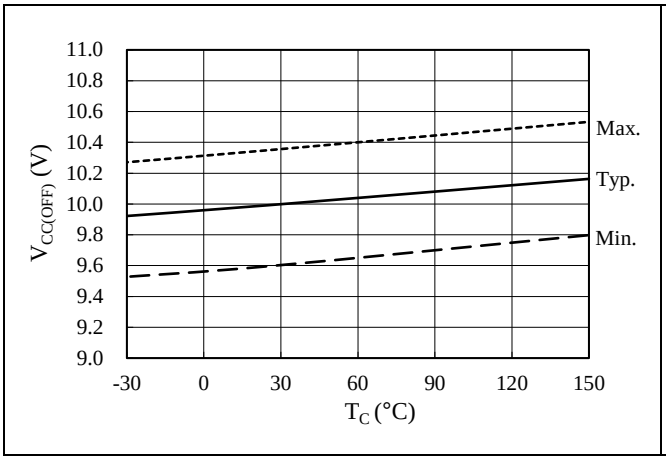

Figure 15-10. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

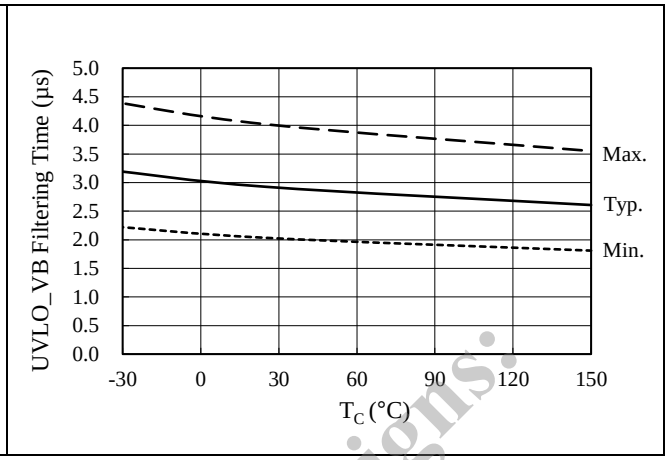

Figure 15-11. UVLO_VB Filtering Time vs. T_C

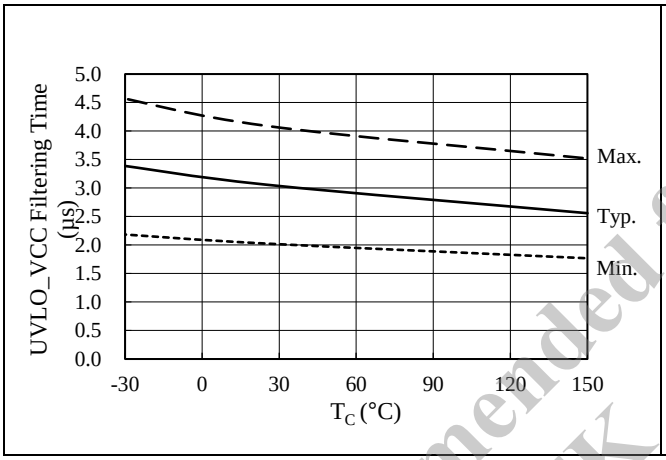

Figure 15-12. UVLO_VCC Filtering Time vs. T_C

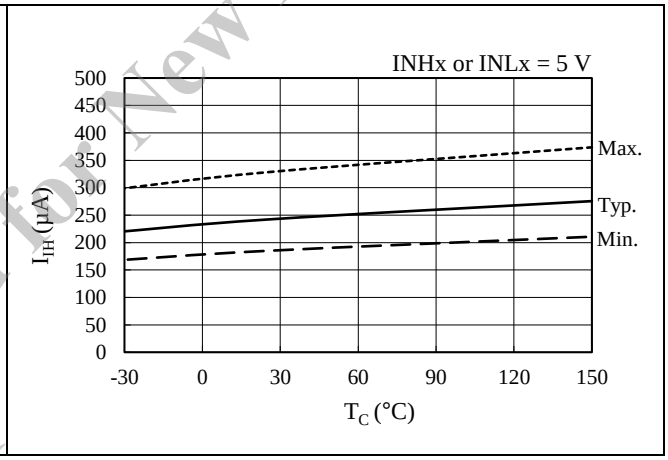

Figure 15-13. Input Current at High Level (HINx or LINx), I_{IH} vs. T_C

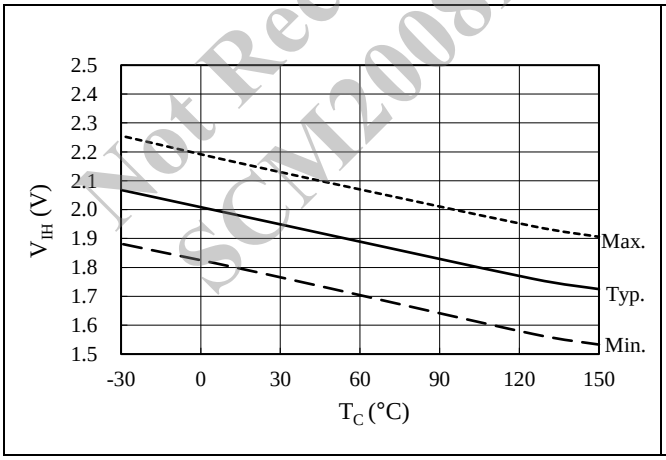

Figure 15-14. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

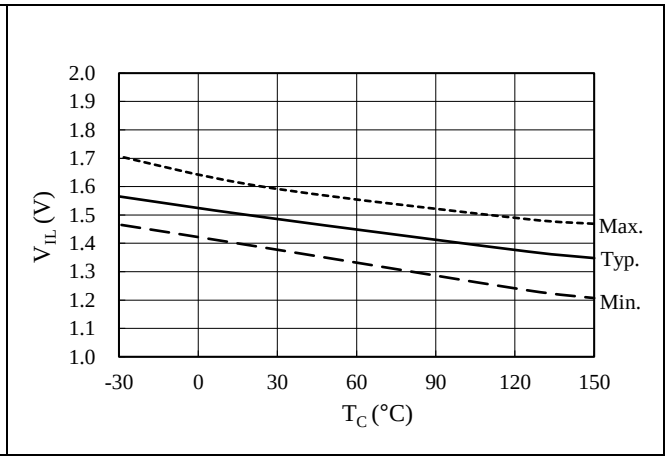

Figure 15-15. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

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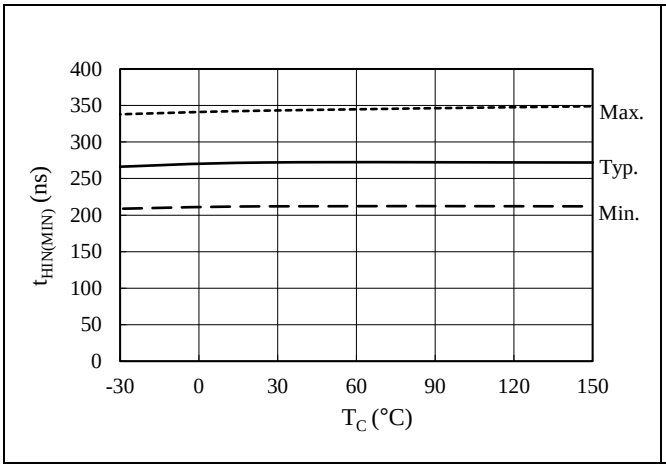

Figure 15-16. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

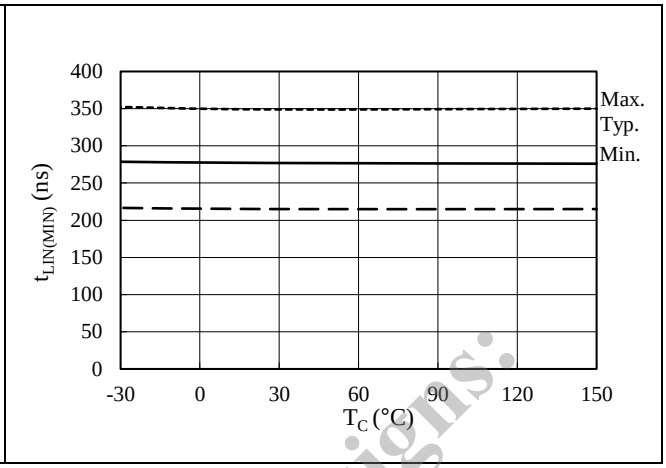

Figure 15-17. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

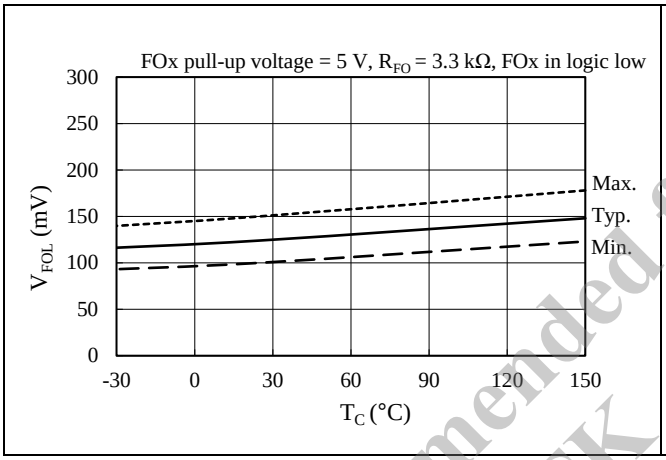

Figure 15-18. FOx Pin Voltage in Normal Operation, V_{FOL} vs. T_C

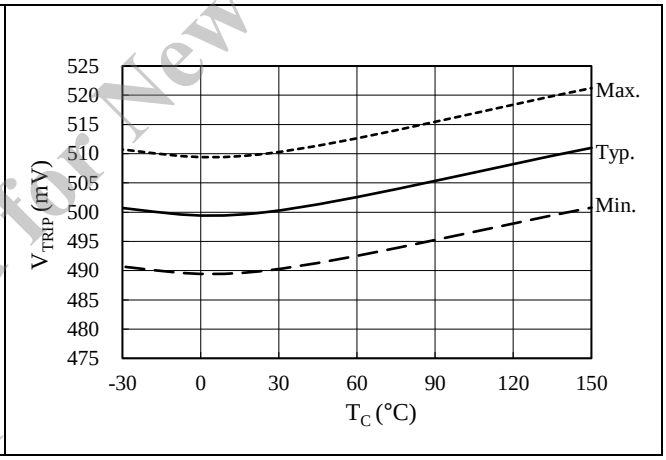

Figure 15-19. OCP Threshold Voltage, V_{TRIP} vs. T_C

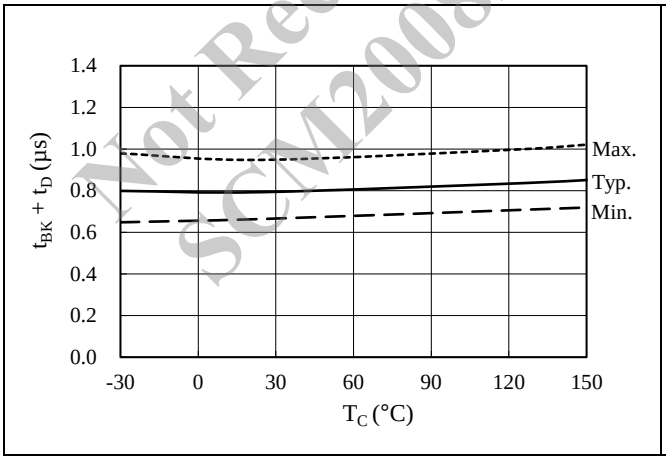

Figure 15-20. Blanking Time, t_{BK} + Propagation Delay, t_D vs. T_C

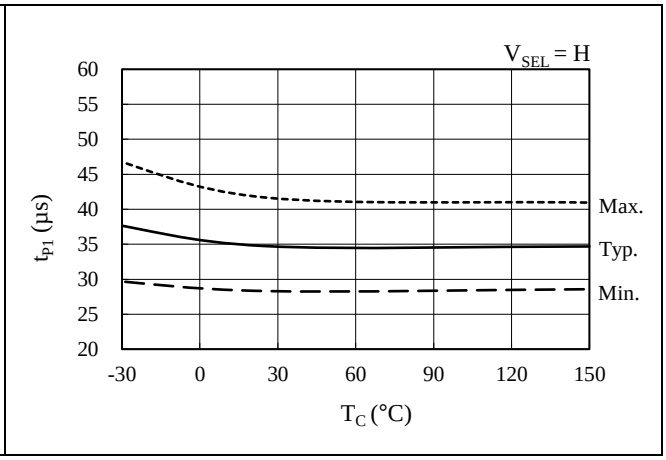

Figure 15-21. OCP Hold Time, t_{P1} vs. T_C

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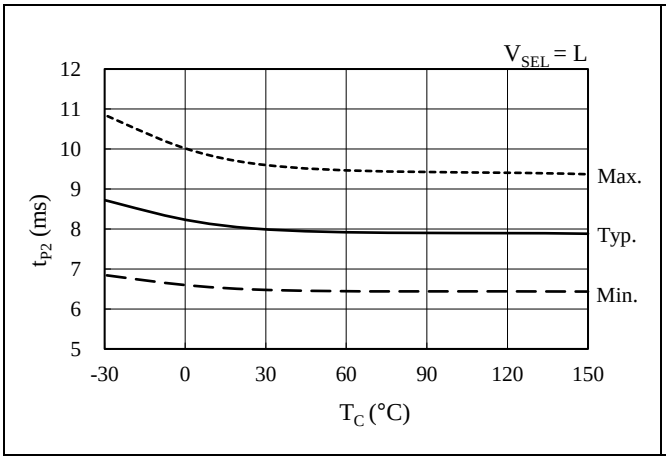

Figure 15-22. OCP Hold Time, t_{P2} vs. T_C

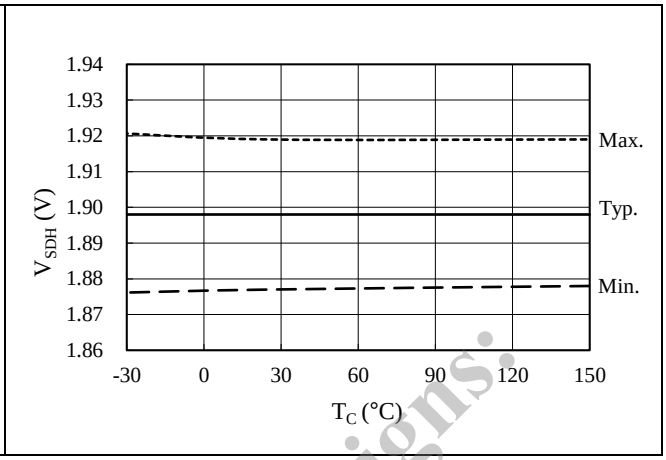

Figure 15-23. SD Pin OVP Operating Voltage, V_{SDH} vs. T_C

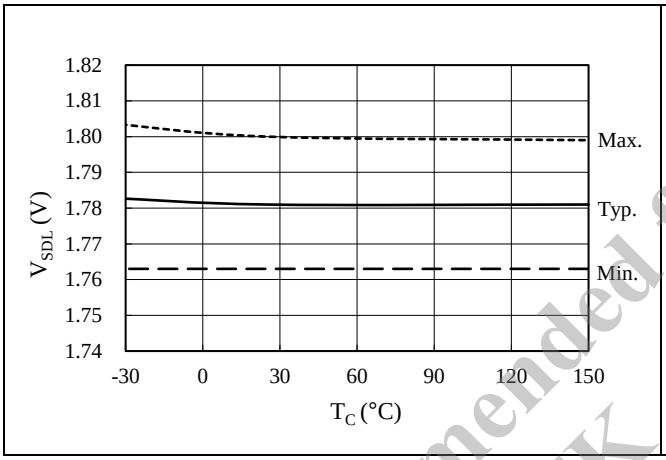

Figure 15-24. SD Pin OVP Release Voltage, V_{SDL} vs. T_C

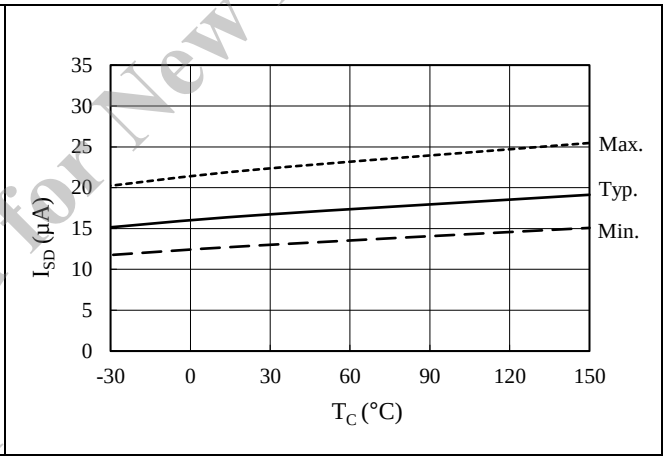

Figure 15-25. SD Pin Input Current, I_{SD} vs. T_C

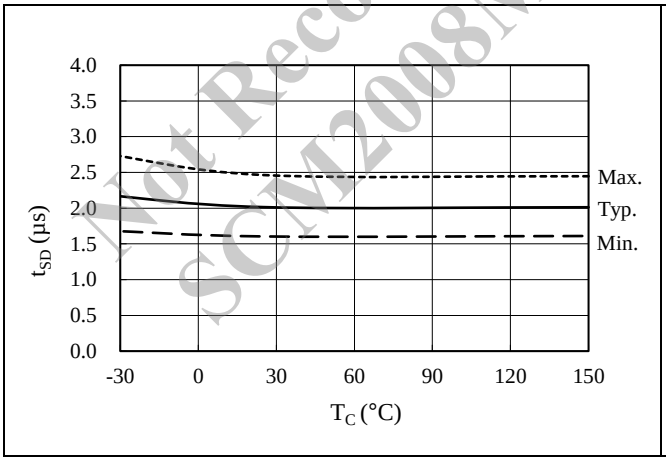

Figure 15-26. SD Pin Filtering Time, t_{SD} vs. T_C

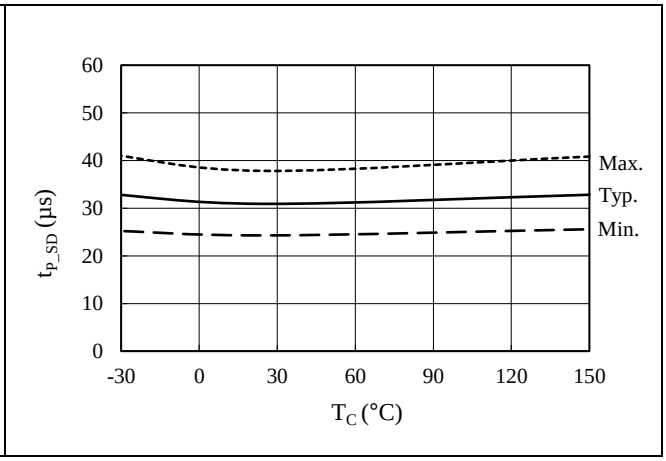

Figure 15-27. OVP Hold Time, t_{P_SD} vs. T_C

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15.3. Performance Curves of Output Parts

15.3.1. Output Transistor Performance Curves

15.3.1.1. SCM2007MKF

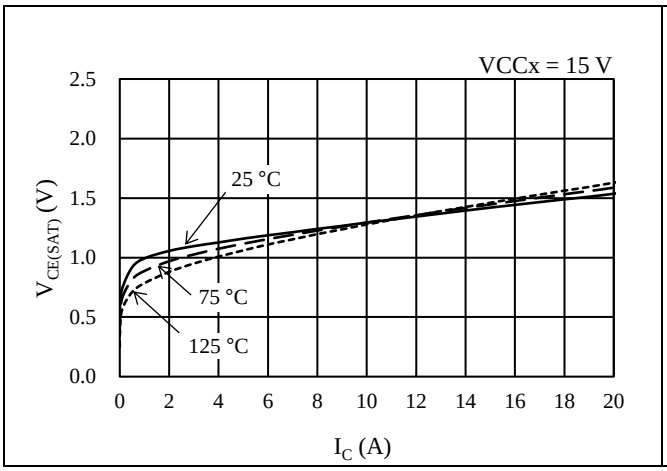

Figure 15-28. IGBT $V_{CE(SAT)}$ vs. I_C

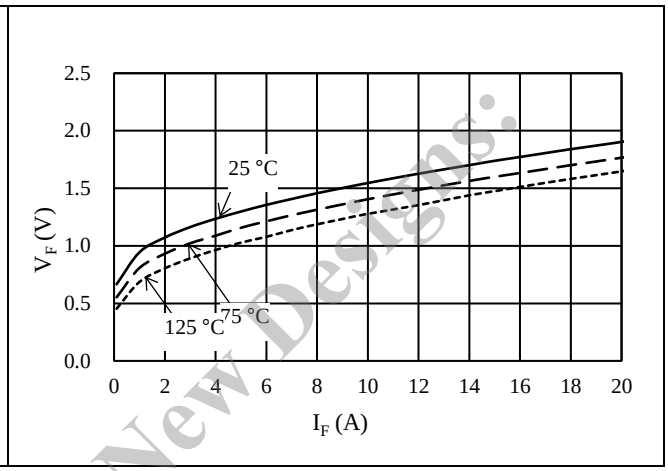

Figure 15-29. Freewheeling Diode V_F vs. I_F

15.3.1.2. SCM2008MKF

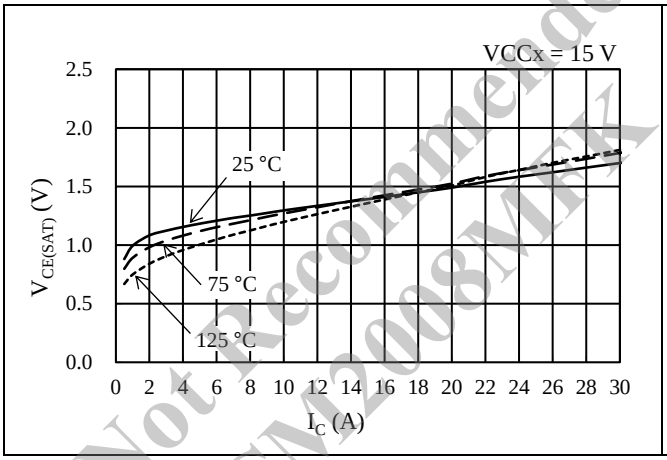

Figure 15-30. IGBT $V_{CE(SAT)}$ vs. I_C

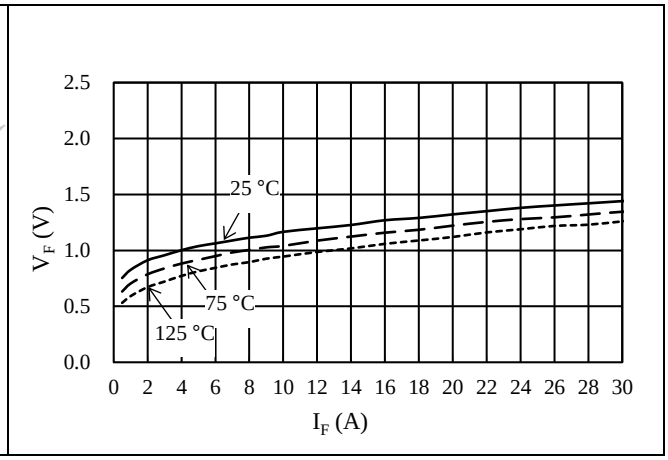

Figure 15-31. Freewheeling Diode V_F vs. I_F

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15.3.2. Switching Losses

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.

15.3.2.1. SCM2007MKF

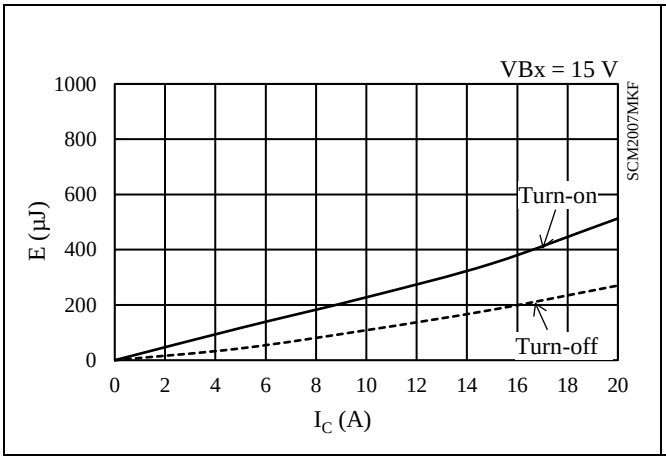

Figure 15-32. High-side Switching Loss (T_J = 25 °C)

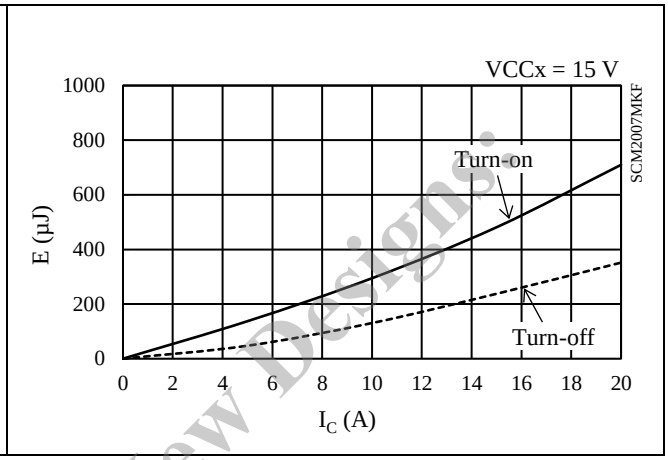

Figure 15-33. Low-side Switching Loss (T_J = 25 °C)

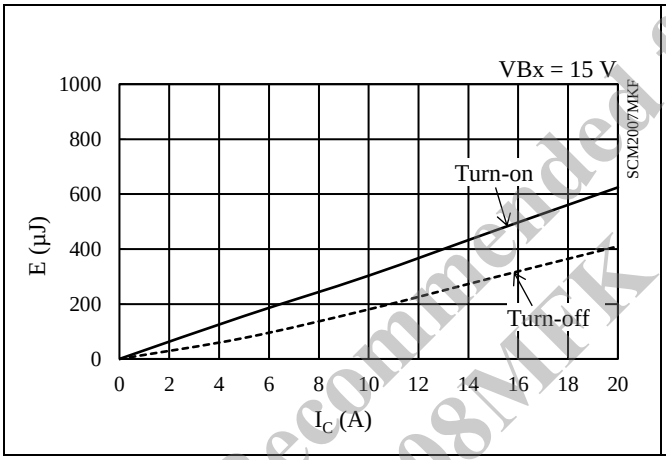

Figure 15-34. High-side Switching Loss (T_J = 125 °C)

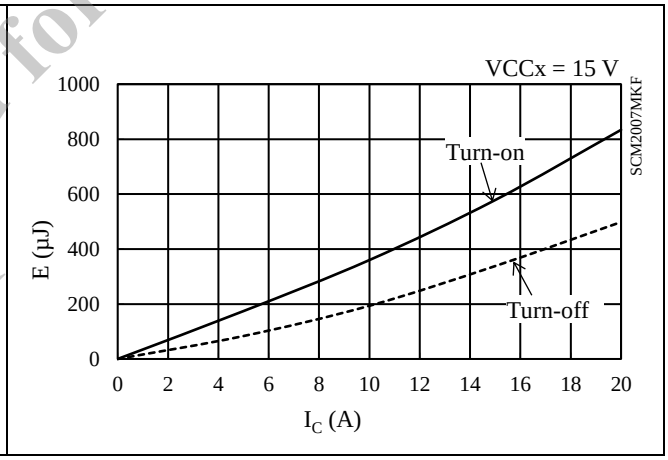

Figure 15-35. Low-side Switching Loss (T_J = 125 °C)

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15.3.2.2. SCM2008MKF

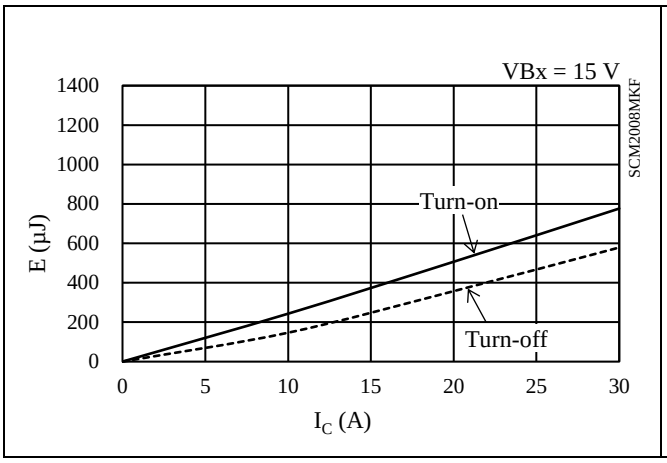

Figure 15-36. High-side Switching Loss (T_J = 25 °C)

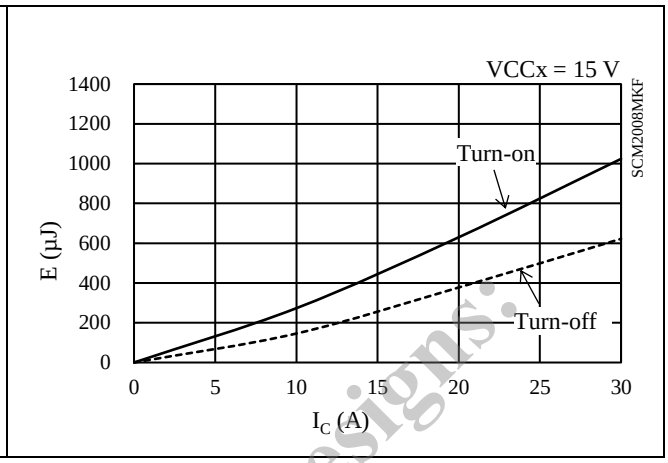

Figure 15-37. Low-side Switching Loss (T_J = 25 °C)

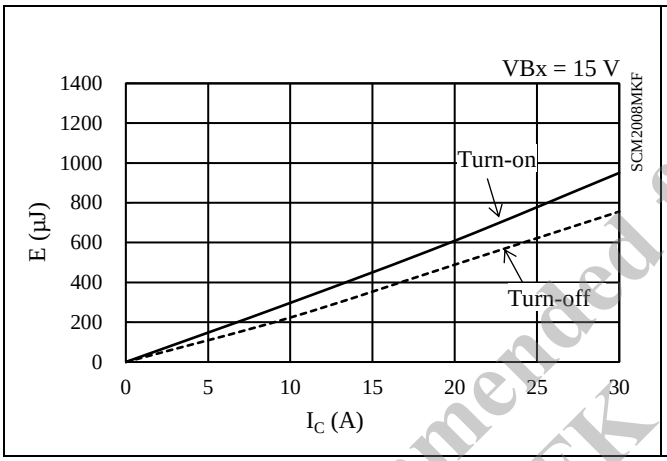

Figure 15-38. High-side Switching Loss (T_J = 125 °C)

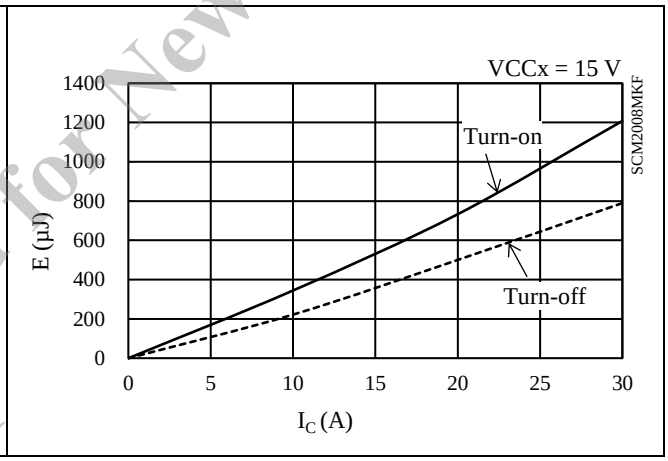

Figure 15-39. Low-side Switching Loss (T_J = 125 °C)

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15.4. Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $V_{CE(SAT)}$ and typical switching losses.

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

15.4.1. SCM2007MKF

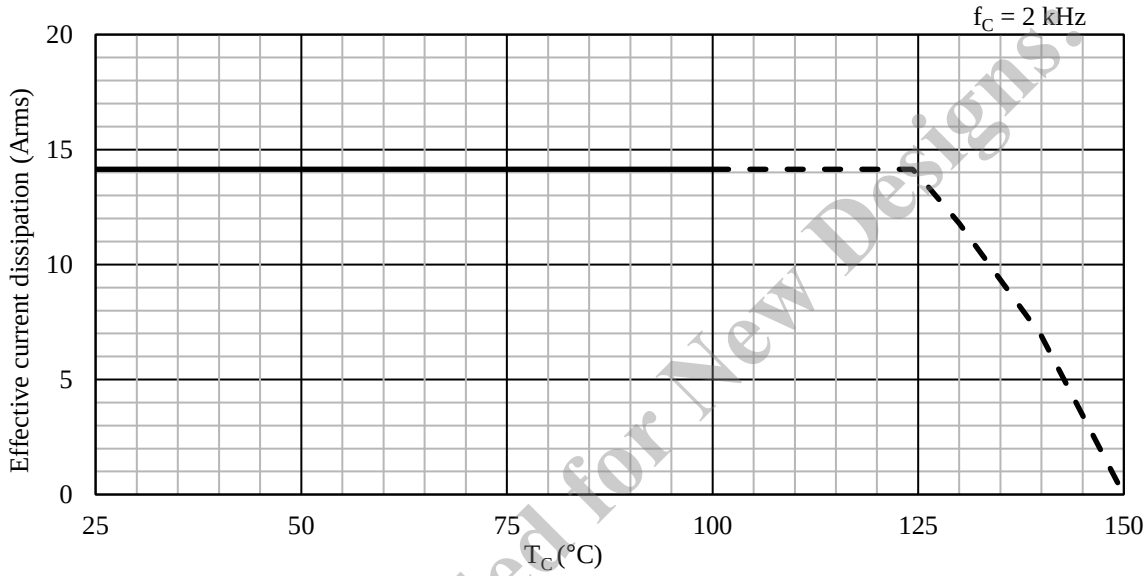

Figure 15-40. Allowable Effective Current (f_C = 2 kHz): SCM2007MKF

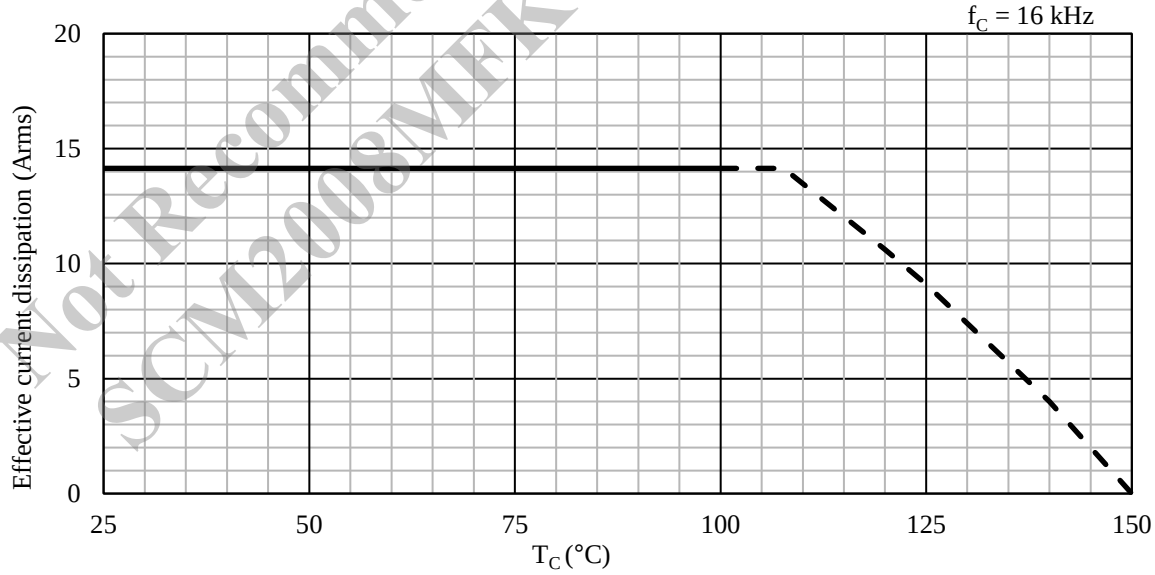

Figure 15-41. Allowable Effective Current (f_C = 16 kHz): SCM2007MKF

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15.4.2. SCM2008MKF

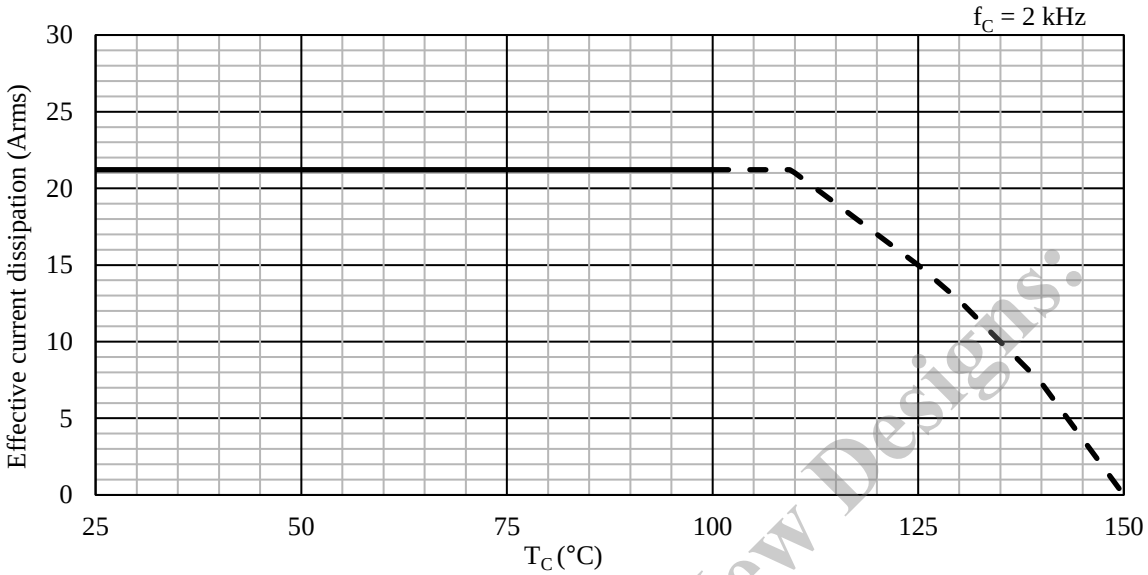

Figure 15-42. Allowable Effective Current (f_C = 2 kHz): SCM2008MKF

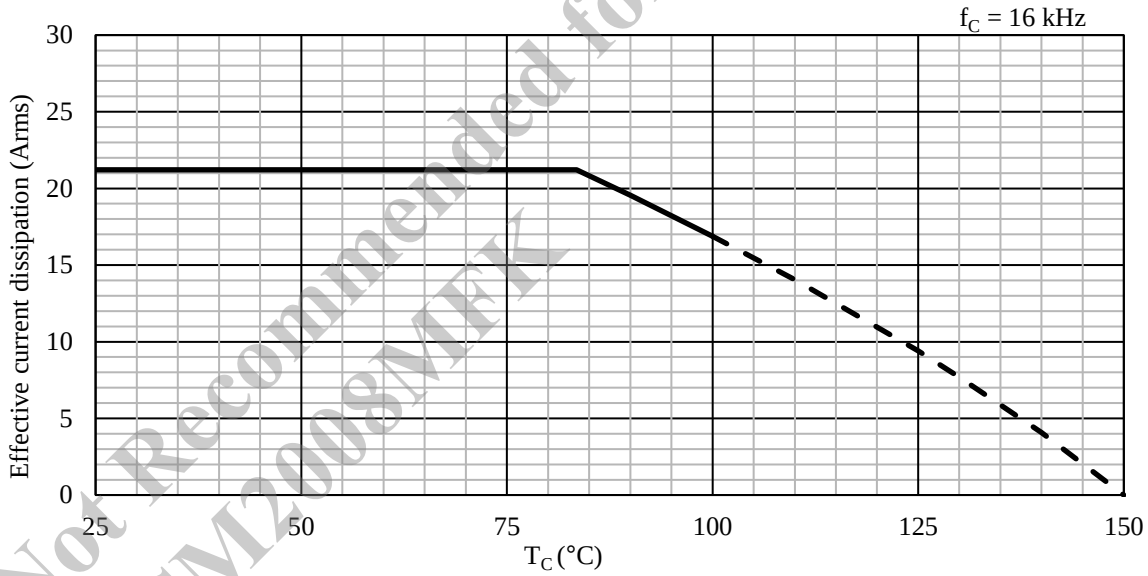

Figure 15-43. Allowable Effective Current (f_C = 16 kHz): SCM2008MKF

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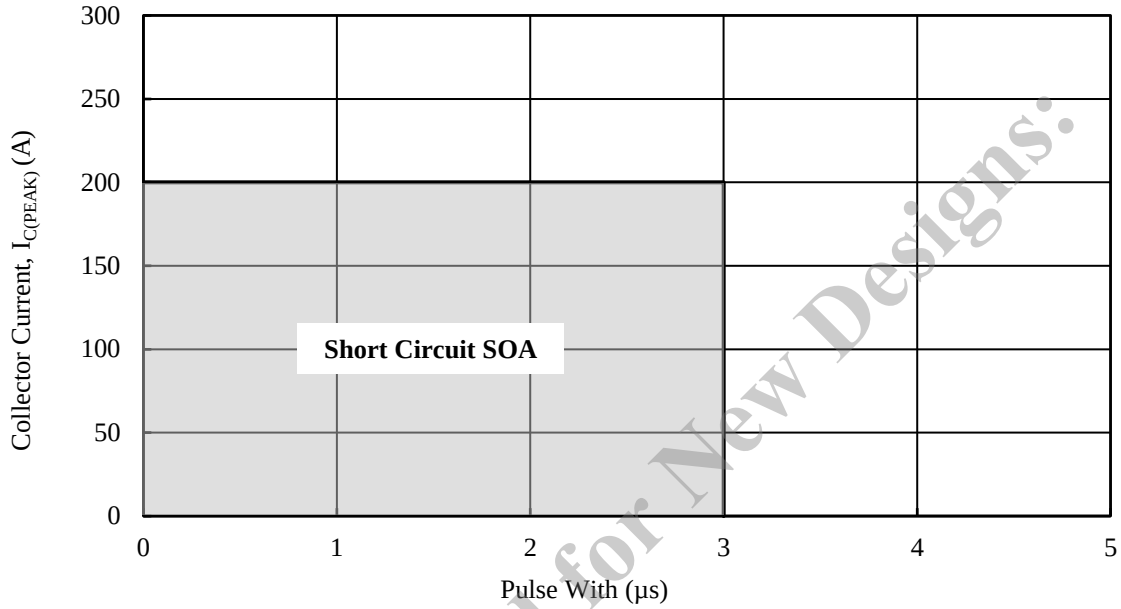
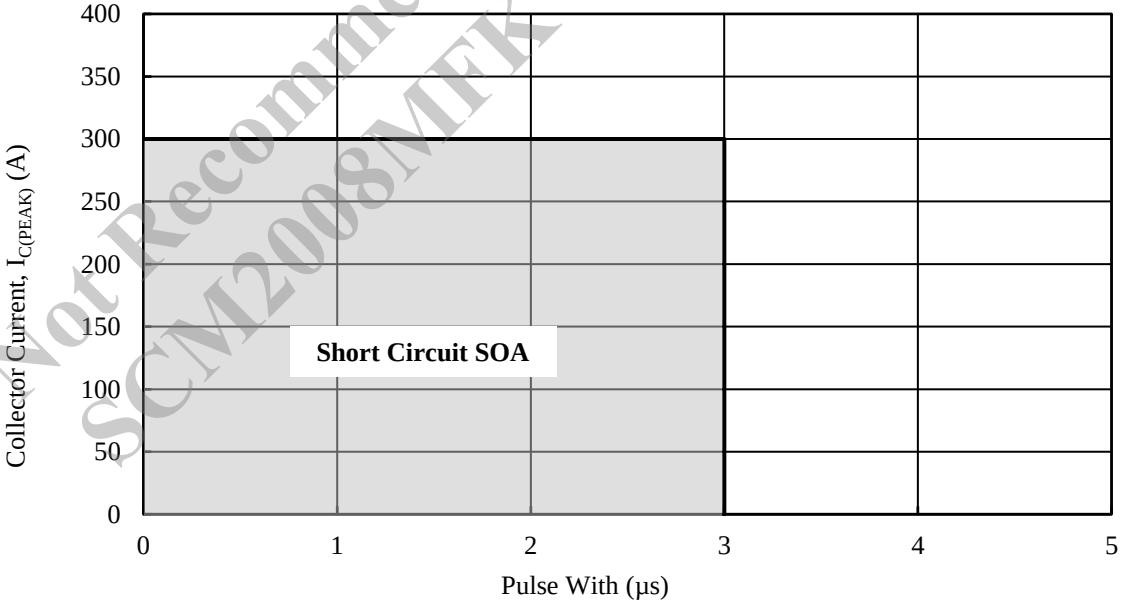
15.5. Short Circuit SOAs (Safe Operating Areas)

Conditions: $V_{DC} \leq 400$ V, 13.5 V $\leq V_{CC} \leq 16.5$ V, $T_J = 125$ °C, 1 pulse.

15.5.1. SCM2007MKF



15.5.2. SCM2008MKF



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16. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SCM2000MKF series device. For reference terminal hole sizes, see Section 10.2.

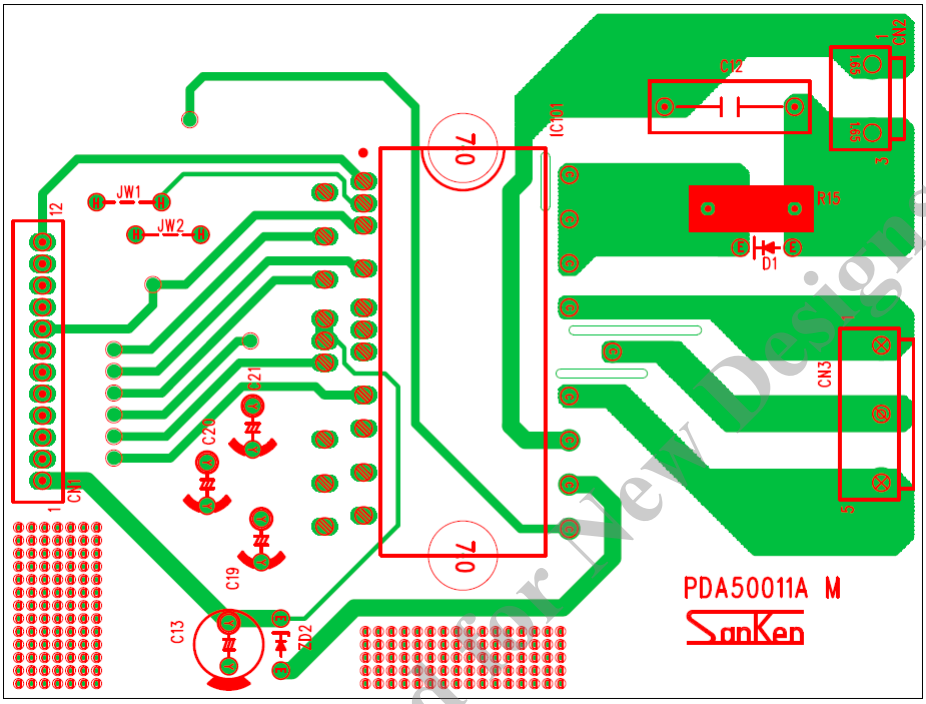

Figure 16-1. Top View

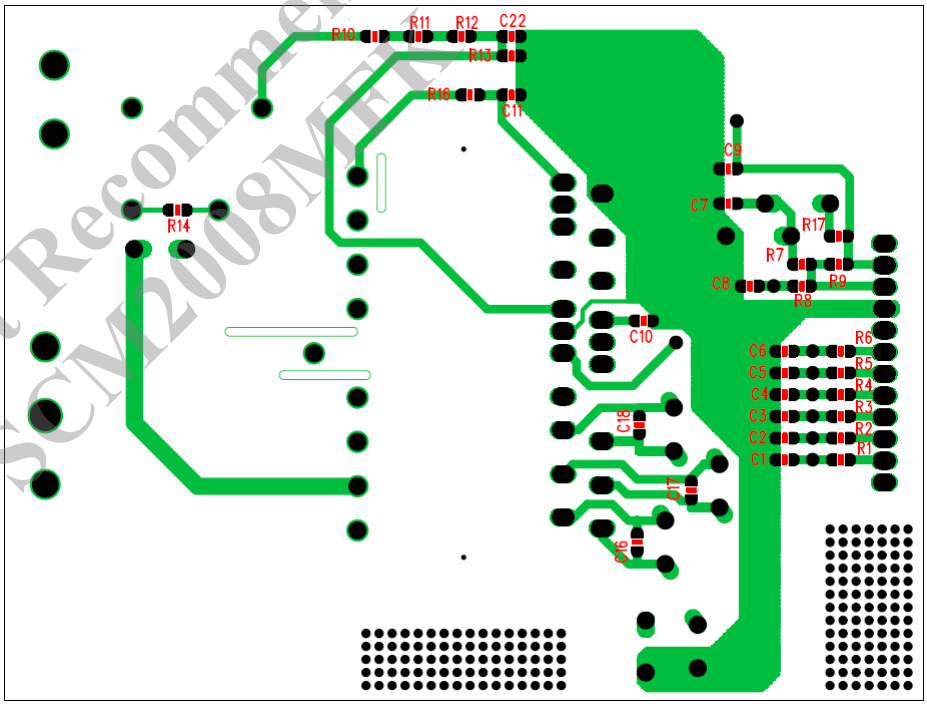

Figure 16-2. Bottom View

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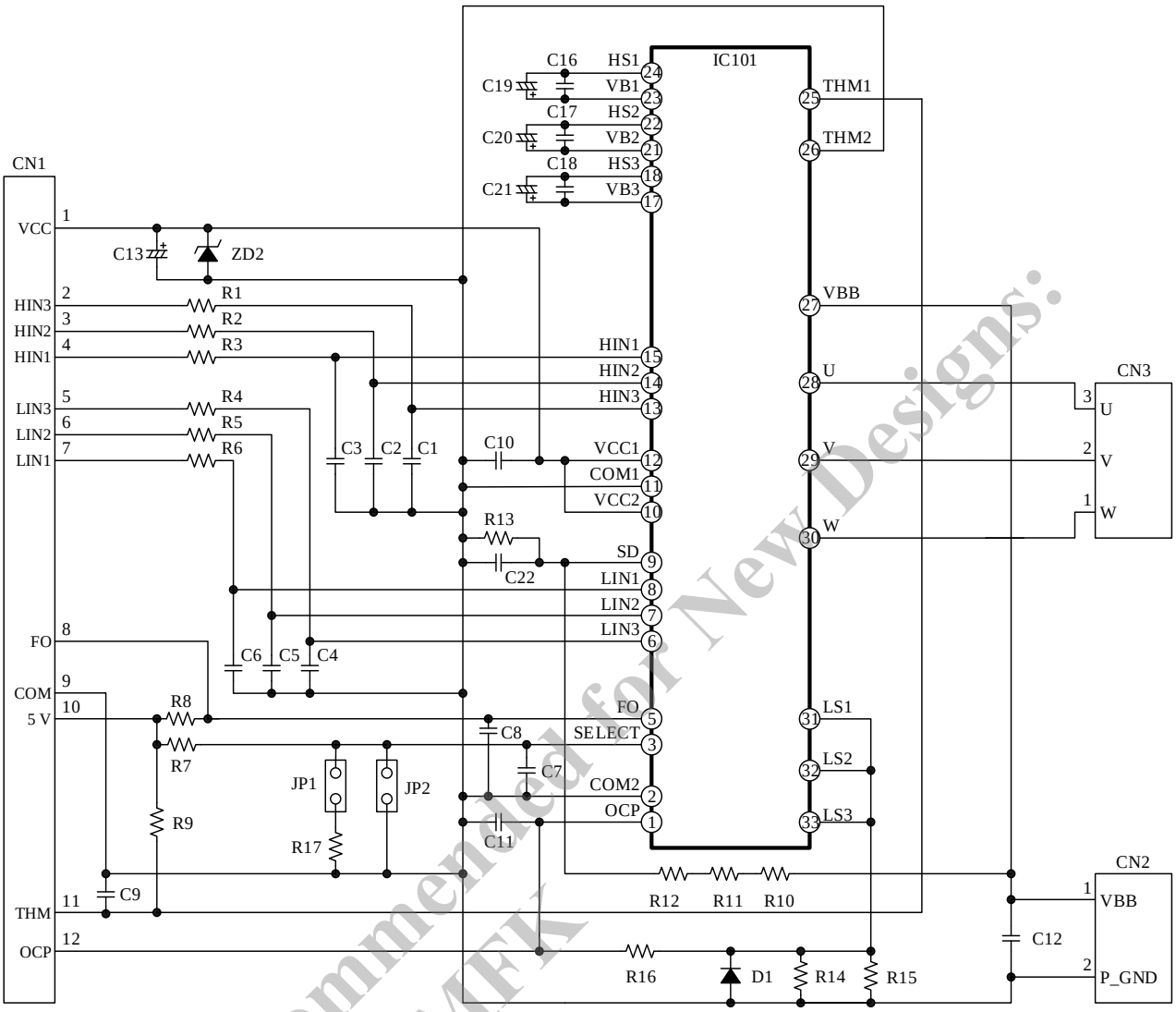

Figure 16-3. Circuit Diagram of PCB Pattern Layout Example

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17. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- Motor Driver Specifications

IC	SCM2007MKF
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	1.5 kW

- Circuit Diagram

See Figure 16-3.

- Bill of Materials

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Ceramic	1000 pF, 50 V	R1	General	100 Ω, 1/8 W
C2	Ceramic	1000 pF, 50 V	R2	General	100 Ω, 1/8 W
C3	Ceramic	1000 pF, 50 V	R3	General	100 Ω, 1/8 W
C4	Ceramic	1000 pF, 50 V	R4	General	100 Ω, 1/8 W
C5	Ceramic	1000 pF, 50 V	R5	General	100 Ω, 1/8 W
C6	Ceramic	1000 pF, 50 V	R6	General	100 Ω, 1/8 W
C7(1)	Ceramic	C7: 0.01 µF, 50 V	R7(1)	General	8.2 kΩ, 1/8 W
C8	Ceramic	0.01 µF, 50 V	R8	General	3.3 kΩ, 1/8 W
C9	Ceramic	0.01 µF, 50 V	R9	General	6.8 kΩ, 1/8 W
C10	Ceramic	0.1 µF, 50 V	R10	General	150 Ω, 1/2 W
C11	Ceramic	1000 pF, 50 V	R11	General	150 Ω, 1/2 W
C12	Film	0.1 µF, 630 V	R12	General	150 Ω, 1/2 W
C13	Electrolytic	47 µF, 50 V	R13	General	1.8 kΩ, 1/8 W
C16	Ceramic	0.1 µF, 50 V	R14(2)	General	Open
C17	Ceramic	0.1 µF, 50 V	R15(2)	Metal plate	18 mΩ, 2 W
C18	Ceramic	0.1 µF, 50 V	R16	General	100 Ω, 1/8 W
C19	Electrolytic	47 µF, 50 V	R17(3)	General	Open
C20	Electrolytic	47 µF, 50 V	JP1(3)	Jumper	Open
C21	Electrolytic	47 µF, 50 V	JP2(1)	Jumper	Open
C22	Ceramic	0.01 µF, 50 V	CN1	Connector	Equiv. to B3P5-VH-LF
D1	General	1 A, 50 V	CN2	Connector	Equiv. to B2P3-VH(LF)(SN)
DZ2	Zener	V_Z = 20 V, 0.5 W	CN3	Connector	Equiv. to B14B-XH-A(LF)(SN)
			IC101	IC	SCM2007MKF

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(1) Refers to when the OCP hold time, t_P = 8 ms. t_P depends on the SELECT pin connection (see Section 12.2.9). When t_P = 34 µs, leave C7 and R7 opened and JP2 shorted.
(2) Refers to a part that requires adjustment based on operation performance in an actual application.
(3) Represents the pin unused despite the layout examples illustrating its installation.

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