



High Common-Mode Rejection Differential Line Receiver

SSM2141

FEATURES

High Common-Mode Rejection

DC: 100 dB typ
60 Hz: 100 dB typ
20 kHz: 70 dB typ
40 kHz: 62 dB typ

Low Distortion: 0.001% typ

Fast Slew Rate: 9.5 V/ μ s typ

Wide Bandwidth: 3 MHz typ

Low Cost

Complements SSM2142 Differential Line Driver

APPLICATIONS

Line Receivers

Summing Amplifiers

Buffer Amplifiers—Drives 600 Ω Load

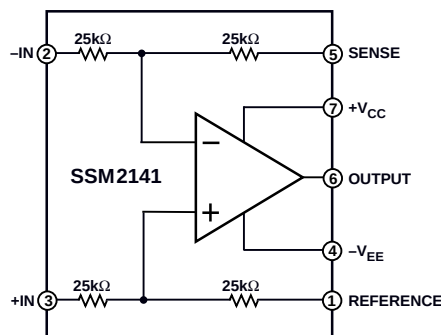
GENERAL DESCRIPTION

The SSM2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM2141 typically achieves 100 dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40 dB of CMR—inadequate for high-performance audio.

The SSM2141 achieves low distortion performance by maintaining a large slew rate of 9.5 V/ μ s and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM2141 complements the SSM2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM2141 include summing signals, differential preamplifiers, and 600 Ω low distortion buffer amplifiers. For similar performance with $G = 1/2$, see SSM2143.

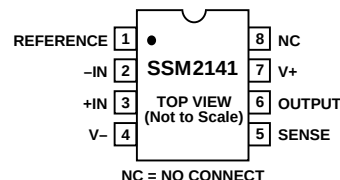
FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

8-Pin Plastic Mini-DIP (P Suffix)

Narrow Body SO (S Suffix)



REV. C

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SSM2141—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 18\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	SSM2141			Units
			Min	Typ	Max	
OFFSET VOLTAGE	V_{OS}	$V_{CM} = 0\text{ V}$	−1000	25	1000	μV
GAIN ERROR		No Load, $V_{IN} = \pm 10\text{ V}$, $R_S = 0\ \Omega$		0.001	0.01	%
INPUT VOLTAGE RANGE	IVR	(Note 1)	± 10			V
COMMON-MODE REJECTION	CMR	$V_{CM} = \pm 10\text{ V}$	80	100		dB
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 6\text{ V}$ to $\pm 18\text{ V}$		0.7	15	$\mu\text{V/V}$
OUTPUT SWING	V_O	$R_L = 2\text{ k}\Omega$	± 13	± 14.7		V
SHORT-CIRCUIT CURRENT LIMIT	I_{SC}	Output Shorted to Ground	+45/−15			mA
SMALL-SIGNAL BANDWIDTH (−3 dB)	BW	$R_L = 2\text{ k}\Omega$		3		MHz
SLEW RATE	SR	$R_L = 2\text{ k}\Omega$	6	9.5		V/ μs
TOTAL HARMONIC DISTORTION	THD	$R_L = 100\text{ k}\Omega$ $R_L = 600\ \Omega$		0.001 0.01		%
CAPACITIVE LOAD DRIVE CAPABILITY	C_L	No Oscillation		300		pF
SUPPLY CURRENT	I_{SY}	No Load		2.5	3.5	mA

NOTES

¹Input Voltage Range Guaranteed by CMR test.

Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFFSET VOLTAGE	V_{OS}	$V_{CM} = 0\text{ V}$	−2500	200	2500	μV
GAIN ERROR		No Load, $V_{IN} = \pm 10\text{ V}$, $R_S = 0\ \Omega$		0.002	0.02	%
INPUT VOLTAGE RANGE	IVR	(Note 1)	± 10			V
COMMON-MODE REJECTION	CMR	$V_{CM} = \pm 10\text{ V}$	75	90		dB
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 6\text{ V}$ to $\pm 18\text{ V}$		1.0	20	$\mu\text{V/V}$
OUTPUT SWING	V_O	$R_L = 2\text{ k}\Omega$	± 13	± 14.7		V
SLEW RATE	SR	$R_L = 2\text{ k}\Omega$		9.5		V/ μs
SUPPLY CURRENT	I_{SY}	No Load		2.6	4.0	mA

NOTES

¹Input Voltage Range Guaranteed by CMR test.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS¹

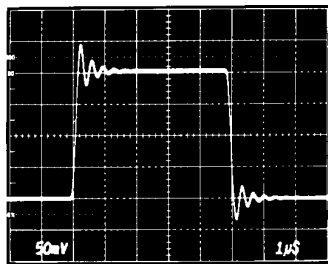
Supply Voltage	± 18 V
Input Voltage ¹	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P Package	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^{\circ}\text{C}$
Junction Temperature	$+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$

Package Type	θ_{JA} ²	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	$^{\circ}\text{C/W}$

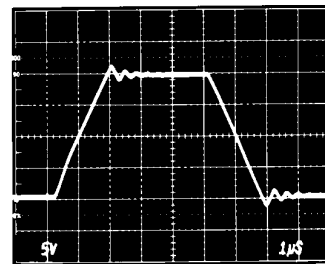
NOTES

¹For supply voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage.

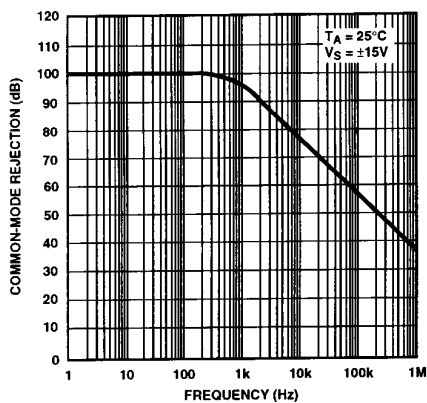
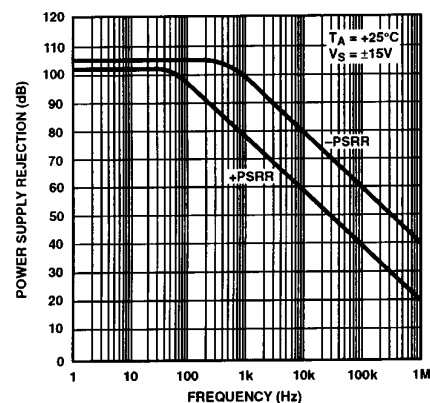
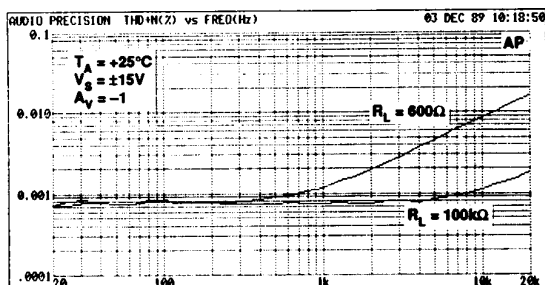
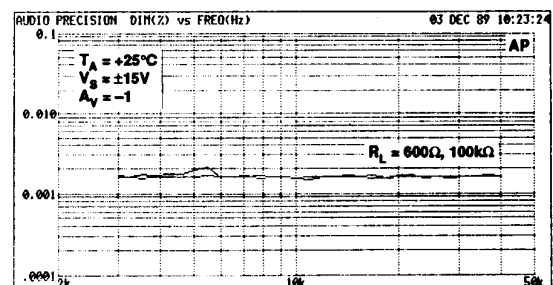
² θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

Typical Performance Characteristics

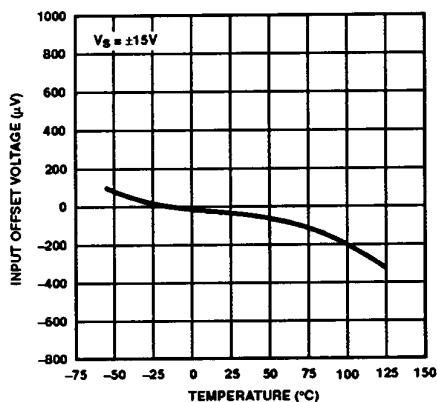
$T_A = +25^{\circ}\text{C}$
 $V_S = \pm 15\text{V}$

Small Signal Transient Response

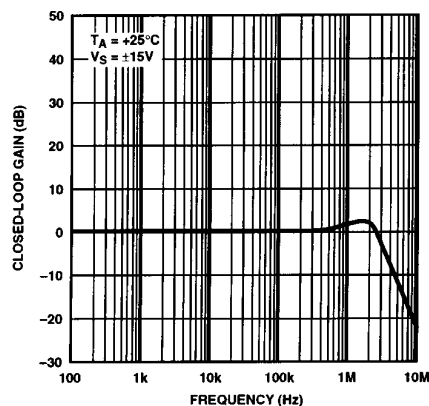
$T_A = +25^{\circ}\text{C}$
 $V_S = \pm 15\text{V}$

Large Signal Transient Response*Common-Mode Rejection vs. Frequency**Power Supply Rejection vs. Frequency**Total Harmonic Distortion vs. Frequency**Dynamic Intermodulation Distortion vs. Frequency*

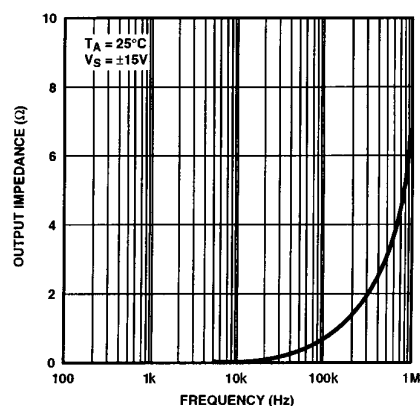
SSM2141—Typical Performance Characteristics



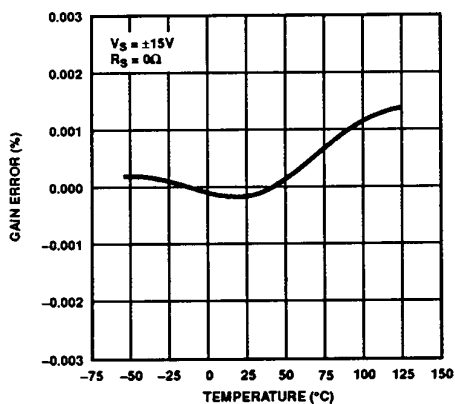
Input Offset Voltage vs. Temperature



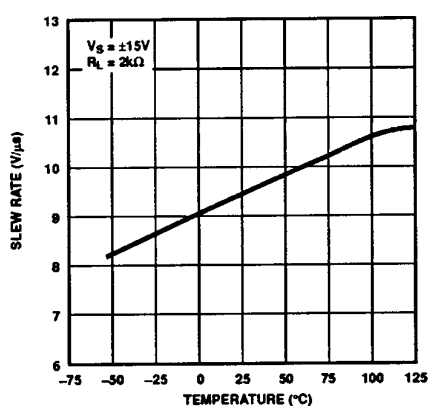
Closed-Loop Gain vs. Frequency



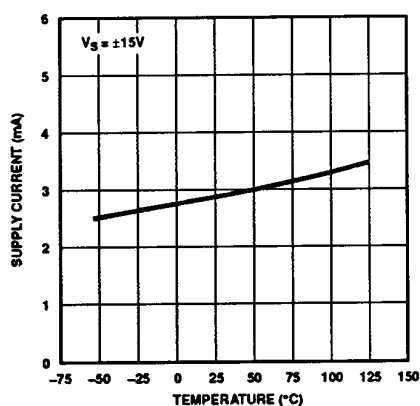
Closed-Loop Output Impedance vs. Frequency



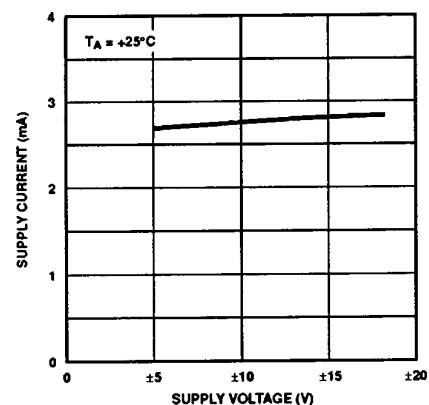
Gain Error vs. Temperature



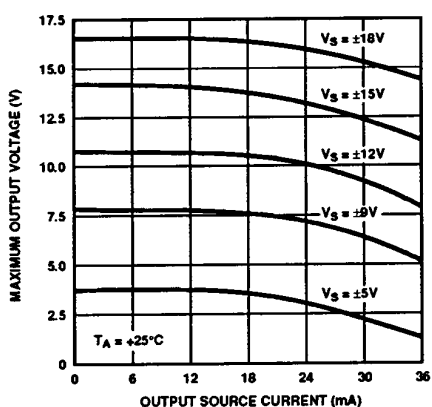
Slew Rate vs. Temperature



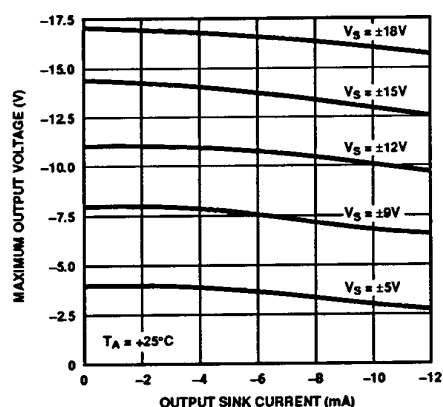
Supply Current vs. Temperature



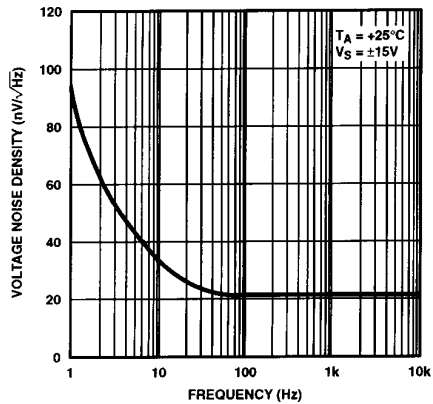
Supply Current vs. Supply Voltage



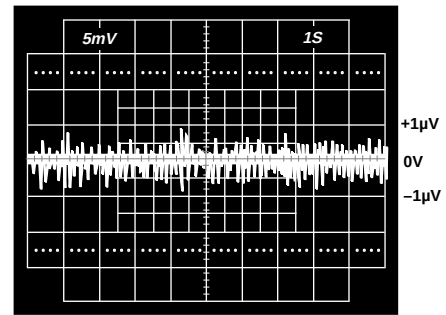
Maximum Output Voltage vs. Output Current (Source)



Maximum Output Voltage vs. Output Current (Sink)

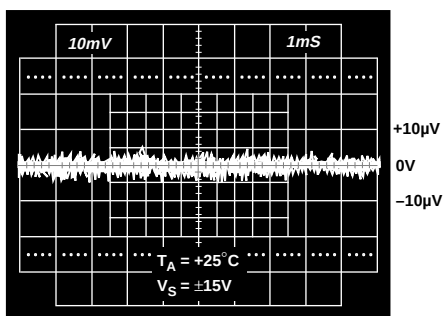


Voltage Noise Density vs. Frequency

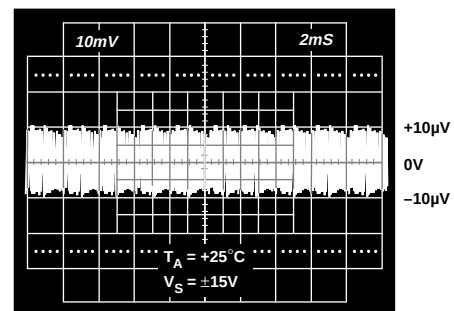


0.1 TO 10Hz PEAK-TO-PEAK NOISE

Low Frequency Voltage Noise

NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

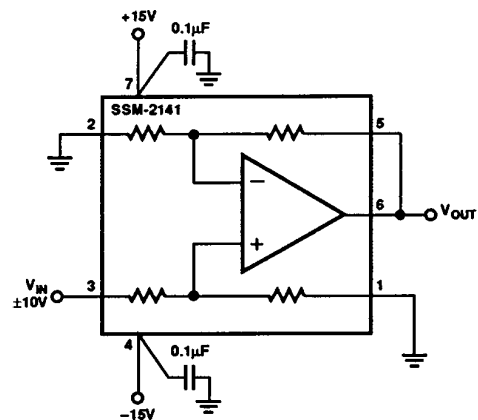
Voltage Noise from 0 kHz to 1 kHz

NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

Voltage Noise from 0 kHz to 10 kHz

APPLICATIONS INFORMATION

The SSM2141 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. For decoupling, place 0.1 μF capacitor located within close proximity from each supply pin to ground.



Slew Rate Test Circuit

SSM2141

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the SSM2141, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR—even a 5 Ω imbalance will degrade CMR by 20 dB. Also, the matching of the reactive source impedance must be matched in order to preserve the CMRR over frequency.

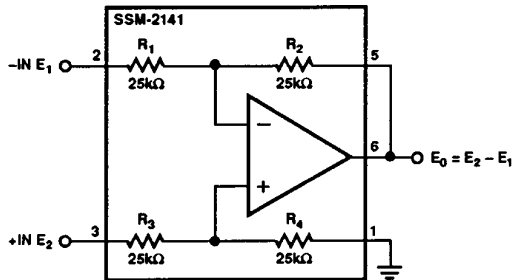


Figure 1. Precision Difference Amplifier. Rejects Common-Mode Signal = $\frac{[E_1 + E_2]}{2}$ by 100 dB

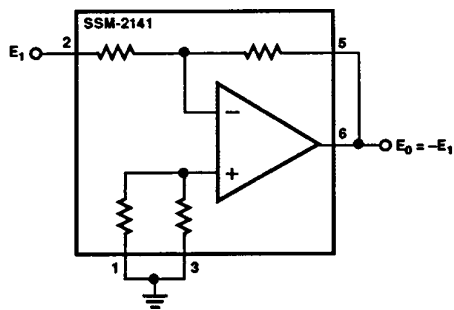


Figure 2. Precision Unity Gain Inverting Amplifier

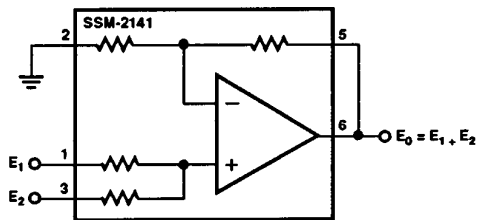


Figure 3. Precision Summing Amplifier

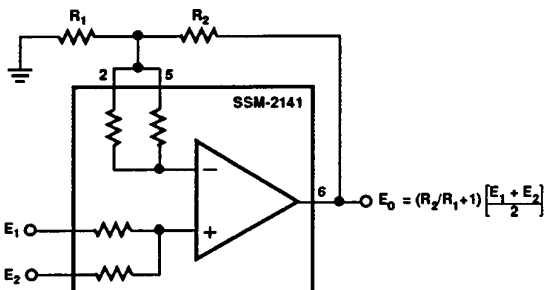


Figure 4. Precision Summing Amplifier with Gain

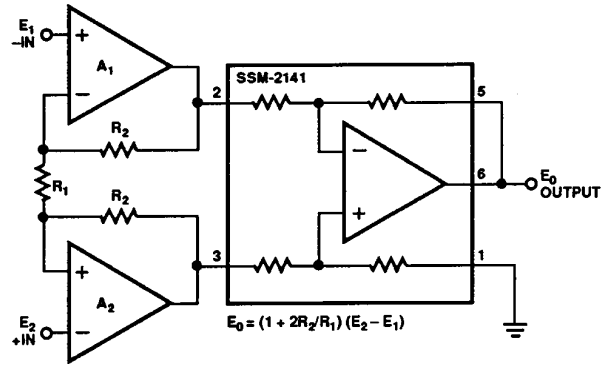
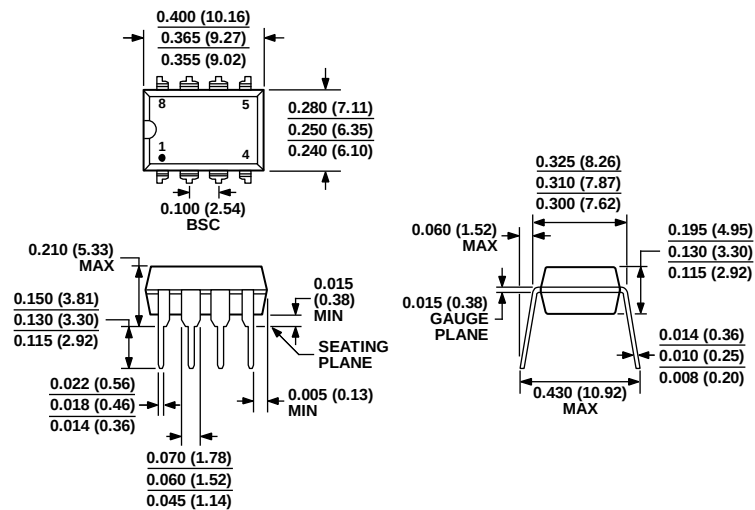


Figure 5. Suitable Instrumentation Amplifier Requirements can be Addressed by Using an Input Stage Consisting of A_1 , A_2 , R_1 and R_2

OUTLINE DIMENSIONS

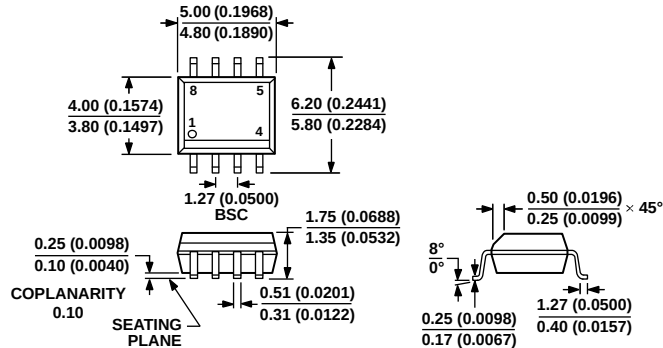


COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 6. 8-Lead Plastic Dual In-Line Package (PDIP)
Narrow Body
(N-8)

Dimensions shown in inches and (millimeters)

070606-A



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 7. 8-Lead Standard Small Outline Package (SOIC_N)
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

012407-A

SSM2141

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
SSM2141PZ	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	8-Lead PDIP	N-8
SSM2141SZ	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	8-Lead SOIC_N	R-8
SSM2141SZ-REEL	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

REVISION HISTORY

6/11—Rev. B to Rev. C

Updated Outline Dimensions 7

Changes to Ordering Guide 8

5/91—Rev. A to Rev. B