Serial-Port, 16-Bit SoundPort Stereo Codec

AD1849

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Multiple Channels of Stereo Input and Output
Digital Signal Mixing
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
44-Lead PLCC Package
Operation from +5 V Supplies
Serial Interface Compatible with ADSP-21xx Fixed Point DSμPs
Pin Compatible with CS4215 (See Text)

PRODUCT OVERVIEW

The Serial-Port AD1849 SoundPort® Stereo Codec integrates the key audio data conversion and control functions into a single integrated circuit. The AD1849 is intended to provide a complete, single-chip audio solution for multimedia applications requiring operation from a single −5 V supply. External signal path circuit requirements are limited to three low tolerance capacitors for line level applications; anti-imaging filters are incorporated on-chip. Dynamic range exceeds 80 dB over the 20 kHz audio band (*K-Grade*). Sample rates from 5.5 kHz to 48 kHz are supported from external crystals, from an external clock, or from the serial interface bit clock.

The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Analog signals can be input at line levels or microphone levels. A software controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The left and right channel 16-bit outputs from the ADCs are available over a single bidirectional serial interface that also supports 16-bit digital input to the DACs and control information. The AD1849 can accept and generate 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantization noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two independent stereo pairs of line-level outputs are generated, as well as drive for a monaural (mono) speaker.

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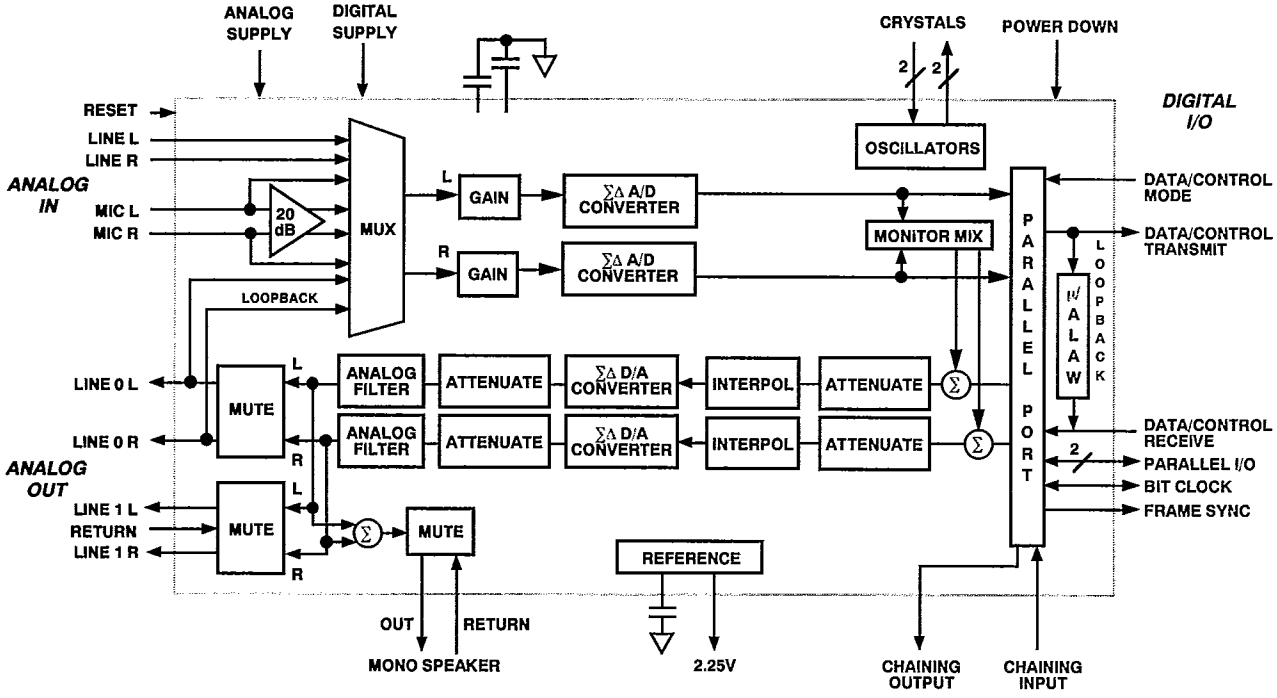
(Continued on page 8)

AD1849K FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD1849—SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Clock (SCLK)	256	F_S
Slave Mode	256 Bits per Frame	
Word Rate (F_S)	48	kHz
Input Signal	1	kHz
Analog Output Passband	20 Hz to 20 kHz	
V_{IH}	2.4	V
V_{IL}	0.8	V
Digital Output Load	100	pF
Analog Output Load	250	pF
External Load Impedance (Line 0 & 1) [*J-Grade*]	10	kΩ
External Load Impedance (Line 0) [*K-Grade*]	10	kΩ
External Load Impedance (Line 1) [*K-Grade*]	48	Ω

DAC Input Conditions
0 dB Attenuation
J-Grade: −2.0 dB Relative to Full Scale
K-Grade: Full Scale Digital Inputs
16-Bit Linear Mode
No Output Resistive Load
Mute Off
Line Out 0

ADC Input Conditions
0 dB PGA Gain
J-Grade: −3.0 dB Relative to Full Scale
K-Grade: −1.0 dB Relative to Full Scale
Line Input
16-Bit Linear Mode

All tests are performed on all ADC and DAC channels.

ANALOG INPUT

	Min	Typ	Max	Units
Input Voltage*				
(RMS Values Assume Sine Wave Input)				
Line and *K-Grade:* Mic with 0 dB Gain	0.88	1.04	1.20	V rms
	2.5	2.94	3.4	V p-p
Mic with +20 dB Gain	0.088	0.104	0.120	V rms
	0.25	0.294	0.34	V p-p
Input Impedance	20k			Ω
Input Capacitance			15	pF

*Accounts for Sum of Worst Case Reference Errors and Worst Case Gain Errors.

PROGRAMMABLE GAIN AMPLIFIER—ADC

	J Grade			K Grade			
	Min	Typ	Max	Min	Typ	Max	Units
Step Size (0 dB to 15 dB) (All Steps Tested, −30 dB Input)	1.1	1.5	1.9	1.3	1.5	1.7	dB
Step Size (16.5 dB to 22.5 dB) (All Steps Tested, −30 dB Input)	0.7	1.5	2.3	1.3	1.5	1.7	dB
PGA Gain Range*							
Line and *K-Grade*: Mic with 0 dB Gain	−0.2		22.7	−0.2		22.7	dB
Mic with +20 dB Gain	19.8		42.7	19.8		42.7	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

	Min	Max	Units
Passband	0	$0.45 \times F_S$	Hz
Passband Ripple		±0.1	dB
Transition Band	$0.45 \times F_S$	$0.55 \times F_S$	Hz
Stopband	$\geq 0.55 \times F_S$		Hz
Stopband Rejection	74		dB
Group Delay		$30/F_S$	
Group Delay Variation Over Passband		0.0	µs

ANALOG DEVICES

AD1849 Rev. 0 Datasheet Errata – June 21, 1993

Two errors have been discovered in the AD1849 Rev. 0 datasheet which require correction.

- The "Phantom-Powered" Microphone Input Circuit shown in Figure 12 is incorrect. The original figure omitted two important 0.33 µF ac coupling capacitors between the final op amp stage output and the AD1849 input pins. The corrected Figure 12 is shown below:

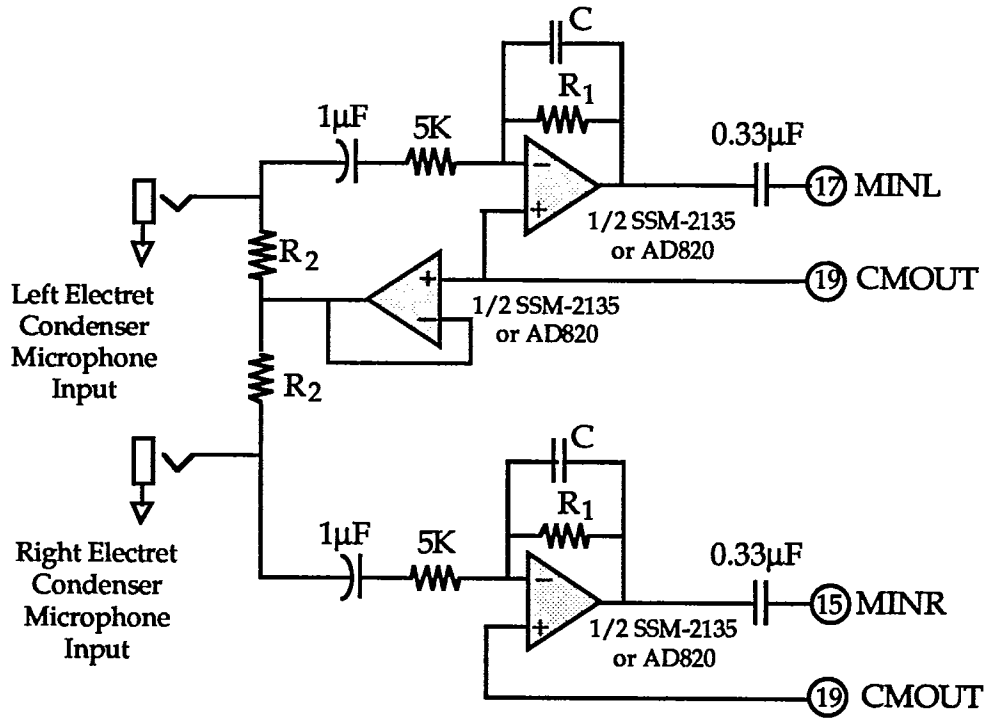


Figure 12. AD1849 "Phantom-Powered" Microphone Input Circuit

- The second error is on page 8 and page 23. The external signal-path filtering capacitor values given in the text in the third paragraph of the left hand column on page 8 and in the paragraph between Figure 17 and Figure 18 on page 23 are not consistent with Figure 18. Figure 18 is correct. The text should state that the *K-Grade* AD1849 must use 1 µF signal-path filtering capacitors.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/821-4273

ANALOG-TO-DIGITAL CONVERTERS

	J Grade			K Grade			
	Min	Typ	Max	Min	Typ	Max	Units
Resolution (No Missing Codes from ±10 LSB Ramp Around Midscale)*		16			16		Bits
ADC Dynamic Range, Line and Mic 0 dB Gain (−60 dB Input, THD+N Referenced to Full Scale)	74	80		80	85		dB
ADC Dynamic Range, Mic with −20 dB Gain (−60 dB Input, THD−N Referenced to Full Scale)	68	77		72	82		dB
ADC THD−N (Referenced to Full Scale, Line and Mic)		0.022	0.056		0.014	0.02	%
		−73	−65		−77	−74	dB
Signal-to-Intermodulation Distortion* (−1 dB Input, Tones at 140 Hz and 984 Hz, Referenced to Full Scale)		75			75		dB
ADC Crosstalk							
Line to Line (Input L, Ground R, Read R; Input R, Ground L, Read L)			−72			−80	dB
Line to Mic (Input LINL&R, Ground and Select MINL&R, Read Both Channels)			−56			−60	dB
Gain Error (Full Scale Span Relative to Nominal)			5			5	%
Gain Drift*		100			100		ppm/°C
ADC Interchannel Gain Mismatch (Line and Mic) (Difference of Gain Errors)			0.5			0.3	dB

DIGITAL-TO-ANALOG CONVERTERS

	J Grade			K Grade			
	Min	Typ	Max	Min	Typ	Max	Units
Resolution*		16			16		Bits
DAC Dynamic Range (−60 dB Input, THD−N Referenced to Full Scale, A-Weight Filter)	78	83		80	85		dB
DAC THD+N (Referenced to Full Scale)							
Line 0 and 1, *J-Grade* or		0.016	0.025		0.016	0.025	%
K-Grade with OLB = 1		−76	−72		−76	−72	dB
Mono Speaker, *J-Grade* (Input −5 dB Relative to Full Scale) or *K-Grade* (Input Full Scale) with OLB = 1, and 48 Ω load*	0.063			0.063			%
	−64			−64			dB
Signal-to-Intermodulation Distortion* (−1 dB Input, Tones at 140 Hz and 984 Hz, Referenced to Full Scale)		89			89		dB
DAC Crosstalk (Input L, Zero R, Measure LOUT0R & 1R; Input R, Zero L, Measure LOUT0L & 1L)			−80			−80	dB
Gain Error (Full Scale Span Relative to Nominal)			5			5	%
Gain Drift*		100			100		ppm/°C
DAC Interchannel Gain Mismatch (Line 0 and 1) (Difference of Gain Errors)			0.5			0.3	dB
Total Out-of-Band Energy* (Measured from 0.55 × F_S to 100 kHz)			−45			−60	dB

*Characterized, not tested.

AD1849

DAC ATTENUATOR

	J Grade			K Grade			
	Min	Typ	Max	Min	Typ	Max	Units
Step Size (0.0 dB to −60 dB) (Tested at Steps −1.5 dB, −19.5 dB, −39 dB and −60 dB)	1.3	1.5	1.7	1.3	1.5	1.7	dB
Step Size (−61.5 dB to −94.5 dB)*	1.0	1.5	2.0	1.0	1.5	2.0	dB
Output Attenuation*	−95		0.2	−95		0.2	dB

SYSTEM SPECIFICATIONS

	J Grade			K Grade			
	Min	Typ	Max	Min	Typ	Max	Units
System Frequency Response* (Line In to Line Out, 0 to 0.45 × F_S)	−1.0		+0.4	−0.5		+0.2	dB
Differential Nonlinearity*			±1			±0.9	LSB
Phase Linearity Deviation*			5			5	Degrees

ANALOG OUTPUT

	Min	Typ	Max	Units
Full Scale Output Voltage (Line 0 & 1)		0.707		V rms
[*J-Grade* or *K-Grade* with OLB = 1]	1.85	2.0	2.1	V p-p
Full Scale Output Voltage (Line 0)		1.0		V rms
[*K-Grade* with OLB = 0]		2.8		V p-p
Full Scale Output Voltage (Line 1) [*K-Grade* with OLB = 0]		4.0		V p-p
Full Scale Output Voltage (Mono Speaker) [*J-Grade* or *K-Grade* with OLB = 1]		4.0		V p-p
Full Scale Output Voltage (Mono Speaker) [*K-Grade* with OLB = 0]		8.0		V p-p
CMOUT Voltage	2.00	2.25	2.50	V
CMOUT Current Drive*		100		µA
Mute Attenuation of 0 dB Fundamental* (LINE 0, 1, & MONO)			−80	dB

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.4	(V_{DD}+) + 0.3	V
XTAL1/2I	2.4	(V_{DD}+) + 0.3	V
Low Level Input Voltage (V_{IL})	−0.3	0.8	V
High Level Output Voltage (V_{OH}) at I_{OH} = −2 mA	2.4		V
Low Level Output Voltage (V_{OL}) at I_{OL} = 2 mA		0.4	V
Input Leakage Current (GO/NOGO Tested)	−10	10	µA
Output Leakage Current (GO/NOGO Tested)	−10	10	µA

DIGITAL TIMING PARAMETERS

	Min	Typ	Max	Units
SCLK Period (t_{CLK})				
Slave Mode, MS = 0	80			ns
Master Mode, MS = 1*		1/(F_S × Bits per Frame)		s
SCLK HI (t_{HI})*				
Slave Mode, MS = 0	25			ns
SCLK LO (t_{LO})*				
Slave Mode, MS = 0	25			ns
CLKIN Frequency			13.5	MHz
CLKIN HI	30			ns
CLKIN LO	30			ns
Input Setup Time (t_S)	15			ns
Input Hold Time (t_{IH})	10			ns
Output Delay (t_D)			20	ns
Output Hold Time (t_{OH})	0			ns
Output Hi-Z to Valid (t_{ZV})	15			ns
Output Valid to Hi-Z (t_{VZ})			12	ns
Power Up $\overline{\text{RESET}}$ LO Time	50			ms
Operating $\overline{\text{RESET}}$ LO Time	100			ns

POWER SUPPLY

	Min	Max	Units
Power Supply Voltage Range* —Digital and Analog	4.75	5.25	V
Power Supply Current—Operating (With 50 Ω Mono Speaker Load)		190	mA
Power Supply Current—Operating* (Without Mono Speaker Load, *K-Grade* only)		100	mA
Analog Supply Current—Operating		120	mA
Digital Supply Current—Operating		70	mA
Digital Power Supply Current—Power Down *K-Grade*		1	mA
Analog Power Supply Current—Power Down *K-Grade*		1	mA
Power Supply Rejection (@ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)	40		dB

CLOCK SPECIFICATIONS*

	Min	Max	Units
Input Clock Frequency, Crystals		27	MHz
Clock Duty Cycle Tolerance		±10	%
Sample Rate (F_S)	5.5125	50	kHz

*Characterized, not tested

Specifications subject to change without notice.

AD1849

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	−0.3	6.0	V
Analog (V_{CC})	−0.3	6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	−0.3	(V_{CC}+) + 0.3	V
Digital Input Voltage (Signal Pins)	−0.3	(V_{DD}+) + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	−65	+150	°C
ESD Tolerance (Human Body Model per Method 3015.2 of MIL-STD-883B)	1000		V

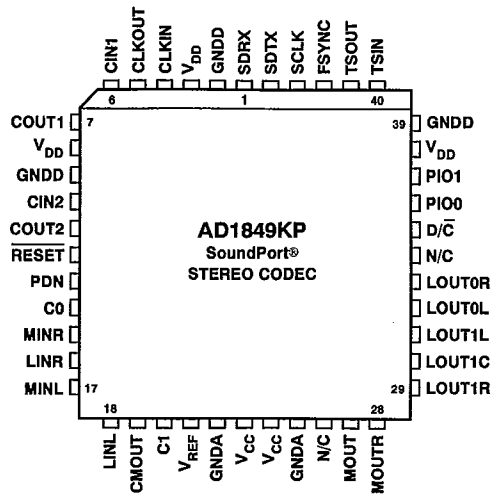
WARNING: CMOS device. May be susceptible to high voltage transient-induced latchup.

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package
AD1849JP	0°C to +70°C	44-Lead PLCC
AD1849KP	0°C to +70°C	44-Lead PLCC

44-Lead Plastic Leaded Chip Carrier Pinout



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1849 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

Digital Signals

Pin Name	Number	I/O	Description
SDRX	1	I	Receive Serial Data Pin
SDTX	44	O	Transmit Serial Data Pin
SCLK	43	I/O	Bidirectional Serial Bit Clock
FSYNC	42	O	Frame Sync Output Signal
TSOUT	41	O	Chaining Word Output
TSIN	40	I	Chaining Word Input
D/$\overline{C}$	35	I	Data/Control Select Input
CIN1	6	I	Crystal 1 Input
COUT1	7	O	Crystal 1 Output
CIN2	10	I	Crystal 2 Input
COUT2	11	O	Crystal 2 Output
CLKIN	4	I	External Sample Clock Input (256 × F_S)
CLKOUT	5	O	External Sample Clock Output (256 × F_S)
PDN	13	I	Power Down Input (Active HI)
$\overline{RESET}$	12	I	Reset Input (Active LO)
PIO1	37	I/O	Parallel Input/Output Bit 1
PIO0	36	I/O	Parallel Input/Output Bit 0

Analog Signals

Pin Name	Number	I/O	Description
LINL	18	I	Left Channel Line Input
LINR	16	I	Right Channel Line Input
MINL	17	I	*J-Grade*: Left Channel Microphone Input (−20 dB from Line Level) *K-Grade*: Left Channel Microphone Input (−20 dB from Line Level if MB = 0 or Line Level if MB = 1)
MINR	15	I	*J-Grade*: Right Channel Microphone Input (−20 dB from Line Level) *K-Grade*: Right Channel Microphone Input (−20 dB from Line Level if MB = 0 or Line Level if MB = 1)
LOUT0L	32	O	Left Channel Line Output 0
LOUT0R	33	O	Right Channel Line Output 0
LOUT1L	31	O	Left Channel Line Output 1
LOUT1R	29	O	Right Channel Line Output 1
LOUT1C	30	I	*J-Grade*: No Connect (Do Not Connect) *K-Grade*: Common Return Path for Large Current from External Headphones
MOUT	27	O	Mono Speaker Output
MOUTR	28	I	Mono Speaker Output Return
C0	14	O	*J-Grade*: External 1,000 pF Capacitor (±10%, NPO) Connection *K-Grade*: External 0.1 µF Capacitor (±10%) Connection
C1	20	O	*J-Grade*: External 1,000 pF Capacitor (±10%, NPO) Connection *K-Grade*: External 0.1 µF Capacitor (±10%) Connection
N/C	26		No Connect (Do Not Connect)
N/C	34		No Connect (Do Not Connect)
V_{REF}	21	O	Voltage Reference (Connect to Bypass Capacitor)
CMOUT	19	O	Common Mode Reference Datum Output (Nominally 2.25 V)

Power Supplies

Pin Name	Number	I/O	Description
V_{CC}	23 & 24	I	Analog Supply Voltage (+5 V)
GNDA	22 & 25	I	Analog Ground
V_{DD}	3, 8, 38	I	Digital Supply Voltage (+5 V)
GNDD	2, 9, 39	I	Digital Ground

(Continued from page 1)

J-GRADES AND K-GRADES

The AD1849JP is released to production manufacturing. The AD1849KP is scheduled for mid-1993 sampling and production in the third calendar quarter of 1993. The AD1849KP is a pin-compatible function and performance enhanced version of the AD1849JP. Analog Devices intends to eventually obsolete the AD1849JP, replacing it with the superior AD1849KP.

There are, however, several minor differences between the *J-Grade* and *K-Grade* parts that require advance planning. The versions can be distinguished externally by brand and internally by reading the Revision ID field in the control registers.

Most important, the *K-Grade* requires a pair of 0.1 μF external filter capacitors where the *J-Grade* requires 1000 pF NPO capacitors. Neither version will function properly with the wrong capacitors.

In general, the *K-Grade* removes virtually all the differences between the AD1849 and the CS4215. The *J-Grade* autocalibrates on the Control-to-Data mode transition only if the autocalibration bit (AC Bit 56 in the Control Mode control register) is set. The *K-Grade* will always autocalibrate on the Control-to-Data mode transition. The autocalibration bit is ignored, and the autocalibration sequence is 194 FSYNC frames in duration. The *K-Grade* will include an Output Level Bit (OLB) in the Control Mode control register (Bit 59) which will allow two selections for the line, headphone and speaker full scale output levels. The line 1 output will drive a 48 Ω load. The *K-Grade* has been modified to remove the requirement for a slow clock during Control Mode setup. The *K-Grade* adds an Immediate Three-State (ITS) bit in the Control Mode control register (Bit 47) which causes SCLK and FSYNC to be three-stated immediately when D/$\overline{C}$ goes LO. On the *K-Grade* a mic bypass path around the +20 dB fixed gain block has been added. The *K-Grade* adds a function on Pin 30 called LOUT1C which is a common return line biased up to the CMOUT voltage for large return current from external headphones. The *J-Grade* and the *K-Grade* define digital loopback mode differently. The *K-Grade*'s DCB handshaking has been generalized to simplify system implementation. See the text below for more details.

FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1849 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1849 SoundPort Stereo Codec accepts stereo line-level and mic-level inputs. These inputs are internally buffered to protect the user from driving a switched-capacitor load. These buffers eliminate the need for active front-end conditioning circuitry. These analog stereo signals are multiplexed to the internal programmable gain amplifier (PGA) stage. The mic inputs can be amplified by +20 dB prior to the PGA to compensate for the voltage swing difference between line levels and typical condenser microphones. On the *K-Grade*, the mic inputs can bypass the +20 dB fixed gain block and go straight to the input multiplexer, which often results in an improved system signal-to-noise ratio.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left-channel inputs appearing at both channel outputs.

Analog-to-Digital Datapath

The ΣΔ ADCs incorporate a proprietary fourth-order modulator similar to that used in the AD1879 18-Bit ΣΔ Stereo ADC. A single pole of passive filtering is all that is required for anti-aliasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include linear-phase digital decimation filters that low-pass filter the input to 0.45 × F_S ("F_S" is the word rate or "sampling frequency"). ADC input overrange conditions will cause a sticky bit to be set that can be read.

Digital-to-Analog Datapath

The ΣΔ DACs are preceded by a programmable attenuator and a low-pass digital interpolation filter. The attenuator allows independent control of each DAC channel from 0 dB to −94.5 dB in 1.5 dB steps plus full digital mute. The anti-imaging interpolation filter oversamples by 64 and digitally filters the higher frequency images. The DACs' ΣΔ noise shapers also oversample by 64 and convert the signal to a single-bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output, including both images at the oversampling rate and shaped quantization noise. No external components are required. Phase linearity at the analog output is achieved by internally compensating for the group delay variation of the analog output filters.

Attenuation settings are specified by control bits in the data stream. Changes in DAC output level take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 10.7 milliseconds at a 48 kHz sampling rate and 64 milliseconds at an 8 kHz sampling rate (Time-out [ms] ≈ 512/Sampling Rate [kHz]).

Monitor Mix

A monitor mix is supported that digitally mixes a portion of the digitized analog input with the analog output (prior to digitization). The digital output from the ADCs going out of the serial data port is unaffected by the monitor mix. Along the monitor mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally the AD1849 always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixteen steps of –6 dB attenuation are supported to –94.5 dB. A "0" implies no attenuation, while a "14" implies 84 dB of attenuation. Specifying full scale "15" completely mutes the monitor datapath, preventing any mixing of the analog input with the digital input. Note that the level of the mixed output signal is also a function of the input PGA settings since they affect the ADCs' output.

The attenuated monitor data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around.

Analog Outputs

Two stereo line-level outputs and one monaural (mono) speaker output are available at external pins. Each of these outputs can be independently muted. Muting either line-level stereo output mutes both left and right channels of that output. When muted, the outputs will settle to a dc value near CMOUT, the midscale reference voltage. The mono speaker output is differential. The chip can operate either in a global stereo mode or in a global mono mode with left channel inputs appearing at both outputs.

Digital Data Types

The AD1849 supports three global data types: 16-bit twos-complement linear PCM, 8-bit companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all three formats is always transferred MSB first. Sixteen-bit linear data output from the ADCs and input to the DACs is in twos-complement format. Eight-bit data is always left-justified in 16-bit fields; said in other words, the MSBs of all data types are always aligned; in yet other words, full scale representations in all three formats correspond to equivalent full scale signals. The eight least-significant bit positions of 8-bit companded data in 16-bit fields are ignored on input and zeroed on output.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use nonlinear coding with less precision for large-amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified in the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits, see Figure 1.

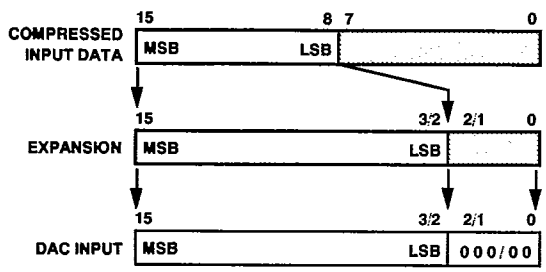


Figure 1. A-Law or μ-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified prior to output. See Figure 2.

Note that all format conversions take place at input or output. Internally, the AD1849 always uses 16-bit linear PCM representations to maintain maximum precision.

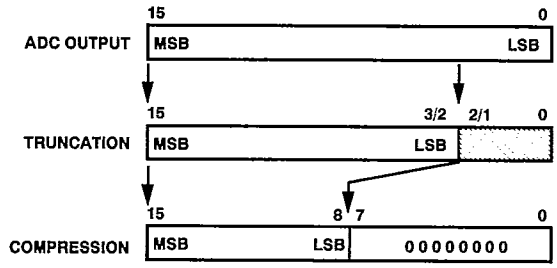


Figure 2. A-Law or μ-Law Compression

Power Supplies and Voltage Reference

The AD1849 operates from +5 V power supplies. Independent analog and digital supplies are recommended for optimal performance, though excellent results can be obtained in single-supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (CMOUT). The reference output can be used for biasing op amps used in dc coupling. The internal reference is externally bypassed to analog ground at the V_{REF} pin. Note that V_{REF} should only be connected to its bypass capacitors.

Autocalibration

The AD1849 supports an autocalibration sequence to eliminate DAC and ADC offsets.

J-Grade: The autocalibration sequence is initiated in the transition from Control Mode to Data Mode if the autocalibration bit (AC, Control Word Bit 56) has been set. (See "Serial Interface" below for more information on Data and Control Modes.) Settings such as source select, gain, and attenuation should be held constant for the 256 frames required for proper autocalibration. (The first four frames of Data Mode input can be changing, however.) The user should specify that analog outputs be muted to prevent undesired outputs. Do not specify any monitor mix during autocalibration, i.e., monitor mix should be muted.

K-Grade: The autocalibration sequence is initiated in the transition from Control Mode to Data Mode, regardless of the state of the AC bit. Settings such as source select, gain, and attenuation should be held constant for the first five of the 194 frames required for proper autocalibration. The AD1849 will sample the Control Word settings presented on the fifth frame after Data Mode is entered. Any changes to the settings after the fifth frame will be locked out for the duration of the 194 frames. Control Word changes made after the fifth frame will be echoed by the Codec, but they will not affect the autocalibration sequence. The user should specify that analog outputs be muted to prevent undesired outputs. Monitor mix will be automatically disabled by the Codec.

During the autocalibration sequence, the serial data output from the ADCs is meaningless. Serial data inputs to the DACs are ignored. Even if the user specified the muting of all analog outputs, near the end of the autocalibration sequence, dc analog outputs very close to CMOUT will be produced at the line outputs and mono speaker output.

An autocalibration sequence is also performed when the AD1849 leaves the reset state (i.e., $\overline{\text{RESET}}$ goes HI). The $\overline{\text{RESET}}$ pin should be held LO for 50 ms after power up or after leaving power-down mode to delay the onset of the autocalibration sequence until after the voltage reference has settled.

AD1849

Loopback

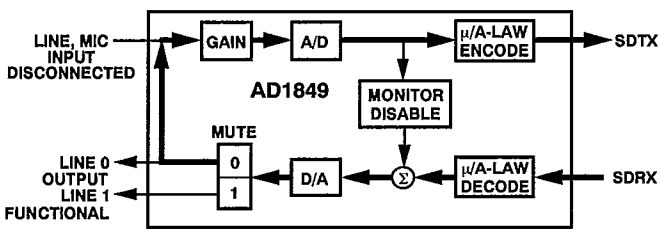
Digital and analog loopback modes are supported for device and system testing. The monitor mix datapath is always available for loopback test purposes. Additional loopback tests are enabled by setting the ENL bit (Control Word Bit 33) to a "1."

Analog loopback mode D-A-D is enabled by setting the ADL bit (Control Word Bit 32) to a "1" when ENL is a "1." In this mode, the DACs' analog outputs are re-input to the PGAs prior to the ADCs, allowing digital inputs to be compared to digital outputs. The monitor mix will be automatically disabled by the Codec during D-A-D loopback. The analog outputs can be individually attenuated, and the analog inputs are internally disconnected. Note that muting the line 0 output mutes the looped-back signal in this mode. The *J-Grade* analog loopback mode D-A-D is equivalent to the *K-Grade* analog loopback mode D-A-D.

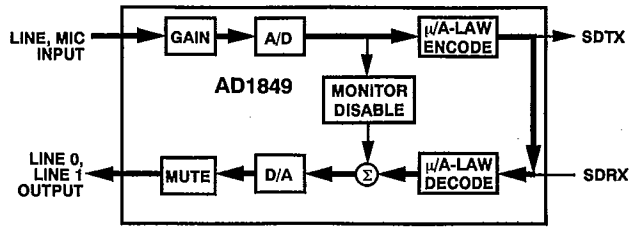
J-Grade: Digital loopback mode A-D-A is enabled by resetting the ADL bit (Control Word Bit 32) to a "0" when ENL is a "1." The ADCs' outputs are passed directly to the DACs' inputs, allowing analog inputs to be compared with analog outputs. (This feature is in addition to the monitor mix described above.) Note that, unlike the monitor datapath, the digital loopback datapath passes through the μ/A-law companding circuitry. The monitor mix must be disabled (MA3:0 = "1111") during A-D-A loopback. If companding is selected, the linear ADCs' output will be compressed and then expanded before input to the DACs. DAC inputs are ignored for the duration of this test.

K-Grade: Digital loopback mode D-D is enabled by resetting the ADL bit (Control Word Bit 32) to a "0" when ENL is a "1." In this mode, the control and data bit pattern presented on the SDRX pin is echoed on the SDTX pin with a one frame delay, allowing the host controller to verify the integrity of the serial interface. During digital loopback mode, the output DACs are operational. Note that *J-Grade* loopback mode A-D-A can be emulated by using the monitor mix datapath, with the monitor mix set for no attenuation (MA3:0 = "0000"). The ENL bit would be reset to a "0" for this emulation. The host or external controller should write zeros to the DACs for the duration of this test.

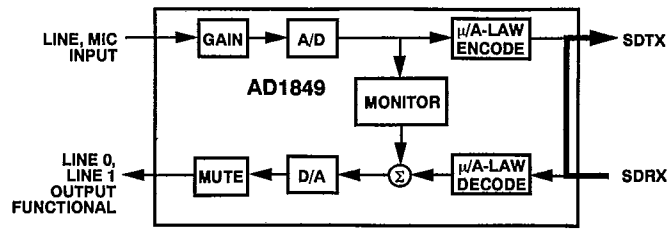
The loopback modes are shown graphically in Figure 3.



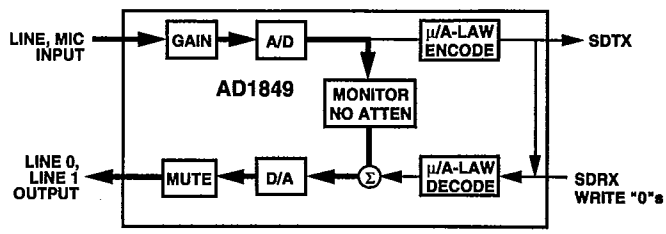
AD1849 Analog Loopback D-A-D



AD1849 J-Grade Digital Loopback A-D-A



AD1849 K-Grade Digital Loopback D-D



AD1849 K-Grade Emulated Digital Loopback A-D-A

Figure 3. AD1849 Loopback Modes

Clocks and Sample Rates

The AD1849 can operate from external crystals, from a 256 × F_S input clock, or from the serial port's bit clock (at 256 × F_S), selected under software control. Two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1849, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them the following sample rates can be internally generated: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz. Regardless of clock input source, a clock output of 256 × F_S is generated (with some skew). If an external input clock or the serial port's bit clocks are selected to drive the AD1849's internal operation, they should be low jitter clocks. If no external clock will be used, Analog Devices recommends tying the clock input pin (CLKIN) to ground. If either external crystal is not used, Analog Devices recommends tying its input (CIN1 and/or CIN2) to ground.

CONTROL REGISTERS

The AD1849 SoundPort Stereo Codec accepts control information through its serial port when in Control Mode. Some control information is also embedded in the data stream when in Data Mode. (See Figure 8.) Control bits can also be read back for system verification. Operation of the AD1849 is determined by the state of these control bits. The 64-bit serial Control Mode and Data Mode control registers have been arbitrarily broken down into bytes for ease of description. All control bits set to default states after $\overline{\text{RESET}}$ or Power Down. Those control bits that cannot be changed in Control Mode are set to defaults on the transition from Data Mode to Control Mode. See below for a definition of these defaults.

Control Mode Control Registers

Control Byte 1, Status Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	1	MB	OLB	DCB	0	AC
63	62	61	60	59	58	57	56

MB Mic bypass.

J-Grade: This bit should always be written "0," and always reads "0."

K-Grade: Mic bypass.

0 Mic inputs applied to +20 dB fixed gain block.

1 Mic inputs bypass +20 dB fixed gain block.

OLB Output level bit.

J-Grade: This bit should always be written "0," and always reads "0."

K-Grade: Output level bit. (Note that the *J-Grade* levels are always 2.0 V p-p, 2.0 V p-p, and 4.0 V p-p for line 0, line 1 and mono speaker, respectively.)

0 Full scale line 0 output is 2.8 V p-p (1 V rms).
Full scale line 1 output is 4.0 V p-p.
Full scale mono speaker output is 8.0 V p-p.

1 Full scale line 0 output is 2.0 V p-p.
Full scale line 1 output is 2.0 V p-p.
Full scale mono speaker output is 4.0 V p-p.

DCB Data/control bit. Used for handshaking in data/control transitions. See "DCB Handshake Protocol."

AC Autocalibration.

J-Grade: Writing "1" will allow an autocalibration sequence to take place when D/$\overline{\text{C}}$ goes HI, i.e., when going from Control Mode to Data Mode. Autocalibration requires an interval of 256 frames. Offsets for all channels of ADC and DAC are zeroed. For the ADC, the autocalibration is performed on the currently selected (or default) input channels at the currently selected gains and attenuations. After the first four frames, these settings should not be allowed to change during the remaining 256 frames required for the autocalibration. The user should specify that analog outputs are muted to prevent undesired outputs, i.e., OM0="0," OM1="0," and SM="0." Monitor mix must be muted, i.e., MA="15."

K-Grade: Autocalibration will always occur on the Control-to-Data mode transition. The AC bit is ignored. Autocalibration requires an interval of 194 frames. Offsets for all channels of ADC and DAC are zeroed. For the ADC, the autocalibration is performed on the currently selected (or default) input channels at the currently selected gains and attenuations. Desired settings must be selected during the first five frames; the settings in frame five are sampled and retained and subsequent changes to these settings are locked out for the duration of the 194 frames required for autocalibration. The user should specify that analog outputs are muted to prevent undesired outputs, i.e., OM0="0," OM1="0," and SM="0." Monitor mix will be automatically disabled by the Codec.

Control Byte 2, Data Format Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	DFR2	DFR1	DFR0	ST	DF1	DF0
55	54	53	52	51	50	49	48

DFR2:0 Data conversion frequency (F_S) select (in kHz):

DFR	Divide Factor	XTAL1 (24.576 MHz)	XTAL2 (16.9344 MHz)
0	3072	8	5.5125
1	1536	16	11.025
2	896	27.42857	18.9
3	768	32	22.05
4	448	N/A	37.8
5	384	N/A	44.1
6	512	48	33.075
7	2560	9.6	6.615

Note that the AD1849's internal oscillators can be overdriven by external clock sources at the crystal input pins. If an external clock source is used, it should be applied to the crystal input pin (CIN1 or CIN2), and the crystal output pin (COUT1 or COUT2) should be left unconnected. The external clock source need not be at the recommended crystal frequencies, and it will be divided down by the selected Divide Factor.

ST Global stereo mode. Both converters are placed in the same mode.
- 0 Mono mode. The left analog input appears at both ADC outputs. The left digital input appears at both DAC outputs
- 1 Stereo mode

DF1:0 Codec data format selection
- 0 16-bit twos-complement PCM linear
- 1 8-bit μ-law companded
- 2 8-bit A-law companded
- 3 reserved

Control Byte 3, Serial Port Control Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
ITS	0	MCK1	MCK0	FSEL1	FSEL0	MS	TXDIS
47	46	45	44	43	42	41	40

ITS Immediate three-state.
J-Grade: This bit should always be written "0," and always reads "0."
K-Grade: Immediate three-state. (Note that the *J-Grade* always three-states within 3 cycles.)
- 0 FSYNC, SDTX and SCLK three-state within 3 SCLK cycles after D/$\overline{C}$ goes LO
- 1 FSYNC, SDTX and SCLK three-state immediately after D/$\overline{C}$ goes LO

MCK1:0 Clock source select for Codec internal operation:
- 0 Serial bit clock (SCLK) is the master clock at 256 × F_S
- 1 24.576 MHz crystal (XTAL1) is the clock source
- 2 16.9344 MHz crystal (XTAL2) is the clock source
- 3 External clock (CLKIN) is the clock source at 256 × F_S

FSEL1:0 Frame size select
- 0 64 bits per frame
- 1 128 bits per frame
- 2 256 bits per frame
- 3 Reserved

Note that FSEL is overridden in Data Mode when SCLK is the clock source (MCK ="0"). When SCLK is providing the 256 × F_S clock for internal Codec operation, 256 bits per frame is effectively selected, regardless of FSEL's contents.

MS Master/slave mode for the serial interface:
- 0 Receive serial clock (SCLK) and TSIN from an external device ("slave mode")
- 1 Transmit serial clock (SCLK) and frame sync (FSYNC) to external devices ("master mode")

Note that MS is overridden when SCLK is the clock source (MCK = "0"). When SCLK is providing the clock for internal Codec operation, slave mode is effectively selected, regardless of the contents of MS.

TXDIS Transmitter disable:
- 0 Enable serial output
- 1 Three-state serial data output (high impedance)

Note that Control Mode overrides TXDIS. In Control Mode, the serial output is always enabled.

Control Byte 4, Test Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	0	0	0	0	ENL	ADL
39	38	37	36	35	34	33	32

ENL Enable loopback testing
- 0 Disabled
- 1 Enabled

ADL Loopback mode
- 0 Digital loopback. (Note that the *K-Grade* A-D-A loopback is accomplished through the monitor mix datapath.)
  J-Grade: From ADCs' output to DACs' input (A-D-A)
  K-Grade: From Data/Control receive to Data/Control transmit (D-D)
- 1 Analog loopback from DACs to ADCs (D-A-D)

Control Byte 5, Parallel Port Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
PIO1	PIO0	0	0	0	0	0	0
31	30	29	28	27	26	25	24

PIO1:0 Parallel I/O bits for system signaling. PIO bits do not affect Codec operation.

Control Byte 6, Reserved Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16

Reserved bits should be written as 0.

Control Byte 7, Revision Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	1	0	REVID3	REVID2	REVID1	REVID0
15	14	13	12	11	10	9	8

REVID3:0 Silicon revision identification. Reads less than or equal to 0001 (i.e., 0000 or 0001) for the AD1849 *J-Grade* and greater than or equal to 0010 (i.e., 0010, 0011, etc.) for the AD1849 *K-Grade*.

Control Byte 8, Reserved Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0

Reserved bits should be written as 0.

Data Mode Data and Control Registers

Data Byte 1, Left Audio Data—Most Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
L15	L14	L13	L12	L11	L10	L9	L8
63	62	61	60	59	58	57	56

In 16-bit linear PCM mode, this byte contains the upper eight bits of the left audio data sample. In the 8-bit companded modes, this byte contains the left audio data sample. In mono mode, only the left audio data is used. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 2, Left Audio Data—Least Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
L7	L6	L5	L4	L3	L2	L1	L0
55	54	53	52	51	50	49	48

In 16-bit linear PCM mode, this byte contains the lower eight bits of the left audio data sample. In the 8-bit companded modes, this byte is ignored on input, zeroed on output. In mono mode, only the left audio data is used. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 3, Right Audio Data—Most Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
R15	R14	R13	R12	R11	R10	R9	R8
47	46	45	44	43	42	41	40

In 16-bit linear PCM mode, this byte contains the upper eight bits of the right audio data sample. In the 8-bit companded modes, this byte contains the right audio data sample. In mono mode, this byte is ignored on input, zeroed on output. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 4, Right Audio Data—Least Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
R7	R6	R5	R4	R3	R2	R1	R0
39	38	37	36	35	34	33	32

In 16-bit linear PCM mode, this byte contains the lower eight bits of the right audio data sample. In the 8-bit companded modes, this byte is not used. In mono mode, this byte is ignored on input, zeroed on output. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 5, Output Setting Register 1

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
OM1	OM0	LO5	LO4	LO3	LO2	LO1	LO0
31	30	29	28	27	26	25	24

OM1 Output Line 1 Analog Mute.
- 0 Mute Line 1
- 1 Line 1 on

OM0 Output Line 0 Analog Mute.
- 0 Mute Line 0
- 1 Line 0 on

LO5:0 Output attenuation setting for the left DAC channel; "0" represents no attenuation. Step size is 1.5 dB; "62" represents 93 dB of attenuation. Attenuation = 1.5 dB × LO, except for LO = "63," which represents full digital mute.

Data Byte 6, Output Setting Register 2

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	SM	RO5	RO4	RO3	RO2	RO1	RO0
23	22	21	20	19	18	17	16

SM Mono Speaker Analog Mute.
- 0 Mute mono speaker
- 1 Mono speaker on

RO5:0 Output attenuation setting for the right DAC channel; "0" represents no attenuation. Step size is 1.5 dB; "62" represents 93 dB of attenuation. Attenuation = 1.5 dB × RO, except for RO = "63," which represents full digital mute.

Data Byte 7, Input Setting Register 1

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
PIO1	PIO0	OVR	IS	LG3	LG2	LG1	LG0
15	14	13	12	11	10	9	8

PIO1:0 Parallel I/O bits for system signaling. PIO bits do not affect Codec operation.

OVR ADC input overrange. This bit is set to "1" if either ADC channel is driven beyond the specified input range. It is "sticky," i.e., it remains set until explicitly cleared by writing a "0" to OVR. A "1" written to OVR is ignored, allowing OVR to remain "0" until an overrange condition occurs.

IS Input selection
- 0 Line-level stereo inputs
- 1 *J-Grade*: Microphone (condenser-type) level inputs
  K-Grade: Microphone (condenser-type) level inputs if MB = 0 (+20 dB gain), or line-level stereo inputs if MB = 1 (0 dB gain).

LG3:0 Input gain for left channel. "0" represents no gain. Step size is 1.5 dB; "15" represents +22.5 dB of input gain. Gain = 1.5 dB × LG.

Data Byte 8, Input Setting Register 2

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
MA3	MA2	MA1	MA0	RG3	RG2	RG1	RG0
7	6	5	4	3	2	1	0

MA3:0 Monitor mix. "0" represents no attenuation, i.e., the ADCs' output is fully mixed with the DACs' input. Step size is 6 dB; "14" represents an attenuation of both channels of the ADCs' output along the monitor datapath of 84 dB. Mix attenuation = 6 dB × MA, except for MA = "15," which disables monitor mix entirely.

RG3:0 Input gain for right channel. "0" represents no gain. Step size is 1.5 dB; "15" represents +22.5 dB of input gain. Gain = 1.5 dB × RG.

Control Register Defaults

Upon coming out of $\overline{\text{RESET}}$ or Power Down, internal control registers will be set to the following values:

Defaults Coming Out of $\overline{\text{RESET}}$ or Power Down		
MB	0	(Mic Input Applied to +20 dB Fixed Gain Block)
OLB	1	(*J-Grade*: Full Scale Line 0 and Line 1 Output 2.0 V p-p, Full Scale Mono Speaker Output 4.0 V p-p)
OLB	0	(*K-Grade*: Full Scale Line 0 Output 2.8 V p-p, Full Scale Line 1 Output 4.0 V p-p, Full Scale Mono Speaker Output 8.0 V p-p)
DCB	1	
AC	0	(Autocalibration Disabled)
DFR2:0	0	(8 or 5.5125 kHz)
ST	0	(Monophonic Mode)
DF1:0	1	(8-Bit μ-Law Data)
ITS	0	(FSYNC, SDTX and SCLK Three-State within 3 SCLK Cycles after D/$\overline{\text{C}}$ Goes LO)
MCK1:0	0	(Serial Bit Clock [SCLK] Is the Master Clock)
FSEL1:0	2	(256 Bits per Frame)
MS	0	(Slave Mode)
TXDIS	1	(Three-State Serial Data Output)
ENL	0	(Loopback Disabled)
ADL	0	(Digital Loopback)
PIO1:0	3	("1"s, i.e., Three-State for the Open Collector Outputs)
OM1:0	0	(Mute Line 0 and Line 1 Outputs)
LO5:0	63	(Mute Left DAC)
SM	0	(Mute Mono Speaker)
RO5:0	63	(Mute Right DAC)
OVR	0	(No Overrange)
IS	0	(Line-Level Stereo Inputs)
LG3:0	0	(No Gain on Left Channel)
MA3:0	15	(No Mix)
RG3:0	0	(No Gain on Right Channel)

Also, when making a transition from Control Mode to Data Mode, those control register values that are *not* changeable in Control Mode get reset to the defaults above (except PIO). The control registers that *can* be changed in Control Mode will have the values they were just assigned. The subset of the above list of control registers that are assigned default values on the transition from Control Mode to Data Mode are:

Defaults at a Control-to-Data Mode Transition		
OM1:0	0	(Mute Line 0 and Line 1)
LO5:0	63	(Mute Left DAC)
SM	0	(Mute Mono Speaker)
RO5:0	63	(Mute Right DAC)
OVR	0	(No Overrange)
IS	0	(Line-Level Stereo Inputs)
LG3:0	0	(No Gain)
MA3:0	15	(No Mix)
RG3:0	0	(No Gain)

Note that all these defaults can be changed with control information in the first Data Word. Note also that the PIO bits in the output serial streams *always* reflect the values most recently read from the external PIO pins. (See "Parallel I/O Bits" below for timing details.) A Control-to-Data Mode transition is no exception.

An important consequence of these defaults is that *the AD1849 Codec always comes out of reset or power down in slave mode with an externally supplied serial bit clock (SCLK) as the clock source.* An external device *must* supply the serial bit clock and the chaining word input signal (TSIN) initially. (See "Codec Startup, Modes, and Transitions" below for more details.)

SERIAL INTERFACE

A single serial interface on the AD1849 provides for the transfer of both data and control information. This interface is similar to AT&T's Concentrated Highway Interface (CHI), allowing simple connection with ISDN and other telecommunication devices. The AD1849's implementation also allows a no-glue direct connection to members of Analog Devices' family of fixed-point DSP processors, including the ADSP-2101, the ADSP-2105, the ADSP-2111, and the ADSP-2115.

Frames and Words

The AD1849 serial interface supports time-division multiplexing. Up to four AD1849 Codecs or compatible devices can be daisy-chained on the same serial lines. A "frame" can consist of one, two, or four 64-bit "words." Thus, frames can be 64, 128, or 256 bits in length, as specified by the FSEL bits in Control Byte 3. Only 64 bits of each frame, a "word," contain meaningful data and/or control information for a particular Codec. See Figure 4 below.

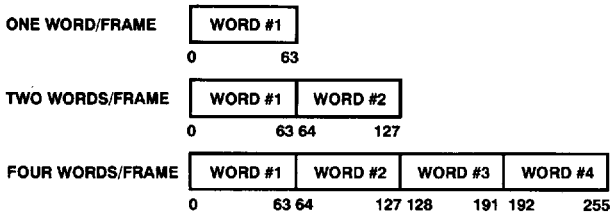


Figure 4. Frames and Words

The AD1849 supports two types of words: Data Words and Control Words. The proper interpretation of a word is determined by the state of the asynchronous Data/Control (D/$\overline{C}$) pin. The D/$\overline{C}$ pin establishes whether the SoundPort Codec is in the "Data" mode or "Control" mode. Transitions between these modes require an adherence to a handshaking protocol to prevent ambiguous bus ownership. The Data/Control transition protocol is described below in a separate section.

Clocks and the Serial Interface

The primary pins of the AD1849's serial interface are the serial data receive (SDRX) input pin, the serial data transmit (SRTX) pin, the serial data bit clock (SCLK) pin, the frame sync output (FSYNC) pin, the chaining word input (TSIN) pin, and the chaining word output (TSOUT) pin. The AD1849 can operate in either master mode—in which case SCLK and FSYNC are outputs and TSIN is an input—or in slave mode—in which case SCLK and TSIN are inputs and FSYNC is three-stated. If the AD1849 is in master mode, the internally selected clock source is used to drive SCLK and FSYNC. Note that in Control Mode, the Codec always behaves as a slave, regardless of the current state of the MS (Master/Slave) bit.

The five possible combinations of clock source and master/slave are summarized in Figure 5.

	INTERNAL OSCILLATORS	CLKIN	SCLK
MASTER	J-GRADE: YES K-GRADE: YES	J-GRADE: YES K-GRADE: YES	IMPOSSIBLE
SLAVE	J-GRADE: NO K-GRADE: CONDITIONAL	J-GRADE: NO K-GRADE: CONDITIONAL	J-GRADE: YES K-GRADE: YES

Figure 5. Clock Source and Master/Slave Combinations

Recommended modes are indicated above by "yes." Note that Codec performance is improved with a clean clock source, and in many systems the lowest jitter clocks available will be those generated by the Codec's internal oscillators. Conversely, SCLK in many systems will be the noisiest source. The master/SCLK clock source combination is impossible because selecting SCLK as the clock source overrides the MS control bit, forcing slave mode. (The SCLK pin cannot be driving out if it is simultaneously receiving an external clock.)

J-Grade: Nothing in the AD1849 SoundPort Codec prevents using the internal oscillators or CLKIN as clock sources (in addition to SCLK) when the serial interface is in slave mode. But these combinations should not be used because they require phase synchronization over temperature between the clock source driving internal Codec operations and the externally supplied SCLK. Skewed phase relationships between these clocks can cause internal setup time violations.

K-Grade: The internal oscillators or CLKIN can be the clock source when the serial interface is in slave mode provided that all clocks applied to the AD1849 SoundPort Codec are derived from the same external source. Precise phase alignment of the clocks is not necessary, rather the requirement is that there is no frequency drift between the clocks.

In master mode, the SCLK output frequency is determined by the number of bits per frame selected (FSEL) and the sampling frequency, F_S. In short, SCLK = FSEL × F_S in master mode.

Timing Relationships

Input data (except PIO) is clocked by the falling edge of SCLK. Data outputs (except PIO) begin driving on the rising edge of SCLK and are always valid well before the falling edge of SCLK.

Word chaining input, TSIN, indicates to a particular Codec the beginning of its word within a frame in both slave and master modes. The master mode Codec will generate a FSYNC output which indicates the beginning of a frame. In single Codec systems, the master's FSYNC output should be tied to the master's TSIN input to indicate that the beginning of the frame is also the beginning of its word. In multiple Codec daisy-chain systems, the master's FSYNC output should be tied to the TSIN input of the Codec (either the master or one of the slaves) which is intended to receive the first word in the frame. FSYNC and TSIN are completely independent, and nothing about the wiring of FSYNC to TSIN is determined by master or slave status (i.e., the master can own any one of the words in the frame). The master Codec's FSYNC can also be tied to all of the slave Codecs' FSYNC pins. When a slave, a Codec's FSYNC output is three-stated. Thus, it can be connected to a master's FSYNC without consequence. See "Daisy-Chaining Multiple Codecs" below for more details.

AD1849

The FSYNC rate is always equal to the data conversion sampling frequency, F_S. In Data Mode, the key significance of "frames" are to synchronize the transfer of digital data between an AD1849's internal ADCs and DACs and its serial interface circuitry. If, for example, a Codec has been programmed for two words per frame (FSEL="1"), then it will trigger the data converters and transfer data between the converters and the interface every 128 SCLKs. The TSIN input signals the Codec where its word begins within the frame. In Control Mode, frame size is irrelevant to the operation of any particular Codec; TSIN and TSOUT are sufficient to convey all the information required.

TSIN is sampled on the falling edge of SCLK. A LO-to-HI transition of TSIN defines the beginning of the word to occur at the next rising edge of SCLK (for driving output data). The LO-to-HI transition is defined by consecutive LO and HI samples of TSIN at the falling edges of SCLK. Both input and output data will be valid at the immediately subsequent falling edge of SCLK. See Figures 6 and 7.

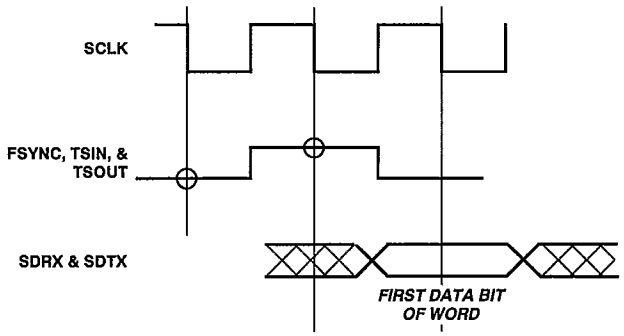


Figure 6. AD1849 Timing Relationships

After the beginning of a word has been recognized, TSIN is a "don't care"; its state will be ignored until one SCLK period before the end of the current word.

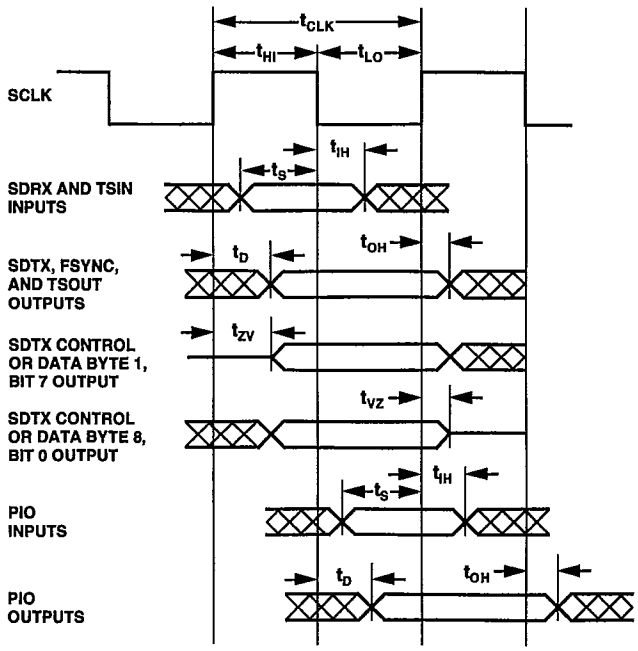


Figure 7. AD1849 Timing Parameters

The AD1849 comes out of reset with the default conditions specified in "Control Register Defaults." It will be in the mode specified by the D/$\overline{C}$ pin. If in Control Mode, the SoundPort Codec can be configured by the host for operation. Subsequent transitions to Control Mode after initialization are expected to be relatively infrequent. Control information that is likely to change frequently, e.g., gain levels, is transmitted along with the data in Data Mode. See Figure 8 for a complete map of the data and control information into the 64-bit Data Word and the 64-bit Control Word.

16-BIT STEREO DATA WORD

63 … 48	47 … 32	31	30	29	24	23	22	21	16	15	14	13	12	11	8	7	4	3	0
Left-Channel Audio	Right-Channel Audio	OM		LO		0	SM		RO		PIO	OVR	IS		LG		MA		RG

16-BIT MONO DATA WORD

63 … 48	47 … 32	31	30	29	24	23	22	21	16	15	14	13	12	11	8	7	4	3	0
Left-Channel Audio	0000 0000 0000 0000	OM		LO		0	SM		RO		PIO	OVR	IS		LG		MA		0000

8-BIT STEREO DATA WORD

63 … 56	55 … 48	47 … 40	39 … 32	31	30	29	24	23	22	21	16	15	14	13	12	11	8	7	4	3	0
Left Audio	0000 0000	Right Audio	0000 0000	OM		LO		0	SM		RO		PIO	OVR	IS		LG		MA		RG

8-BIT MONO DATA WORD

63 … 56	55 … 32	31	30	29	24	23	22	21	16	15	14	13	12	11	8	7	4	3	0
Left Audio	0000 0000 0000 0000 0000 0000	OM		LO		0	SM		RO		PIO	OVR	IS		LG		MA		0000

CONTROL WORD

63 61	60	59	58	57 56	55 54	53 51	50	49	48	47	46	45	44	43 42	41	40	39 … 34	33	32 31 30 29	16 15 12	11 … 8	7 … 0
001	MB	OLB	DCB	0	AC	00	DFR	ST	DF	ITS	0	MCK		FSEL	MS	TXDIS	000 000	ENL	ADL	PIO	00 0000 0000 0000	0010	REVID	0000 0000

Figure 8. AD1849 Bit Positions for Data and Control

Daisy-Chaining Multiple Codecs

Up to four SoundPort Codecs can be daisy-chained with frame sizes in multiples of 64 bits. The serial data is time-division multiplexed (TDM), allocating each Codec its own 64-bit word in the frame.

The pins that support TDM daisy-chaining of multiple Codecs are the word chaining input (TSIN) and the word chaining output (TSOUT). As described above, TSIN is used to indicate the position of the first bit of a particular Codec's 64-bit word within the total frame.

The word chaining output (TSOUT) is generated by every Codec during the transmission of the last bit of its 64-bit word. The first device in any Codec chain uses an externally generated or self-generated FSYNC signal as an input to TSIN. The TSOUT of the first Codec is wired directly to the TSIN of the second Codec and so on. The waveform of TSOUT is a pulse of one SCLK period in duration. All Codecs share the same SCLK, FSYNC, SDRX, and SDTX lines since they are selecting different words from a common frame.

Note that a powered-down Codec immediately echoes TSIN on TSOUT. Thus, a Codec can be added or removed from the chain simply by using the PDN pin. See "Reset and Power Down" below for more details. See Figure 9 for an illustration of daisy-chained Codecs.

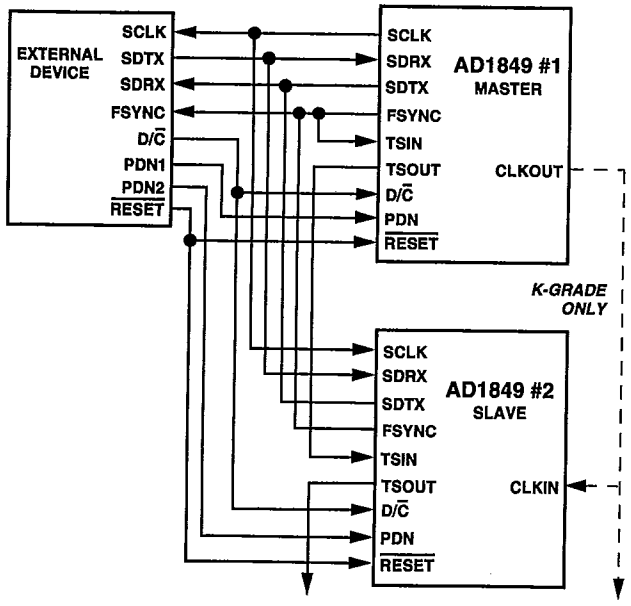


Figure 9. AD1849 Daisy-Chaining

Note that at most, one Codec in a daisy-chain can be in master mode without contention. All other Codecs must be in slave mode, receiving SCLK and TSIN externally.

J-Grade: Each slave uses SCLK as its clock source, which must run at 256 × F_S.

K-Grade: Each slave can still use SCLK as its clock source. However, as an alternative, it is possible to connect the CLKOUT pin of the master Codec to the CLKIN pins of the slaves, so that the sample frequency selected by the master (from one of its two crystals) will be automatically applied to the slaves. The master must be programmed for the desired sample frequency and the correct number of bits per frame. The slaves must be programmed for CLKIN as the clock source, the correct number of bits per frame, and SCLK as an input. The slaves FSYNC outputs will be three-stated and thus can be connected to the master's FSYNC without contention.

If SCLK is the clock source, it must run at 256 × F_S, and therefore the frame size must be 256 bits, i.e., four words. By contrast, if the master Codec's CLKOUT is used as the clock source, then it can run at either 256 × F_S or 128 × F_S.

Parallel I/O Bits

Both Data and Control Words allocate bit positions for "parallel I/O," PIO1:0. This provides a convenient mechanism for transferring signaling information between the serial data and control streams and the external pair of bidirectional pins also named "PIO1" and "PIO0." The states of the parallel I/O bits and pins do not affect the internal operation of the Codec in any way; their exclusive use is for system signaling.

The PIO pins are open-drain and should be pulled HI externally. They can be read (through serial output data) in either Control or Data Mode and can be written (through serial input data) in Data Mode exclusively. The values in the PIO field of the Control Word serial input in Control Mode will be ignored. An external device may drive either PIO pin LO even when written HI by the Codec, since the pin outputs are open-drain. Thus, a PIO value read back as a serial output bit may differ from the value just written as a serial input bit.

The PIO pins are read on the rising edge of SCLK five (5) SCLK periods before the first PIO bit is transmitted out over the serial interface. In Data Mode, the PIO pins are sampled as Bit 20 starts to be driven out. In Control Mode, the PIO pins are sampled as Bit 36 starts being driven out. Timing parameters are as shown in Figure 7; PIO pin input data is relative to the rising edge of SCLK. (Note that *only* the PIO pins are read on SCLK *rising* edges.)

The PIO pins are driven very shortly after the PIO data bits in the input Data Word are read (Data Mode only). They are driven on the *falling* edge of SCLK (unlike any other output). The PIO data bits in the input are located at Bits 15 and 14 in the Data Word and at Bits 31 and 30 in the Control Word (Figure 8). Due to the five (5) SCLK period delay, the PIO pins will be driven out with new values for Data Mode on the SCLK falling edge when Bit 8 is read in, and for Control Mode on the SCLK falling edge when Bit 24 is read in.

CODEC STARTUP, MODES, AND TRANSITIONS

Reset and Power Down

The AD1849 Stereo Codec can be reset by either of two closely related digital input signals, $\overline{\text{RESET}}$ and Power Down (PDN). $\overline{\text{RESET}}$ is active LO and PDN is active HI. Asserting PDN is equivalent to asserting $\overline{\text{RESET}}$ with two exceptions. First, if PDN is asserted (when $\overline{\text{RESET}}$ is HI), then the TSIN and TSOUT chaining pins remain active. TSOUT will immediately echo whatever signal is applied to TSIN during power down. This feature allows a very simple system test to detect "life" even in a power-down state. It also allows the user to selectively shut off Codecs in a daisy chain by powering down the unwanted Codecs. The down-stream Codecs will simply move up a word position in frame. The second difference is that power consumption will be lower in power-down mode than in exclusive reset mode. The CMOUT and LOUT1C pins will not supply current while the AD1849 is in the power-down state.

$\overline{\text{RESET}}$ should be asserted when power is first applied to the AD1849. $\overline{\text{RESET}}$ should be asserted for a minimum of 50 ms at power-up or when leaving the power-down mode to allow the power supplies and the voltage reference to settle. Any time $\overline{\text{RESET}}$ is asserted during normal operation, it should remain asserted for a minimum of 100 ns to insure a complete reset. Note that an autocalibration sequence will always occur when $\overline{\text{RESET}}$ is deasserted, in addition to on the Control Mode to Data Mode transition.

Coming out of either reset or power down, the state of the Data/Control pin (D/$\overline{\text{C}}$) will determine whether the Codec is in Data Mode or Control Mode. In the unlikely event that the control register defaults are desired for Codec operation, it is possible to go directly from reset or power down to Data Mode and begin audio operation.

Control Mode

More typically, users coming out of reset or power down will want to change the control register defaults by transmitting a Control Word in Control Mode. The user of the AD1849 SoundPort Codec can also enter Control Mode at any time during normal Data Mode operation. The D/$\overline{\text{C}}$ pin is provided to make this possible. The Codec enters Control Mode when the D/$\overline{\text{C}}$ pin is driven LO or held LO when coming out of reset and/or power down.

In Control Mode, the location of a word within a frame is determined solely by the behavior of the TSIN and TSOUT signals. Each Codec by itself does not care where the frame boundaries fall as defined by the system. The contents of the frame size select (FSEL1:0, Control Word Bits 43 and 42) bits are irrelevant to the operation of each AD1849 in Control Mode. In Control Mode, a Codec requires 64 SCLK cycles to be fully programmed. Additional SCLK cycles (more than 64) that occur before the end of the frame will be ignored.

If four Codecs, for example, were daisy-chained, then each Codec would receive TSIN every 256 bits. In this case, Codec #2's input Control Word will be positioned between Bit 64 and Bit 127 in the input frame.

Control Word Echo

While in Control Mode, the AD1849 Codec will echo the Control Word received as a serial input on the SDRX pin as a serial output in the next frame on the SDTX pin. (SDTX will be enabled regardless of the setting of the TXDIS bit, Control Word Bit 40.) This echoing of the control information allows the external controller to confirm that the Codec has received the intended Control Word. For the four Codec daisy chain example above, the Control Word will be echoed bit for bit as an output between Bit 64 and Bit 127 in the *next* output frame. In general, in Control Mode, the location of the echo Control Word *within a frame* will be at the same word location as the input Control Word.

In the first frame of Control Mode, the AD1849 will output a Control Word that reflects the control register values operative during the most recent Data Mode operation. If Control Mode was entered prior to any Data Mode operation, this first output word will simply reflect the standard default settings. DCB will always be "1" in the first output echoed Control Word.

J-Grade TSIN Upper Frequency Limit

The AD1849 must receive TSIN and SCLK signals externally as a slave while in Control Mode. If the clock source selected in Control Mode (for Data Mode operation) is CLKIN (MCK = "3") or SCLK (MCK = "0"), then during Control Mode, the TSIN input can operate up to its specified limit.

J-Grade: If, however, the clock source selected requires either XTAL1 or XTAL2 (MCK = "1" or "2") and that required crystal had not been operating in the immediately preceding Data Mode, then there is a restriction on the system. The TSIN input must run no faster than 8 kHz. By adhering to this restriction, the AD1849's internal clocks are guaranteed to have settled if the DCB handshaking sequence described below is adhered to.

K-Grade: This TSIN upper frequency constraint is eliminated.

DCB Handshaking Protocol

The D/$\overline{\text{C}}$ pin can make transitions completely asynchronously to internal Codec operation. This fact necessitates a handshaking protocol to ensure a smooth transition between serial bus masters (i.e., the external controller and the Codec) and guarantee unambiguous serial bus ownership. This software handshake protocol for Data Mode to Control Mode transitions makes use of the Data/Control Bit (DCB) in the Control Mode Control Word (Bit 58). Prior to initiating the change to Control Mode, the external controller should gradually attenuate the audio outputs. The DCB handshake protocol requires the following steps:

Enter Control Mode

The external controller drives the D/$\overline{\text{C}}$ pin LO, forcing the Codec into Control Mode as a slave. The DCB transmitted from the external controller to the Codec may be "0" or "1" at this point in the handshake.

For the *J-Grade* or the *K-Grade* with ITS = 0 (Control Word Bit 47) and if the Codec was operating as the master in the preceding Data Mode, immediately after D/$\overline{\text{C}}$ goes LO, the Codec will drive FSYNC, TSOUT and SDTX LO for one SCLK period, then three-state FSYNC and SDTX. TSOUT is not three-stated. The Codec will drive SCLK for three (3) SCLK periods after D/$\overline{\text{C}}$ goes LO and then three-state SCLK. The external controller must wait at least three (3) SCLK periods after it drives D/$\overline{\text{C}}$ LO, and then start driving SCLK.

For the *K-Grade* with ITS = 1 (Control Word Bit 47) and if the Codec was operating as the master in the preceding Data Mode, the Codec will three-state FSYNC, SDTX, and SCLK immediately after D/$\overline{\text{C}}$ goes LO. TSOUT is driven LO immediately after D/$\overline{\text{C}}$ goes LO and is not three-stated. The external controller may start driving SCLK immediately.

For the *J-Grade* or the *K-Grade* with ITS = 0 and if the external controller was operating as the master in the preceding Data Mode, the external controller must continue to supply SCLK to the slave Codec for at least three (3) SCLK periods after D/$\overline{C}$ goes LO before a Control Mode TSIN is issued to the Codec. TSIN must be held LO externally until the first Control Word in Control Mode is supplied by the external controller. This prevents false starts and can be easily accomplished by using a pull-down resistor on TSIN as recommended. The slave Codec drives TSOUT and SDTX LO, then three-states SDTX, all within 1 1/2 (one and one half) SCLK periods after D/$\overline{C}$ goes LO. TSOUT is not three-stated.

For the *K-Grade* with ITS = 1 and if the external controller was operating as the master in the preceding Data Mode, the external controller must continue to supply SCLK to the slave Codec. A Control Mode TSIN may be issued to the Codec immediately after D/$\overline{C}$ goes LO. The slave Codec drives TSOUT LO and three-states SDTX immediately after D/$\overline{C}$ goes LO. TSOUT is not three-stated.

The Codec initializes its Data Mode Control Registers to the defaults identified above, which among other actions, mutes all audio outputs.

First DCB Interlock

When the external controller is ready to continue with the DCB handshake, the Control Word sent by the external controller should have the DCB reset to "0" along with arbitrary control information (i.e., the control information does not have to be valid, although if it is valid, it allows the external controller to verify that the echoed Control Word is correct). The external controller should continue to transmit this bit pattern with DCB = "0" until the echoed DCB from the Codec also is reset to "0" (i.e., it must poll DCB until a "0" is read). This is the first interlock of the DCB handshake.

J-Grade: The DCB = "0" is echoed on SDTX in the next frame after it was received on SDRX.

K-Grade: The DCB = "0" is echoed on SDTX in the next frame after it was received on SDRX if a sample rate has been consistently selected AND the clock source is generated using the internal oscillator. Otherwise DCB = "0" will be echoed on SDTX in the frame after at least 2 ms of consistent sample rate selection expires. If SCLK or CLKIN is used as the clock source, the user must guarantee that the source selection and sample rate are stable for 2 ms before D/$\overline{C}$ is driven HI.

Note that after sending a Control Word with DCB = "0," the external controller must take care *not* to set (or glitch) DCB = "1" until after the echoed DCB = "0" has been received from the Codec.

Second DCB Interlock

After it sees the DCB = "0" (and has optionally verified that the echoed Control Word is correct), and when it is ready to continue with the DCB handshake, the external controller should transmit the desired and valid control information, but now with DCB set to "1." The external controller can then transmit arbitrary control information until the echoed DCB from the Codec is also set to "1" (i.e., it must poll DCB until a "1" is read). After this Control Word with DCB = "1," all future control information received by the Codec during Control Mode (i.e., while D/$\overline{C}$ is LO) will be ignored. This is the second and final interlock of the DCB handshake.

J-Grade: The Codec counts four [4] frames (the sample rate must be 8 kHz or lower) before it echoes DCB = "1." This is to allow 500 µs for the internal clocks of the AD1849 to settle to the selected sample rate. After these four [4] frames, the Codec will transmit only the first seven [7] bits of the Control Word with DCB = "1," and then three-state the SDTX pin. Thus the bit sequence in the echoed, output Control Word will be: 0, 0, 1, 0, 0, 1, 0, three-state. The external controller must continue to supply SCLK to the Codec until the Codec three-states the SDTX pin (i.e., seven [7] SCLK periods into the transmitted Control Word with DCB = "1"). By three-stating SDTX shortly after the DCB = "1" has been transmitted, the Codec ensures that there will be no serial bus contention. Note that the controller should not continue verifying subsequent bits in this Control Word since their values will no longer echo the input.

K-Grade: The Codec will echo DCB = "1" in the next frame after it was received on SDRX if a sample rate has been consistently selected AND the clock source is generated using the internal oscillator. Otherwise DCB = "1" will be echoed on SDTX once one sample rate selction has been held constant for at least 2 ms. If SCLK or CLKIN is used as the clock source, the user must guarantee that the source selection and sample rate are stable for 2 ms before D/$\overline{C}$ is driven HI. The Codec will transmit the full 64-bit Control Word with DCB = "1" and then three-state the SDTX pin. The external controller must continue to supply SCLK to the Codec until all 64 bits of the Control Word with DCB = "1" have been transmitted by the Codec, plus at least one [1] more SCLK after this 64-bit Control Word (i.e., at least 65 SCLKs). Note that echoing the full 64-bit Control Word makes the AD1849K match the behavior of the CS4215.

Exit Control Mode

Control mode DCB handshake is now complete. The Codec will remain inactive until D/$\overline{C}$ goes HI or $\overline{\text{RESET}}$ and or PDN are asserted.

Control Mode to Data Mode Transition and Autocalibration

The AD1849 will enter Data Mode when the asynchronous D/$\overline{C}$ signal goes HI. The serial interface will become active immediately and begin receiving and transmitting Data Words in accordance with the SCLK, FSYNC, TSIN, and TSOUT signals as shown in Figure 6. If the Codec enters Data Mode as a master, it will generate one complete SCLK period before it drives FSYNC HI; FSYNC will go HI with the *second* rising edge of SCLK. This allows external devices driven by SCLK to recognize a complete FSYNC LO-to-HI transition. If an AD1849 Codec enters Data Mode as a slave, it can recognize a TSIN LO-to-HI transition even if SCLK is simultaneously making its first LO-to-HI transition. In fact, the AD1849 serial interface will operate properly even if D/$\overline{C}$, SCLK, and TSIN all go HI at the same time.

J-Grade: Note that if an autocalibration sequence was specified in the most recent Control Mode (AC = "1," Control Word Bit 56) , the AD1849 will use the next 256 frames for zeroing ADC and DAC offsets.

K-Grade: The AD1849 will always autocalibrate on the Control Mode to Data Mode transition. The user should select, by the fifth frame, the Data Mode control settings to which he wishes the Codec to autocalibrate. Data Word input control information can change after the fifth frame, but these changes will be locked out by the Codec for the duration of the 194 frames. Any

changes to the control information after the fifth frame will be echoed, but these changed settings will not be used by the Codec for autocalibration.

See Figure 10 for a flow chart representation of a typical startup sequence, including the DCB handshake.

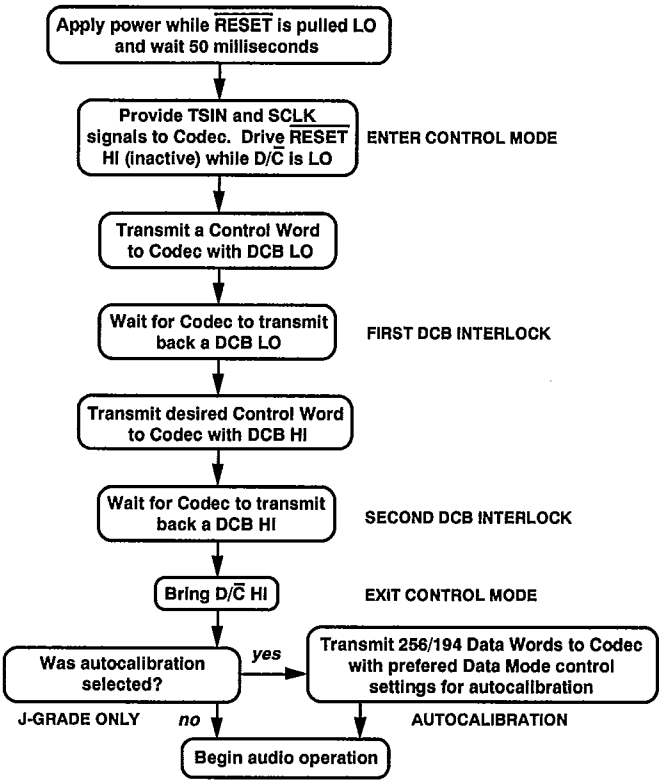


Figure 10. Typical AD1849 Startup Sequence

APPLICATIONS CIRCUITS

The AD1849 Stereo Codec has been designed to require a minimum of external circuitry. The recommended circuits are shown in Figures 11 through 20 and summarized in Figure 21. Analog Devices estimates that the total cost of all the components shown in these Figures, including crystals, to be less than $5 in 10,000 piece quantities.

Industry-standard compact disc "line-levels" are 2 V rms centered around analog ground. (For other audio equipment, "line level" is much more loosely defined.) The AD1849 SoundPort is a +5V only powered device. Line level voltage swings for the AD1849 are defined to be 1 V rms for ADC input and 0.707 V rms for DAC output. Thus, 2 V rms input analog signals must be attenuated and either centered around the reference voltage intermediate between 0 V and +5 V or ac-coupled. The CMOUT pin will be at this intermediate voltage, nominally 2.25 V. It has limited drive but can be used as a voltage datum to an op amp input. Note, however, that dc-coupled inputs are not recommended, as they provide no performance benefits with the AD1849 *K-Grade* architecture. Furthermore, dc offset differences between multiple dc-coupled inputs create the potential for "clicks" when changing the input mux selection.

A circuit for 2 V rms line-level inputs is shown in Figure 11. Note that this is approximately a divide-by-two resistive divider.

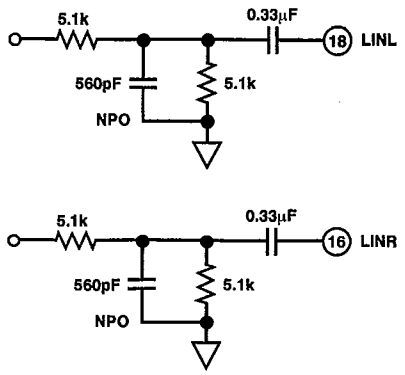


Figure 11. AD1849 2 V rms Line-Level Input Circuit

J-Grade: The 560 pF capacitor is not strictly required, since the ADC antialias filter is on-chip. However, if the environment in which the AD1849 is "noisy" in the MHz region, this capacitor is good insurance.

K-Grade: An external passive antialias filter is required. If line-level inputs are already at the 1 V rms levels expected by the AD1849, the resistors in parallel with the 560 pF capacitors can be omitted.

The AD1849 Codec contains a +20 dB gain block to accommodate condenser microphones, bypassable with the *K-Grade*. Particular system requirements will depend upon the characteristics of the intended microphone. Figure 12 illustrates one example of how an electret condenser mike requiring phantom power could be connected to the AD1849. CMOUT is shown buffered by an op amp; a transistor like a 2N4124 will also work fine for this purpose. Note that if a battery-powered microphone is used, the buffer and R2s are not needed. The values of R1, R2, and C should be chosen in light of the mic characteristics and intended gain. Typical values for these might be R1 = 20 kΩ, R2 = 2 kΩ, and C = 220 pF.

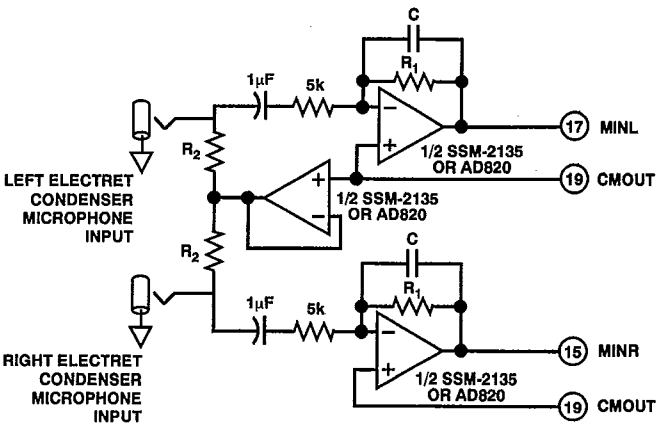


Figure 12. AD1849 "Phantom-Powered" Microphone Input Circuit

Figure 13 shows ac-coupled line outputs. The resistors are used to center the output signals around analog ground. If dc-coupling is desired, CMOUT could be used with op amps as mentioned above.

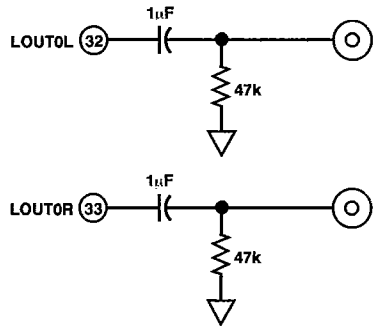


Figure 13. AD1849 Line Output Connections

A circuit for headphone drive is illustrated in Figure 14. Drive is supplied by +5 V operational amps. The circuit shown ac couples the headphones to the line output.

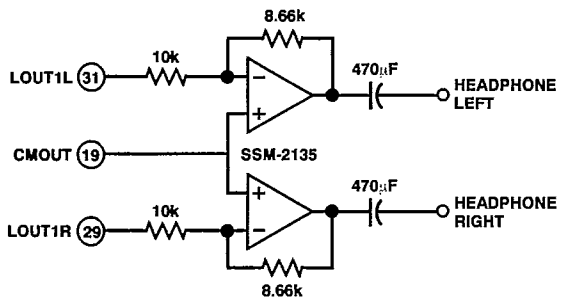


Figure 14. AD1849 Headphone Drive Connections

The *K-Grade* adds a common return path LOUT1C on Pin 30 which is biased up to the CMOUT voltage, nominally 2.25 V. The *K-Grade* also allows for 6 dB larger output voltage swings by resetting the OLB bit (Bit 59 of the Control Word) to "0." Figure 15 illustrates an alternative headphone connection for the *K-Grade* which uses the LOUT1C pin to eliminate the need for ac coupling. The 12 Ω resistors minimize output level variations caused by different headphone impedances. LOUT1L, LOUT1R and LOUT1C are short-circuit protected. Note that driving headphones directly as shown in Figure 15 with OLB = 0 will cause clipping for large input signals and will only work with very efficient "Walkman-type" headphones. For high quality headphone listening, Analog Devices recommends the circuit shown in Figure 14 for the *J-Grade* and the *K-Grade* with OLB = 1.

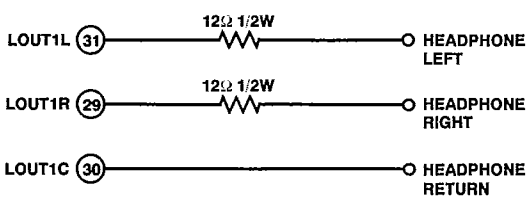


Figure 15. K-Grade Optional Headphone Drive Connections

No external circuitry is required for driving a single speaker from the AD1849's mono outputs as shown in Figure 16. Note that this output is differential. Analog Devices guarantees specified distortion performance for speaker impedances of 48 Ω or greater. Lower impedance speakers can be used, but at the cost of some distortion. When using the *J-Grade* driving speakers

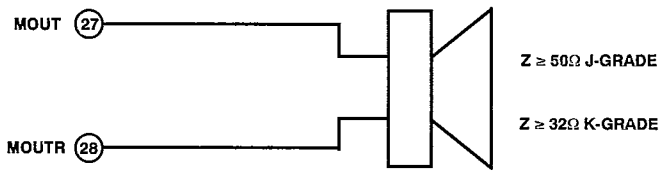


Figure 16. AD1849 External Mono Speaker Connections

much less than 48 Ω, a power amp should be used. The *K-Grade* can drive speakers of 32 Ω or greater.

Figure 17 illustrates reference bypassing. V_{REF} should only be connected to its bypass capacitors, which should be located as close to Pin 21 as possible (especially the 0.1 µF capacitor).

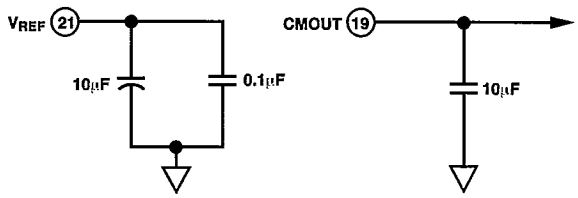


Figure 17. AD1849 Voltage Reference Bypassing

Figure 18 illustrates signal-path filtering capacitors, C0 and C1. Note that the values recommended here for the *J-Grade* AD1849, 1000 pF NPO, will increase to 0.1 µF for the *K-Grade* AD1849. Make plans for the PC board layout to accommodate the larger capacitor value. *The AD1849J must use 1000 pF capacitors; the AD1849J silicon will not perform properly with 0.1 µF capacitors. The AD1849K must use 0.1 µF capacitors; the AD1849K silicon will not perform properly with 1000 pF capacitors.*

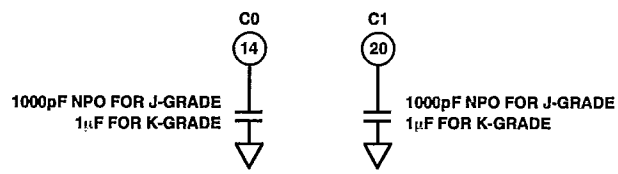


Figure 18. AD1849 External Filter Capacitor Connections

The crystals shown in the crystal connection circuitry of Figure 19 should be fundamental-mode and parallel-tuned. Two sources for the exact crystals specified are Component Marketing Services in Massachusetts, U.S. at 617-762-4339 and Cardinal Components in New Jersey, U.S. at 201-746-0333. Note that using the exact data sheet frequencies is not required and that external clock sources can be used to overdrive the AD1849's internal oscillators. (See the description of the MCK1:0 control bits above.) If using an external clock source, apply it to the crystal input pins while leaving the crystal output pins unconnected. Attention should be paid to providing low jitter external input clocks.

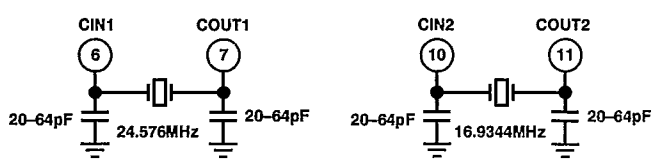


Figure 19. AD1849 Crystal Connections

AD1849

Good, standard engineering practices should be applied for power-supply decoupling. Decoupling capacitors should be placed as close as possible to package pins. If a separate analog power supply is not available, we recommend the circuit shown in Figure 20 for using a single +5 V supply. Ferrite beads suffice for the inductors shown. This circuitry should be as close to the supply pins as is practical.

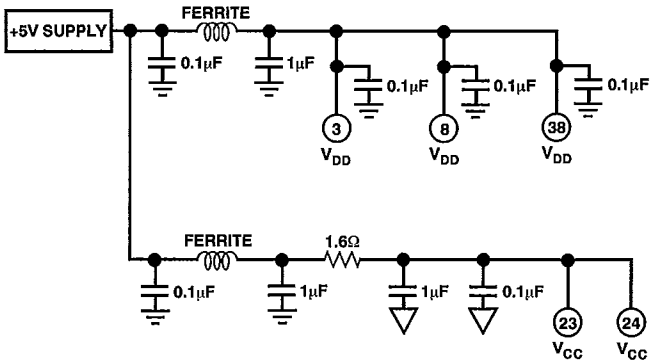


Figure 20. AD1849 Recommended Power Supply Bypassing

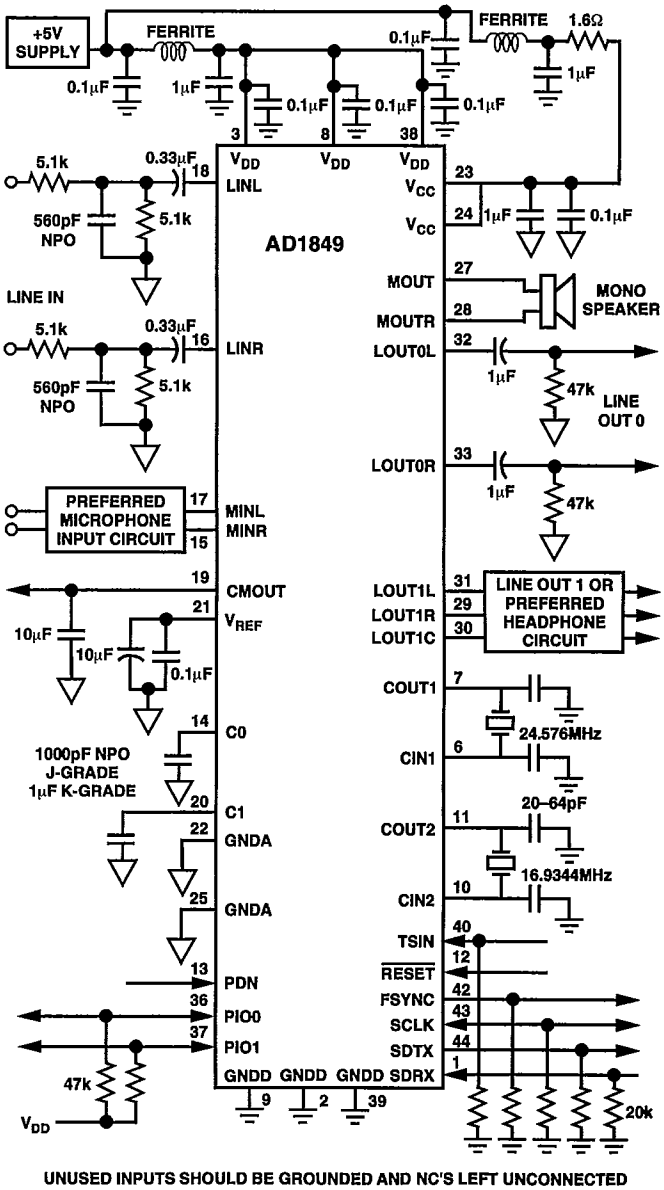
The two PIO pins must be pulled HI, as they have open drain outputs. Analog Devices also recommends pull-down resistors for SCLK, FSYNC, SDTX, SDRX, and TSIN to provide margin against system noise. CLKIN, CIN1, and CIN2, if not used, should be grounded. A typical connection diagram is shown in Figure 21, which serves to summarize the preceding application circuits.

Analog Devices recommends a split ground plane as shown in Figure 22. The analog plane and the digital plane are connected directly under the AD1849. Splitting the ground plane directly under the SoundPort Codec is optimal because analog pins will be located above the analog ground plane and digital pins will be located directly above the digital ground plane for the best isolation. The digital ground and analog grounds should be tied together in the vicinity of the AD1849. Other schemes may also yield satisfactory results.

Figure 23 illustrates the "zero-chip" interfaces of the AD1849 SoundPort Codec to four of Analog Devices' Fixed-Point DSµPs. The ADSP-2111, ADSP-2101 and ADSP-2115 use their multichannel serial port for the data interface and flag outputs for D/$\overline{C}$. The ADSP-2105 has a single serial port which operates in its frameless mode. Because the ADSP-2105 lacks a flag output, it alone does require additional circuitry to generate D/$\overline{C}$. Shown is an implementation using a single D-flop, an OR-gate, and two pull-down resistors.

Low level ADSP-21xx software drivers for the AD1849 are supplied with the AD1849 Evaluation Board. Source and object codes are available from your Analog Devices Sales Representative or on the Analog Devices DSP Bulletin Board. The DSP Bulletin Board telephone number is (617) 461-4258, 8 data bits, no parity, 1 stop bit, 300 to 2400 baud.

Note that the interface to the Texas Instruments TMS320C25 must be significantly more complicated than these three examples because the C25's serial port cannot be a master, which is required of the external controller during Control Mode.



UNUSED INPUTS SHOULD BE GROUNDED AND NC'S LEFT UNCONNECTED

Figure 21. Typical Connection Diagram

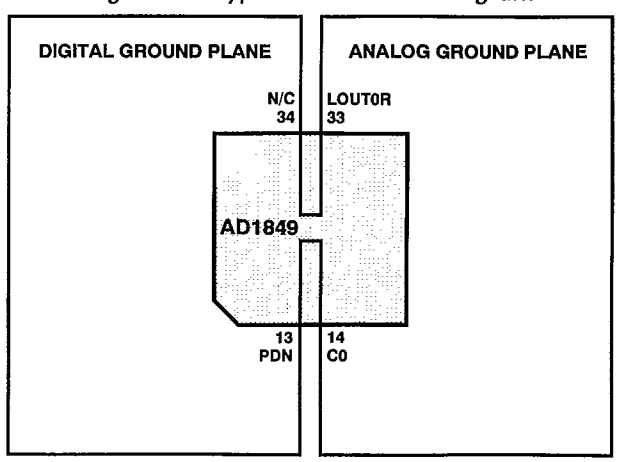


Figure 22. AD1849 Recommended Ground Plane

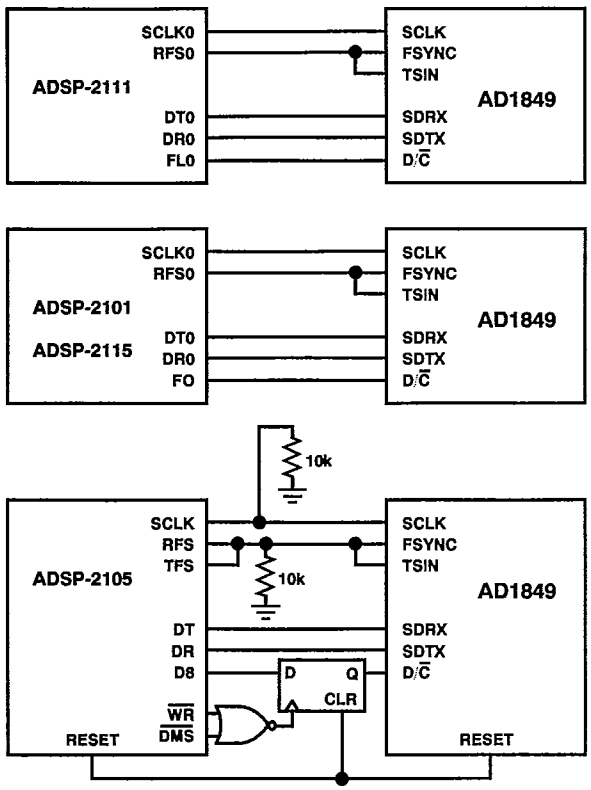


Figure 23. Interfaces to Analog Devices' Fixed-Point DSμPs

CS4215 COMPATIBILITY

The Analog Devices AD1849 SoundPort Stereo Codec is pin-compatible with the CS4215. These chips were independently codeveloped to a common specification provided by Sun Microsystems, Inc. Because of their independent development, they will differ in performance and in minor details. A board can be designed to accommodate either chip by attending to a few differences in their required support circuitry. Note that the *K-Grade* reduces these compatibility issues to a bare minimum.

K-Grade issues:

- If consistent control information is transmitted to the Codec during Control Mode, the AD1849 DCB handshake is compatible with the CS4215. See text for more details.
- The Analog Devices *K-Grade* AD1849 uses two external capacitors to complete its internal input filter as shown in Figure 18. The CS4215 calls the two pins on the AD1849 for these capacitor connections, "no connects." By laying out a board with these capacitors, either chip will work.
- The *K-Grade* AD1849 requires an external *passive* antialias filter as shown in Figure 11. In contrast, the recommended input circuit for the CS4215 is a single-pole *active* filter requiring a dual op amp. Though overkill for the AD1849, this input circuit will work with the AD1849 as well.
- The *K-Grade* AD1849 was designed to require no external low-pass filters on analog outputs. As shown in Figure 13, the AD1849 only requires ac coupling capacitors and resistors for line-level dc bias. In contrast, the most recent CS4215 data sheet has added a single-pole passive filter for its recommended line-level output circuit. Though overkill for the AD1849, this output circuit will work with the AD1849 as well.
- Pin 38 on the *K-Grade* AD1849 is used as a digital power supply. On the CS4215, this pin is a "no connect." We strongly recommend connecting Pin 38 to the digital supply. Both chips should operate in this configuration. Pin 39 on the *K-Grade* AD1849 is used as a digital ground. On the CS4215, this pin is a "no connect." We strongly recommend connecting Pin 39 to the digital ground plane. Both chips should operate in this configuration.
- The *K-Grade* AD1849 adds a mic gain block bypass signal path that the CS4215 does not offer. By setting MB (Control Word Bit 60) to a "1," the mic input will bypass the +20 dB fixed gain block.
- Analog Devices recommends a 10 μF bypass capacitor on the voltage reference output, CMOUT (Pin 19). Using a 0.47 μF capacitor may be acceptable in many systems, however DAC performance at low sample rates will be improved with the larger capacitor.

J-Grade issues:

- The DCB handshake protocol for the *K-Grade* AD1849 is somewhat different than the CS4215. See text for details.
- The AD1849 was designed to require no external buffering amplifiers on the analog inputs. As shown in Figure 11, the *J-Grade* AD1849 only requires a resistive divider and ac coupling capacitors, though an additional filtering capacitor is recommended in "noisy" environments. In contrast, the recommended input circuit for the CS4215 is a single-pole active filter requiring a dual op amp. Though overkill for the AD1849, this input circuit will work with the AD1849 as well.
- Related to the above, the Analog Devices *J-Grade* AD1849 uses two external capacitors to complete its internal input filter as shown in Figure 18. The CS4215 calls the two pins on the AD1849 for these capacitor connections, "no connects." By laying out a board with these capacitors, either chip will work.
- The *J-Grade* AD1849 was designed to require no external low-pass filters on analog outputs. As shown in Figure 13, the AD1849 only requires ac coupling capacitors and resistors for line-level dc bias. In contrast, the most recent CS4215 data sheet has added a single-pole passive filter for its recommended line-level output circuit. Though overkill for the AD1849, this output circuit will work with the AD1849 as well.
- Analog Devices recognized the wide range of impedance and sensitivities of available headphones and therefore recommends the external headphone drive circuit shown in Figure 14. The CS4215 recommended headphone circuit suggests that this buffer circuit is not required. Note that the *K-Grade* AD1849 adds the OLB bit (Bit 59 of the Control Word) which when reset to "0" provides compatibility with the CS4215. With the circuit of Figure 14, either chip will drive the majority of "Walkman-type" headphones to acceptable volume levels (though with clipping at full volume).
- Pin 38 on the *J-Grade* AD1849 is used as a digital power supply. On the CS4215, this pin is a "no connect." We strongly recommend connecting Pin 38 to the digital supply. Both chips should operate in this configuration. Pin 39 on the *J-Grade* AD1849 is used as a digital ground. On the CS4215, this pin is a "no connect." We strongly recommend connecting Pin 39 to the digital ground plane. Both chips should operate in this configuration.

- One of the test modes—digital loopback—has been defined differently between the *J-Grade* AD1849 and the CS4215. The Analog Devices *J-Grade* AD1849 in this mode accepts analog inputs to its ADCs, converts them to digital signals, passes these values directly to the DACs, and makes these signals available as analog outputs. This mode allows a simple analog-domain test of the AD1849's signal paths. The CS4215 performs an all-digital test of its serial interface in its "digital loopback" mode. Note that the *K-Grade* digital loopback mode D-D has been implemented identically to the CS4215, i.e., the serial interface only is looped back.
- The *J-Grade* AD1849 requires a "slow" serial clock in Control Mode if the transition will be to Data Mode using a non-settled (new or different) on-chip oscillator as described in "Clock Source Constraints" above. Note that on the *K-Grade* this restriction has been removed.
- The *J-Grade* AD1849 does not include the Immediate Three-State bit (Control Word Bit 47) which has been added to the *K-Grade* AD1849.
- The *J-Grade* AD1849 does not include the line 1 analog output return pin LOUT1C Pin 30 which has been added to the *K-Grade* AD1849. This pin is a N/C (no connect) on the *J-Grade* AD1849.
- The *J-Grade* AD1849 will not autocalibrate on the Control-to-Data Mode transition unless the AC bit (Control Word Bit 56) is a "1." Note that the *K-Grade* AD1849 will always autocalibrate on the Control-to-Data Mode transition, regardless of the state of the AC bit.
- The *J-Grade* AD1849 autocalibration sequence requires 256 FSYNC frames to complete. The CS4215 autocalibration sequence requires 194 FSYNC frames to complete.
- The *J-Grade* AD1849 may consume excessive power due to internal bus contentions when the power down or reset state is entered from Data Mode. The *J-Grade* AD1849 should not be allowed to remain in either of these states for very long for reasons of reliability. Entering power down or reset from Control Mode avoids this problem. The *K-Grade* AD1849 eliminates this issue.

FREQUENCY RESPONSE PLOTS

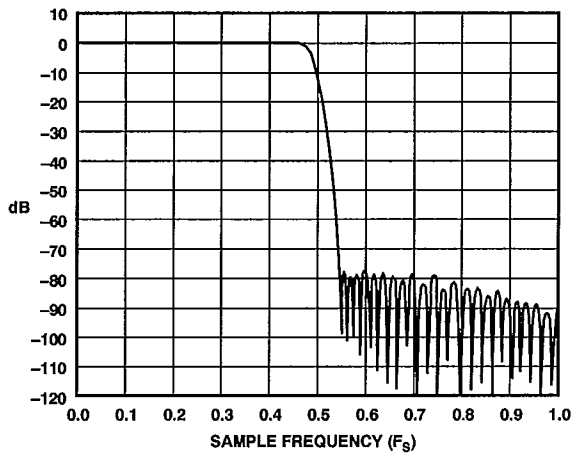


Figure 24. AD1849K Analog-to-Digital Frequency Response to F_S (Full Scale Line-Level Inputs, 0 dB Gain)

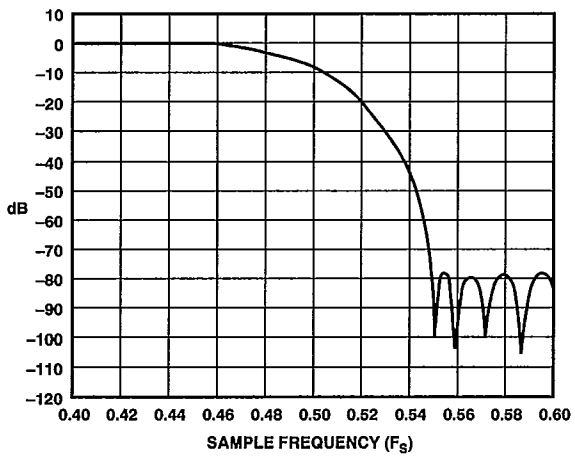


Figure 25. AD1849K Analog-to-Digital Frequency Response —Transition Band (Full Scale Line-Level Inputs, 0 dB Gain)

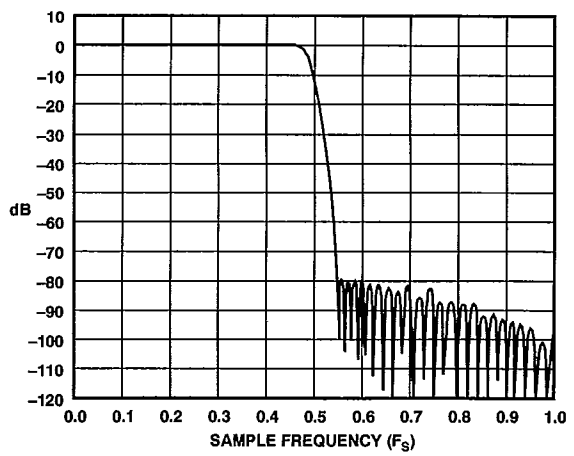


Figure 26. AD1849K Digital-to-Analog Frequency Response (Full Scale Inputs, 0 dB Attenuation)

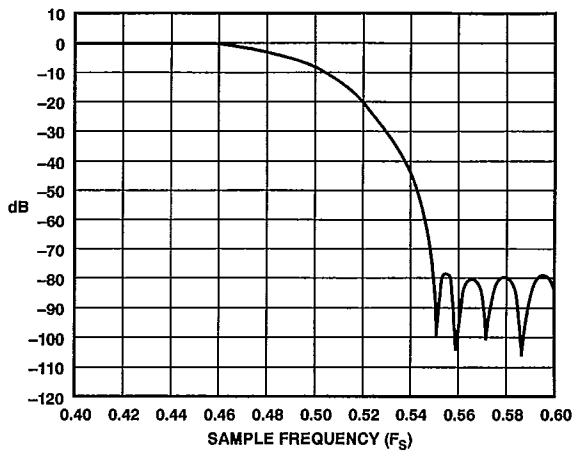


Figure 27. AD1849K Digital-to-Analog Frequency Response —Transition Band (Full Scale Inputs, 0 dB Attenuation)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Leaded Chip Carrier (PLCC)