

Excellent EMI Immunity Low Noise, Precision Operational Amplifiers

■ FEATURES ($V^+=5V$, $V_-=0V$, $T_a=25^\circ C$)

- Precision $V_{IO}=50\mu V$ max.
 $V_{IO}=100\mu V$ max. ($-40^\circ C$ to $+125^\circ C$)
- Low Offset Drift $0.6\mu V/^\circ C$ max.
- Integrated EMI filter EMIRR=78dB typ. @ $f=900MHz$
- Low Bias Current $2.5nA$ max.
- Low Noise $8nV/\sqrt{Hz}$ typ. @ $f=1kHz$
- Unity Gain Stable
- No Phase Reversal
- Supply Voltage $\pm 2.25V$ to $\pm 18V$
- Operating Temperature $-40^\circ C$ to $+125^\circ C$
- Package

NJMOP277 SOP8 JEDEC150mil, MSOP8 (VSP8)*

NJMOP2277 SOP8 JEDEC150mil, MSOP8 (VSP8)*

DFN8-W2 (ESON8-W2) (3mm x 3mm)

*meet JEDEC MO-187-DA

■ APPLICATION

- Temperature Sensor
- Current Sensor
- Bridge Amplifier
- Battery Monitor
- Photodiode Amplification
- Automatic Test Equipment

■ GENERAL DESCRIPTION

The NJMOP277 (Single) / NJMOP2277 (Dual) are high precision operational amplifiers featuring low offset voltage drift of top-class, low offset voltage and low noise and high voltage gain. The NJMOP277 / NJMOP2277 excellent electrical characteristics are guaranteed over a wide operating range ($-40^\circ C$ to $+125^\circ C$, $\pm 5V$ to $\pm 15V$).

Therefore, it is most suitable for measuring instruments that require stability against ambient temperature change and/or for applications such as configuring high gain circuits to process very small signals.

Moreover, they have the advantage very small package and high RF noise immunity. It is easy to replacement from defect standard precision operational amplifier: OP-177 series and to design against RF immunity, too.

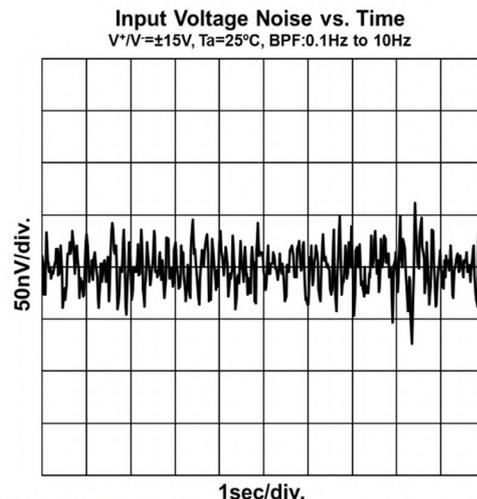
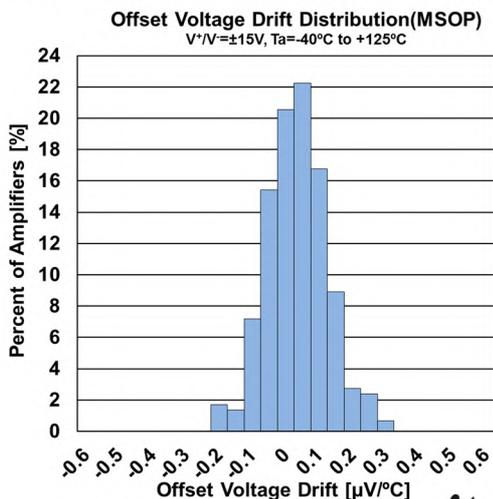
■ RELATED PRODUCTS

FEATURES	Single	Dual	Quad
JFET Input Precision OP-AMP ($V_{IO}=400\mu V$, $SR=20V/\mu s$)	-	NJM8512	NJM8513
CMOS Precision OP-AMP ($V_{IO}=150\mu V$)	NJU7076	NJU7077	NJU7078

■ INPUT OFFSET VOLTAGE GRADE

Grade	PART NUMBER	Offset Voltage (μV max.) $T_a = 25^\circ C$	Offset Drift ($\mu V/^\circ C$ max.) $T_a = -40$ to $125^\circ C$	Offset Current (nA max.) $T_a = -40$ to $125^\circ C$
F-Grade	NJMOP277FE NJMOP277FR NJMOP2277FE NJMOP2277FR	20	0.15	2
G-Grade	NJMOP277GE NJMOP277GR NJMOP2277GE NJMOP2277GR	50	0.6	3
-	NJMOP2277KW2	100	0.7	3

■ TYPICAL CHARACTERISTICS

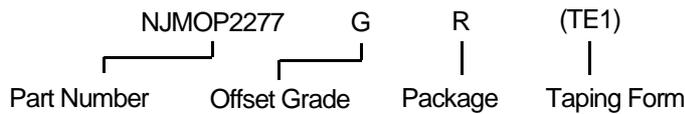


■ PIN CONFIGURATIONS

PRODUCT NAME	NJMOP277GE / NJMOP277FE	NJMOP277GR / NJMOP277FR
Package	SOP8 JEDEC150mil	MSOP8 (VSP8)
Pin Functions		
PRODUCT NAME	NJMOP2277GE / NJMOP2277FE	NJMOP2277GR
Package	SOP8 JEDEC150mil	MSOP8 (VSP8)
Pin Functions		
PRODUCT NAME	NJMOP2277KW2	
Package	DFN8-W2 (ESON8-W2)	
Pin Functions		

*Connect to exposed pad to V⁻

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJMOP277GE (TE1)	SOP8	Yes	Yes	Sn2Bi	277G	76	2000
NJMOP277FE (TE1)	JEDEC150mil				277F		
NJMOP277GR (TE1)	MSOP8	Yes	Yes	Sn2Bi	277G	21	2000
NJMOP277FR (TE1)	(VSP8)				277F		
NJMOP2277GE (TE1)	SOP8	Yes	Yes	Sn2Bi	2277G	76	2000
NJMOP2277FE (TE1)	JEDEC150mil				2277F		
NJMOP2277GR (TE1)	MSOP8	Yes	Yes	Sn2Bi	2277G	21	2000
NJMOP2277FR (TE1)	(VSP8)				2277F		
NJMOP2277KW2 (TE3)	DFN8-W2 (ESON8-W2)	Yes	Yes	Sn2Bi	2277	18	1500

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	
Supply Voltage	$V^+ - V^-$	40	V	
Differential Input Voltage ⁽¹⁾	V_{ID}	$\pm 40^{(2)}$	V	
Input Voltage ⁽³⁾	V_{IN}	$V^- - 0.3$ to $V^+ + 0.3$	V	
Input Current ⁽⁴⁾	I_{IN}	10	mA	
Output Short-Circuit Duration ⁽⁵⁾	-	Infinite ($T_a \leq 25^\circ\text{C}$)	-	
Power Dissipation ($T_a = 25^\circ\text{C}$)	P_D	NJMOP277	mW	
		2-Layer / 4-Layer		2-Layer / 4-Layer
		700 / 1000		800 / 1200
		500 / 660		600 / 820
SOP8 JEDEC150mil ⁽⁶⁾				
MSOP8 (VSP8) ⁽⁶⁾				
DFN8-W2 (ESON8-W2) ⁽⁷⁾				
Maximum Junction Temperature	T_{jmax}	150	$^\circ\text{C}$	
Storage Temperature Range	T_{stg}	-55 to 150	$^\circ\text{C}$	

(1) Differential voltage is the voltage difference between +INPUT and - INPUT.

(2) For supply voltage less than +40V, the absolute maximum rating is equal to the supply voltage.

(3) The absolute maximum input voltage is limited at 40V.

(4) If the input voltage exceeds the supply voltage, the input current must be limited 10 mA or less by using a restriction resistance.

(5) Continuous short-circuits from output to GND is guaranteed only when $V^+ \leq 11\text{V}$ ($\pm 5.5\text{V}$) and into 1ch.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-Ambient Thermal Resistance	θ_{ja}	NJMOP277	NJMOP2277	$^\circ\text{C} / \text{W}$
		2-Layer / 4-Layer	2-Layer / 4-Layer	
		181 / 122	160 / 104	
		252 / 189	207 / 152	
SOP8 JEDEC150mil ⁽⁶⁾				
MSOP8 (VSP8) ⁽⁶⁾				
DFN8-W2 (ESON8-W2) ⁽⁷⁾				
Junction-to-Top of package characterization parameter	ψ_{jt}	NJMOP277	NJMOP2277	$^\circ\text{C} / \text{W}$
		2-Layer / 4-Layer	2-Layer / 4-Layer	
		32 / 27	16 / 13	
		62 / 53	32 / 24	
SOP8 JEDEC150mil ⁽⁶⁾				
MSOP8 (VSP8) ⁽⁶⁾				
DFN8-W2 (ESON8-W2) ⁽⁷⁾				

(6) 2-Layer: Mounted on glass epoxy board. (76.2x114.3x1.6mm: based on EIA/JDEC standard, 2-layers FR-4)

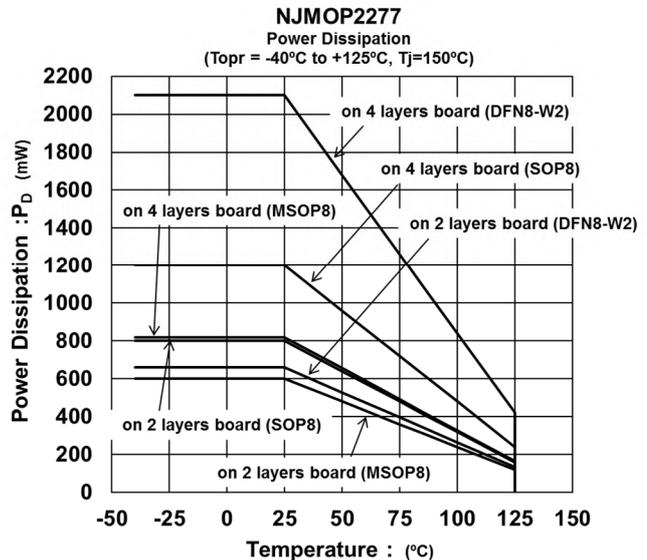
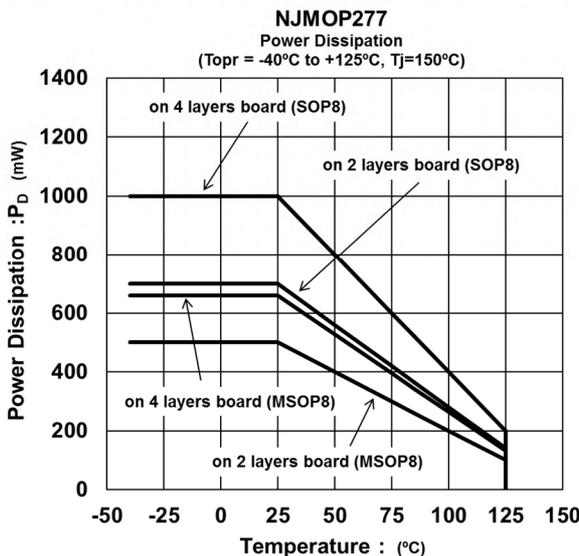
4-Layer: Mounted on glass epoxy board. (76.2x114.3x1.6mm: based on EIA/JDEC standard, 4-layers FR-4), internal Cu area: 74.2 x 74.2mm

(7) 2-Layer: Mounted on glass epoxy board. (101.5x114.5x1.6mm: based on EIA/JDEC standard, 2-layers FR-4, with Exposed Pad)

4-Layer: Mounted on glass epoxy board. (101.5x114.5x1.6mm: based on EIA/JDEC standard, 4-layers FR-4, with Exposed Pad)

*For 4-Layers: Applying 99.5x99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage Single Supply Dual Supply	V ⁺ -V ⁻ V ⁺ /V ⁻	T _a =25°C	4.5 to 36 ±2.25 to ±18	V
Operating Temperature Range	T _{opr}		-40 to 125	°C

ELECTRICAL CHARACTERISTICS

NJMOP277GE / NJMOP277FE / NJMOP277GR / NJMOP277FR, NJMOP2277GE / NJMOP2277FE / NJMOP2277GR / NJMOP2277FR
(V⁺/V⁻ = ±5V to ±15V, T_a=25°C, V_{COM}=0V, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
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INPUT CHARACTERISTICS

Input Offset Voltage	V _{IO}	F-Grade	V _{COM} =0V, R _S =50Ω T _a = -40°C to 125°C	-	10	20	μV
		G-Grade	V _{COM} =0V, R _S =50Ω T _a = -40°C to 125°C	-	-	50	μV
Input Offset Voltage Drift	ΔV _{IO} /ΔT	F-Grade	V _{COM} =0V, R _S =50Ω, T _a = -40°C to 125°C	-	0.1	0.15	μV/°C
		G-Grade		-	0.1	0.6	μV/°C
Input Bias Current	I _B	V _{COM} =0V T _a = -40°C to 125°C		-	0.5	2.5	nA
				-	-	4	nA
Input Offset Current	I _{IO}	F-Grade	V _{COM} =0V T _a = -40°C to 125°C	-	0.5	1	nA
		G-Grade	V _{COM} =0V T _a = -40°C to 125°C	-	-	2	nA
Open-Loop Voltage Gain	A _{V1}	V _O =(V ⁺ +0.5V) to (V ⁺ -1.5V) R _L =10kΩ to 0V		126	140	-	dB
	A _{V2}	V _O =(V ⁺ +1.5V) to (V ⁺ -2V), R _L =2kΩ to 0V T _a = -40°C to 125°C		126 120	134 -	- -	dB
Common-Mode Rejection Ratio	CMR	V _{ICM} =(V ⁺ +2V) to (V ⁺ -2V) T _a = -40°C to 125°C		115 115	140 -	- -	dB
Common-Mode Input Voltage Range	V _{ICM}	CMR	115dB	V ⁺ +2	-	V ⁺ -2	V
				V ⁺ +2	-	V ⁺ -2	V

OUTPUT CHARACTERISTICS

High-level Output Voltage	V _{OH1}	R _L =10kΩ to 0V T _a = -40°C to 125°C	V ⁺ -1.5 V ⁺ -1.5	V ⁺ -1.25 -	- -	V V
	V _{OH2}	R _L =2kΩ to 0V T _a = -40°C to 125°C	V ⁺ -2 V ⁺ -2	V ⁺ -1.3 -	- -	V V
Low-level Output Voltage	V _{OL1}	R _L =10kΩ to 0V T _a = -40°C to 125°C	- -	V ⁺ +0.2 -	V ⁺ +0.5 V ⁺ +0.5	V V
	V _{OL2}	R _L =2kΩ to 0V T _a = -40°C to 125°C	- -	V ⁺ +0.5 -	V ⁺ +1.5 V ⁺ +1.5	V V
Short-circuit Output Current	I _{SC}	Short to 0V	-	±30	-	mA

POWER SUPPLY CHARACTERISTICS

Supply Current per Channel	I _{SUPPLY}	No Signal, R _L =OPEN T _a = -40°C to 125°C	- -	760 -	800 900	μA μA
				120 120	140 -	- -
Supply Voltage Rejection Ratio	SVR	V ⁺ /V ⁻ = ±2.25V to ±15V T _a = -40°C to 125°C	120 120	140 -	- -	dB dB

■ ELECTRICAL CHARACTERISTICS

NJMOP277GE / NJMOP277FE / NJMOP277GR / NJMOP277FR, NJMOP2277GE / NJMOP2277FE / NJMOP2277GR / NJMOP2277FR
continued

($V^+ / V^- = \pm 5V$ to $\pm 15V$, $T_a = 25^\circ C$, $V_{COM} = 0V$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS						
Gain Bandwidth Product	GBW	$R_L = 2k\Omega$ to $0V$, $C_L = 20pF$, $f = 10kHz$	-	1	-	MHz
Phase Margin	Φ_m	$R_L = 2k\Omega$ to $0V$, $C_L = 20pF$	-	65	-	deg
Gain Margin	G_m	$R_L = 2k\Omega$ to $0V$, $C_L = 20pF$	-	20	-	dB
Slew Rate	SR	$G_V = 0dB$, $R_L = 2k\Omega$ to $0V$, $C_L = 20pF$ $V_{IN} = 5V_{pp}$	-	0.7	-	$V/\mu s$
Settling Time to 0.1%	t_s	$G_V = 0dB$, $R_L = 2k\Omega$ to $0V$, $C_L = 20pF$ $V_{IN} = 10V_{pp}$	-	14	-	μs
Equivalent Input Noise Voltage	e_n	$f = 1kHz$	-	8	-	nV/\sqrt{Hz}
	V_n	$f = 0.1Hz$ to $10Hz$	-	0.2	-	μV_{pp}
Equivalent Input Noise Current	i_n	$f = 1kHz$	-	0.2	-	pA/\sqrt{Hz}
Total Harmonic Distortion + Noise	THD+N	$G_V = 0dB$, $R_L = 2k\Omega$ to $0V$, $C_L = 20pF$ $V_O = 10V_{pp}$, $f = 1kHz$	-	0.002	-	%
Channel Separation	CS	$f = 1kHz$	-	120	-	dB

■ ELECTRICAL CHARACTERISTICS

NJMOP2277KW2

($V^+ / V^- = \pm 5V$ to $\pm 15V$, $T_a = 25^\circ C$, $V_{COM} = 0V$, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{IO}	$V_{COM}=0V, R_S=50\Omega$	-	20	100	μV
		$T_a = -40^\circ C$ to $125^\circ C$	-	-	150	μV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$V_{COM}=0V, R_S=50\Omega, T_a = -40^\circ C$ to $125^\circ C$	-	0.15	0.7	$\mu V/^\circ C$
Input Bias Current	I_B	$V_{COM}=0V$	-	0.5	2.5	nA
		$T_a = -40^\circ C$ to $125^\circ C$	-	-	6	nA
Input Offset Current	I_{IO}	$V_{COM}=0V$	-	0.5	2	nA
		$T_a = -40^\circ C$ to $125^\circ C$	-	-	3	nA
Open-Loop Voltage Gain	A_{V1}	$V_O=(V^++0.5V)$ to $(V^+-1.5V)$ $R_L=10k\Omega$ to $0V$	126	140	-	dB
	A_{V2}	$V_O=(V^++1.5V)$ to (V^+-2V) , $R_L=2k\Omega$ to $0V$ $T_a = -40^\circ C$ to $125^\circ C$	126 120	134 -	- -	dB
Common-Mode Rejection Ratio	CMR	$V_{ICM}=(V^++2V)$ to (V^+-2V) $T_a = -40^\circ C$ to $125^\circ C$	115 115	140 -	- -	dB
Common-Mode Input Voltage Range	V_{ICM}	CMR 115dB	V^++2	-	V^+-2	V
		$T_a = -40^\circ C$ to $125^\circ C$	V^++2	-	V^+-2	V

OUTPUT CHARACTERISTICS

High-level Output Voltage	V_{OH1}	$R_L=10k\Omega$ to $0V$ $T_a = -40^\circ C$ to $125^\circ C$	$V^+-1.5$ $V^+-1.5$	$V^+-1.25$ -	- -	V V
	V_{OH2}	$R_L=2k\Omega$ to $0V$ $T_a = -40^\circ C$ to $125^\circ C$	V^+-2 V^+-2	$V^+-1.3$ -	- -	V V
Low-level Output Voltage	V_{OL1}	$R_L=10k\Omega$ to $0V$ $T_a = -40^\circ C$ to $125^\circ C$	- -	$V^++0.2$ -	$V^++0.5$ $V^++0.5$	V V
	V_{OL2}	$R_L=2k\Omega$ to $0V$ $T_a = -40^\circ C$ to $125^\circ C$	- -	$V^++0.5$ -	$V^++1.5$ $V^++1.5$	V V
Short-circuit Output Current	I_{SC}	Short to $0V$	-	± 30	-	mA

POWER SUPPLY CHARACTERISTICS

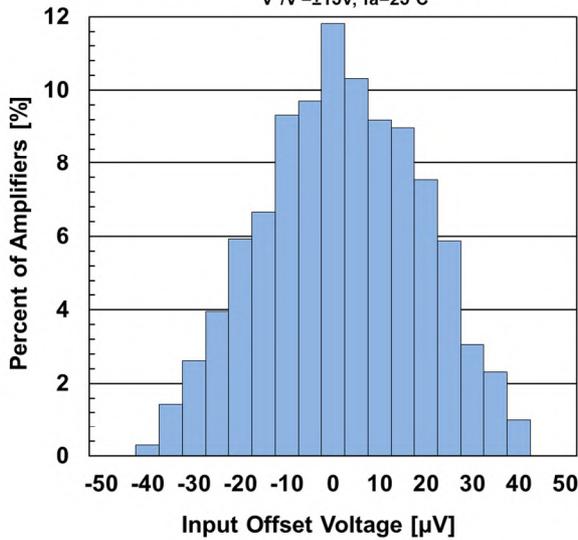
Supply Current per Channel	I_{SUPPLY}	No Signal, $R_L=OPEN$	-	760	800	μA
		$T_a = -40^\circ C$ to $125^\circ C$	-	-	900	μA
Supply Voltage Rejection Ratio	SVR	$V^+ / V^- = \pm 2.25V$ to $\pm 15V$	120	140	-	dB
		$T_a = -40^\circ C$ to $125^\circ C$	120	-	-	dB

AC CHARACTERISTICS

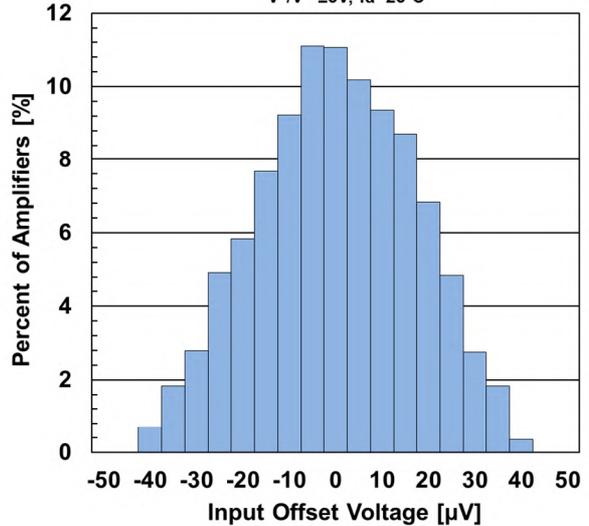
Gain Bandwidth Product	GBW	$R_L=2k\Omega$ to $0V, C_L=20pF, f=10kHz$	-	1	-	MHz
Phase Margin	Φ_m	$R_L=2k\Omega$ to $0V, C_L=20pF$	-	65	-	deg
Gain Margin	G_m	$R_L=2k\Omega$ to $0V, C_L=20pF$	-	20	-	dB
Slew Rate	SR	$G_V=0dB, R_L=2k\Omega$ to $0V, C_L=20pF$ $V_{IN}=5V_{pp}$	-	0.7	-	V/ μs
Settling Time to 0.1%	t_s	$G_V=0dB, R_L=2k\Omega$ to $0V, C_L=20pF$ $V_{IN}=10V_{pp}$	-	14	-	μs
Equivalent Input Noise Voltage	e_n	$f=1kHz$	-	8	-	nV/ Hz
	V_n	$f=0.1Hz$ to $10Hz$	-	0.2	-	μV_{pp}
Equivalent Input Noise Current	I_n	$f=1kHz$	-	0.2	-	pA/ Hz
Total Harmonic Distortion + Noise	THD+N	$G_V=0dB, R_L=2k\Omega$ to $0V, C_L=20pF$ $V_O=10V_{pp}, f=1kHz$	-	0.002	-	%
Channel Separation	CS	$f=1kHz$	-	120	-	dB

■ TYPICAL CHARACTERISTICS

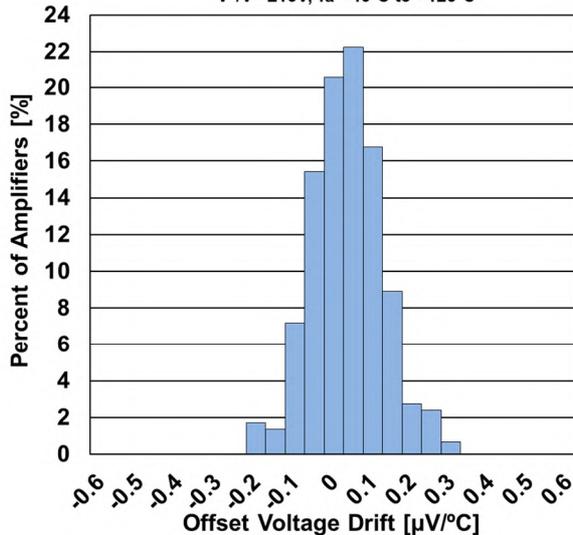
Input Offset Voltage Distribution(MSOP)
 $V^+ / V^- = \pm 15V, T_a = 25^\circ C$



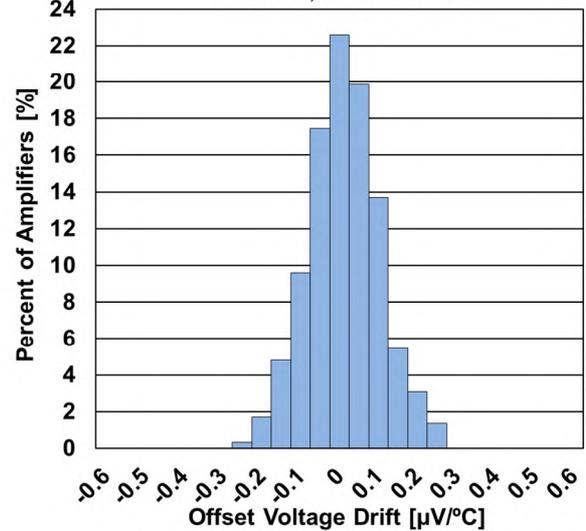
Input Offset Voltage Distribution(MSOP)
 $V^+ / V^- = \pm 5V, T_a = 25^\circ C$



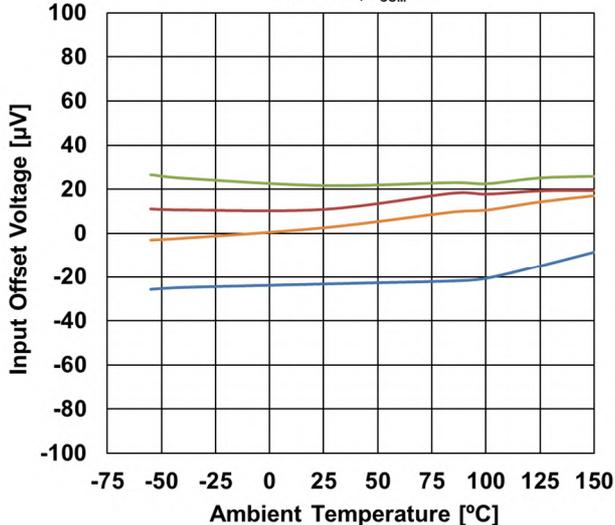
Offset Voltage Drift Distribution(MSOP)
 $V^+ / V^- = \pm 15V, T_a = -40^\circ C \text{ to } +125^\circ C$



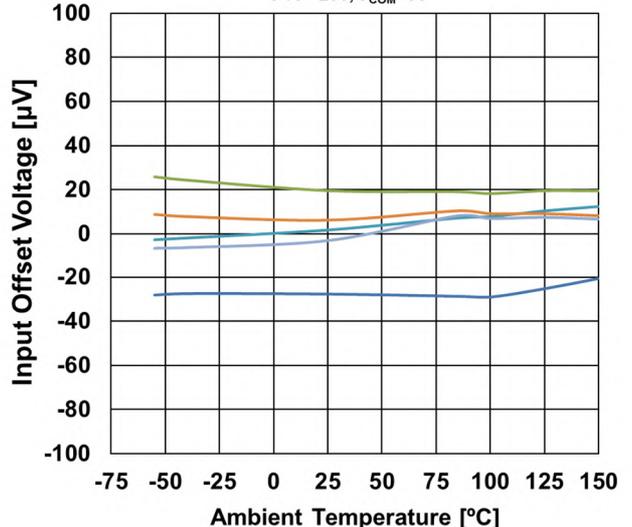
Offset Voltage Drift Distribution(MSOP)
 $V^+ / V^- = \pm 5V, T_a = -40^\circ C \text{ to } +125^\circ C$



Input Offset Voltage vs. Temperature
 $V^+ / V^- = \pm 15V, V_{COM} = 0V$



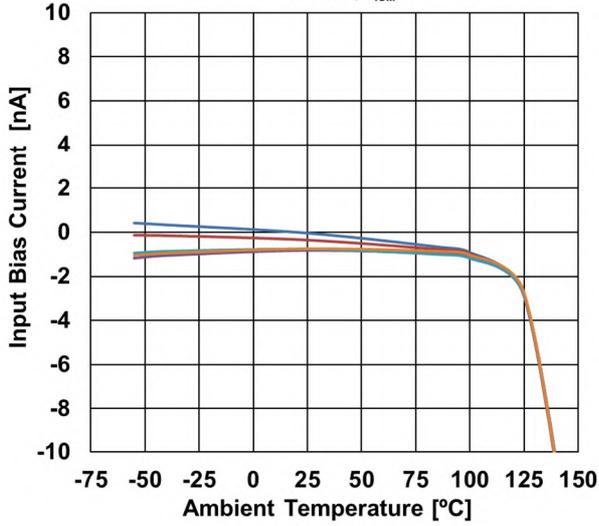
Input Offset Voltage vs. Temperature
 $V^+ / V^- = \pm 5V, V_{COM} = 0V$



■ TYPICAL CHARACTERISTICS

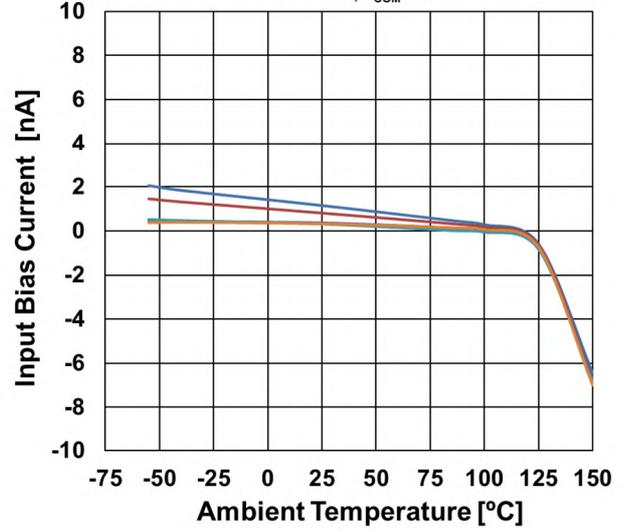
Input Bias Current vs. Temperature

$V^*/V = \pm 15V, V_{COM} = 0V$



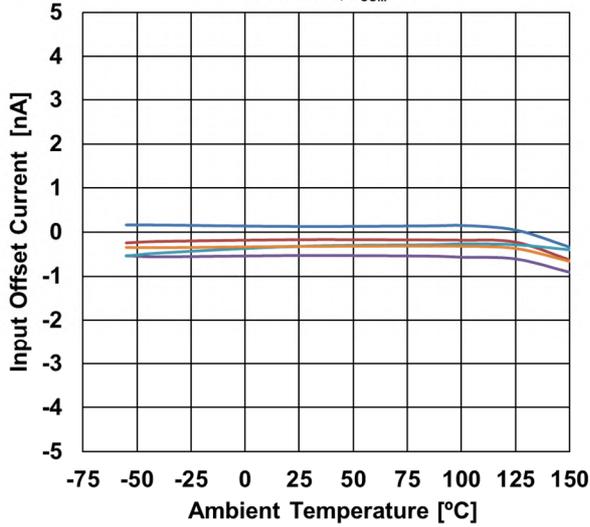
Input Bias Current vs. Temperature

$V^*/V = \pm 5V, V_{COM} = 0V$



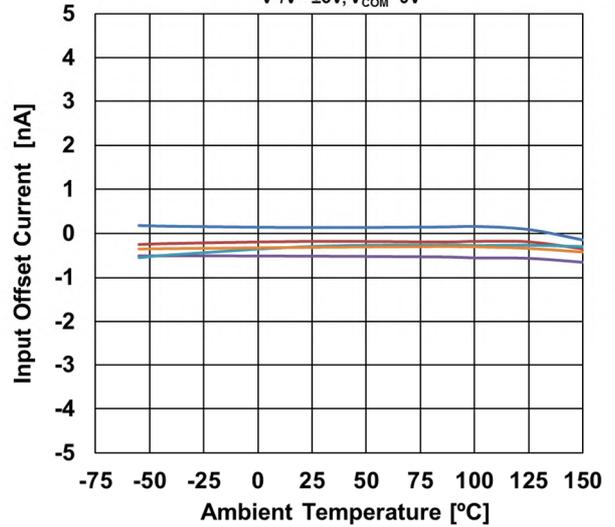
Input Offset Current vs. Temperature

$V^*/V = \pm 15V, V_{COM} = 0V$



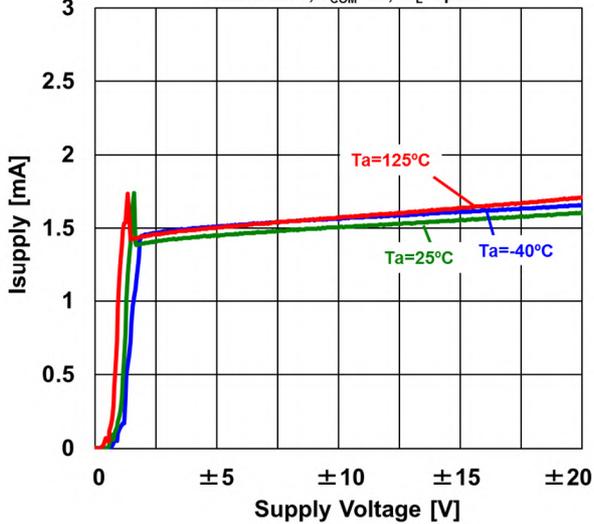
Input Offset Current vs. Temperature

$V^*/V = \pm 5V, V_{COM} = 0V$



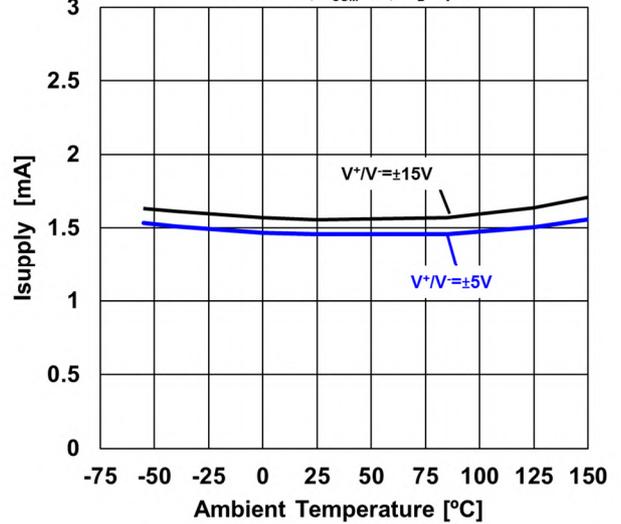
Supply Current vs. Supply Voltage

NJMOP2277, $V_{COM} = 0V, R_L = \text{open}$



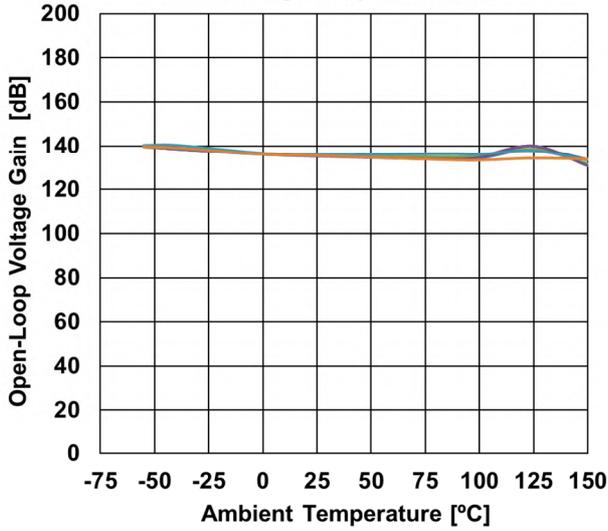
Supply Current vs. Temperature

NJMOP2277, $V_{COM} = 0V, R_L = \text{open}$

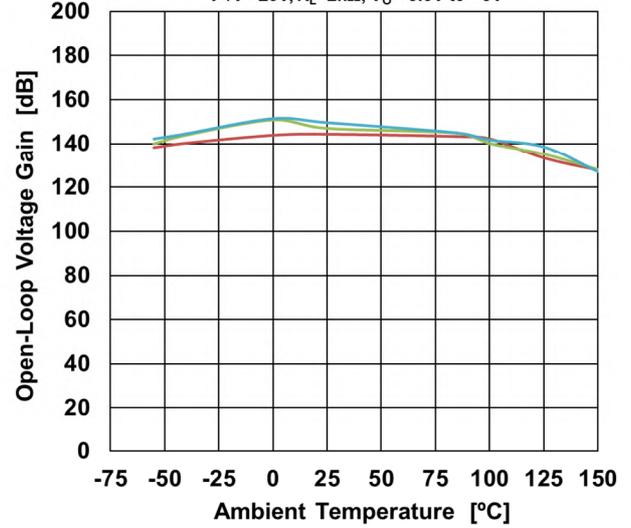


■ TYPICAL CHARACTERISTICS

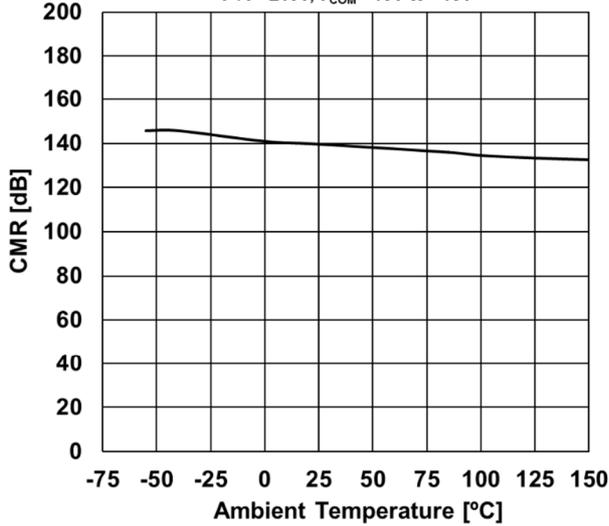
Open-Loop Voltage Gain vs. Temperature
 $V^+ / V^- = \pm 15V, R_L = 2k\Omega, V_O = -13.5V \text{ to } +13V$



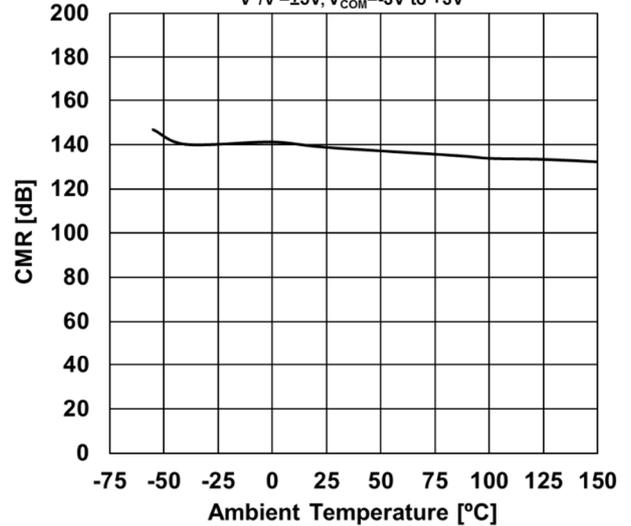
Open-Loop Voltage Gain vs. Temperature
 $V^+ / V^- = \pm 5V, R_L = 2k\Omega, V_O = -3.5V \text{ to } +3V$



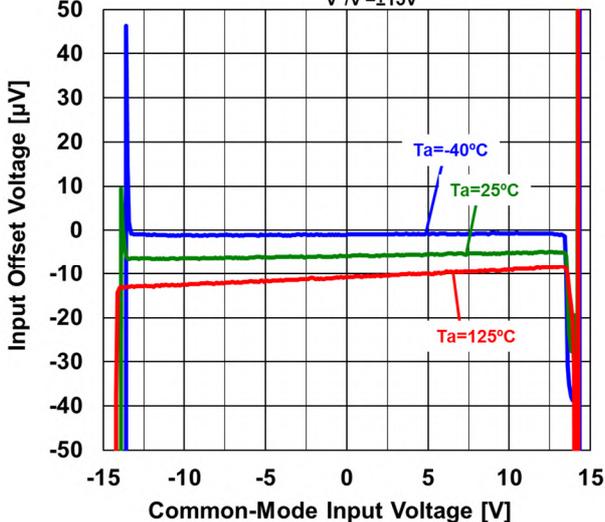
CMR vs. Temperature
 $V^+ / V^- = \pm 15V, V_{COM} = -13V \text{ to } +13V$



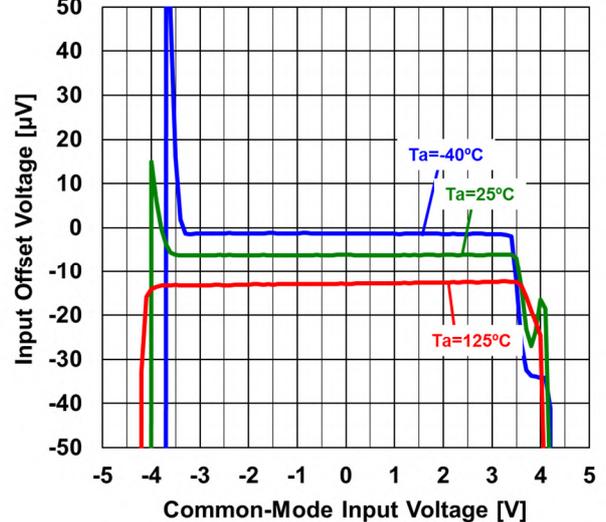
CMR vs. Temperature
 $V^+ / V^- = \pm 5V, V_{COM} = -3V \text{ to } +3V$



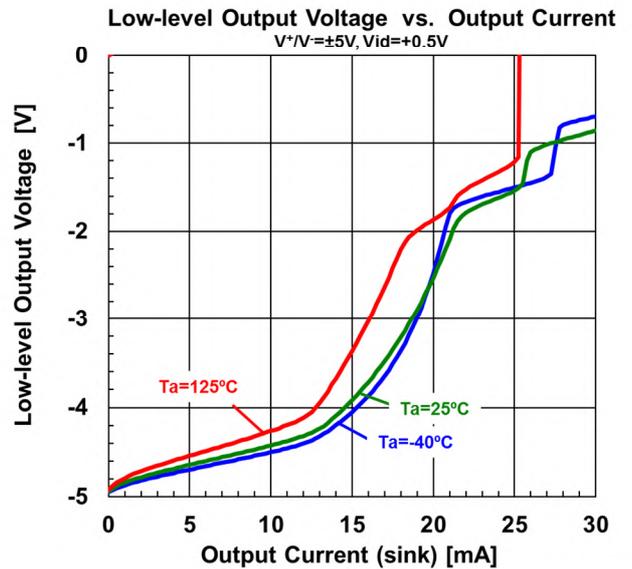
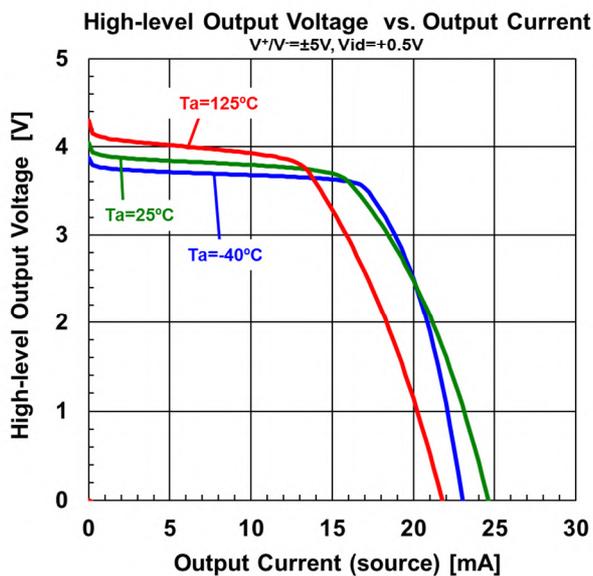
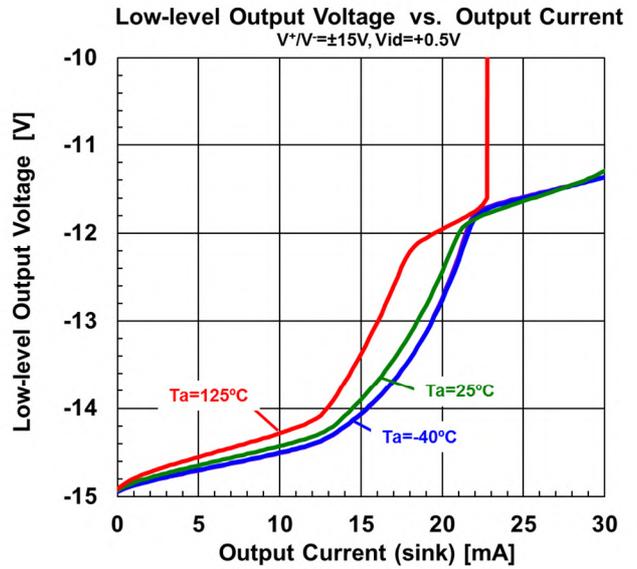
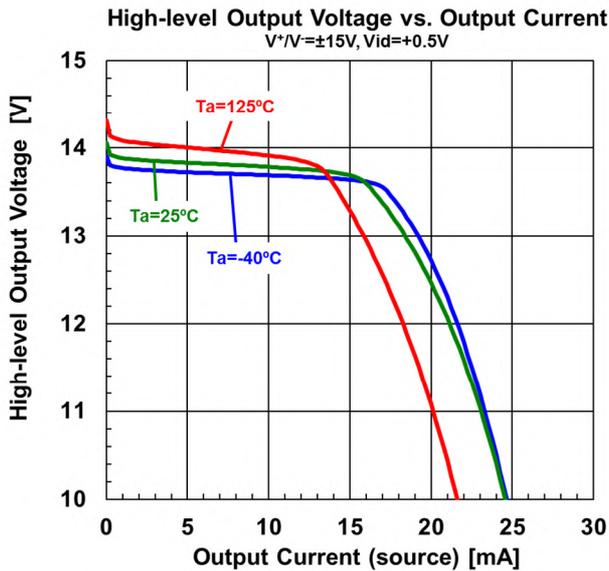
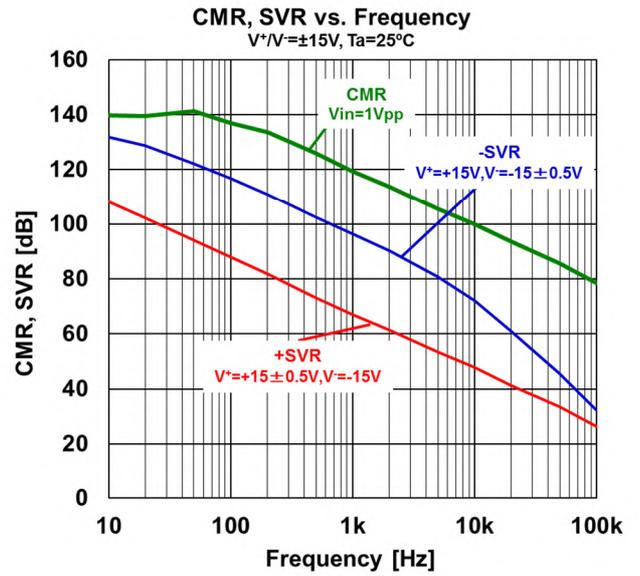
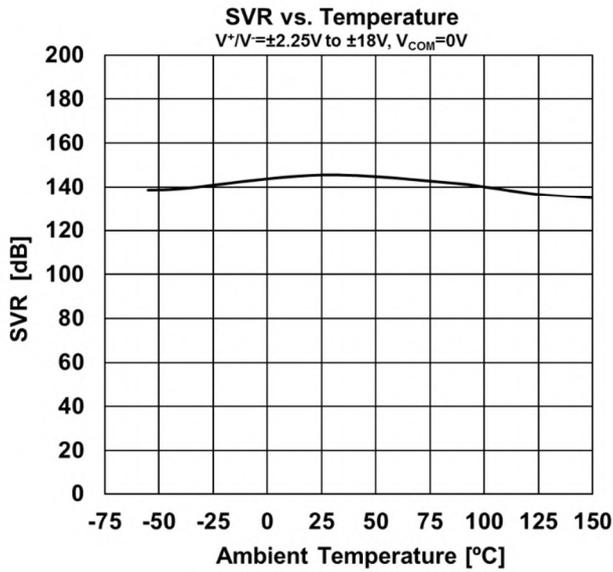
Input Offset Voltage vs. Common-Mode Input Voltage
 $V^+ / V^- = \pm 15V$



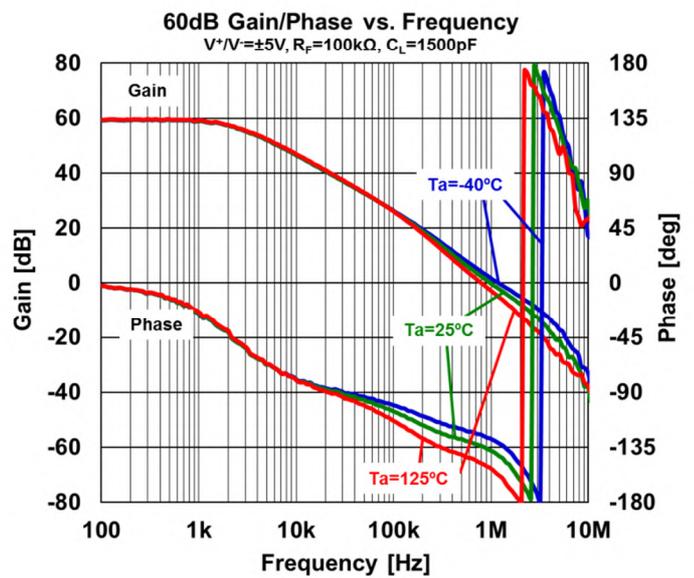
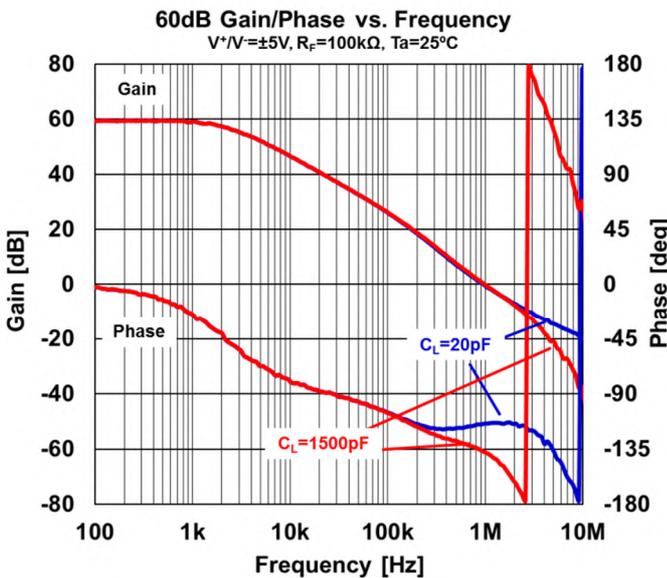
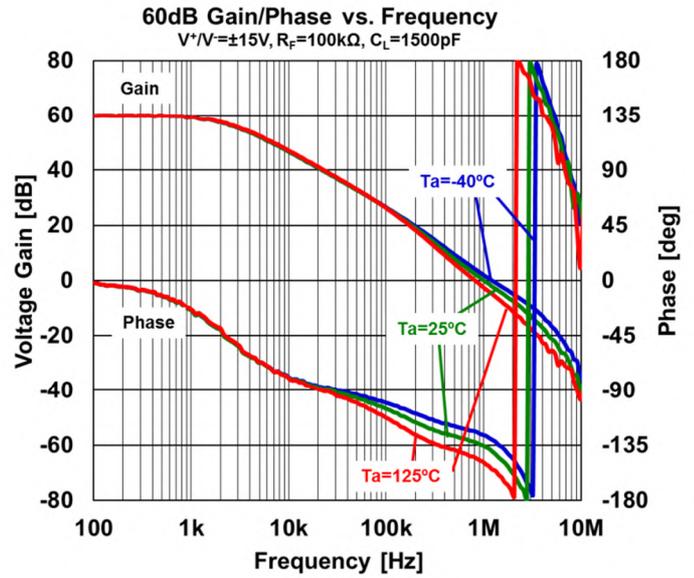
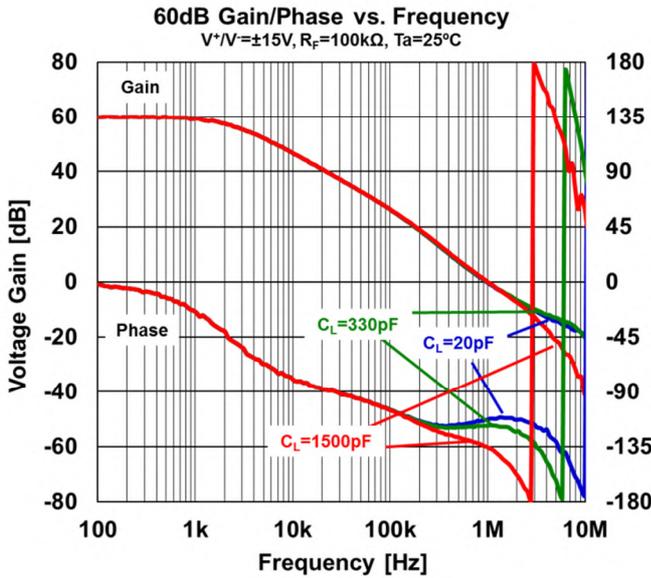
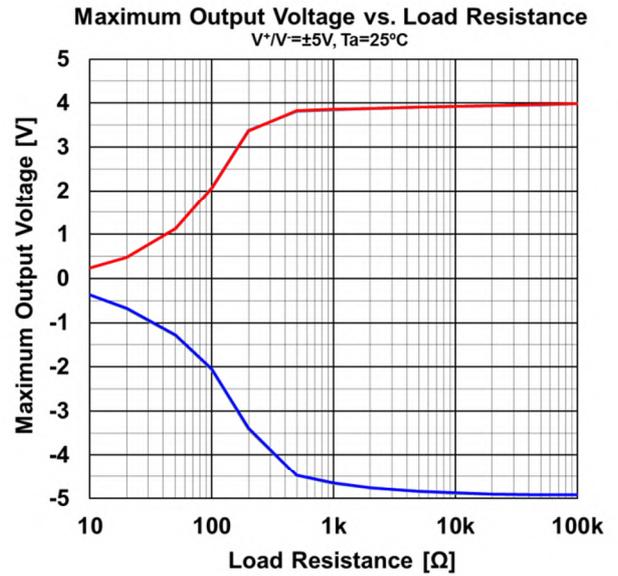
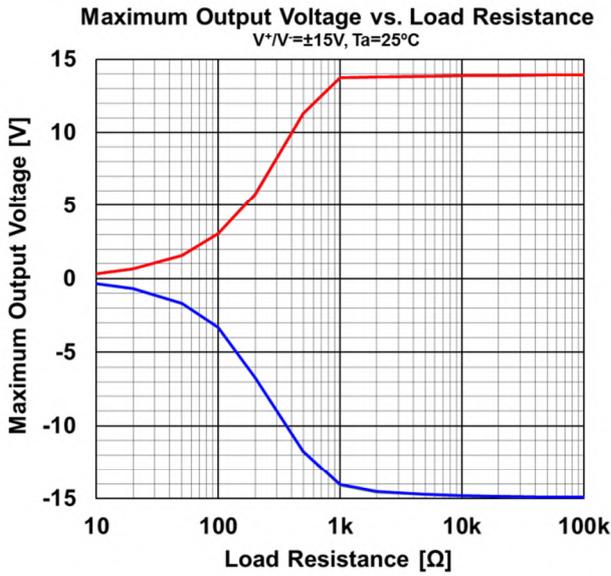
Input Offset Voltage vs. Common-Mode Input Voltage
 $V^+ / V^- = \pm 5V$



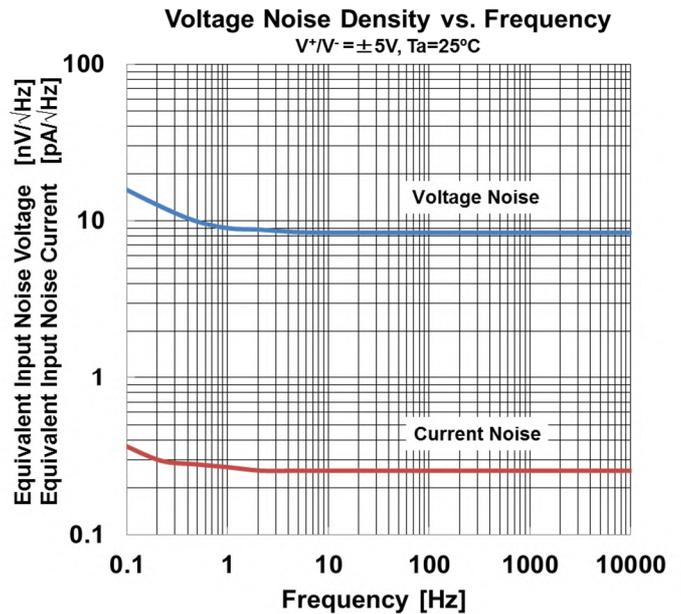
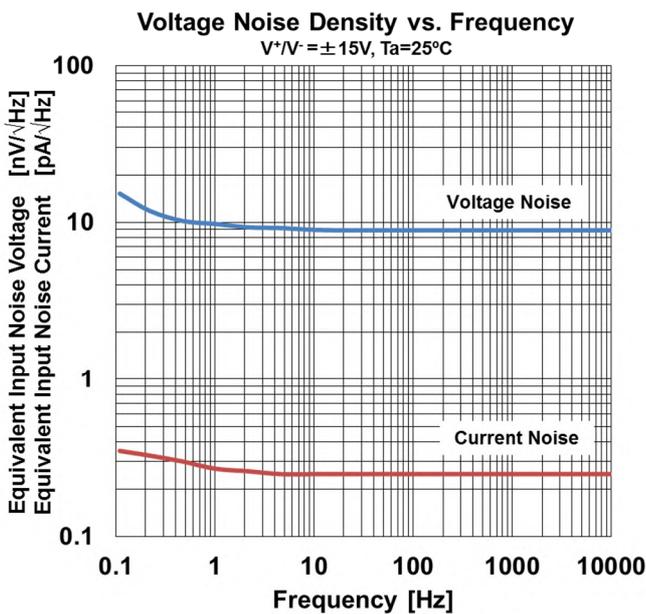
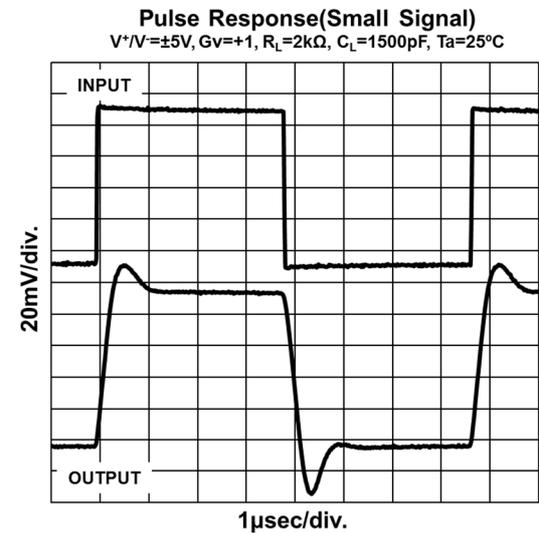
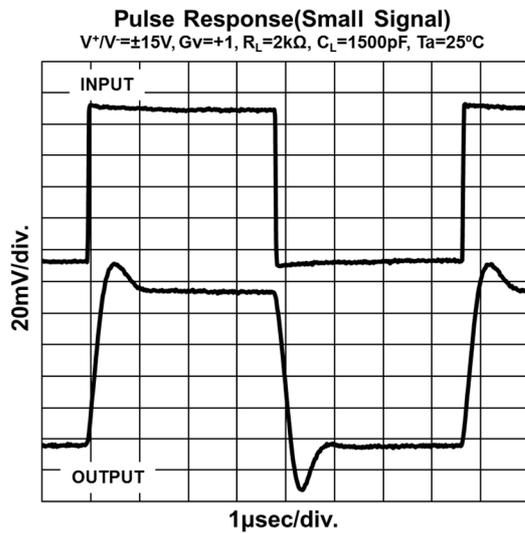
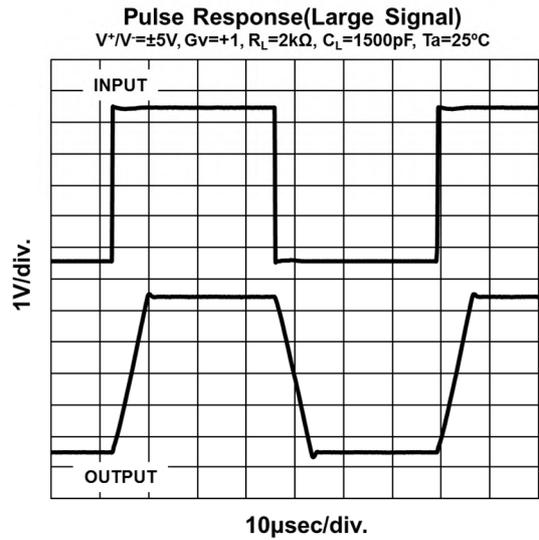
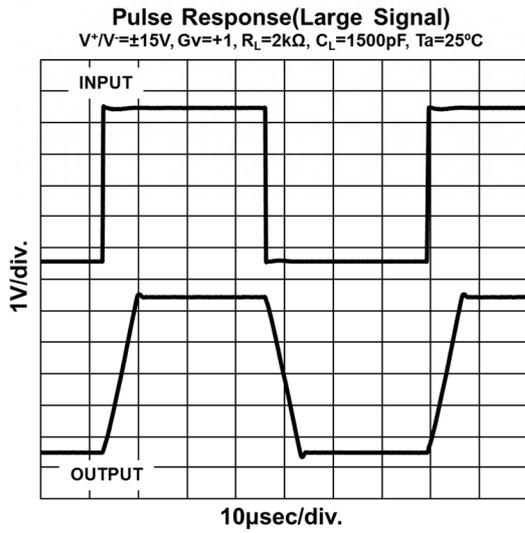
■ TYPICAL CHARACTERISTICS



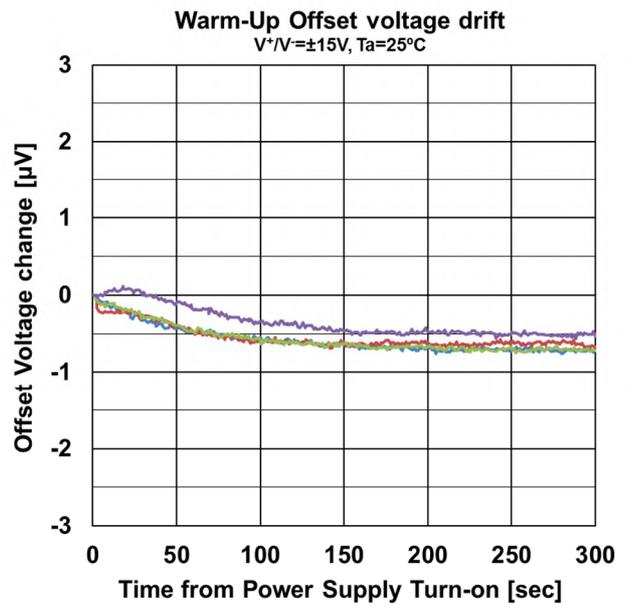
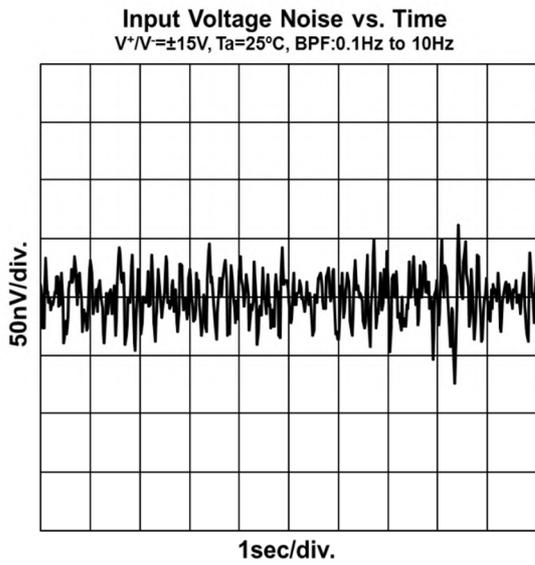
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



APPLICATION NOTE

Regarding High Precision Operational Amplifier

The NJMOP277 / NJMOP2277 are High Precision Operational Amplifiers featuring low offset voltage and low offset voltage thermal drift. To maximize such a high performance with stable operation, please pay attention to thermocouple effect (Seebeck Effect) and/or Piezo effect.

Thermoelectronic Effect [Seebeck Effect]

The thermoelectromotive force is generated by a temperature gradient when there is contact with dissimilar metals such as relays and switches. The difference in thermoelectromotive force (EMF) between both input pins is output as the input offset voltage. In addition, it is effective to take care to generate an equivalent thermoelectromotive force (EMF) at both input pins in order to reduce the influence of thermoelectromotive force (EMF) on the input offset voltage.

Piezoelectric Effect

When IC is mounted, when stress is applied to the IC, such as warping or bending of the board, a transistor characteristics inside the IC may fluctuate by the piezoelectric effect. Mainly the input offset voltage fluctuates. For high-precision operational amplifiers, chip layout design has been carefully designed to reduce the influence of stress, but the input offset voltage of several μV to several tens μV may fluctuate due to stress at the time of mounting.

Attention: the specification value guarantees the characteristics at the time of factory shipment. The characteristic values after mounting may vary depending on the package type, component placement on the board, material of the board and mounting conditions etc., you should evaluate sufficiently with the actual application.

Power Supply Bypassing

The NJMOP277 / NJMOP2277 are high precision operational amplifier featuring low offset voltage, high voltage gain, high CMR, high SVR and so on. To maximize such a high performance with stable operation, the NJMOP277 / NJMOP2277 should be operated by clean and low impedance supply voltage. So, the bypass capacitor should be connected to these both power supply terminals (V^+ and V^-) as shown in figure1. The bypass capacitors should be placed as close as possible to IC package.

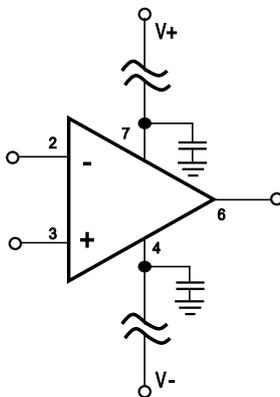


figure1.

Differential Amplifier

NJMOP277 / NJMOP2277 are Operational Amplifier featuring $\text{CMR}=140\text{ dB typ.}$

Differential amplifier (see below figure2) is used in high accuracy circuit to improve common mode rejection ratio (CMR).

A matching between the ratio $R_1/R_2 = R_3/R_4$ and $R_1=R_3$ makes the high CMR For example, acceptable error range to obtain CMR of 130dB or more is about 0.1ppm.

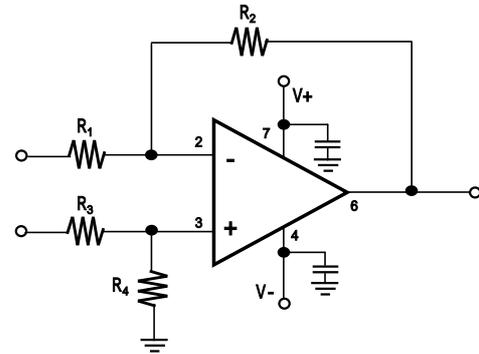


figure2.

Single and Dual Supply Voltage Operation

NJMOP277 / NJMOP2277 works with both single supply and dual supply when the voltage supplied is between V^+ and V^- . These amplifiers operate from single +4.5 to +36V supply and dual $\pm 2.25\text{V}$ to $\pm 18\text{V}$ supply.

Input Voltage Exceeding the Supply Voltage

NJMOP277 / NJMOP2277 are protected by ESD diodes (shown in figure3) that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply, inputs can be tolerated if the current is limited to 10mA. figure4 is easily accomplished with an input resistor. If the input voltage exceeds the supply voltage, the input current must be limited 10mA or less by using a restriction resistance (R_{LIMIT}) as shown in figure4.

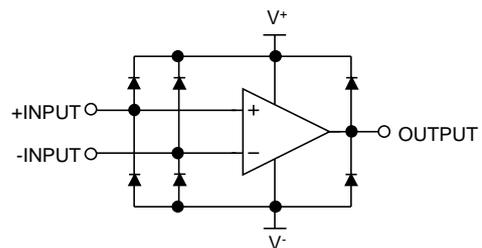


figure3. Simplified Schematic

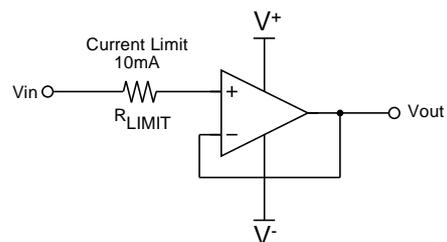


figure4.. Input Current Protection

■ APPLICATION NOTE

EMIRR (EMI Rejection Ratio) Definition

EMIRR is a parameter indicating the EMI robustness of an OP-Amp. The definition of EMIRR is given by the following a formula (1). We can grasp the tolerance of the RF signal by measuring an RF signal and offset voltage shift quantity.

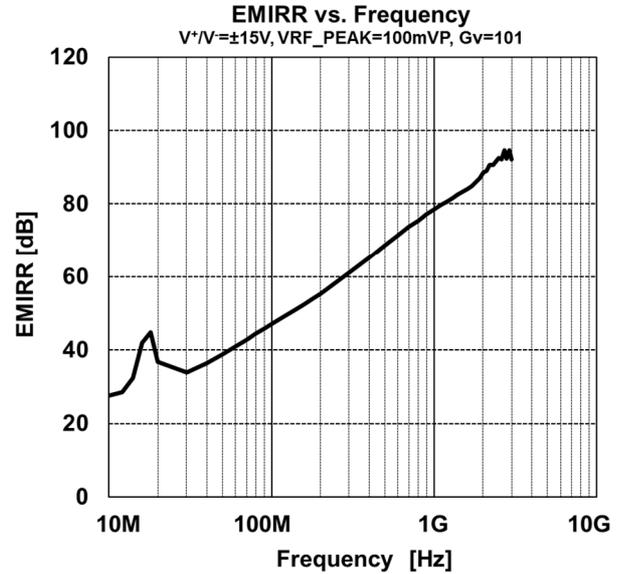
$$EMIRR = 20 \cdot \log \left(\frac{V_{RF_PEAK}}{|\Delta V_{IO}|} \right) \quad \dots(1)$$

V_{RF_PEAK} : RF Signal Amplitude [V_p]

V_{IO} : Input offset voltage shift quantity [V]

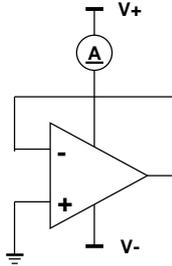
Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

*For details, refer to " Application Note for EMI Immunity" in our HP: <http://www.njr.com/>

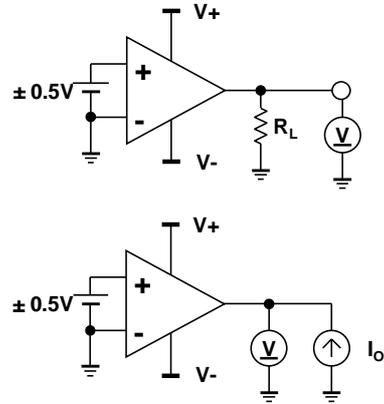


■ TYPICAL TEST CIRCUIT

• Supply Current (I_{SUPPLY})

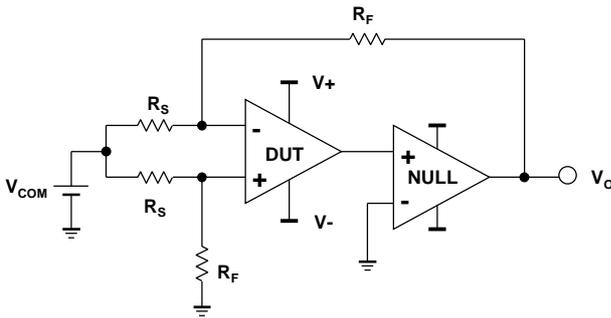


• Output Voltage (V_{OH}, V_{OL})

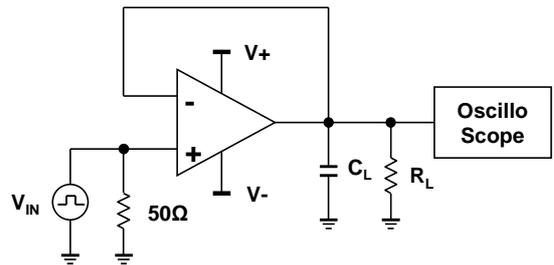


• Input Offset Voltage (V_{IO})

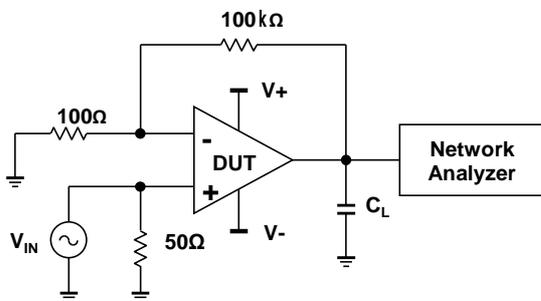
$$R_S=50, R_F=500k \quad V_{IO} = \frac{R_S}{R_S + R_F} \times V_O \quad [V]$$



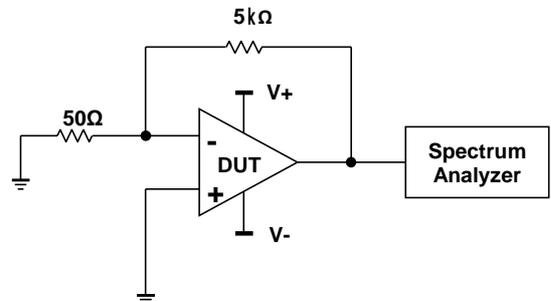
• Slew Rate (SR)



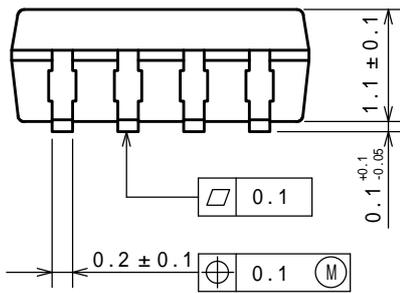
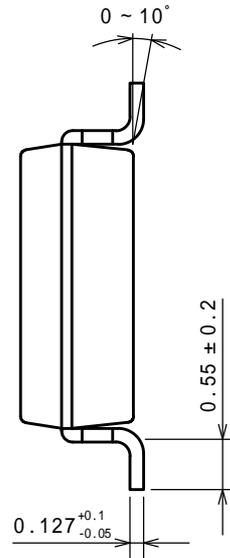
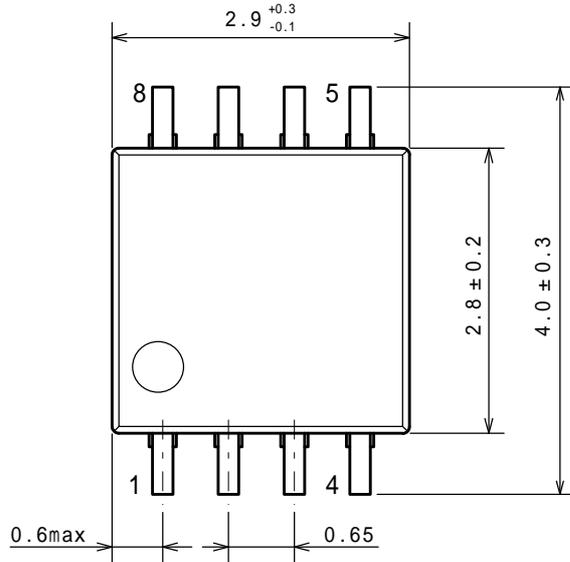
• Gain Bandwidth Product (GBW)



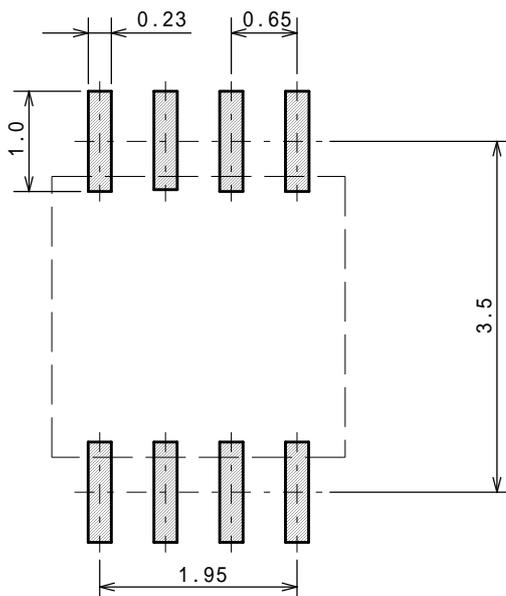
• Equivalent Input Noise Voltage (e_n)



■ PACKAGE DIMENSIONS

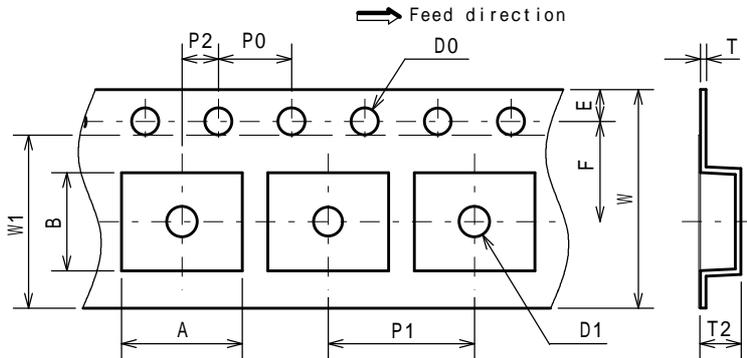


■ EXAMPLE OF SOLDER PADS DIMENSIONS



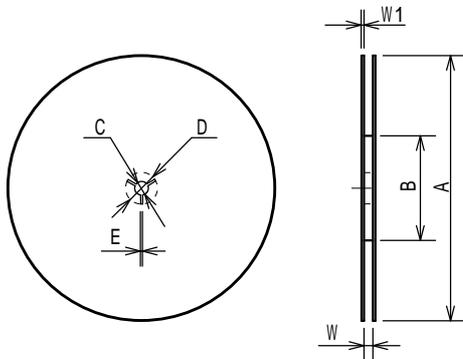
PACKING SPEC

TAPING DIMENSIONS



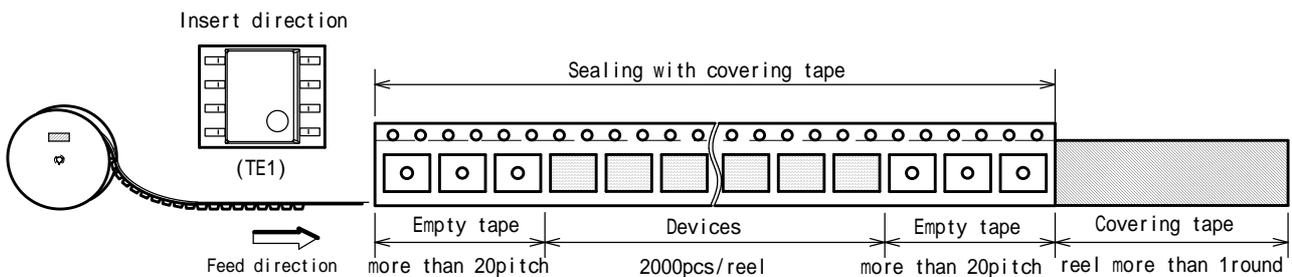
SYMBOL	DIMENSION	REMARKS
A	6.6	BOTTOM DIMENSION
B	5.4	BOTTOM DIMENSION
D0	1.5 ^{+0.1} ₀	
D1	1.7 ± 0.1	
E	1.75 ± 0.1	
F	5.5 ± 0.05	
P0	4.0 ± 0.1	
P1	8.0 ± 0.1	
P2	2.0 ± 0.05	
T	0.30 ± 0.05	
T2	2.2	
W	12.0 ± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

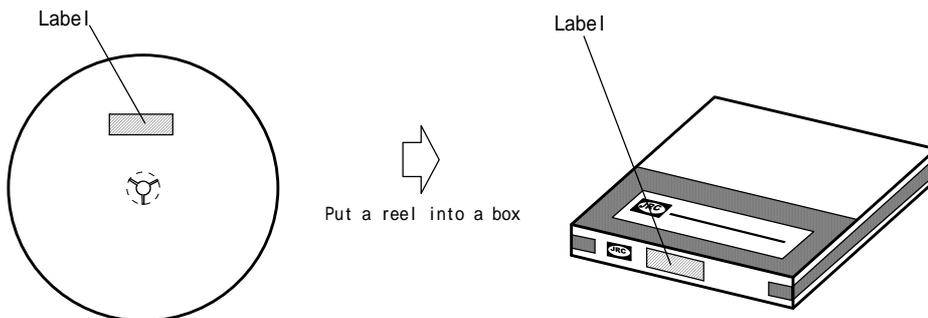


SYMBOL	DIMENSION
A	330 ± 2
B	80 ± 1
C	13 ± 0.2
D	21 ± 0.8
E	2 ± 0.5
W	13.5 ± 0.5
W1	2.0 ± 0.2

TAPING STATE

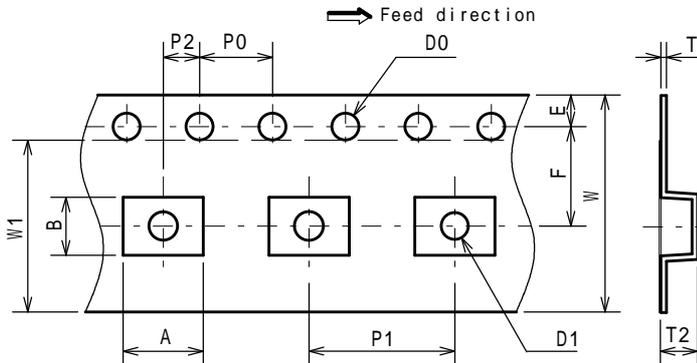


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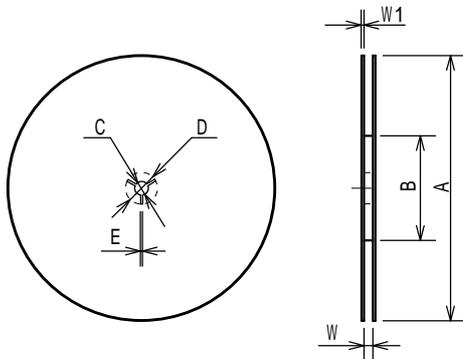
PACKING SPEC

TAPING DIMENSIONS



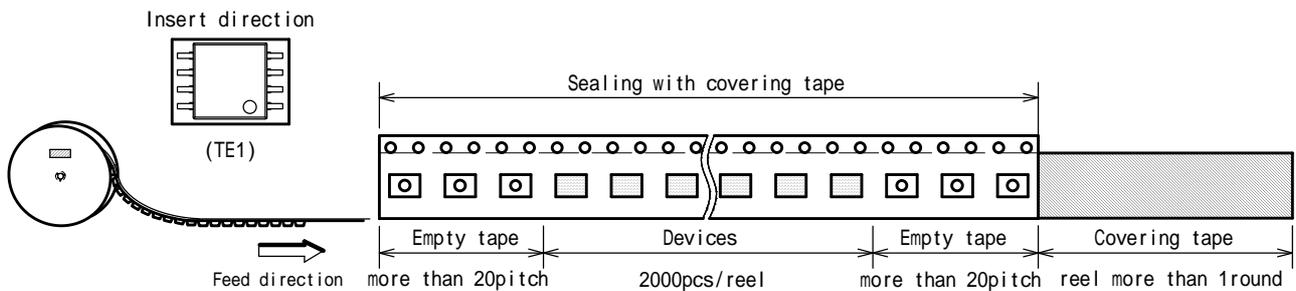
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	1.5 ^{+0.1} ₀	
D1	1.5 ^{+0.1} ₀	
E	1.75 ± 0.1	
F	5.5 ± 0.05	
P0	4.0 ± 0.1	
P1	8.0 ± 0.1	
P2	2.0 ± 0.05	
T	0.30 ± 0.05	
T2	2.0 (MAX.)	
W	12.0 ± 0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

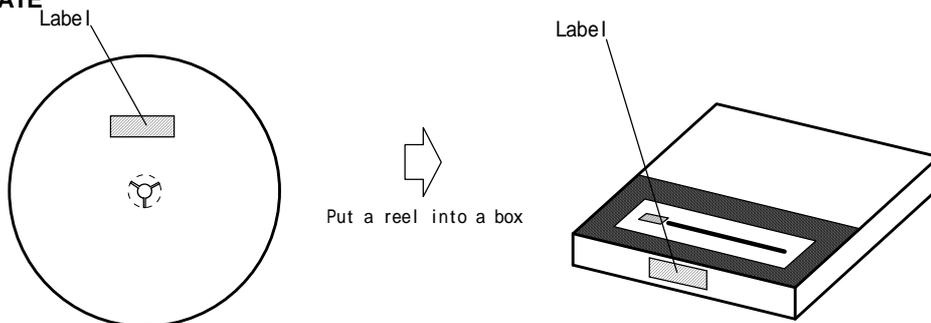


SYMBOL	DIMENSION
A	254 ± 2
B	100 ± 1
C	13 ± 0.2
D	21 ± 0.8
E	2 ± 0.5
W	13.5 ± 0.5
W1	2.0 ± 0.2

TAPING STATE



PACKING STATE

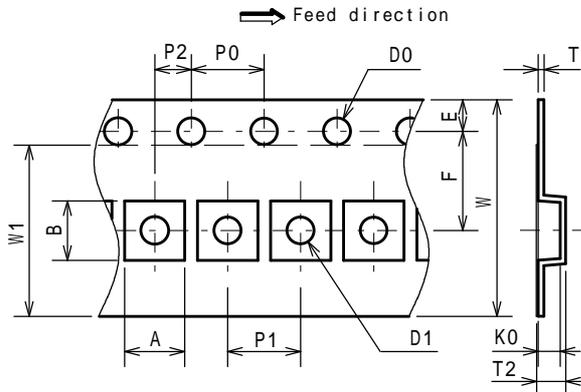


DFN8-W2 (ESON8-W2)

Unit: mm

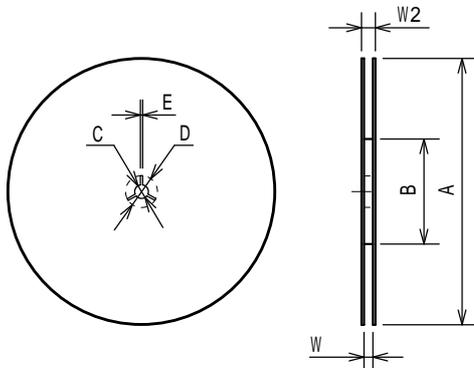
PACKING SPEC

TAPING DIMENSIONS



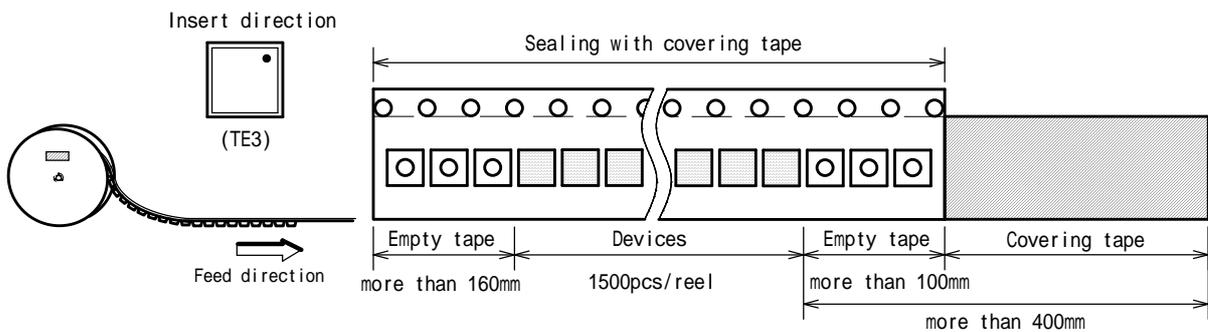
SYMBOL	DIMENSION	REMARKS
A	3.3 ± 0.1	BOTTOM DIMENSION
B	3.3 ± 0.1	BOTTOM DIMENSION
D0	$1.5^{+0.1}_0$	
D1	$1.5^{+0.1}_0$	
E	1.75 ± 0.1	
F	5.5 ± 0.05	
P0	4.0 ± 0.1	
P1	8.0 ± 0.1	
P2	2.0 ± 0.05	
T	0.30 ± 0.05	
T2	1.3 ± 0.07	
K0	0.9 ± 0.05	
W	$12.0^{+0.3}_{-0.1}$	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

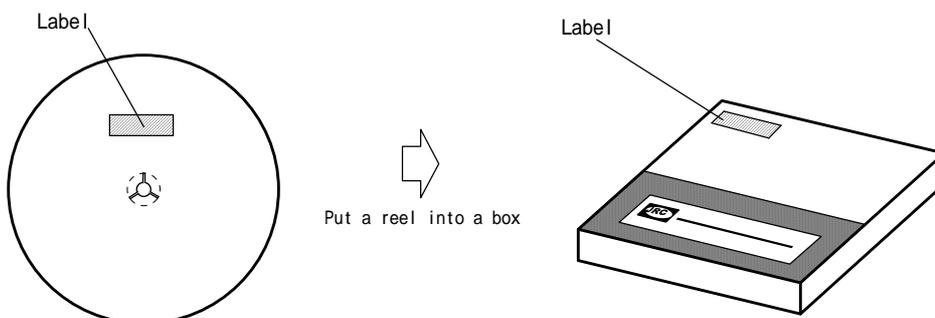


SYMBOL	DIMENSION
A	180^{0}_{-3}
B	60^{+1}_0
C	13 ± 0.2
D	21 ± 0.8
E	2 ± 0.5
W	13^{+1}_0
W2	15.4 ± 1.0

TAPING STATE

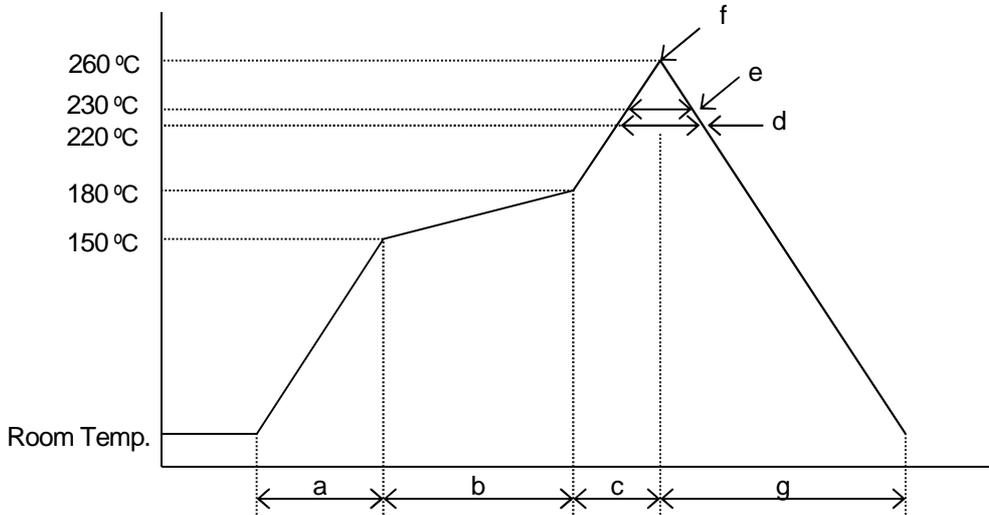


PACKING STATE



RECOMMENDED MOUNTING METHOD

*Recommended reflow soldering procedure



- a : Temperature ramping rate : 1 to 4 °C /s
- b : Pre-heating temperature : 150 to 180 °C
time : 60 to 120s
- c : Temperature ramp rate : 1 to 4 °C /s
- d : 220 °C or higher time : Shorter than 60s
- e : 230 °C or higher time : Shorter than 40s
- f : Peak temperature : Lower than 260 °C
- g : Temperature ramping rate : 1 to 6 °C /s

*The temperature indicates at the surface of mold package.

REVISION HISTORY

DATE	REVISION	CHANGES
April 6, 2017	Ver.1.0	Initial Version
January 25, 2018	Ver.1.1	Updated order information.
August 25, 2020	Ver.2.0	Updated Product lineup.

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