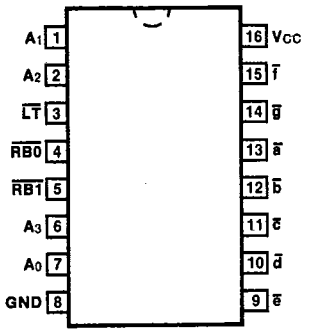
9317B
9317C
7-SEGMENT DECODER/DRIVER

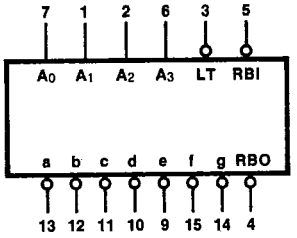
DESCRIPTION — The '17 is a seven segment decoder/driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a 7-segment numerical display. The decoder can be used to directly drive 7-segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, numeric displays). The '17 is available in two output current and latch voltage versions, the '17B and C.

- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING AND/OR TRAILING-EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY/BLANKING INPUT**
- **CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9317PC		9B
Ceramic DIP (D)	A	9317DC	9317DM	7B
Flatpak (F)	A	9317FC	9317FM	4L

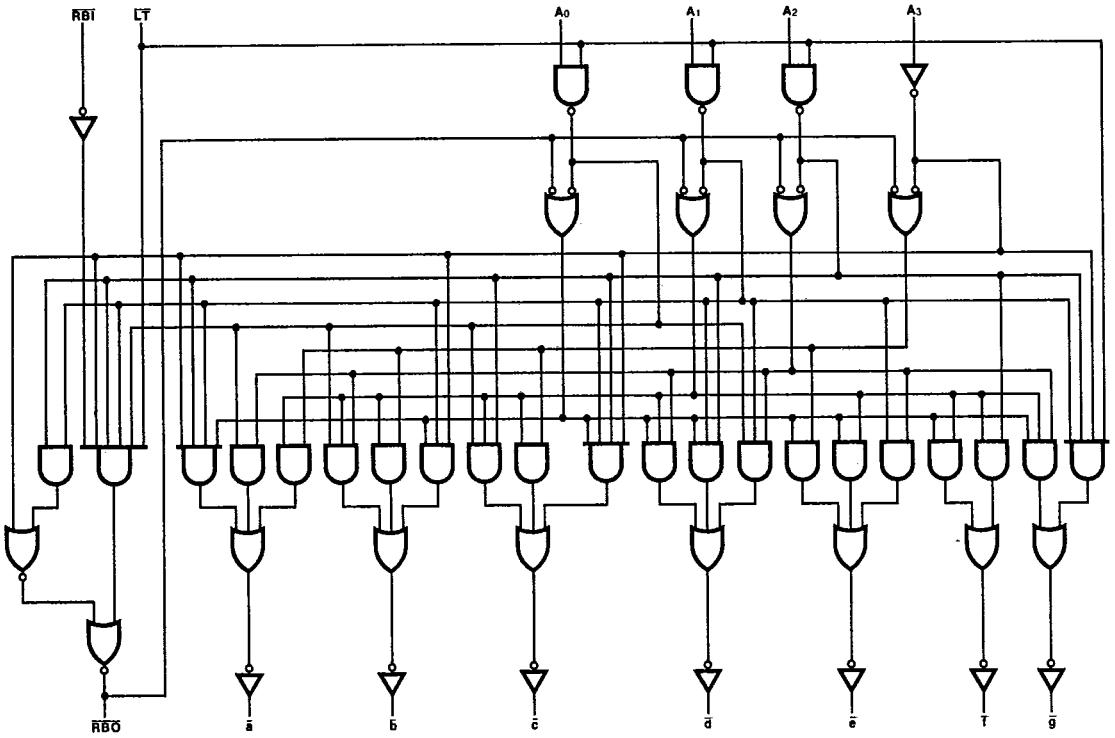
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	1.0/1.0
$\overline{LT}$	Lamp Test Input (Active LOW)	5.0/4.0
$\overline{RBI}$	Ripple Blanking Input (Active LOW)	1.0/0.5
$\overline{RBO}$	Ripple Blanking Output (Active LOW)	1.5/1.5
$\overline{a} - \overline{g}$	Outputs	See Options

OPTIONS

PARAMETER	9317B	9317C
Latch Voltage	20 V	30 V
Output Current (Pins 9 through 15)	40 mA	20 mA

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								DECIMAL OR FUNCTION
$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	H	L	L	L	L	L	L	L	L	L	L	H	H	0
H	X	H	L	L	L	H	H	H	H	L	L	H	H	1
H	X	L	H	L	L	L	L	H	L	L	H	L	H	2
H	X	H	H	L	L	L	L	L	L	H	H	L	H	3
H	X	L	L	H	L	H	L	L	H	H	L	L	H	4
H	X	H	L	H	L	L	H	L	L	H	L	L	H	5
H	X	L	H	H	L	H	H	L	L	L	L	L	H	6
H	X	H	H	H	L	L	L	L	H	H	H	H	H	7
H	X	L	L	L	H	L	L	L	L	L	L	L	H	8
H	X	H	L	L	H	L	L	L	H	H	L	L	H	9
H	X	L	H	L	H	H	H	H	H	H	H	H	L	10
H	X	H	H	L	H	H	H	H	H	H	H	H	L	11
H	X	L	L	H	H	H	H	H	H	H	H	H	L	12
H	X	H	L	H	H	H	H	H	H	H	H	H	L	13
H	X	L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

FUNCTIONAL DESCRIPTION— The '17 7-segment decoder/driver accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0—9. The seven outputs ($\overline{a}$—$\overline{g}$) of the decoder select the corresponding segments in the matrix shown in *Figure a*. The numeric designations chosen to represent the decimal numbers are shown in *Figure c*. Code configurations in excess of binary nine disable the outputs.

The decoder has active LOW outputs so that it may be used directly to drive incandescent displays or light emitting diode indicators. The device has provision for automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar precedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and allows checking on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL gates. Forcing the $\overline{RBO}$ LOW will blank the display, regardless of the $\overline{LT}$ or A_n inputs.

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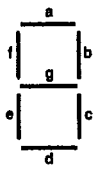

Fig. a Segment Designation

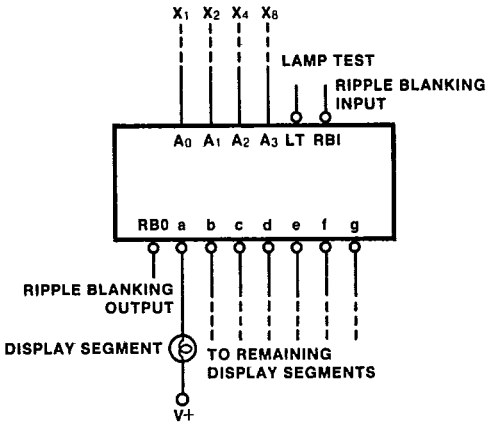

Fig. b Seven segment Decoder Driving Incandescent Lamp Display

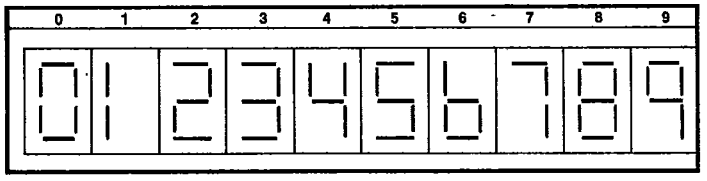

Fig. c Numerical Designations

DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE: V_{CC} = +5.0 V ±5%

SYMBOL	PARAMETER		0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0		3.0		V	V_{CC} = 4.75 V I_{OH} = -70 μA Pin 5 = V_{IH} Pins 1,2,6,7=0V
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.45		0.45		0.45	V	V_{CC} = 5.25 V I_{OL} = 2.75 mA Inputs at V_{IH} or V_{OL} per Truth Table
				0.45		0.45		0.45		V_{CC} = 4.75 V I_{OL} = 2.4 mA Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	9317B		0.9		0.9		0.9	V	V_{CC} = 4.75 I_{OL} = 40 mA Pin 3 = 0 V
		9317C		0.45		0.45		0.45		V_{CC} = 4.75 V I_{OL} = 20 mA Pin 3 = 0 V
V_{LATCH}	Output Latch Voltage	9317B 9317C	20 30		20 30		20 30		V	I_{OL} = 10 mA Inputs = Open
V_{IH}	Input HIGH Voltage		2.0		2.0		2.0		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
I_{OH}	Output HIGH Current					200		250	μA	V_{CC} = 5.25 V V_{CEX} = 30 V ('17C) 20 V ('17B) Inputs at V_{IH} or V_{IL} per Truth Table
t_{PLH} t_{PHL}	Propagation Delay					500 500			ns	Fig. 3-20

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE: V_{CC} = +5.0 V ±10%

SYMBOL	PARAMETER		-55°C Min	-55°C Max	25°C Min	25°C Max	125°C Min	125°C Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0		3.0		V	V_{CC} = 4.5 V I_{OH} = -70 μA Pin 5 = V_{IH} Pins 1,2,6,7 = 0 V
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.4		0.4		0.4	V	V_{CC} = 5.5 V I_{OL} = 3.1 mA Inputs at V_{IH} or V_{IL} per Truth Table
				0.4		0.4		0.4		V_{CC} = 4.5 V I_{OL} = 2.4 mA Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	9317B		0.8		0.8		0.8	V	V_{CC} = 4.5 V I_{OL} = 40 mA Pin 3 = 0 V
		9317C		0.4		0.4		0.4		V_{CC} = 4.5 V I_{OL} = 20 mA Pin 3 = 0 V
V_{LATCH}	Output Latch Voltage	9317B 9317C	20 30		20 30		20 30		V	I_{OUT} = 10 mA Inputs = Open
V_{IH}	Input HIGH Voltage		2.1		1.9		1.7		V	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage			1.4		1.1		0.8	V	Guaranteed Input LOW Threshold
I_{OH}	Output HIGH Current					200		250	μA	V_{CC} = 5.5 V V_{CEX} = 30 V ('17C) 20 V ('17B) Inputs at V_{IH} or V_{IL} per Truth Table
t_{PLH} t_{PHL}	Propagation Delay					500 500			ns	Fig. 3-20

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