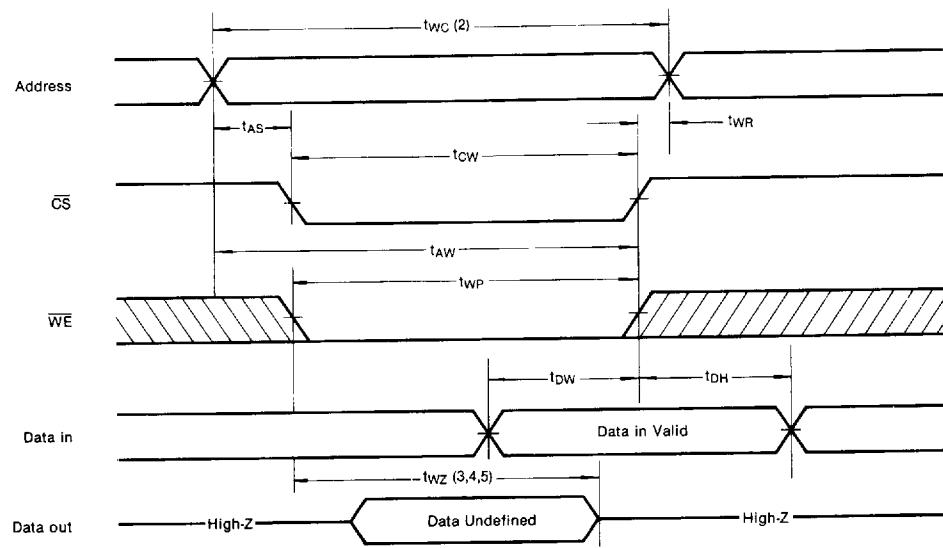


TIMING WAVEFORM OF WRITE CYCLE (CS Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of CS low and WE low.
2. All write cycle timing is referenced from the last valid address to the first transition address.

**54ACT11002, 74ACT11002
QUADRUPLE 2-INPUT POSITIVE-NOR GATES**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)^t

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA

SAMSUNG

ELECTRONICS

54ACT11002, 74ACT11002
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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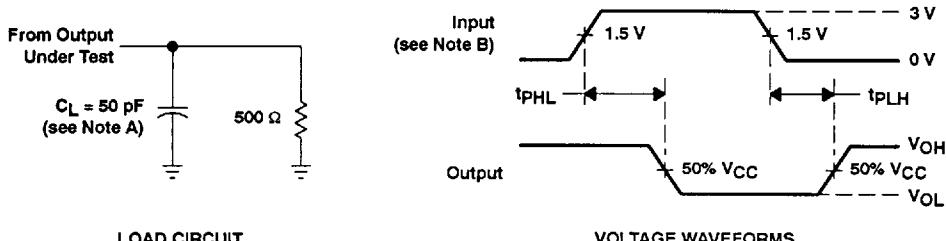
switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11002		74ACT11002		UNIT
			MIN	Typ	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	1.5	6.1	9.4	1.5	11.3	1.5	10.6	ns
			1.5	5.3	7.8	1.5	9.5	1.5	8.7	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	Typ	UNIT
C_{pd} Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$, $f = 1 \text{ MHz}$	29	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms