

74LVT126

3.3 V quad buffer; 3-state

Rev. 6 — 27 July 2021

Product data sheet

1. General description

The 74LVT126 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs (nOE). A LOW on nOE causes the outputs to assume a high impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

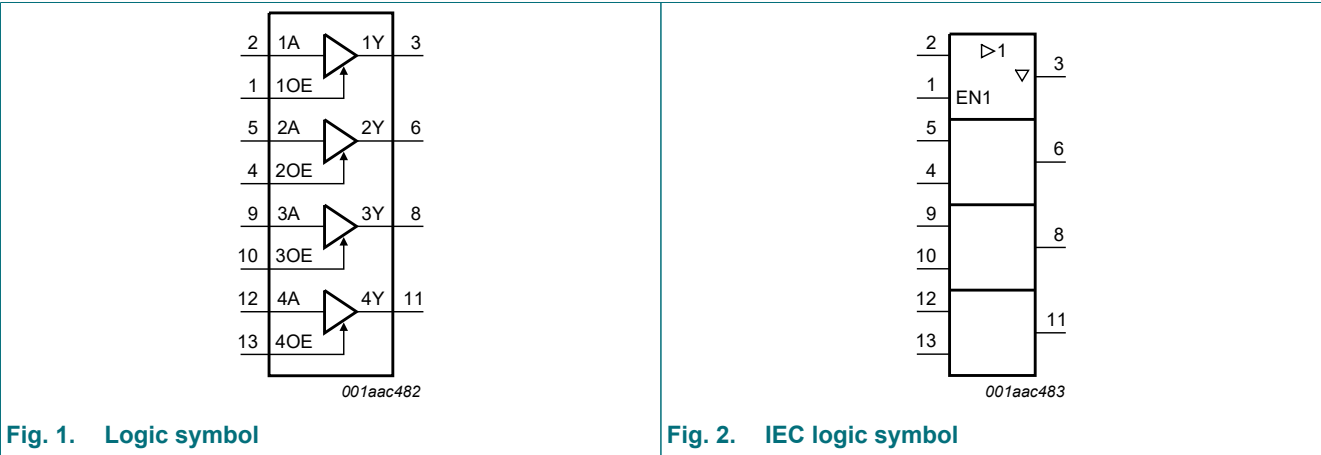
- Quad bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - MIL STD 883 method 3015: exceeds 2000 V
 - MM: exceeds 200 V

3. Ordering information

Table 1. Ordering information

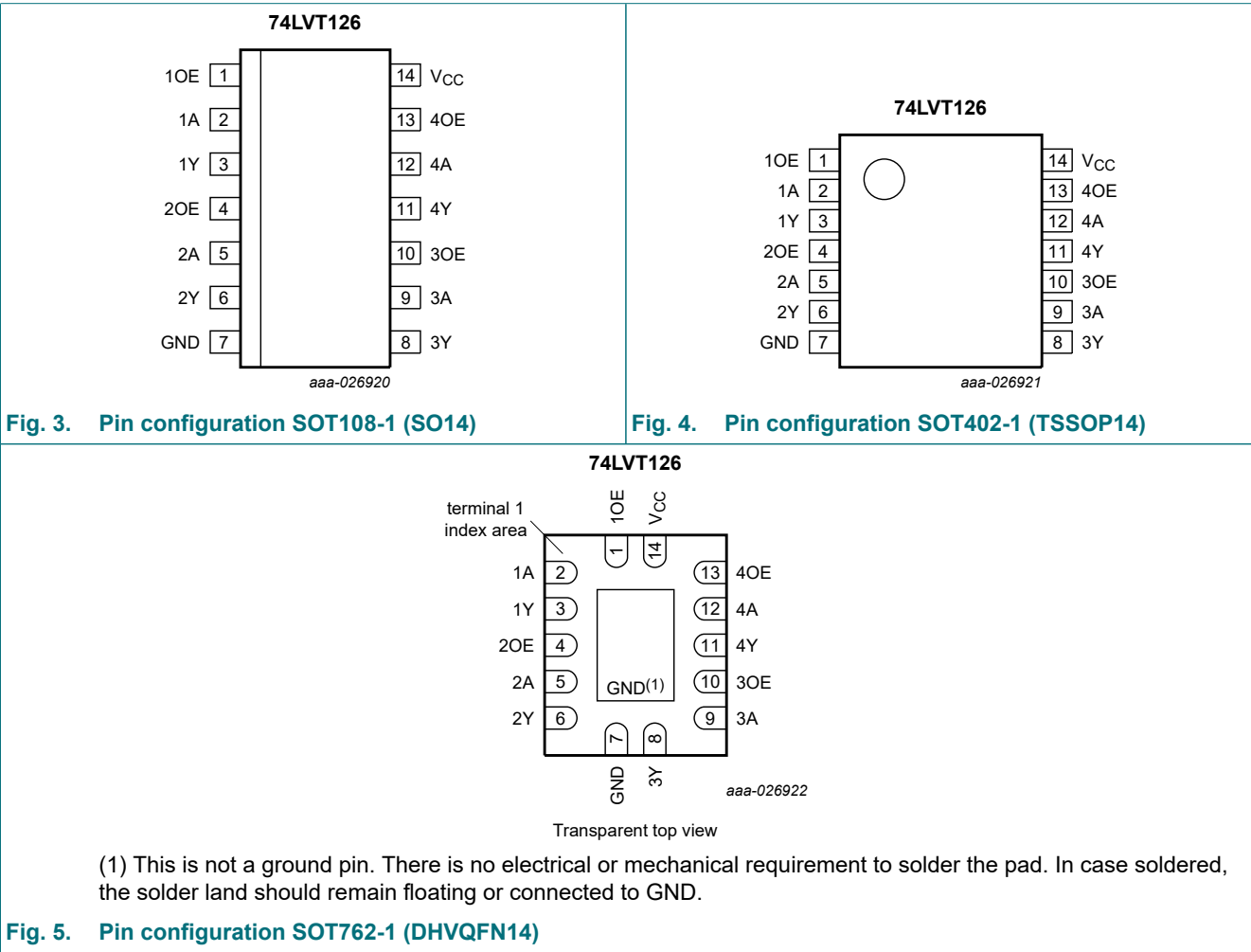
Type number	Package			
	Temperature range	Name	Description	Version
74LVT126D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT126PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT126BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 4, 10, 13	output enable inputs
1A, 2A, 3A, 4A	2, 5, 9, 12	data inputs
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data outputs
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f \geq 1$ kHz	-	-	64	mA
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 2.7$ V; $I_{IK} = -18$ mA	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7$ V to 3.6 V; $I_{OH} = -100$ μ A	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7$ V; $I_{OH} = -8$ mA	2.4	2.5	-	V
		$V_{CC} = 3.0$ V; $I_{OH} = -32$ mA	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7$ V; $I_{OL} = 100$ μ A	-	0.1	0.2	V
		$V_{CC} = 2.7$ V; $I_{OL} = 24$ mA	-	0.3	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 16$ mA	-	0.25	0.4	V
		$V_{CC} = 3.0$ V; $I_{OL} = 32$ mA	-	0.3	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 64$ mA	-	0.4	0.55	V
I_I	input leakage current	all input pins				
		$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	-	1	10	μ A
		control pins				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	-	± 0.1	± 1	μ A
		data pins				
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ ^[2]	-	0.1	1	μ A
		$V_{CC} = 3.6$ V; $V_I = 0$ V ^[2]	-	-1	-5	μ A
I_{OFF}	power-off leakage current	$V_{CC} = 0$ V; V_I or $V_O = 0$ V to 4.5 V	-	1	± 100	μ A
I_{BHL}	bus hold LOW current	$V_{CC} = 3$ V; $V_I = 0.8$ V	75	150	-	μ A
I_{BHH}	bus hold HIGH current	$V_{CC} = 3$ V; $V_I = 2.0$ V	-75	-150	-	μ A
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V ^[3]	500	-	-	μ A
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V ^[3]	-	-	-500	μ A
I_{EX}	external current	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5$ V; $V_{CC} = 3.0$ V	-	60	125	μ A
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $\text{nOE} = \text{don't care}$ ^[4]	-	± 1	± 100	μ A

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	$V_{CC} = 3.6\text{ V}$				
		output HIGH: $V_O = 3.0\text{ V}$	-	1	5	μA
		output LOW: $V_O = 0.5\text{ V}$	-	-1	-5	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	2	7	mA
		outputs disabled [5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at V_{CC} or GND [6]	-	0.1	0.2	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or 3.0 V	-	8	-	pF

[1] Typical values are measured at nominal V_{CC} and $T_{amb} = 25\text{ }^\circ\text{C}$.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms .

From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.

[5] Measured with outputs pulled up to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$			Unit
			Min	Typ[1]	Max	
t_{PLH}	LOW to HIGH propagation delay	nA to nY; see Fig. 6				
		$V_{CC} = 2.7\text{ V}$	-	-	4.5	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.3	3.8	ns
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Fig. 6				
		$V_{CC} = 2.7\text{ V}$	-	-	4.4	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.4	3.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	nOE to nY; see Fig. 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.1	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.6	5.4	ns
t_{PZL}	OFF-state to LOW propagation delay	nOE to nY; see Fig. 7				
		$V_{CC} = 2.7\text{ V}$	-	-	5.8	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.1	3.6	5.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	nOE to nY; see Fig. 7				
		$V_{CC} = 2.7\text{ V}$	-	-	4.3	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.2	3.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	nOE to nY; see Fig. 7				
		$V_{CC} = 2.7\text{ V}$	-	-	6.1	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.3	3.6	5.5	ns

[1] Typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

10.1. Waveforms and test circuit

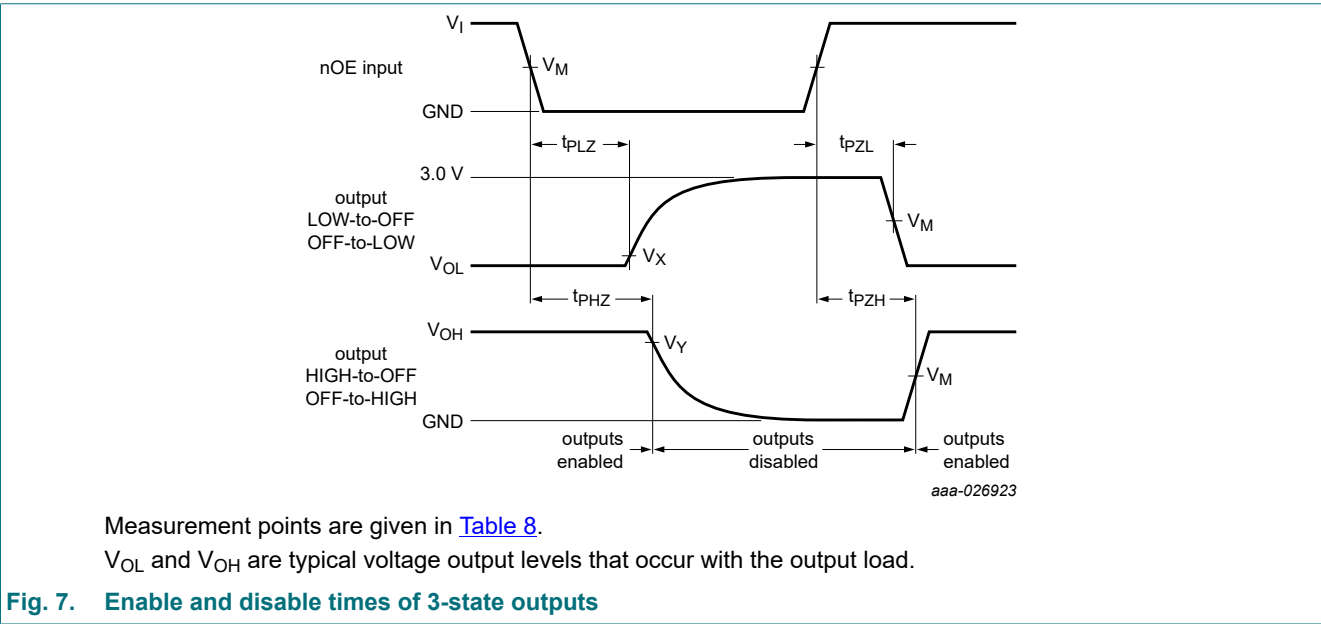
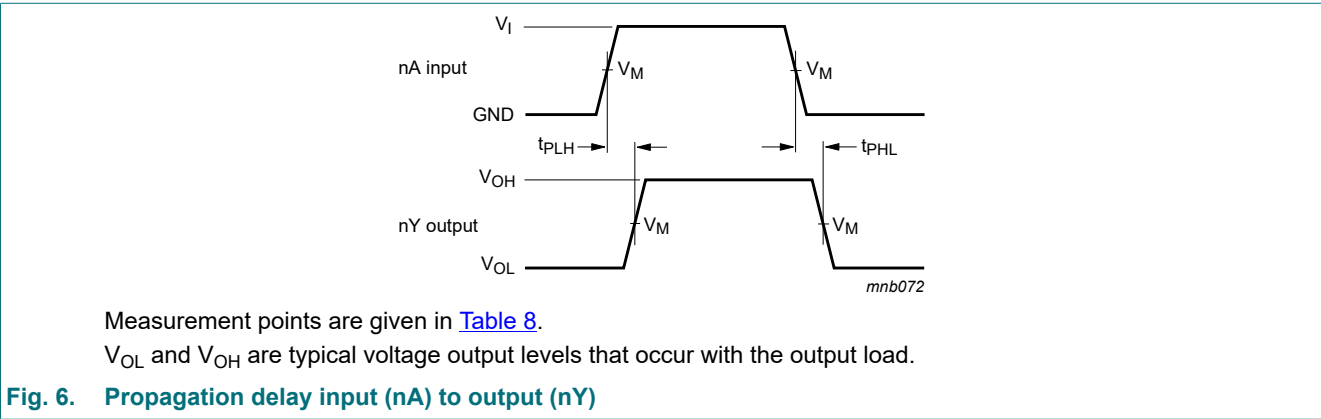


Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

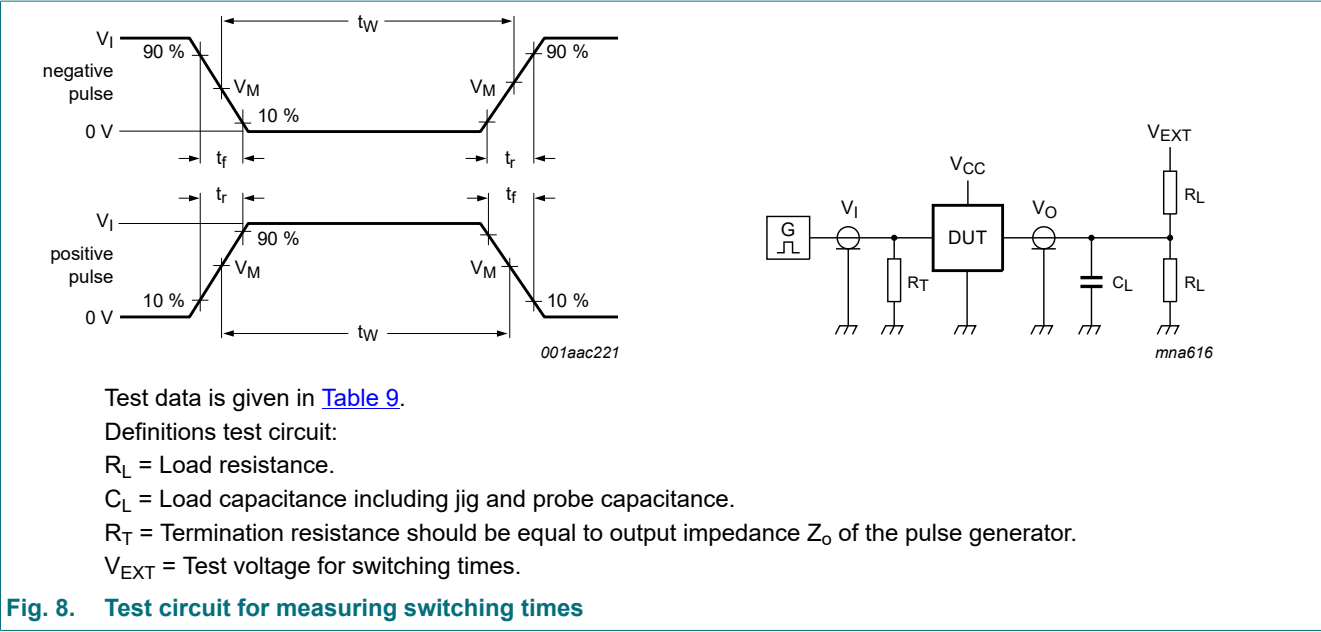


Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

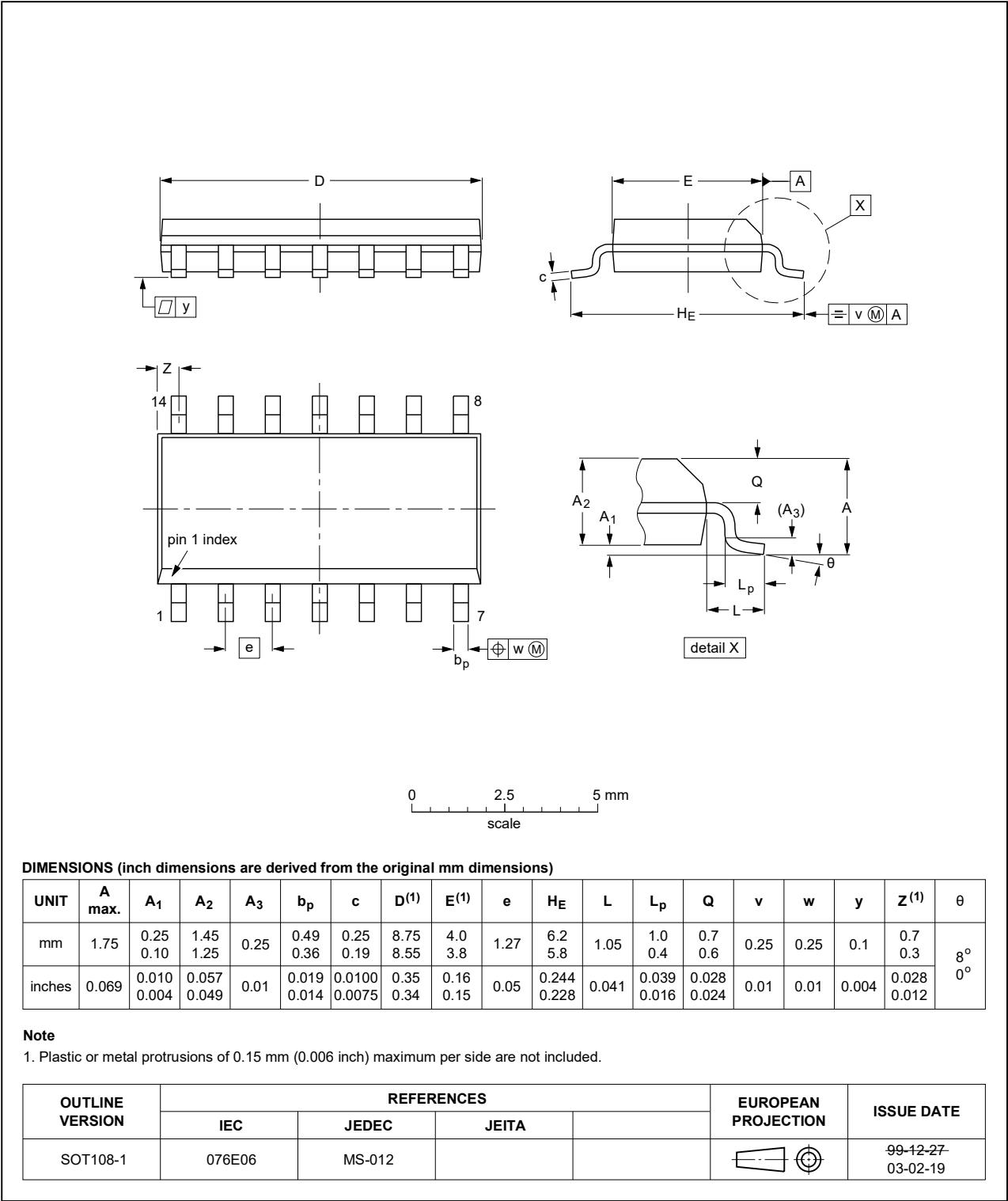


Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

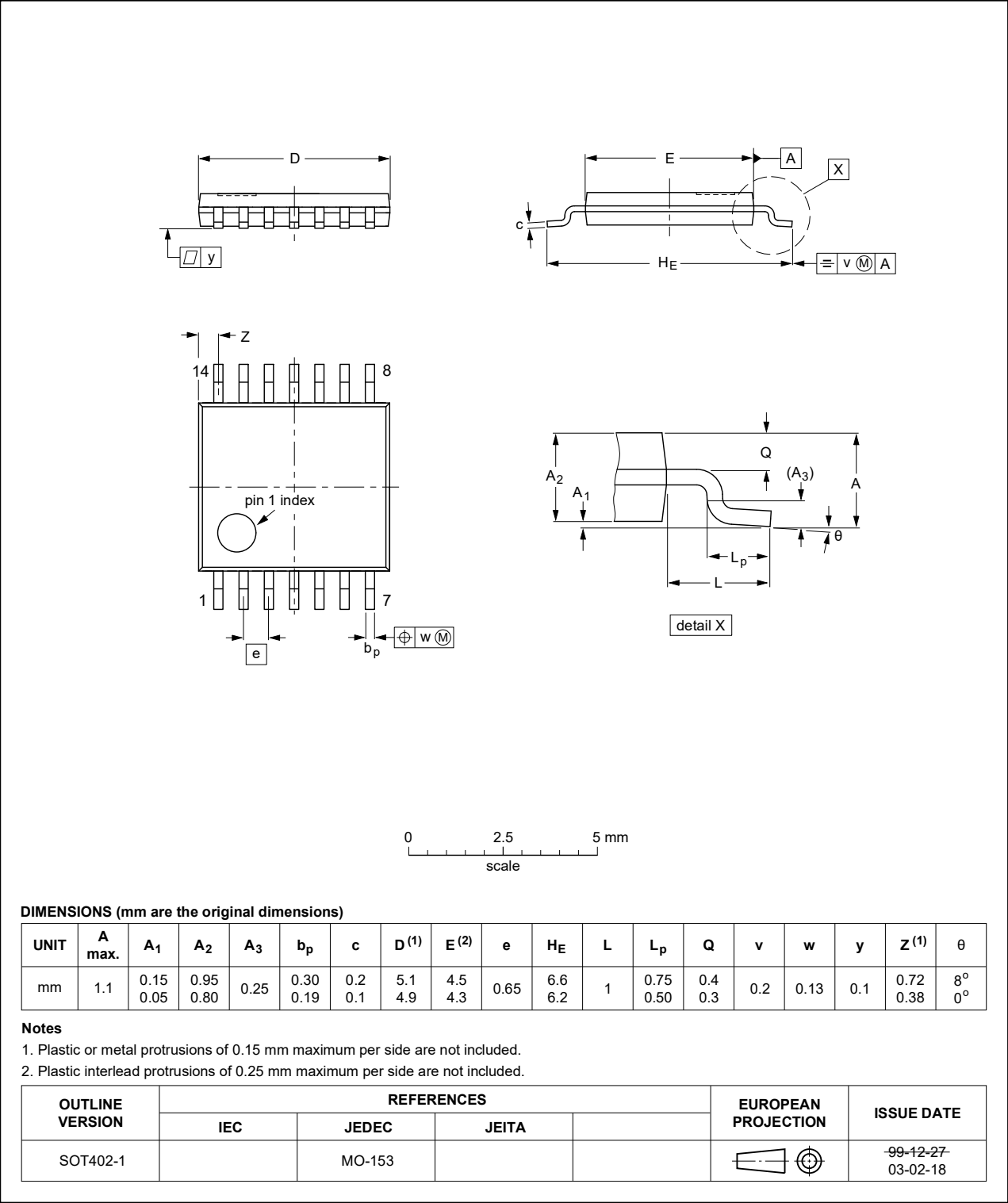


Fig. 10. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

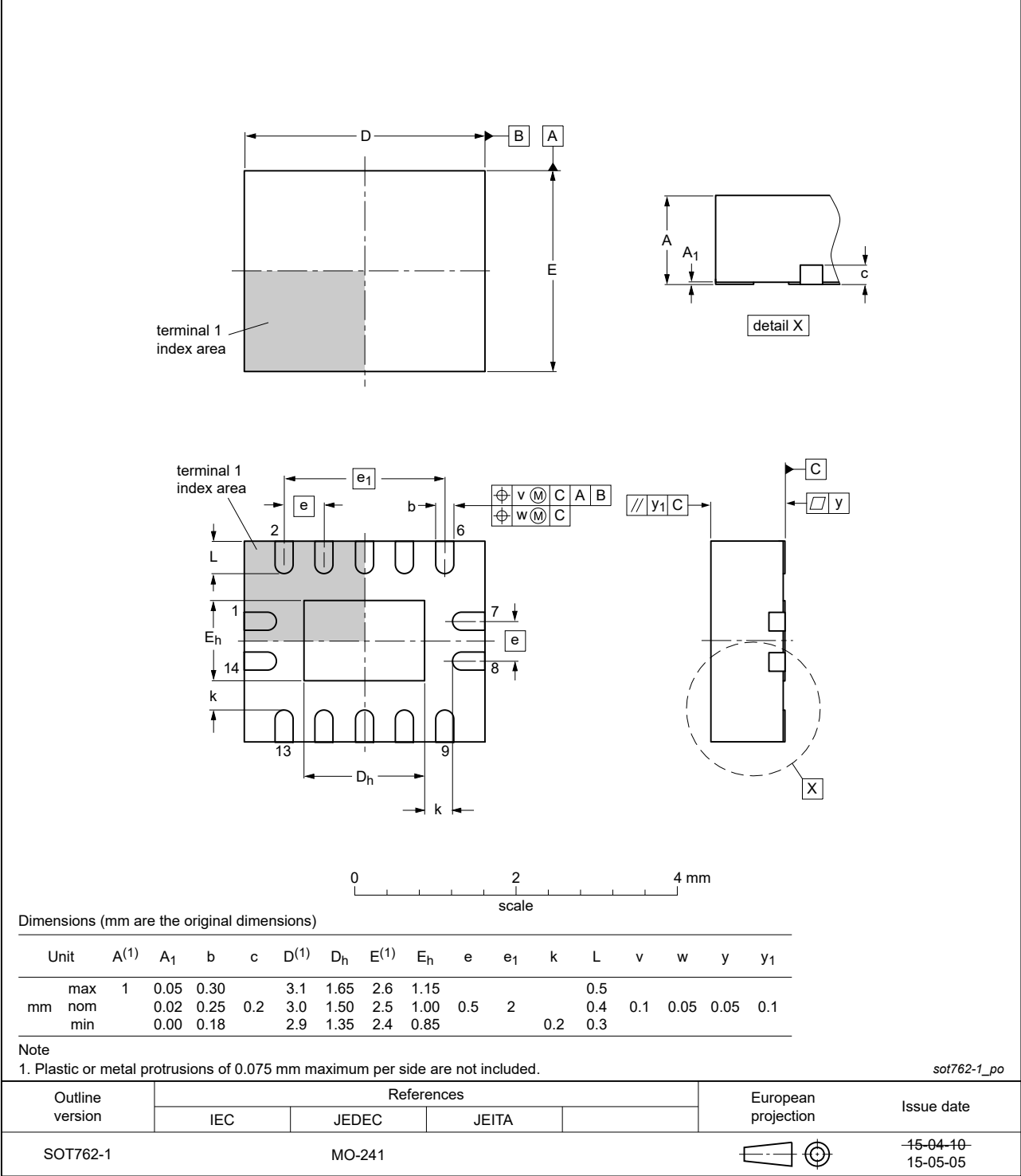


Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT126 v.6	20210727	Product data sheet	-	74LVT126 v.5
Modifications:	- Type number 74LVT126DB (SOT337-1/SSOP14) removed. Section 1 and Section 2 updated.			
74LVT126 v.5	20170614	Product data sheet	-	74LVT126 v.4
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74LVT126 v.4	20050211	Product data sheet	-	74LVT126 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Fig. 5: added note 1.			
74LVT126 v.3	20040624	Product data sheet	-	74LVT126 v.2
74LVT126 v.2	19980219	Product specification	-	74LVT126 v.1
74LVT126 v.1	19951221	-	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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