M37475M2-XXXSP, M37475M4-XXXSP
M37475M8-XXXSP, M37476M2-XXXSP/FP
M37476M4-XXXSP/FP, M37476M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37475M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 32-pin shrink plastic molded DIP. The M37476M2-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 42-pin shrink plastic molded DIP or a 56-pin plastic molded QFP. These single-chip microcomputer are useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37476M2-XXXSP and the M37476M2-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

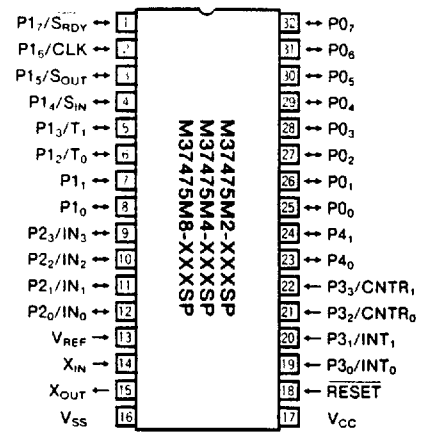
The differences among M37475M2-XXXSP, M37475M4-XXXSP, M37475M8-XXXSP, M37476M2-XXXSP/FP, M37476M4-XXXSP/FP and M37476M8-XXXSP/FP are noted below. The following explanations apply to the M37476M2-XXXSP/FP. Specificaiton variations for other chips are noted accordingly.

Type name	ROM size	RAM size	I/O ports
M37475M2-XXXSP	4096bytes	128bytes	26
M37476M2-XXXSP/FP			36
M37475M4-XXXSP	8192bytes	192bytes	26
M37476M4-XXXSP/FP			36
M37475M8-XXXSP	16384bytes	384bytes	26
M37476M8-XXXSP/FP			36

FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size
  ROM ..... 4096 bytes (M37476M2)
  RAM ..... 128 bytes (M37476M2)
- Instruction execution time
  ..... 1μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 2.7 to 5.5V
- Power dissipation normal operation mode
  ..... 17.5mW (at 4MHz frequency)
- Subroutine nesting
  ..... 64 levels max. (M37475M2, M37476M2)
- Interrupt 12types, 10vectors
- 8-bit timer 4
- Programmable I/O ports
  (Ports P0, P1, P2, P4) 22 (M37475M2)
  28 (M37476M2)
- Input port (Port P3) 4 (M37475M2)
  (Ports P3, P5) 8 (M37476M2)
- Serial I/O (8-bit) 1
- A-D converter 8-bit, 4channel (M37475M2)
  8-bit, 8channel (M37476M2)

PIN CONFIGURATION (TOP VIEW)



Outline 32P4B

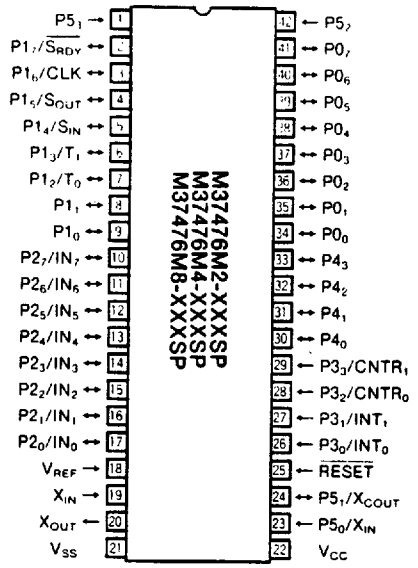
APPLICATION

Audio-visual equipment, VCR, Tuner
Office automation equipment

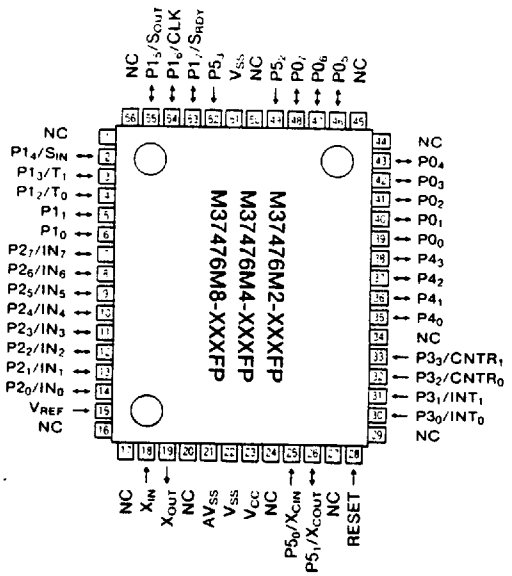
M37475M2-XXXSP,M37475M4-XXXSP
M37475M8-XXXSP,M37476M2-XXXSP/FP
M37476M4-XXXSP/FP,M37476M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN CONFIGURATION (TOP VIEW)



Outline 42P4B



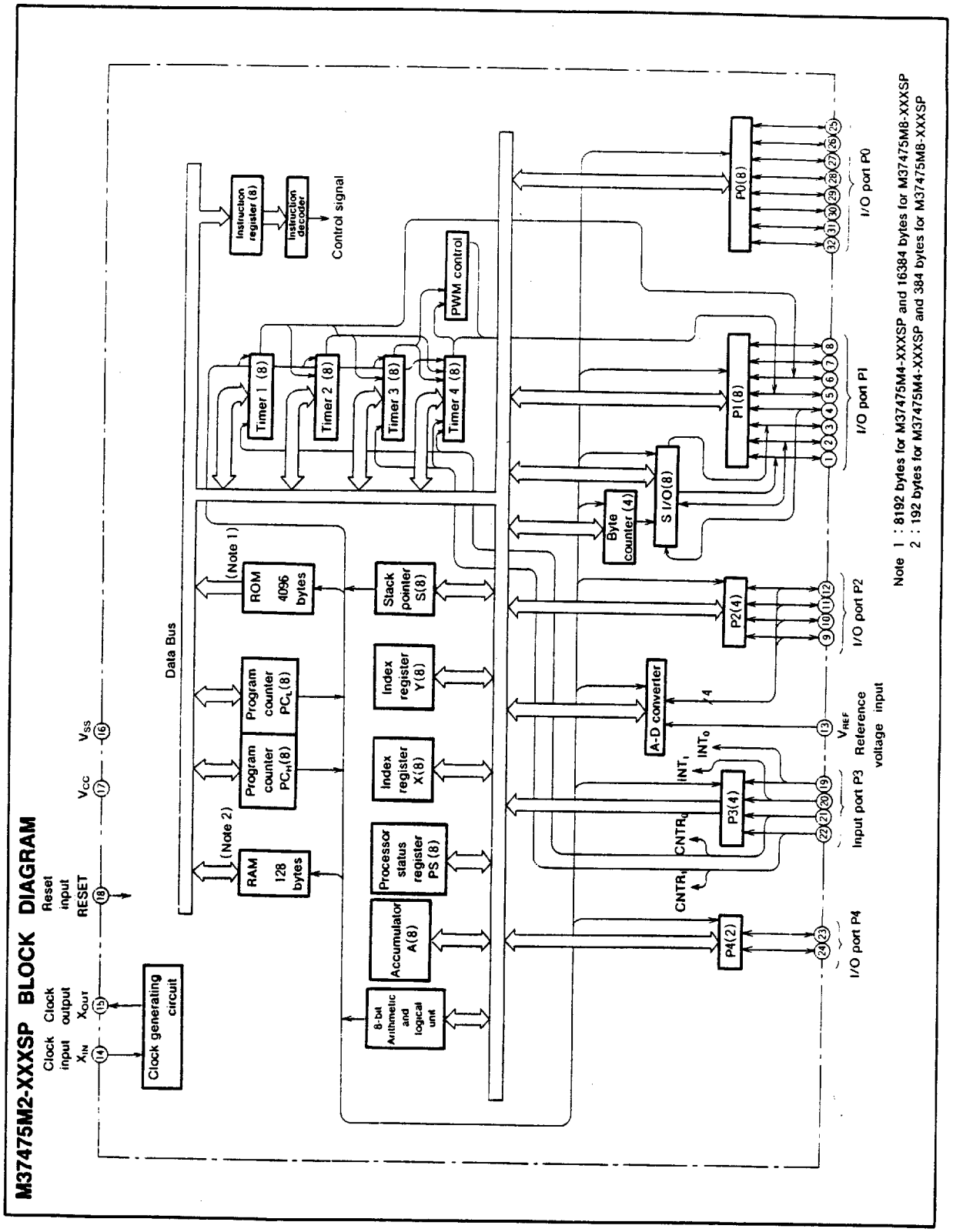
Outline 56P6N-A

NC : No connection

M37475M2-XXXSP,M37475M4-XXXSP
M37475M8-XXXSP,M37476M2-XXXSP/FP
M37476M4-XXXSP/FP,M37476M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

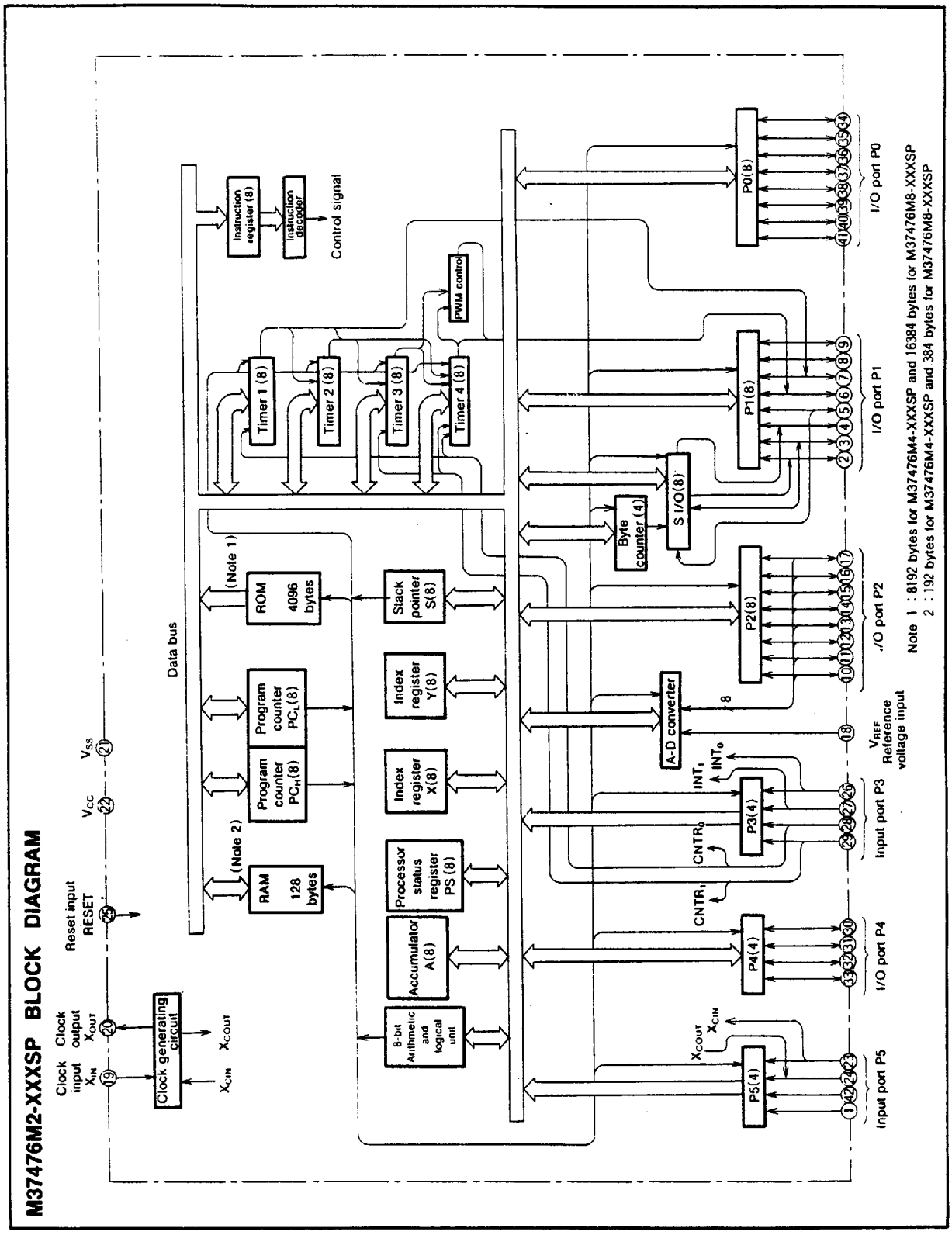
M37475M2-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37475M4-XXXSP and 16384 bytes for M37475M8-XXXSP
2 : 192 bytes for M37475M4-XXXSP and 384 bytes for M37475M8-XXXSP

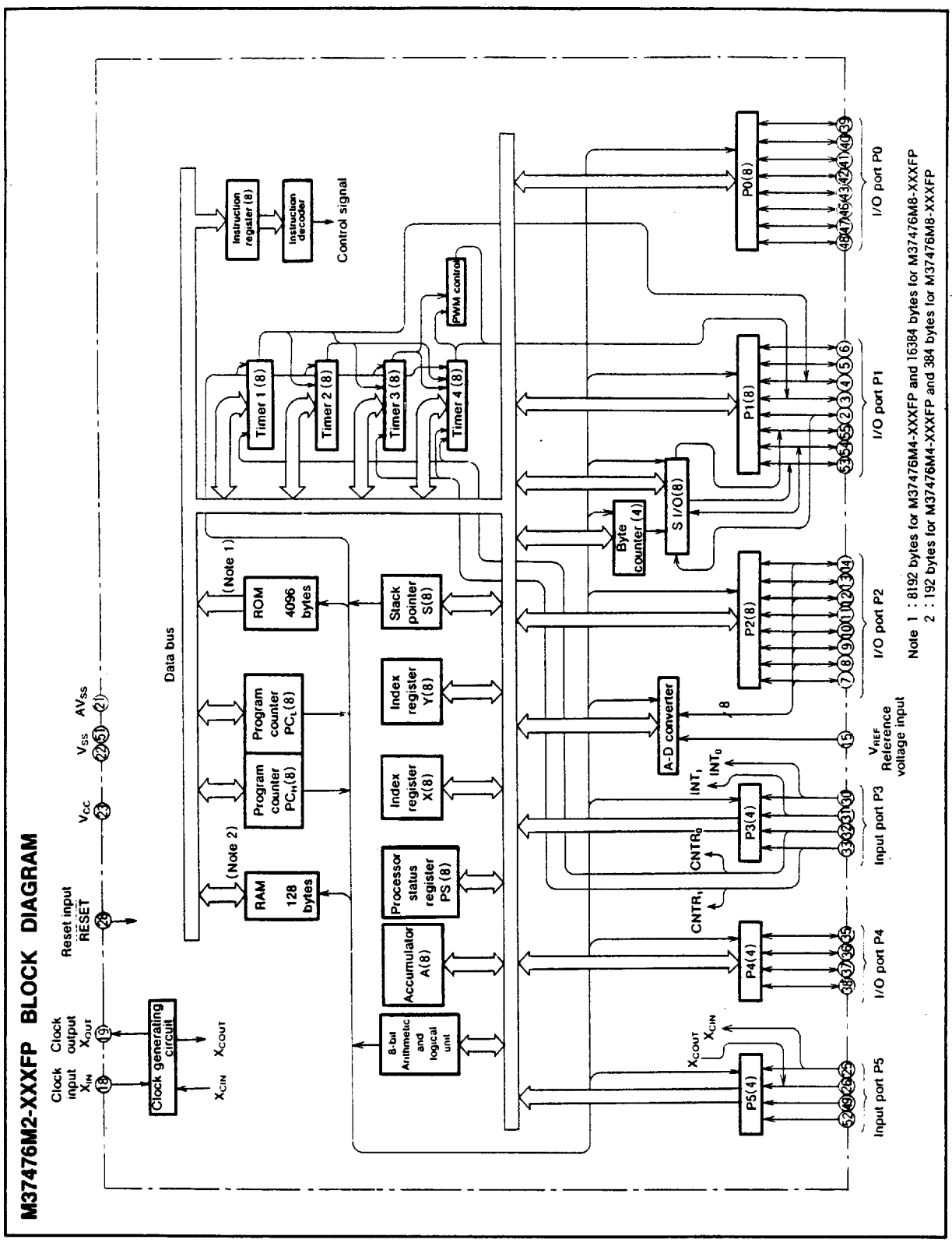
M37475M2-XXXSP,M37475M4-XXXSP
M37475M8-XXXSP,M37476M2-XXXSP/FP
M37476M4-XXXSP/FP,M37476M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER



M37475M2-XXXSP,M37475M4-XXXSP
M37475M8-XXXSP,M37476M2-XXXSP/FP
M37476M4-XXXSP/FP,M37476M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER



FUNCTIONS OF M37475M2-XXXSP, M37475M4-XXXSP, M37475M8-XXXSP, M37476M2-XXXSP/FP, M37476M4-XXXSP/FP, M37476M8-XXXSP/FP

Parameter			Functions
Number of basic instructions			71 (69 MELPS 740 basic instructions + 2)
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz (max.)
Memory size	M37475M2-XXXSP, M37476M2-XXXSP/FP	ROM	4096 bytes
		RAM	128 bytes
	M37475M4-XXXSP, M37476M4-XXXSP/FP	ROM	8192 bytes
		RAM	192 bytes
	M37475M8-XXXSP, M37476M8-XXXSP/FP	ROM	16384 bytes
		RAM	384 bytes
Input/Output port	P0, P1	I/O	8-bit×2
	P2	I/O	8-bit×1 (4-bit×1 for M37475M2/M4/M8)
	P3, P5	Input	4-bit×2 (Port P5 is not included in M37475M2/M4/M8)
	P4	I/O	4-bit×1 (2-bit×1 for M37475M2/M4/M8)
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (8 channels) (8-bit×1 (4 channels)for M37475M2/M4/M8)
Subroutine nesting	M37475M2-XXXSP, M37476M2-XXXSP/FP		64 (max.)
	M37475M4-XXXSP, M37476M4-XXXSP/FP		96 (max.)
	M37475M8-XXXSP, M37476M8-XXXSP/FP		192 (max.)
Interrupt			5 external interrupts, 6 internal interrupts, 1 software interrupt
Clock generating circuit			Built-in circuit with internal feedback resistor (ceramic or quartz crystal oscillator)
Supply voltage			2.7 to 5.5V
Power dissipation			17.5mW (at 4MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		−5 to 10mA (P0, P1, P2, P4 : CMOS tri-states)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37475M2/M4/M8-XXXSP		32-pin shrink plastic molded DIP
	M37476M2/M4/M8-XXXSP		42-pin shrink plastic molded DIP
	M37476M2/M4/M8-XXXFP		56-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 2.7 to 5.5V to V_{CC}, and 0V to V_{SS}.
AV_{SS}	Analog power supply		Ground level input pin for A-D converter. Same voltage as V_{SS} is applied. This pin is for M37476M2/M4/M8-XXXFP only.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions).
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open. Feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converters.
$P0_0$—$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided.
$P1_0$—$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1. $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively. The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output.
$P2_0$—$P2_7$ (Note 1)	I/O port P2	I/O	Port P2 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. This port is in common with analog input pins IN_0—IN_7.
$P3_0$—$P3_3$	Input port P3	Input	Port P3 is a 4-bit input port. $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$.
$P4_0$—$P4_3$ (Note 2)	I/O port P4	I/O	Port P4 is a 4-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.
$P5_0$—$P5_3$ (Note 3)	Input port P5	Input	Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz crystal oscillator between X_{CIN} and X_{COUT}. If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin. Feedback resistor is connected between X_{CIN} and X_{COUT} pins.

Note 1 : Only $P2_0$—$P2_3$ (IN_0—IN_3) 4-bit for M37475M2, M37475M4, M37475M8.
2 : Only $P4_0$ and $P4_1$ 2-bit for M37475M2, M37475M4, M37475M8.
3 : This port is not included in M37475M2, M37475M4, M37475M8.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37476 microcomputers use the standard MELPS 740 instruction set. For details of instruction operations, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Programming Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions can be used.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address $00FB_{16}$. This register has a stack page selection bit.

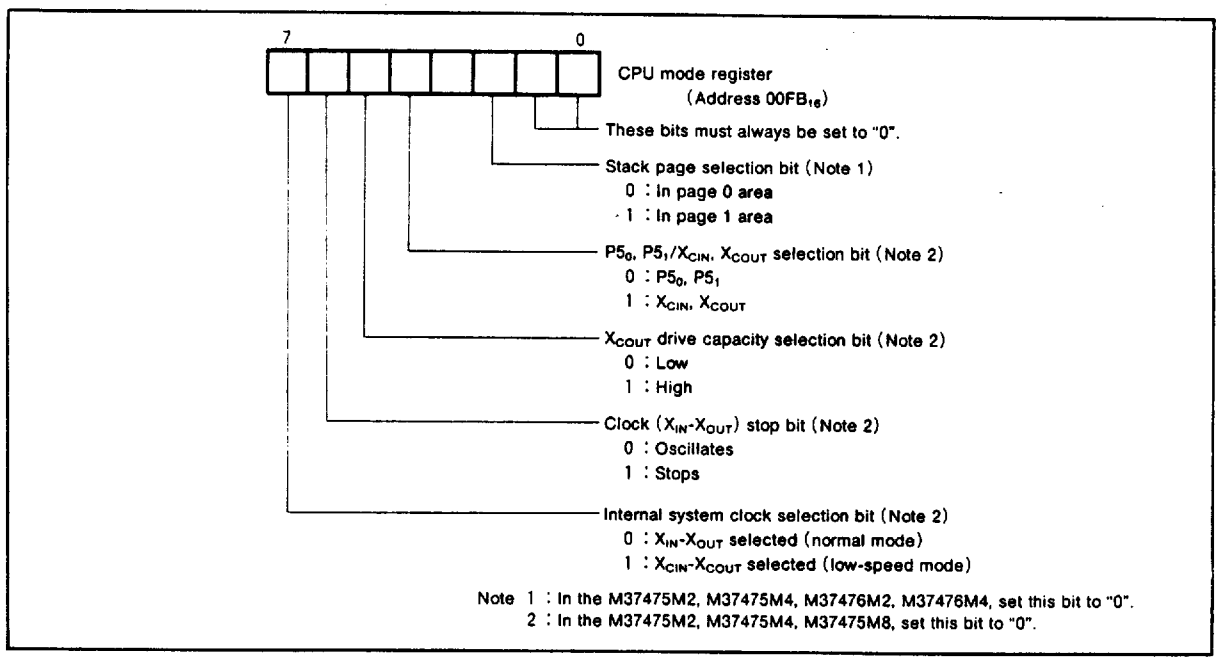


Fig. 1 Structure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

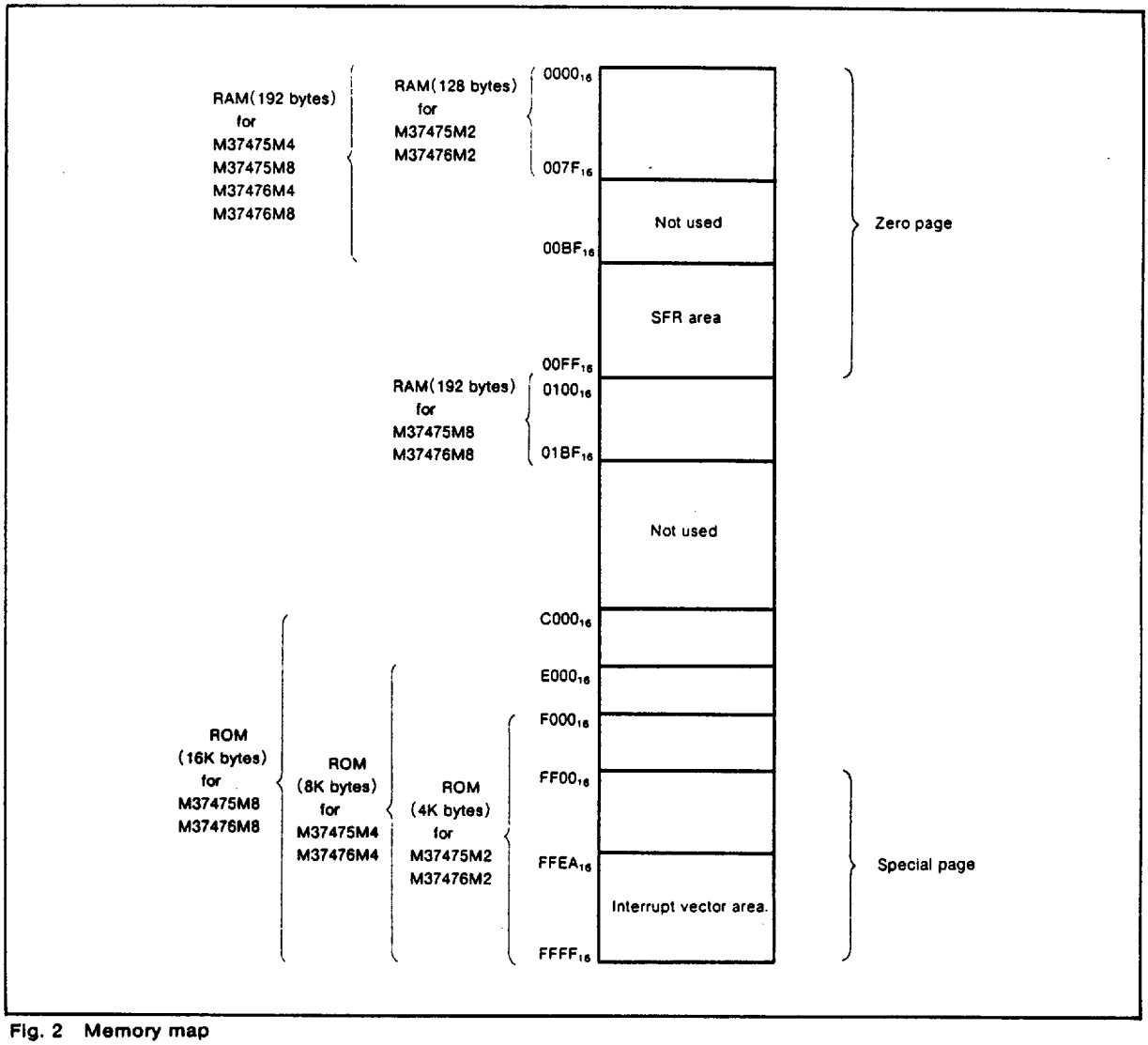


Fig. 2 Memory map

$00C0_{16}$	Port P0
$00C1_{16}$	Port P0 direction register
$00C2_{16}$	Port P1
$00C3_{16}$	Port P1 direction register
$00C4_{16}$	Port P2
$00C5_{16}$	Port P2 direction register
$00C6_{16}$	Port P3
$00C7_{16}$	
$00C8_{16}$	Port P4
$00C9_{16}$	Port P4 direction register
$00CA_{16}$	Port P5 (Note 1)
$00CB_{16}$	
$00CC_{16}$	
$00CD_{16}$	
$00CE_{16}$	
$00CF_{16}$	
$00D0_{16}$	P0 pull-up control register
$00D1_{16}$	P1—P5 pull-up control register (Note 2)
$00D2_{16}$	
$00D3_{16}$	
$00D4_{16}$	Edge polarity selection register
$00D5_{16}$	
$00D6_{16}$	Input latch register
$00D7_{16}$	
$00D8_{16}$	
$00D9_{16}$	A-D control register
$00DA_{16}$	A-D conversion register
$00DB_{16}$	
$00DC_{16}$	Serial I/O mode register
$00DD_{16}$	Serial I/O register
$00DE_{16}$	Serial I/O counter / Byte counter
$00DF_{16}$	

$00E0_{16}$	
$00E1_{16}$	
$00E2_{16}$	
$00E3_{16}$	
$00E4_{16}$	
$00E5_{16}$	
$00E6_{16}$	
$00E7_{16}$	
$00E8_{16}$	
$00E9_{16}$	
$00EA_{16}$	
$00EB_{16}$	
$00EC_{16}$	
$00ED_{16}$	
$00EE_{16}$	
$00EF_{16}$	
$00F0_{16}$	Timer 1
$00F1_{16}$	Timer 2
$00F2_{16}$	Timer 3
$00F3_{16}$	Timer 4
$00F4_{16}$	
$00F5_{16}$	
$00F6_{16}$	
$00F7_{16}$	Timer FF register
$00F8_{16}$	Timer 12 mode register
$00F9_{16}$	Timer 34 mode register
$00FA_{16}$	Timer mode register 2
$00FB_{16}$	CPU mode register
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Note 1 : This address is not used M37475M2, M37475M4, and M37475M8.
2 : This address is allocated P1—P4 pull-up control register for M37475M2, M37475M4, and M37475M8.

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 12 different events consisting of five external, six internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. External interrupts INT_0 and INT_1 can be asserted on either the falling or rising edge as set in the edge polarity selection register. When "0" is set to this register, the interrupt is activated on the falling edge; when "1" is set to the register, the interrupt is activated on the rising edge.

When the device is put into power-down state by the STP instruction or the WIT instruction, if bit 5 in the edge polarity selection register is "1", the INT_1 interrupt becomes a key on wake up interrupt. When a key on wake up interrupt is valide, an interrupt request is generated by applying the "L" level to any pin in port P0. In this case, the port used for interrupt must have been set for the input mode.

If bit 5 in the edge polarity selection register is "0" when the device is in power-down state, the INT_1 interrupt is selected. Also, if bit 5 in the edge polarity selection register is set to "1" when the device is not in a power-down state, neither key on wake up interrupt request nor INT_1 interrupt request are generated.

The $CNTR_0$/$CNTR_1$ interrupts function in the same as INT_0 and INT_1. The interrupt input pin can be specified for either $CNTR_0$ or $CNTR_1$ pin by setting bit 4 in the edge polarity selection register.

Figure 4 shows the structure of the edge polarity selection register, interrupt request registers 1 and 2, and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_0 interrupt	2	$FFFD_{16}$, $FFFC_{16}$	External interrupt (polarity programmable)
INT_1 interrupt or key on wake up interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt (INT_1 is polarity programmable)
$CNTR_0$ interrupt or $CNTR_1$ interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (polarity programmable)
Timer 1 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 2 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
Timer 3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 4 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Serial I/O interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
A-D conversion completion interrupt	10	$FFED_{16}$, $FFEC_{16}$	
BRK instruction interrupt	11	$FFEB_{16}$, $FFEA_{16}$	Non-maskable software interrupt

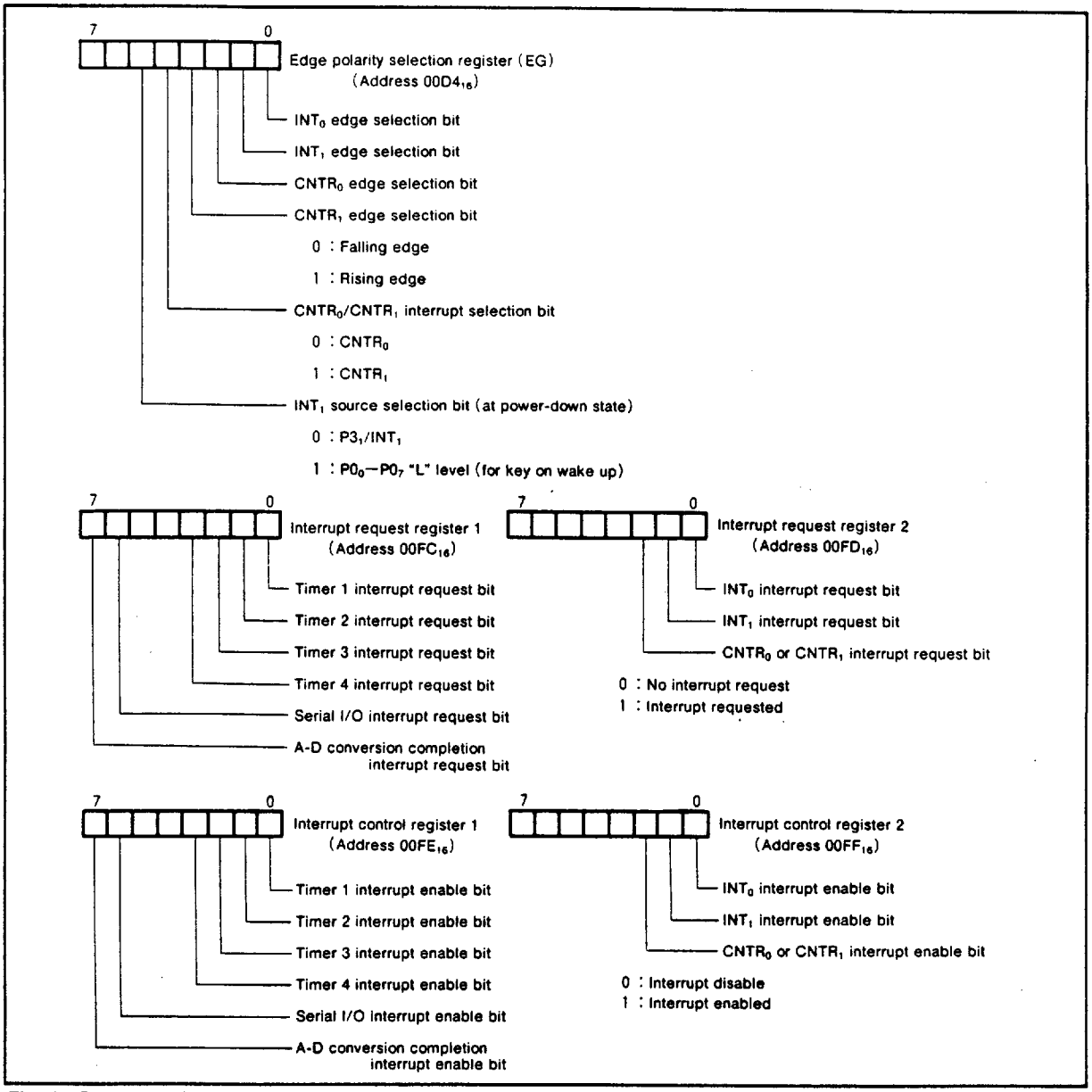


Fig. 4 Structure of registers related to interrupt

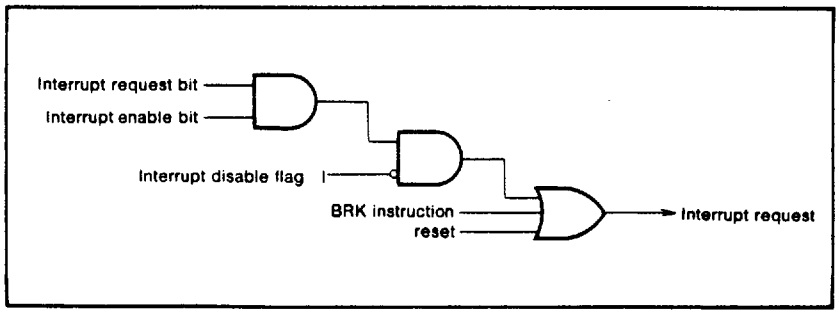


Fig. 5 Interrupt control

TIMER

The M37476M2-XXXSP/FP has four timers; timer 1, timer 2, timer 3, and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

Timer 1 can be operated in the timer mode, event count mode, or pulse output mode. Timer 1 starts counting when bit 0 in the timer 12 mode register (address $00F8_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, or event input from $P3_2/CNTR_0$ pin. Do not select $f(X_{CIN})$ as the count source in the M37475M2, M37475M4, and M37475M8. When bit 1 and bit 2 in the timer 12 mode register are "0", $f(X_{IN})$ divided by 16 or $f(X_{CIN})$ divided by 16 is selected. Selection between $f(X_{IN})$ and $f(X_{CIN})$ is done by bit 7 in the CPU mode register (address $00FB_{16}$). When bit 1 in the timer 12 mode register is "0" and bit 2 is "1", $f(X_{CIN})$ is selected. And, when bit 1 in the timer 12 mode register is "1", an event input from the $CNTR_0$ pin is selected. Event inputs are selected depending on bit 2 in the edge polarity selection register (address $00D4_{16}$). When this bit is "0", the inverted value of $CNTR_0$ input is selected; when the bit is "1", $CNTR_0$ input is selected.

When bit 3 in the timer 12 mode register is set to "1", the $P1_2$ pin becomes timer output T_0. When the direction register of $P1_2$ is set for the output mode at this time, the timer 1 overflow divided by 2 is output from T_0. The initial output value can be set by writing the value to bit 0 in the timer FF register (address $00F7_{16}$) after setting "1" to bit 0 in timer mode register 2.

Timer 2 can only be operated in the timer mode. Timer 2 starts counting when bit 4 in the timer 12 mode register is set to "0".

The count source can be selected from the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ or $f(X_{CIN})$, and timer 1 overflow. Do not select $f(X_{CIN})$ as the count source in the M37475M2, M37475M4, and M37475M8. When bit 5 in the timer 12 mode register is "0", any of the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ or (X_{CIN}) is selected. The divide ratio is selected according to bit 6 and bit 7 in the timer 12 mode register, and selection between $f(X_{IN})$ and $f(X_{CIN})$ is made according to bit 7 in the CPU made register. When bit 5 in the timer 12 mode register is "1", timer 1 overflow is selected as the count source.

Timer 3 can be operated in the timer mode, event count mode, or PWM mode. Timer 3 starts counting when bit 0 in the timer 34 mode register (address $00F9_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, timer 1 or timer 2 overflow, or an event input from $P3_3/CNTR_1$ pins according to the statuses of bit 1 and bit 2 in the timer 34 mode register, bit 6 in the timer mode register 2 (address $00FA_{16}$) and bit 7 in the CPU mode register. Do not select $f(X_{CIN})$ as the count source in the M37475M2, M37475M4, and M37475M8. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 3 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

Timer 4 can be operated in the timer mode, event count mode, pulse output mode, pulse width measuring mode, or PWM mode. Timer 4 starts counting when bit 3 in the timer 34 mode register is set to "0" when bit 6 in this register is "0". When bit 6 is "1", the pulse width measuring mode is selected. The count source can be selected from timer 3 overflow, $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, timer 1 or timer 2 overflow, or an event input from $P3_3/CNTR_1$ pins according to the statuses of bit 4 and bit 5 in the timer 34 mode register, bit 6 in the timer mode register 2, and bit 7 in the CPU mode register. Do not select $f(X_{CIN})$ as the count source in the M37475M2, M37475M4, and M37475M8. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 4 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

When bit 7 in the timer 34 mode register is set to "1", the $P1_3$ pin becomes timer output T_1. When the direction register of $P1_3$ is set for the output mode at this time, the timer 4 overflow divided by 2 is output from T_1 when bit 7 in the timer mode register 2 is "0". The initial output value can be set by writing the value to bit 1 in the timer FF register after setting "1" to bit 1 in timer mode register 2.

(1) Timer mode

Timer perform down count operations with the dividing ratio being $1/(n+1)$. Writing a value to the timer latch sets a value to the timer. When the value to be set to the timer latch is nn_{16}, the value to be set to a timer is nn_{16}, which is down counted at the falling edge of the count source from nn_{16} to $(nn_{16}-1)$ to $(nn_{16}-2)$ to...01_{16} to 00_{16} to FF_{16}. At the falling edge of the count source immediately after timer value has reached FF_{16}, value $(nn_{16}-1)$ obtained by subtracting one from the timer latch value is set (reloaded) to the timer to continue counting. At the rising edge of the count source immediately after the timer value has reached FF_{16}, an overflow occurs, an interrupt request.

(2) Event count mode

Timer operates in the same way as in the timer mode except that it counts input from the $CNTR_0$ or $CNTR_1$ pin.

(3) Pulse output mode

In this mode, duty 50% pulses are output from the T_0 or T_1 pin. When the timer overflows, the polarity of the T_0 or T_1 pin output level is inverted.

(4) Pulse width measuring mode

The M37475 and M37476 can measure the "H" or "L" width of the $CNTR_0$ or $CNTR_1$ input waveform by using the pulse width measuring mode of timer 4. The pulse width measuring mode is selected by writing "1" to bit 6 in the timer 34 mode register. In the pulse width measuring mode, the timer counts the count source while the $CNTR_0$ or $CNTR_1$ input is "H" or "L". Whether the $CNTR_0$ input or $CNTR_1$ input be measured can be specified by the status of bit 4 in the edge polarity selection register; whether the "H" width or "L" width be measured can be specified by the status of bit 2 ($CNTR_0$) and bit 3 ($CNTR_1$) in the edge polarity selection register.

(5) PWM mode

The PWM mode can be entered for timer 3 and timer 4 by setting bit 7 in the timer mode register 2 to "1". In the PWM mode, the $P1_3$ pin is set for timer output T_1 to output PWM waveforms by setting bit 7 in the timer 34 mode register to "1". The direction register of $P1_3$ must be set for the output mode before this can be done.

In the PWM mode, timer 3 is counting and timer 4 is idle while the PWM waveform is "L". When timer 3 overflows, the PWM waveform goes "H". At this time, timer 3 stops counting simultaneously and timer 4 starts counting. When timer 4 overflows, the PWM waveform goes "L", and timer 4 stops and timer 3 starts counting again. Consequently, the "L" duration of the PWM waveform is determined by the value of timer 3; the "H" duration of the PWM waveform is determined by the value of timer 4.

When a value is written to the timer in operation during the PWM mode, the value is only written to the timer latch, and not written to the timer. In this case, if the timer overflows, a value one less the value in the timer latch is written to the timer. When any value is written to an idle timer, the value is written to both the timer latch and the timer.

In this mode, do not select timer 3 overflow as the count source for timer 4.

INPUT LATCH FUNCTION

The M37475 and M37476 can latch the $P3_0/INT_0$, $P3_1/INT_1$, $P3_2/CNTR_0$, and $P3_3/CNTR_1$ pin level into the input latch register (address $00D6_{16}$) when timer 4 overflows. The polarity of each pin latched to the input latch regiser can be selected by using the edge polarity selection register. When bit 0 in the edge polarity selection register is "0", the inverted value of the $P3_0/INT_0$ pin level is latched; when the bit is "1", the $P3_0/INT_0$ pin level is latched as is. When bit 1 in the edge polarity selection register is "0", the inverted value of the $P3_1/INT_1$ pin level is latched; when the bit is "1", the $P3_1/INT_1$ pin level is latched as is. When bit 2 in the edge polarity selection register is "0", the inverted value of the $P3_2/CNTR_0$ pin level is latched; when the bit is "1", the $P3_2/CNTR_0$ pin level is latched as is. When bit 3 in the edge polarity selection register is "0", the inverted value of the $P3_3/CNTR_1$ pin level is latched; when the bit is "1", the $P3_3/CNTR_1$ pin level is latched as is.

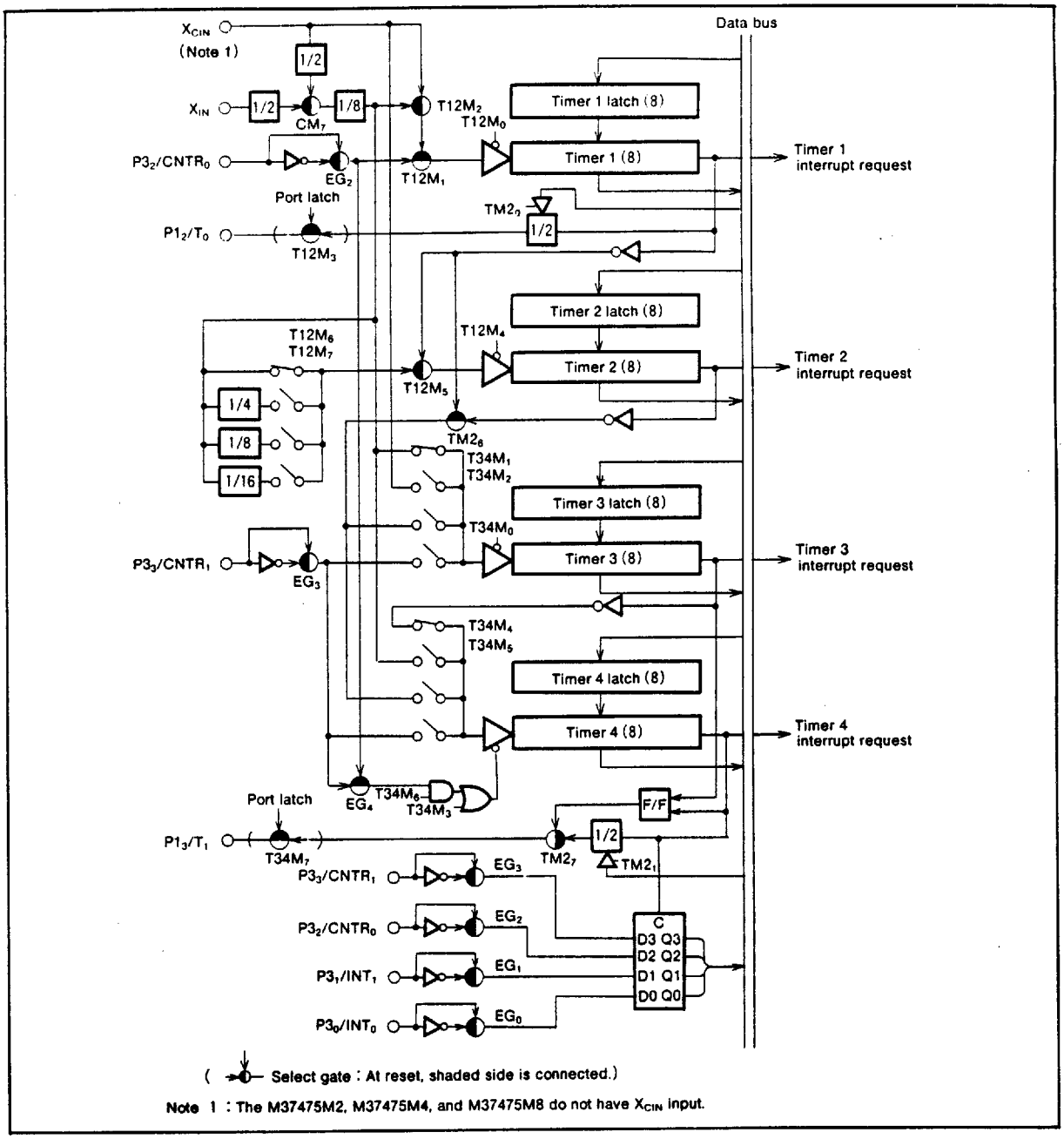
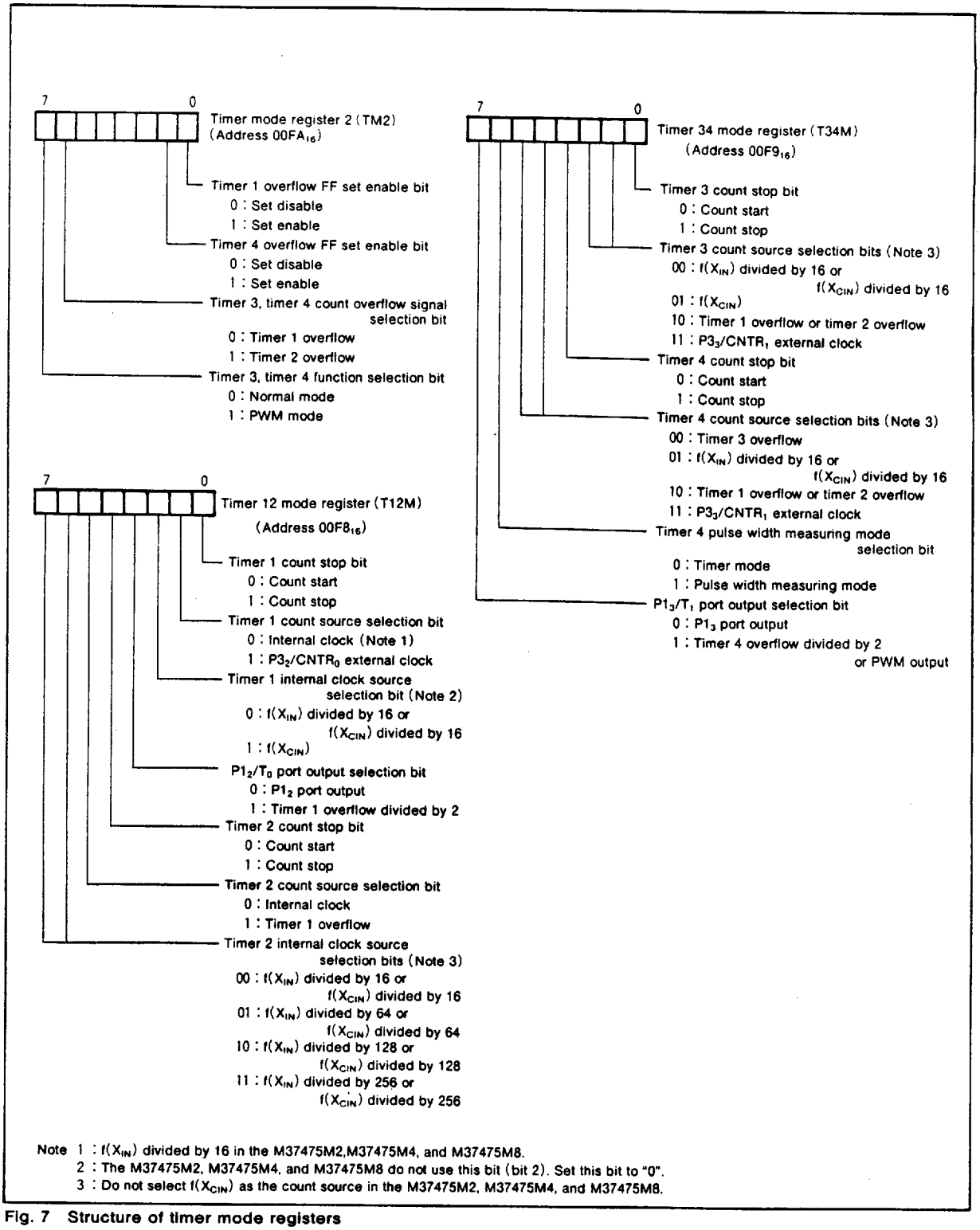


Fig. 6 Block diagram of timer 1 through 4



Note 1 : f(XIN) divided by 16 in the M37475M2,M37475M4, and M37475M8.
2 : The M37475M2, M37475M4, and M37475M8 do not use this bit (bit 2). Set this bit to "0".
3 : Do not select f(XCIN) as the count source in the M37475M2, M37475M4, and M37475M8.

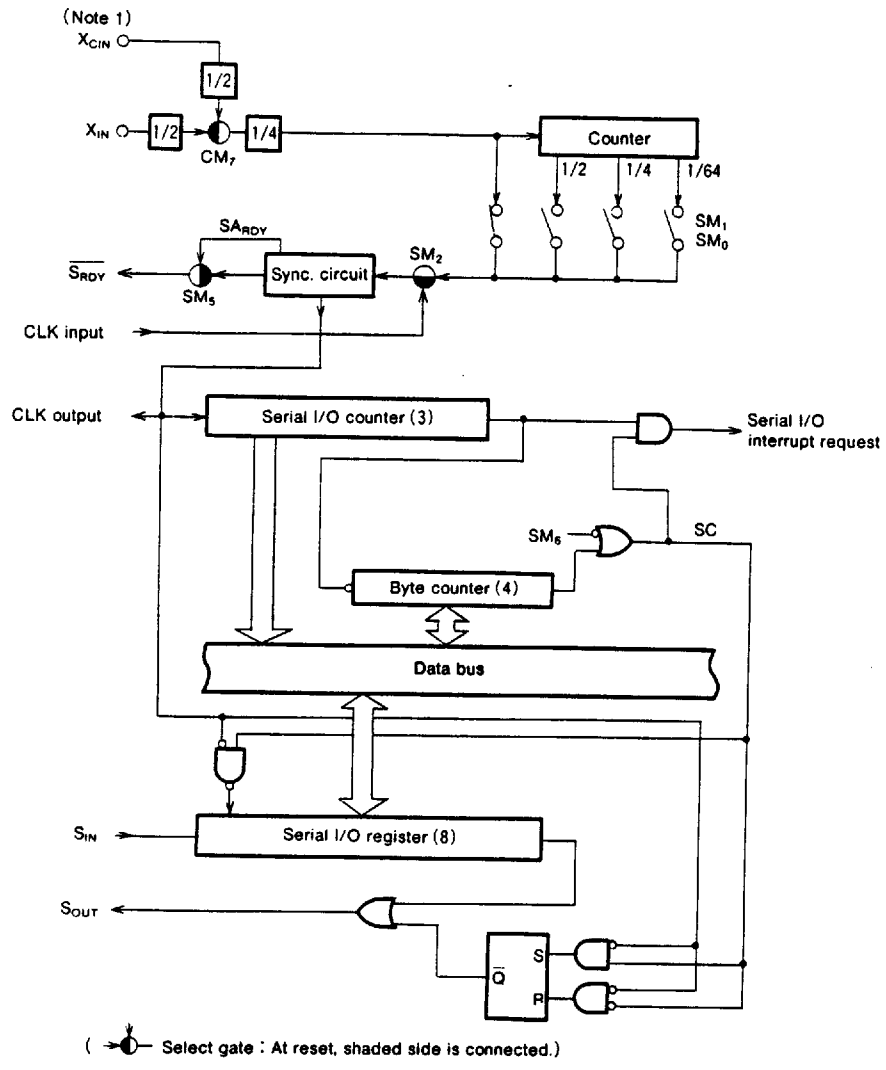
Fig. 7 Structure of timer mode registers

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode, the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P1_7$, $P1_6$, $P1_5$, and $P1_4$, respectively. The serial I/O mode register (address $00DC_{16}$) is an 8-bit register. Bit 2 of this register is used to select a synchronous clock source. When this bit is "0", an external clock from $P1_6$ is selected. When this bit is "1", an internal clock is selected.

The internal clock can be selected from among the divide by 8, divide by 16, divide by 32, divide by 512 frequency of the oscillator frequency $f(X_{IN})$ or $f(X_{CIN})$. Do not select $f(X_{CIN})$ as the count source in the M37475M2, M37475M4, and M37475M8. The divide ratio is selected according to bit 0 and bit 1 in the serial I/O mode register, and selection between $f(X_{IN})$ and $f(X_{CIN})$ is mode according to bit 7 in the CPU mode register.

Bits 3 and 4 decide whether parts of P1 will be used as a serial I/O or not. When bit 3 is "1", $P1_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P1_6$. If the external synchronous clock is selected, the clock is input to $P1_6$. And $P1_5$ will be a serial output. To use $P1_4$ as a serial input, set the direction register bit which corresponds to $P1_4$, to "0". For more information on the direction register, refer to the I/O pin section.



Note 1 : The M37475M2, M37475M4, and M37475M8 do not have X_{CIN} input.

Fig. 8 Block diagram of serial I/O

Bit 4 determines if $P1_7$ is used as an output pin for the receive ready signal (bit 4="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 4="0").

When the $P1_7$ pin is used as the $\overline{S_{RDY}}$ output pin, output signal can be selected between $\overline{S_{RDY}}$ signal and SA_{RDY} signal by using bit 5 in the serial I/O mode register. The $\overline{S_{RDY}}$ signal is driven "L" by a signal written into the serial I/O register to inform that the device is ready to receive. Then, the $\overline{S_{RDY}}$ signal is driven "H" on the first falling edge of the transfer clock.

The SA_{RDY} signal is driven "H" by a signal written into the serial I/O register, and driven "L" on the last rising edge of the transfer clock.

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock — The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P1_5$. During the rising edge of this clock, data can be input from $P1_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside.

Timing diagrams are shown in Figure 9.

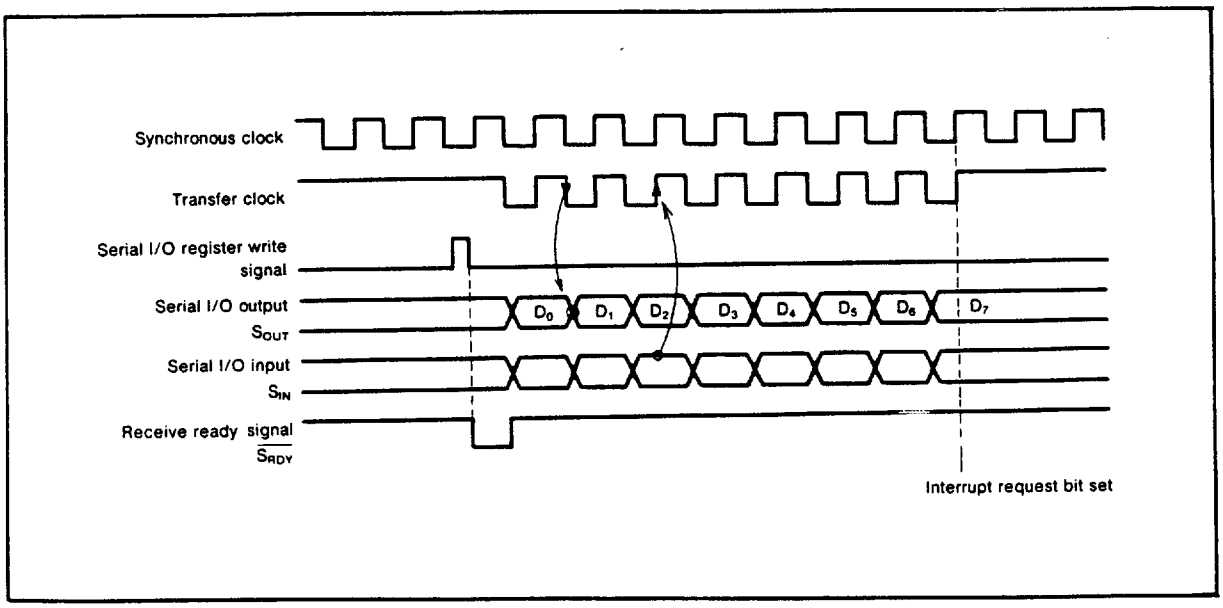


Fig. 9 Serial I/O timing

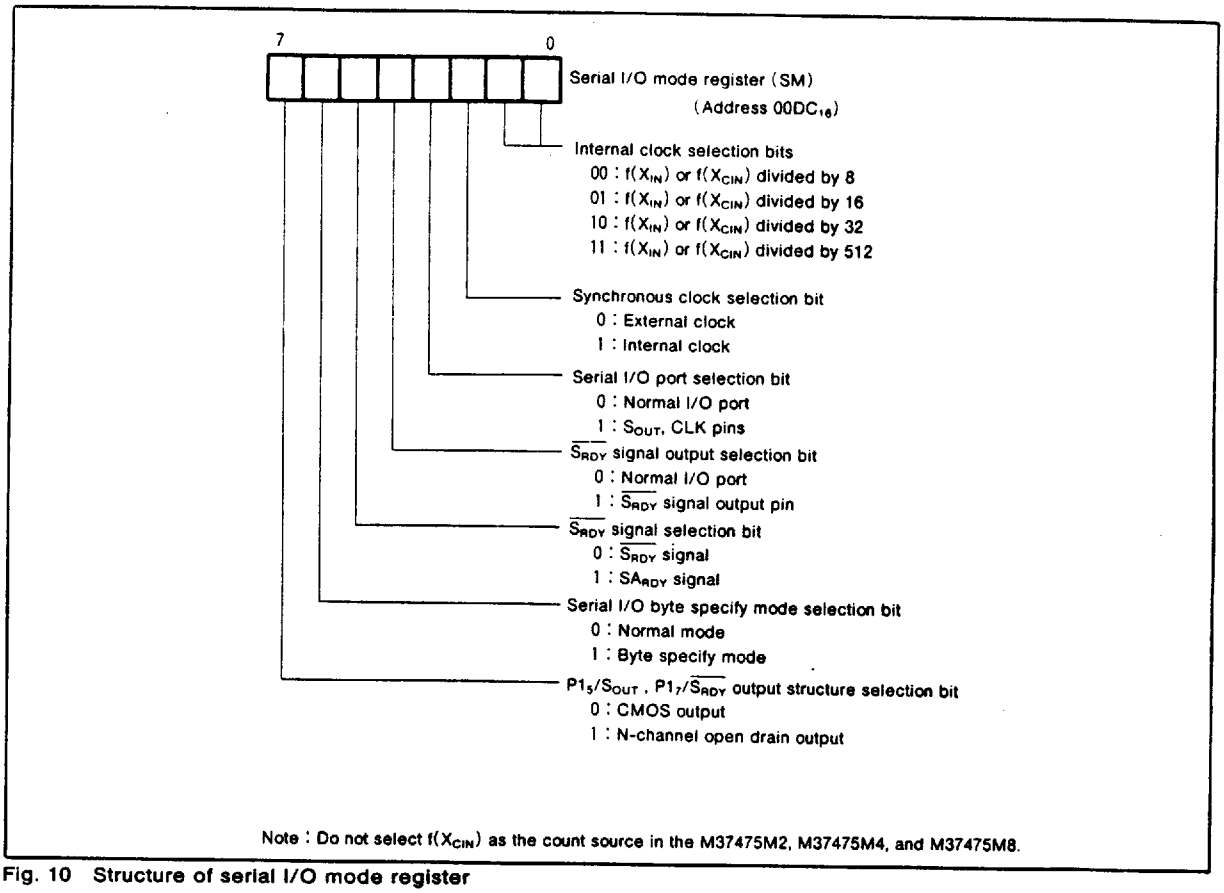


Fig. 10 Structure of serial I/O mode register

BYTE SPECIFY MODE

The serial I/O has a byte specify mode that allows one specific byte data to be selected for transmission or reception when serial I/O circuits of two or more microcomputers are connected to send or receive data through one bus. The data to be sent or received can be specified by writing a value into the byte counter. The value written in the byte counter is decremented by one each time eight cycles of transfer clock are input. When the value in the byte counter becomes "0", serial transmission/reception is done by the next eight cycles of transfer clock. When the value in the byte counter is not "0", the output on the S_{OUT} pin is driven "H" by the falling edge of the first transfer clock pulse to inhibit transmission/reception.

Serial I/O interrupt requests are generated only when serial transmission/reception is done after the value in the byte counter is decremented to "0". When the SA_{RDY} signal output is selected, the SA_{RDY} signal is driven "L" by the last rising edge of the transfer clock after the value in the byte counter is decremented to "0".

Note that in the byte mode, an external clock must be used as the sync. clock for the purpose of the mode.

A-D CONVERTER

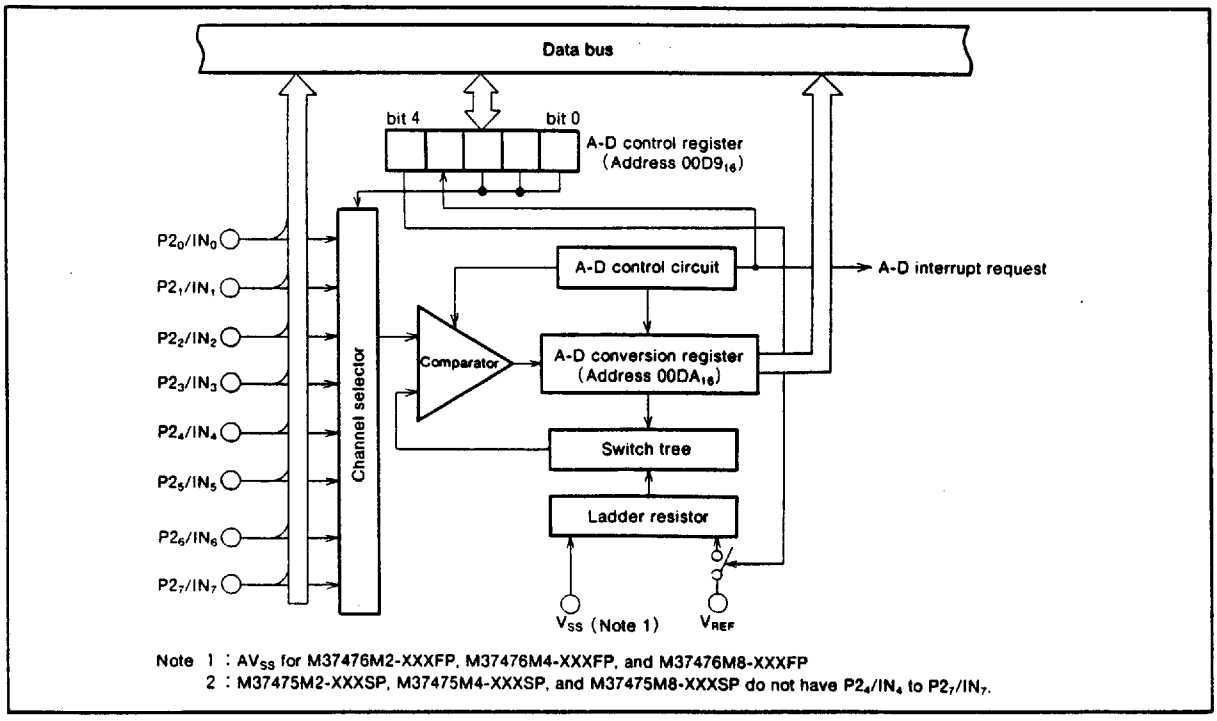
The A-D conversion uses an 8-bit successive comparison method. Figure 11 shows a block diagram of the A-D conversion circuit. Conversion is automatically carried out once started by the program.

There are eight analog input pins which are shared with $P2_0$ to $P2_7$ of port P2 (Only $P2_0$ to $P2_3$ 4-bit for M37475M2, M37475M4, and M37475M8). Which analog inputs are to be A-D converted is specified by using bit 2 to bit 0 in the A-D control register (address $00D9_{16}$). Pins for inputs to be A-D converted must be set for input by setting the direction register bit to "0". Bit 3 in the A-D control register is an A-D conversion end bit. This is "0" during A-D conversion; it is set to "1" when the conversion is terminated. Therefore, it is possible to know whether A-D conversion is terminated by checking this bit. Bit 4 in the A-D control register is a V_{REF} connection selection bit.

During A-D conversion, this bit must be set "1" for the ladder resistor and V_{REF} pin to be connected; after the A-D conversion is terminated, this bit can be reset to "0" to separate the ladder resistor from the V_{REF} pin. In this way, power consumption in the ladder resistor can be suppressed while no A-D conversion is performed. Figure 13 shows the relationship between the contents of A-D control register and the selected input pins.

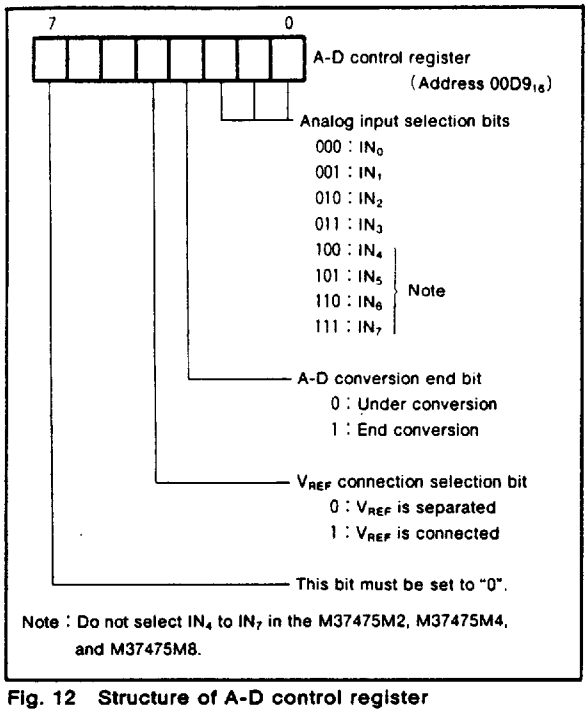
The A-D conversion register (address $00DA_{16}$) contains information on the results of conversion, so that it is possible to know the results of conversion by reading the contents of this register.

The following explains the procedure to execute A-D conversion. First, set values to bit 2 to bit 0 in the A-D control register to select the pins that you want to execute A-D conversion. Next, clear the A-D conversion terminate bit to "0". When the above is done, A-D conversion is initiated. The A-D conversion is completed after an elapse of 50 machine cycles (25μs when $f(X_{IN})=4MHz$), the A-D conversion end bit is set to "1", and the interrupt request bit is set to "1". The results of conversion are contained in the A-D conversion register.



Note 1 : AV_{SS} for M37476M2-XXXFP, M37476M4-XXXFP, and M37476M8-XXXFP
2 : M37475M2-XXXSP, M37475M4-XXXSP, and M37475M8-XXXSP do not have $P2_4/IN_4$ to $P2_7/IN_7$.

Fig. 11 A-D converter circuit



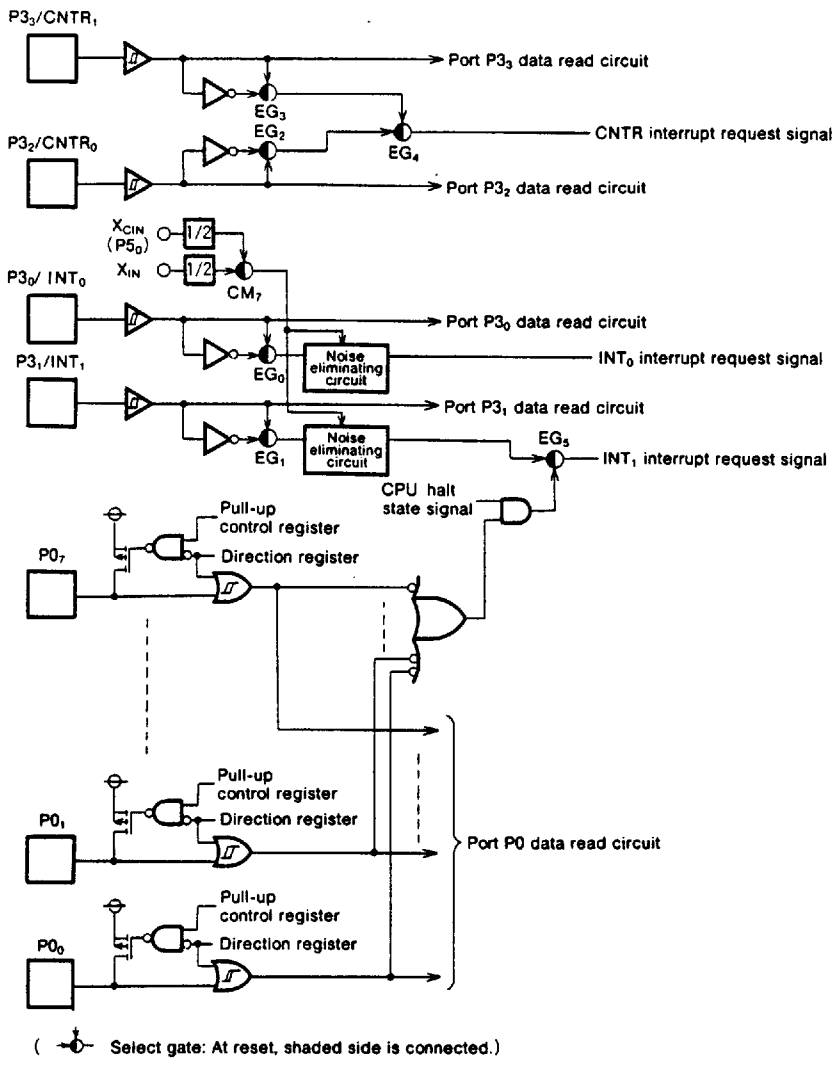
Note : Do not select IN_4 to IN_7 in the M37475M2, M37475M4, and M37475M8.

Fig. 12 Structure of A-D control register

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P0 has a "L" level applied, after bit 5 of the edge polarity selection register (EG_5) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. A key matrix can be connected to port P0 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_1}$ interrupt. When EG_5 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_1}$ are invalid.



Note : The M37475M2, M37475M4, and M37475M8 do not have X_{CIN} input.

Fig. 13 Block diagram of interrupt input and key on wake up circuit

RESET CIRCUIT

The M37475M2-XXXSP, M37476M2-XXXSP/FP are reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is in the recommended operating condition and then returned to "H" level.

The internal initializations following reset are shown in Figure 16.

Example of reset circuit is Figure 14. Immediately after reset, timer 3 and timer 4 are connected, and the f(X_{IN}) divided by 16 are counted. At this time, FF_{16} is set to timer 3, and 07_{16} is set to timer 4. The reset is cleared when timer 4 overflows.

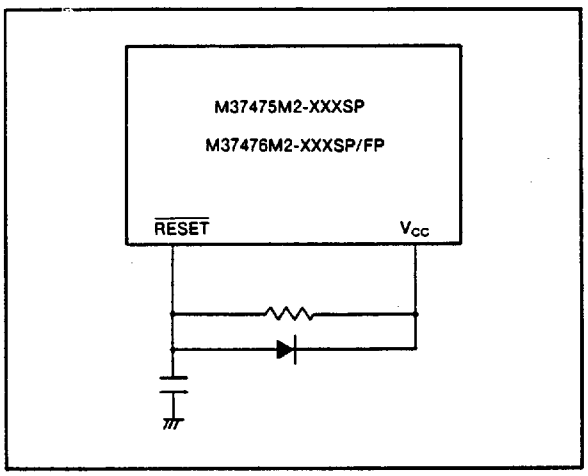
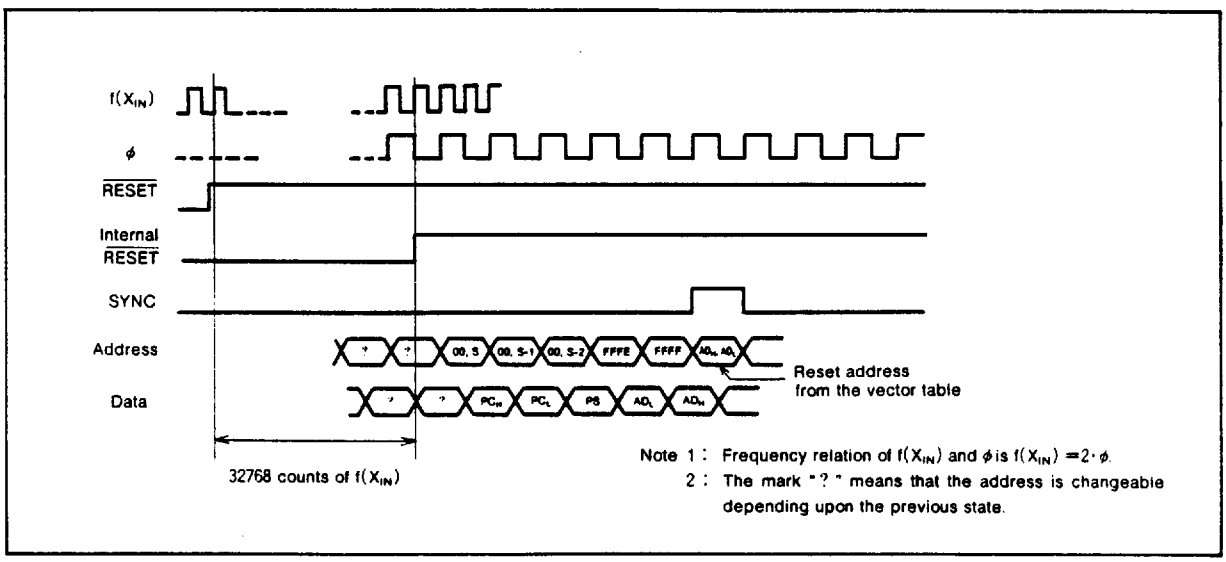


Fig. 14 Example of reset circuit

			Address
(1)	Port P0 direction register	($C1_{16}$)···	00_{16}
(2)	Port P1 direction register	($C3_{16}$)···	00_{16}
(3)	Port P2 direction register	($C5_{16}$)···	00_{16}
(4)	Port P4 direction register	($C9_{16}$)···	? ? ? 0 0 0 0
(5)	P0 pull-up control register	($D0_{16}$)···	00_{16}
(6)	P1—P5 pull-up control register (Note 1)	($D1_{16}$)···	? 0 ? 0 0 0 0 0
(7)	Edge selection register (EG)	($D4_{16}$)···	? ? 0 0 0 0 0 0
(8)	A-D control register	($D9_{16}$)···	0 ? ? 0 1 0 0 0
(9)	Serial I/O mode register (SM)	(DC_{16})···	00_{16}
(10)	Timer 12 mode register (T12M)	($F8_{16}$)···	00_{16}
(11)	Timer 34 mode register (T34M)	($F9_{16}$)···	00_{16}
(12)	Timer mode register 2 (TM2)	(FA_{16})···	0 0 ? ? ? ? 0 0
(13)	CPU mode register (CM)	(FB_{16})···	0 0 0 0 ? ? 0 0
(14)	Interrupt request register 1	(FC_{16})···	0 0 ? ? 0 0 0 0
(15)	Interrupt request register 2	(FD_{16})···	? ? ? ? 0 0 0 0
(16)	Interrupt control register 1	(FE_{16})···	0 0 ? ? 0 0 0 0
(17)	Interrupt control register 2	(FF_{16})···	? ? ? ? 0 0 0 0
(18)	Program counter	(PC_H)···	Contents of address $FFFF_{16}$
		(PC_L)···	Contents of address $FFFE_{16}$
(19)	Processor status register	(PS)···	? ? ? ? ? 1 ? ?

Note 1 : This address is allocated P1—P4 pull-up control register for M37475M2, M37475M4, M37475M8. Bit 6 is not used.
2 : Since the contents of both registers other than those listed above (including timers and the serial I/O register) are undefined at reset, it is necessary to set initial values.

Fig. 16 Internal state of microcomputer at reset



Note 1 : Frequency relation of f(X_{IN}) and ϕ is f(X_{IN}) = 2·ϕ.
2 : The mark "?" means that the address is changeable depending upon the previous state.

Fig. 15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs. As shown in Figure 2, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's direction register allows each bit to be programmed individually as input or output. The direction register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port latch and output. When data is read from the output port, the output pin level is not read, only the latched data of the port latch is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output latch and the pin still remains in the high impedance state. Following the execution of STP or WIT instruction, key matrix with port P0 can be used to generate the interrupt to bring the microcomputer back in its normal state. When this port is selected for input, pull-up transistor can be connected in units of 1-bit.

(2) Port P1

Port P1 has the same function as port P0. $P1_2 - P1_7$ serve dual functions, and the desired function can be selected by the program. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(3) Port P2

Port P2 has the same function as port P0. In the M37475M2, M37475M4, and M37475M8, this port is $P2_0 - P2_3$, a 4-bit I/O port. This port can also be used as an analog voltage input pin. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(4) Port P3

Port P3 is a 4-bit input port.

(5) Port P4

Port P4 is a 4-bit I/O port and has basically the same functions as port P0. In the M37475M2, M37475M4, and M37475M8, this port is $P4_0$ and $P4_1$, a 2-bit I/O port. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(6) Port P5

Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$ and $P5_1$ are shared with clock generating circuit input/output pins.

The M37475M2, M37475M4, and M37475M8 do not have this port.

(7) INT_0 pin ($P3_0/INT_0$ pin)

This is an interrupt input pin, and is shared with port $P3_0$. When a "H" to "L" or a "L" to "H" transition input is applied to this pin, the INT_0 interrupt request bit (bit 0 of address $00FD_{16}$) is set to "1".

(8) INT_1 pin ($P3_1/INT_1$ pin)

This is an interrupt input pin, and is shared with port $P3_1$. When a "H" to "L" or a "L" to "H" transition input is applied to this pin, the INT_1 interrupt request bit (bit 1 of address $00FD_{16}$) is set to "1".

(9) Counter input $CNTR_0$ pin ($P3_2/CNTR_0$ pin)

This is a timer input pin, and is shared with port $P3_2$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and a "H" to "L" or a "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

(10) Counter input $CNTR_1$ pin ($P3_3/CNTR_1$ pin)

This is a timer input pin, and is shared with port $P3_3$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and a "H" to "L" or a "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

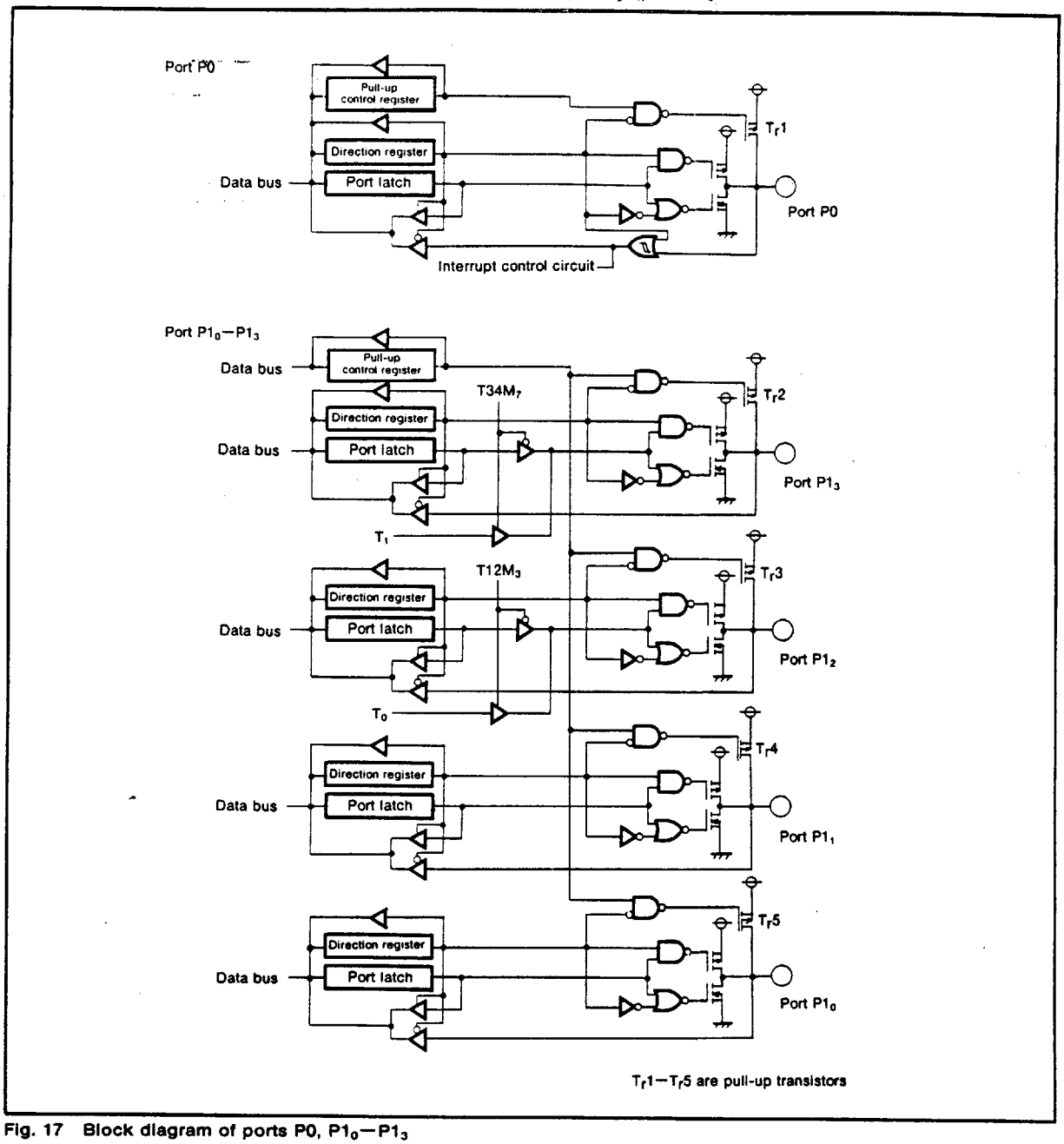


Fig. 17 Block diagram of ports P0, $P1_0$—$P1_3$

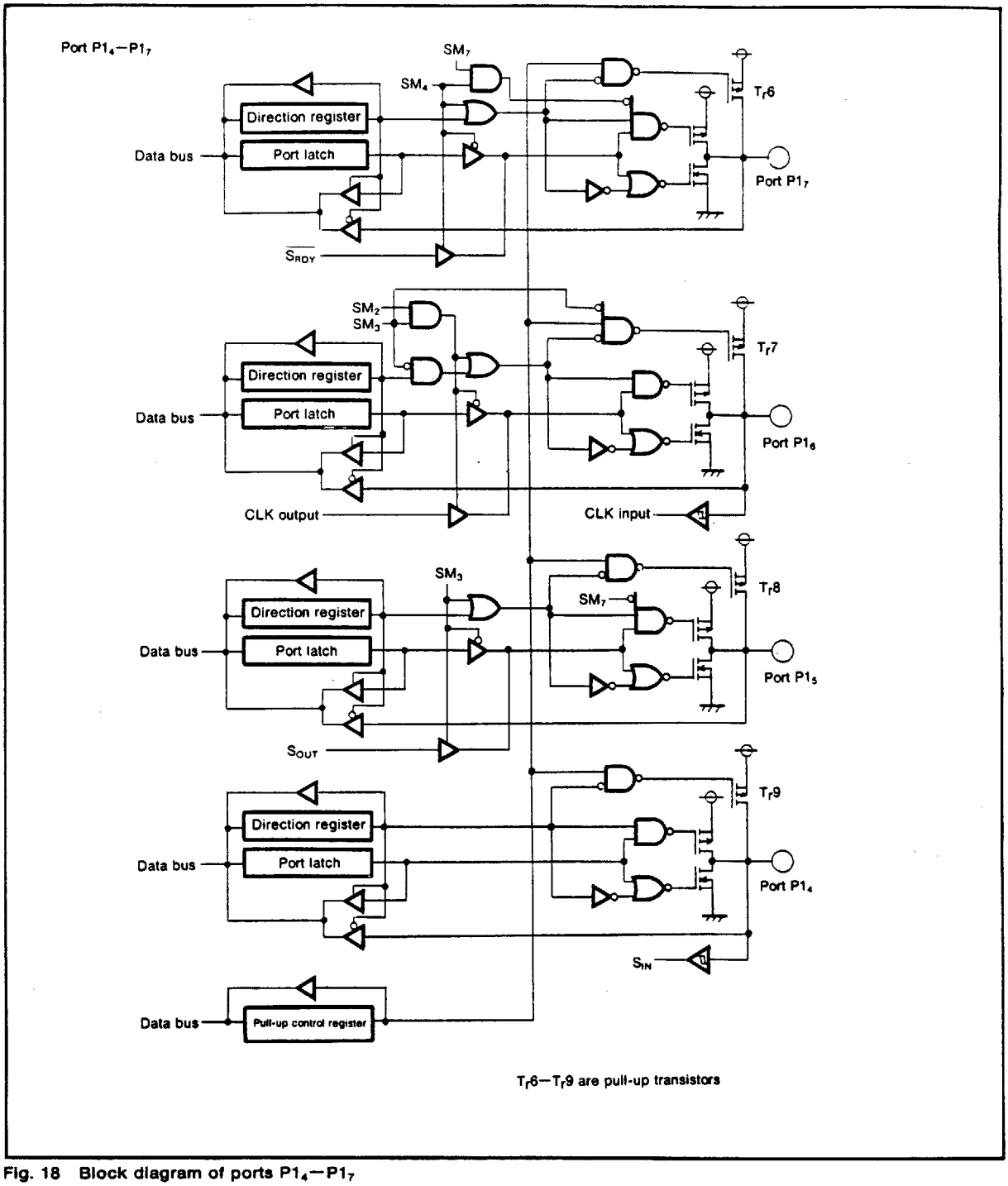


Fig. 18 Block diagram of ports $P1_4$—$P1_7$

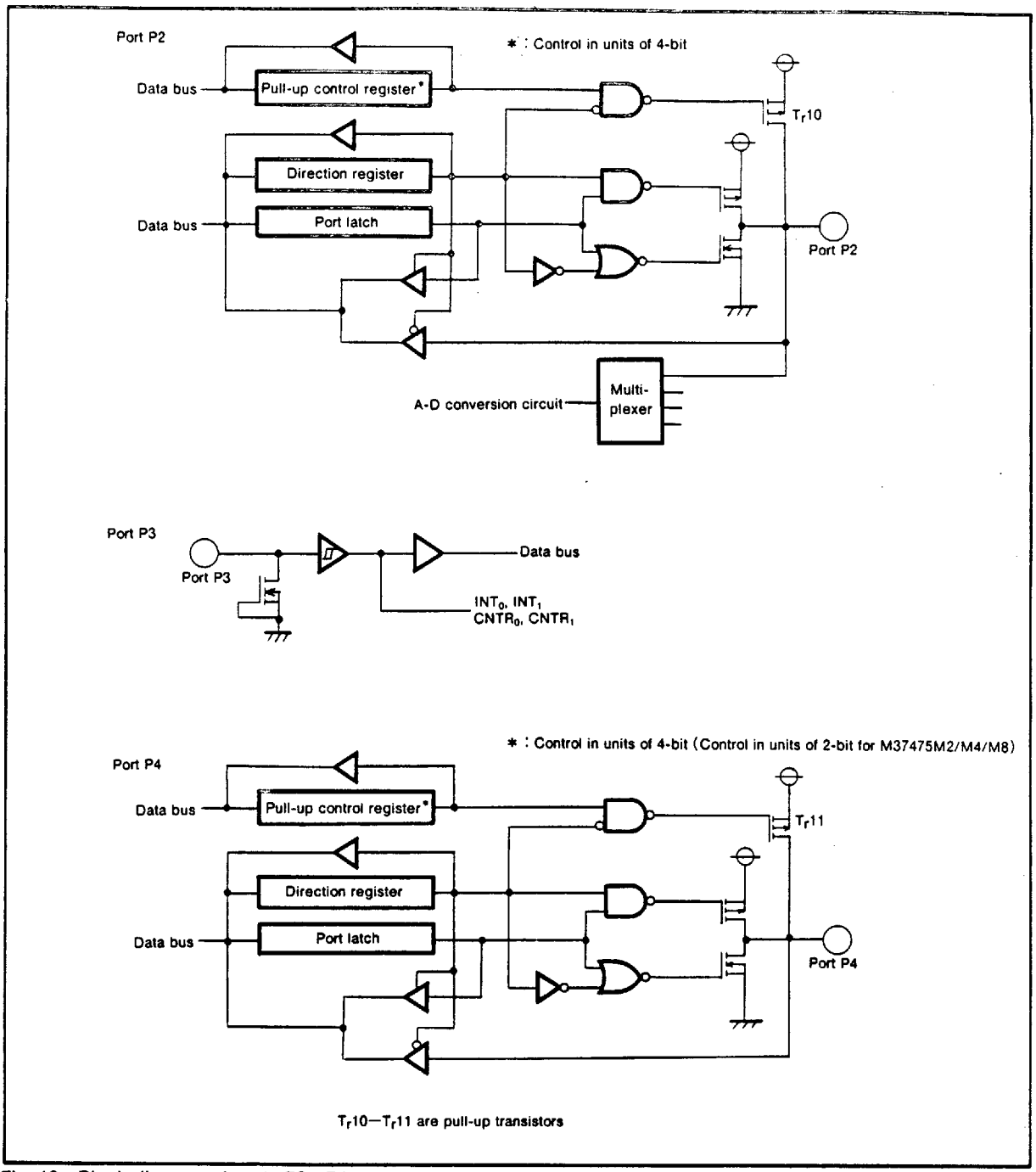


Fig. 19 Block diagram of ports P2—P4

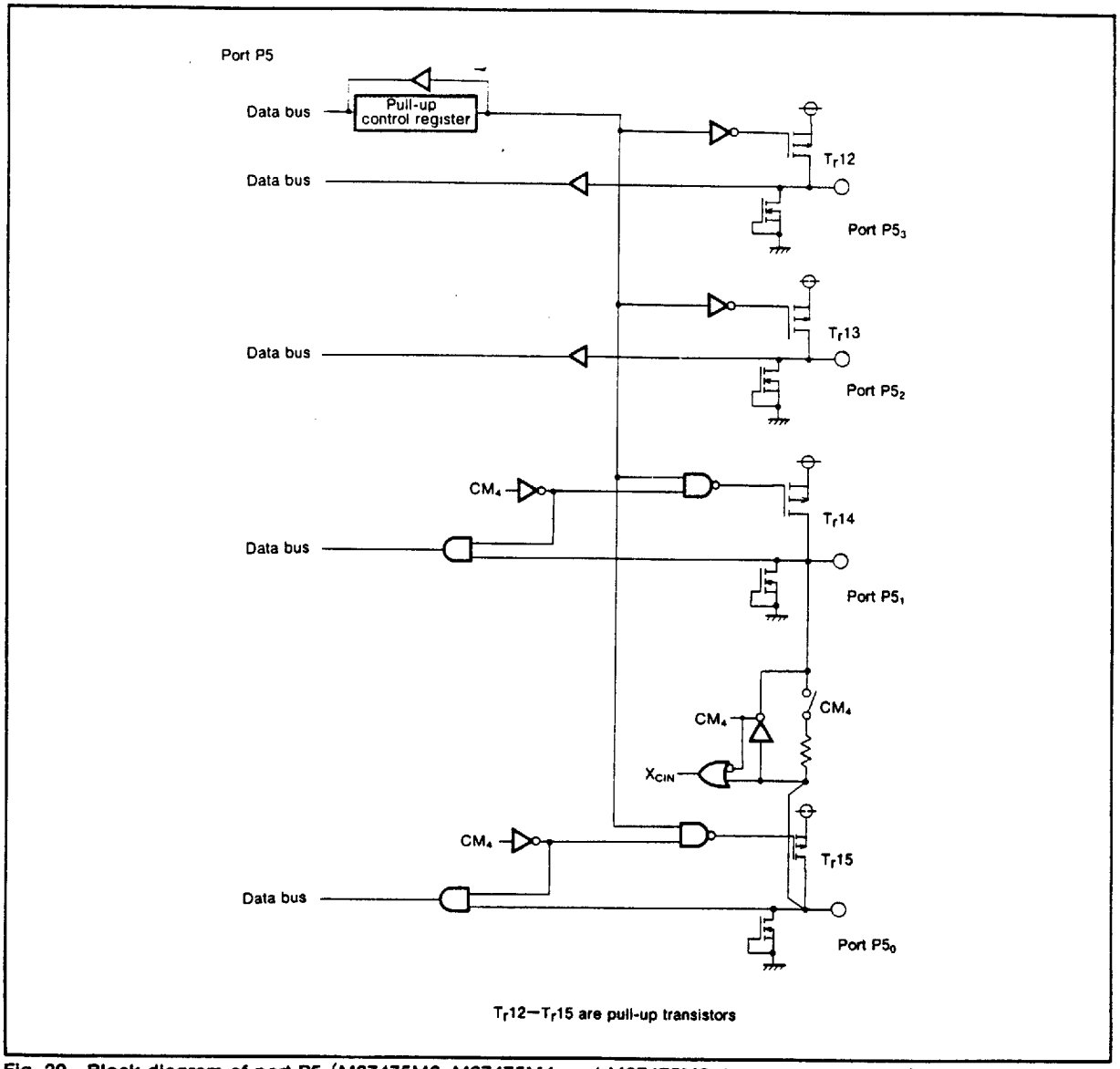


Fig. 20 Block diagram of port P5 (M37475M2, M37475M4, and M37475M8 do not have this port)

CLOCK GENERATING CIRCUIT

The M37475M2-XXXSP has one internal clock generating circuit and M37476M2-XXXSP/FP has two internal clock generating circuits. Figure 25 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by two is used as the internal clock ϕ. Bit 7 of CPU mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} in the M37476M2-XXXSP/FP.

Figure 21, 22 show a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 23, 24.

The M37475M2-XXXSP and M37476M2-XXXSP/FP have two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 3 and timer 4 are forcibly connected and FF_{16} is automatically set in timer 3 and 07_{16} in timer 4.

Although oscillation is restarted when an external interrupt is accepted, the internal clock ϕ remains in the "H" state until timer 4 overflows. In other words, the internal clock ϕ is not supplied until timer 4 overflows. This is because when a ceramic or similar other oscillator is used, a finite time is required until stable oscillation is obtained after restart.

The microcomputer enters an wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer recieves an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode or the stop mode must be set to "1" before executing the WIT or the STP instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($30\mu A$ typ. at $f(X_{CIN})=32kHz$).This operation is only M37476M2-XXXSP/FP X_{IN} clock oscillation is stopped when the bit 6 of CPU mode register is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 27 shows the transition of states for the system clock.

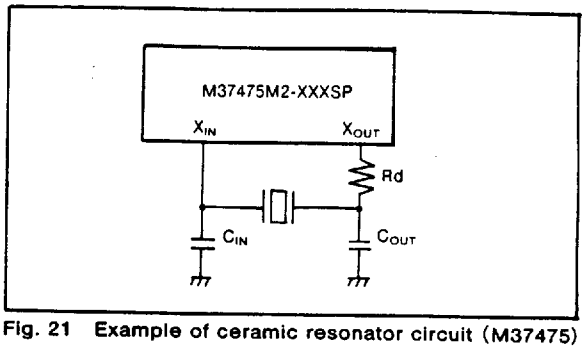


Fig. 21 Example of ceramic resonator circuit (M37475)

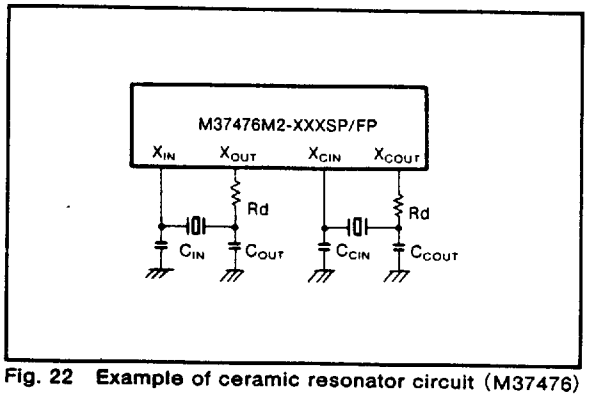


Fig. 22 Example of ceramic resonator circuit (M37476)

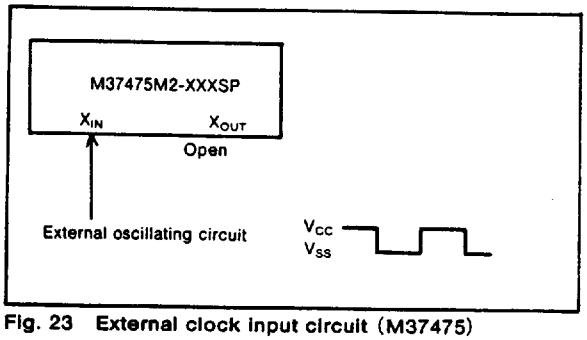


Fig. 23 External clock input circuit (M37475)

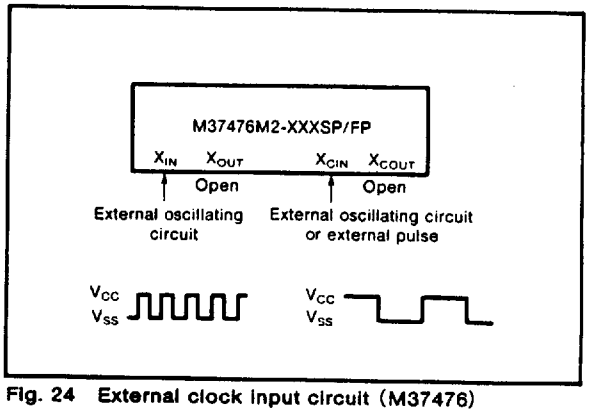


Fig. 24 External clock input circuit (M37476)

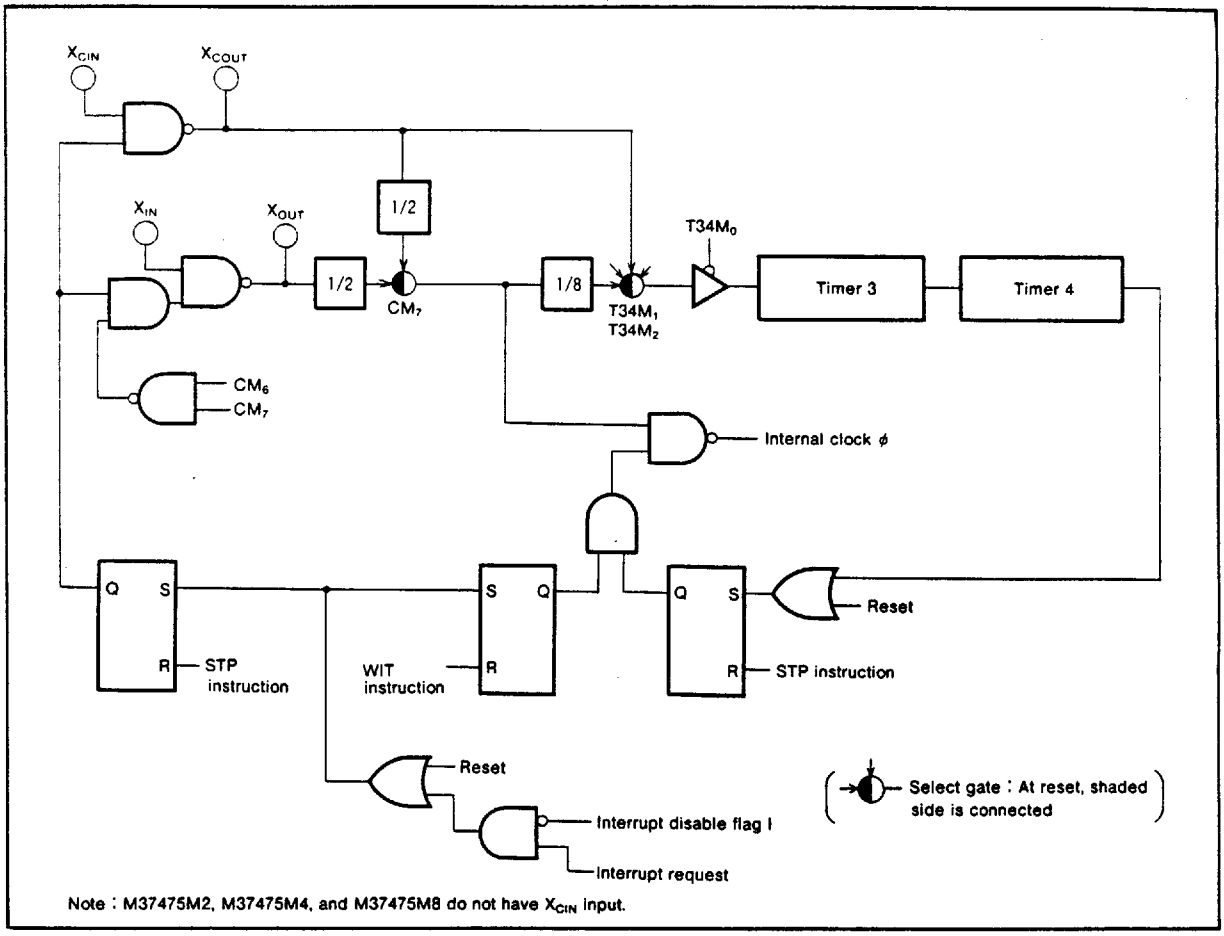


Fig. 25 Block diagram of clock generating circuit

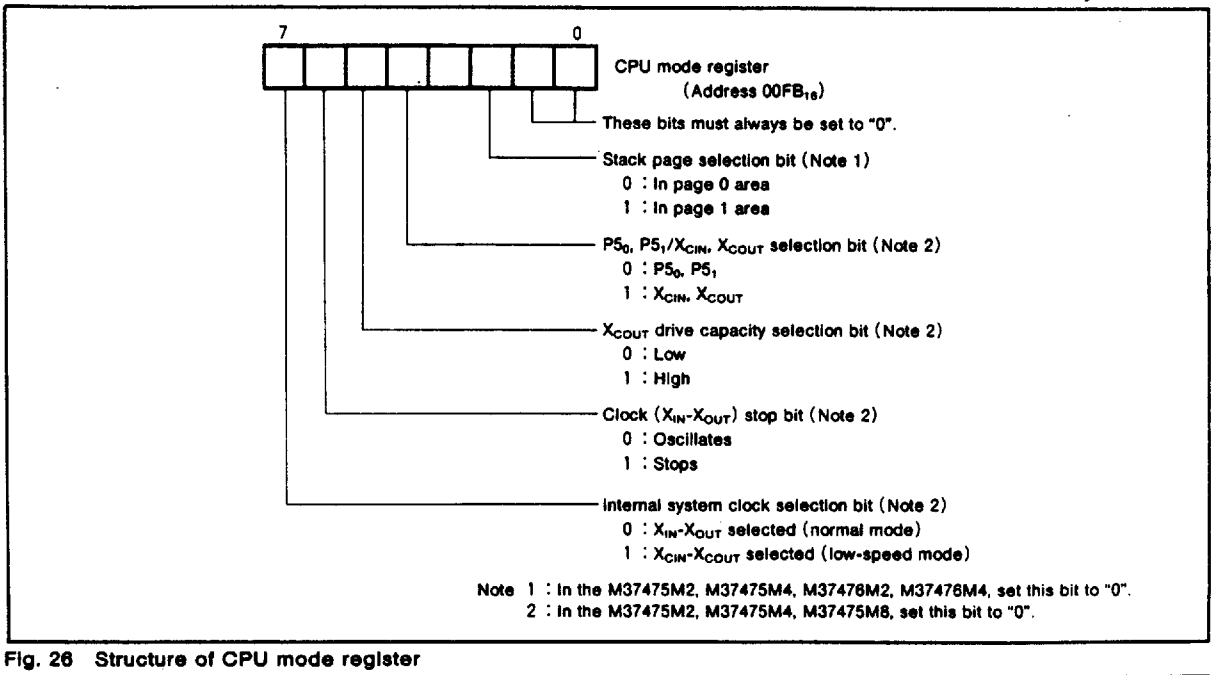
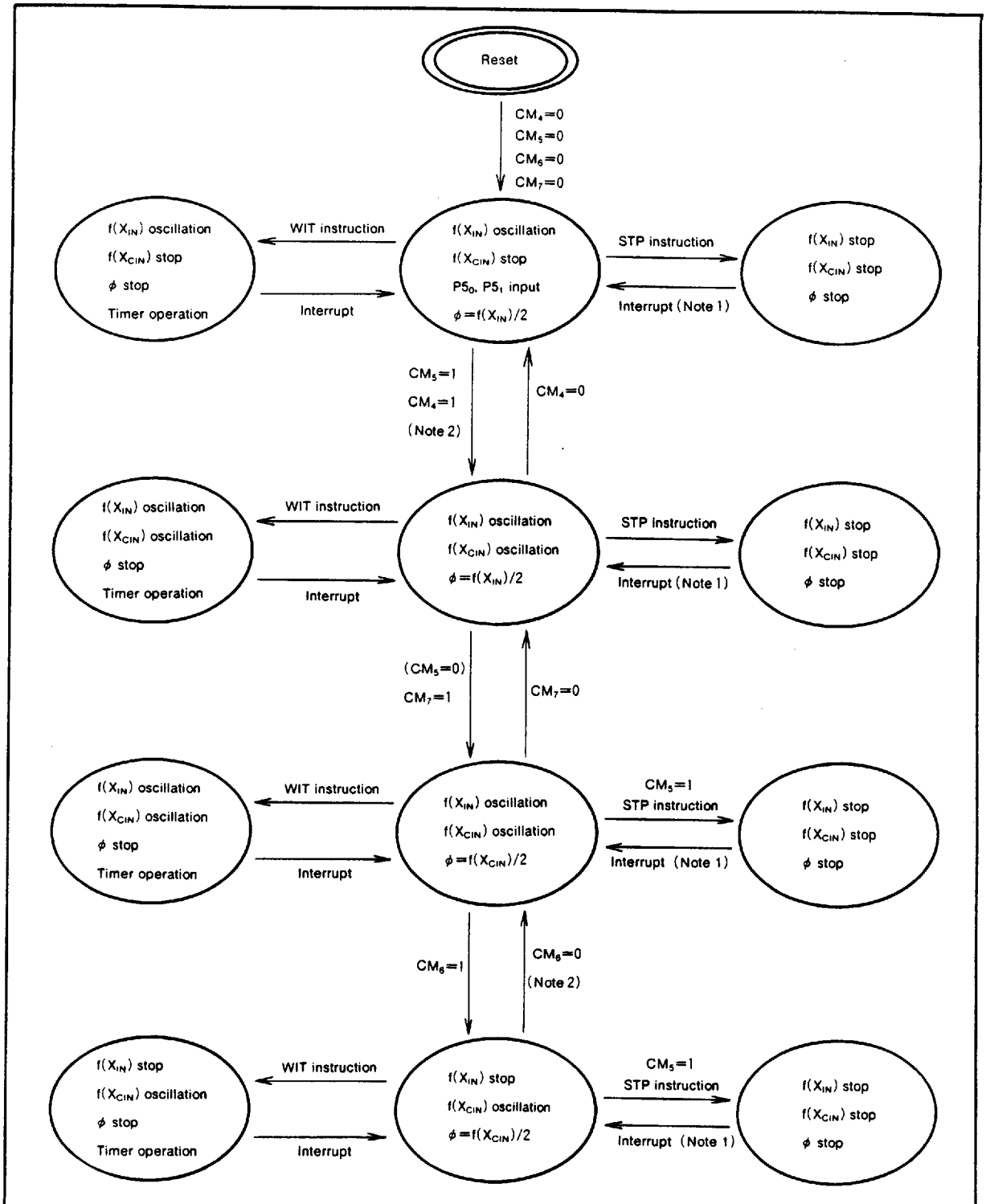


Fig. 26 Structure of CPU mode register

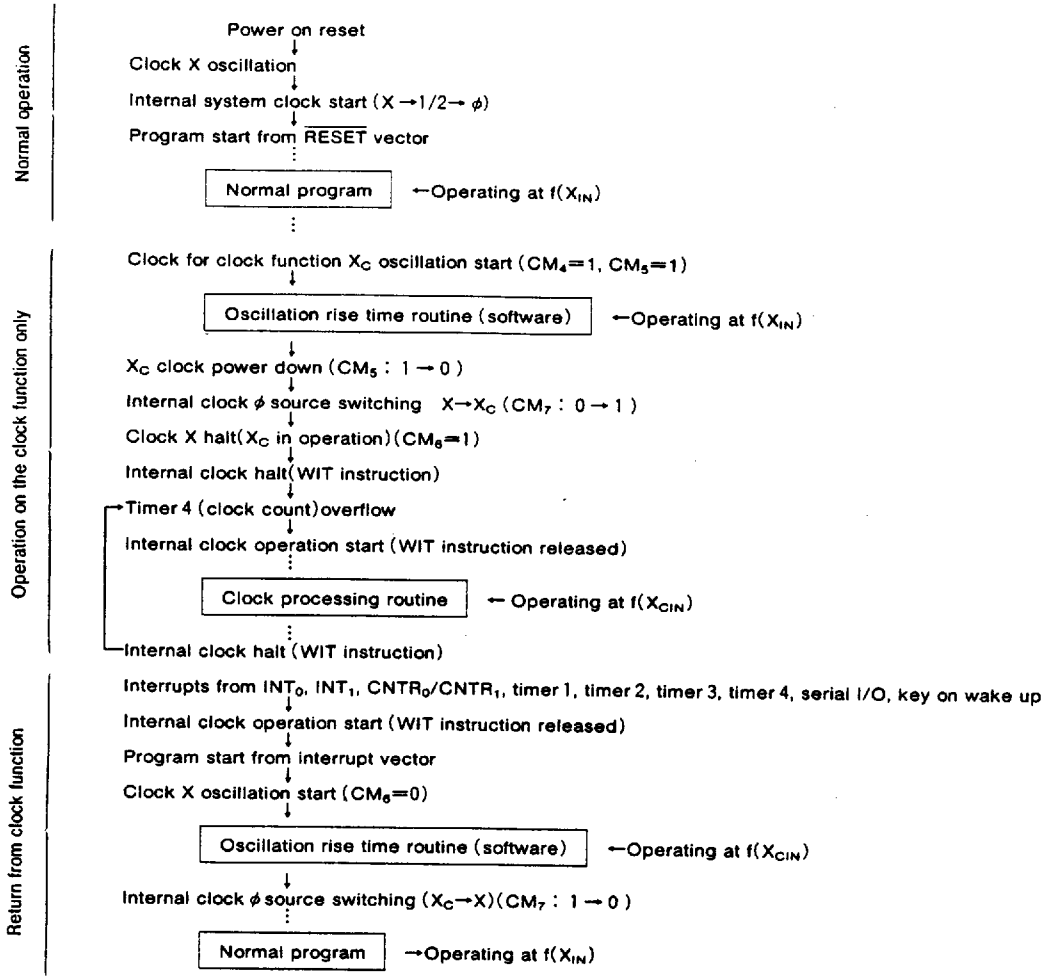


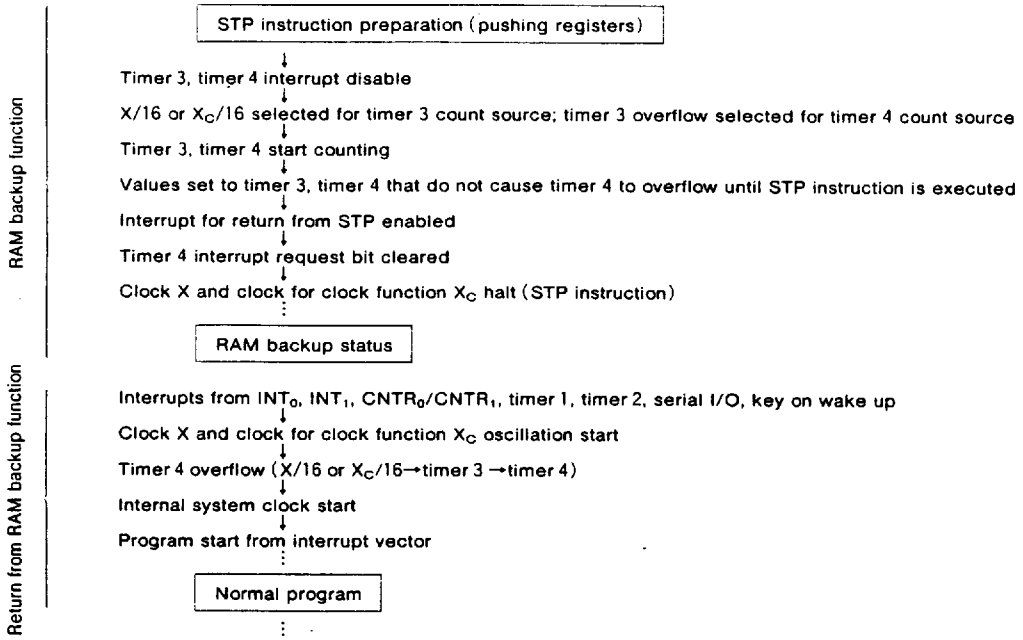
Note 1 : Latency time are automatically generated upon release from the STP instruction due to the connections of timer 3 and 4.

2 : When the system clock is switched over by restarting clock oscillation, a certain wait time required for oscillation to stabilize must be inserted by the program.

Fig. 27 Transition of states for the system clock.

<An example of flow for system>




RAM backup function
STP instruction preparation (pushing registers)
Timer 3, timer 4 interrupt disable
X/16 or X_C/16 selected for timer 3 count source; timer 3 overflow selected for timer 4 count source
Timer 3, timer 4 start counting
Values set to timer 3, timer 4 that do not cause timer 4 to overflow until STP instruction is executed
Interrupt for return from STP enabled
Timer 4 interrupt request bit cleared
Clock X and clock for clock function X_C halt (STP instruction)
RAM backup status
Return from RAM backup function
Interrupts from INT_0, INT_1, $CNTR_0$/$CNTR_1$, timer 1, timer 2, serial I/O, key on wake up
Clock X and clock for clock function X_C oscillation start
Timer 4 overflow (X/16 or X_C/16→timer 3 →timer 4)
Internal system clock start
Program start from interrupt vector
Normal program

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(4) An NOP instruction must be used after the execution of a PLP instruction.

(5) During A-D conversion, don't use STP instruction.

(6) In the M37475M2, M37475M4, and M37475M8, set bit 0, bit 1, and bit 3 — bit 7 to "0" of the CPU mode register.

(7) Multiply/Divide instructions

1. The MUL and DIV instructions are not affected by the T and D flags.
2. The contents of the processor status register are unaffected by multiply or divide instructions.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mask specification form

(3) ROM data ..... EPROM 3 sets

M37475M2-XXXSP, M37475M4-XXXSP, M37475M8-XXXSP ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3 to 7	V
V_I	Input voltage X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P3_0$−$P3_3$, $P4_0$, $P4_1$, V_{REF}, $\overline{RESET}$		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$, X_{OUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25°C	1000	mW
Topr	Operating temperature		−20 to 85	°C
Tstg	Storage temperature		−40 to 150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_3$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $P2_0$−$P2_3$, $P4_0$, $P4_1$	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_3$	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $P2_0$−$P2_3$, $P4_0$, $P4_1$	0		0.25V_{CC}	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$−$P0_7$, $P4_0$, $P4_1$			−30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$−$P1_7$, $P2_0$−$P2_3$			−30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$−$P0_7$, $P4_0$, $P4_1$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$−$P1_7$, $P2_0$−$P2_3$			60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$			−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$			20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$ (Note 2)			−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$ (Note 2)			10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 1)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK ($P1_5$) (Note 1)			1	MHz
$f(X_{IN})$	Clock input oscillating frequency (Note 1)			4	MHz

Note 1 : Oscillation frequency is at 50% duty cycle.
2 : The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100ms.

M37475M2-XXXSP, M37475M4-XXXSP, M37475M8-XXXSP
ELECTRICAL CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=0 V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_3$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{T+}−V_{T-}	Hysteresis $P0_0$−$P0_7$, $P3_0$−$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}−V_{T-}	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_2$, $P4_0$, $P4_1$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$−$P2_3$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_2$, $P4_0$, $P4_1$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$−$P2_3$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At wait mode, X_{IN}=4MHz	V_{CC}=5V		1	2	
			V_{CC}=3V		0.5	1	
		Stop all oscillation V_{CC}=5V	T_a=25℃		0.1	1	μA
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

M37476M2-XXXSP/FP, M37476M4-XXXSP/FP, M37476M8-XXXSP/FP ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3 to 7	V
V_I	Input voltage X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_3$, $P4_0$−$P4_3$, $P5_0$−$P5_3$, V_{REF}, $\overline{RESET}$		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$, X_{OUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 150	℃

Note 1 : 500mW for M37476M2/M4/M8-XXXFP.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_3$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$−$P2_7$, $P4_0$−$P4_3$, $P5_0$−$P5_3$ (Note 1)	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_3$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$−$P2_7$, $P4_0$−$P4_3$, $P5_0$−$P5_3$ (Note 1)	0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$−$P0_7$, $P4_0$−$P4_3$			−30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$−$P1_7$, $P2_0$−$P2_7$			−30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$−$P0_7$, $P4_0$−$P4_3$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$−$P1_7$, $P2_0$−$P2_7$			60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$			−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$			20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$ (Note 2)			−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$ (Note 2)			10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 3)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK ($P1_6$) (Note 3)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 3)			4	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 3, 4)		32	50	kHz

Note 1 : It is except to use $P5_0$ as X_{CIN}.
2 : The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100ms.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the clock oscillating frequency for clock function should be $f(X_{CIN}) < f(X_{IN})/3$.

M37476M2-XXXSP/FP, M37476M4-XXXSP/FP, M37476M8-XXXSP/FP
ELECTRICAL CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P4_0$−$P4_3$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{T+}−V_{T-}	Hysteresis $P0_0$−$P0_7$, $P3_0$−$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}−V_{T-}	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_2$, $P4_0$−$P4_3$, $P5_0$−$P5_3$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$−$P2_7$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_2$, $P4_0$−$P4_3$, $P5_0$−$P5_3$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$−$P2_7$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At low-speed mode, X_{COUT} is low-power mode, A-D conversion is not executed X_{IN}=0Hz, X_{CIN}=32kHz, T_a=25℃	V_{CC}=5V		30	80	μA
			V_{CC}=3V		15	40	
		At wait mode, X_{IN}=4MHz	V_{CC}=5V		1	2	mA
			V_{CC}=3V		0.5	1	
		At wait mode, X_{IN}=0Hz, X_{CIN}=32kHz, X_{COUT} is low-power mode, T_a=25℃	V_{CC}=5V		3	12	μA
			V_{CC}=3V		2	8	
		Stop all oscillation V_{CC}=5V	T_a=25℃		0.1	1	
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, T_a=−20 to 85°C, f(X_{IN})=4MHz, unless otherwise noted)

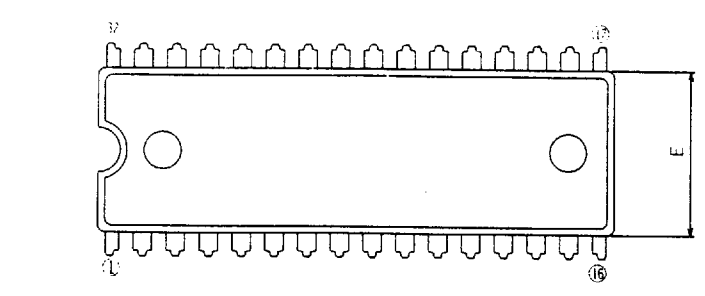
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

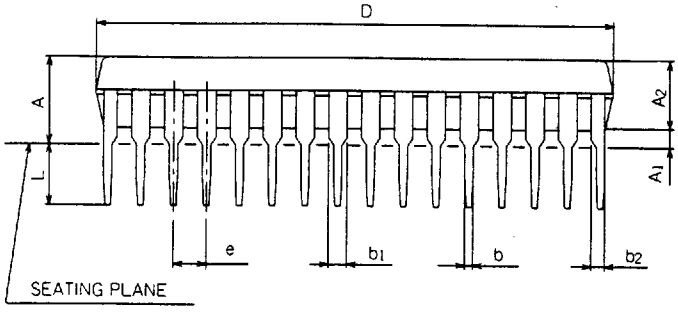
32P4B

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP032-P-0400	-	2.2

Scale 2.5 1





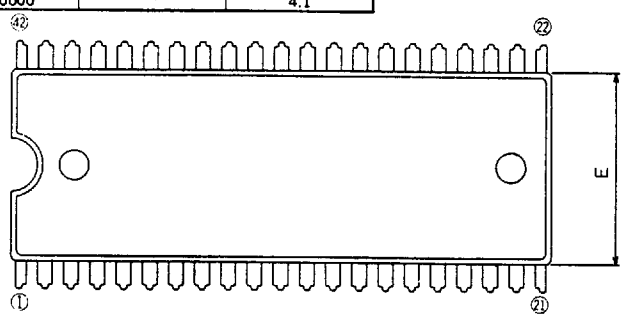
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A1	0.51	–	–
A2	–	3.8	–
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
|e1|	–	10.16	–
L	3.0	–	–
θ	0	–	15

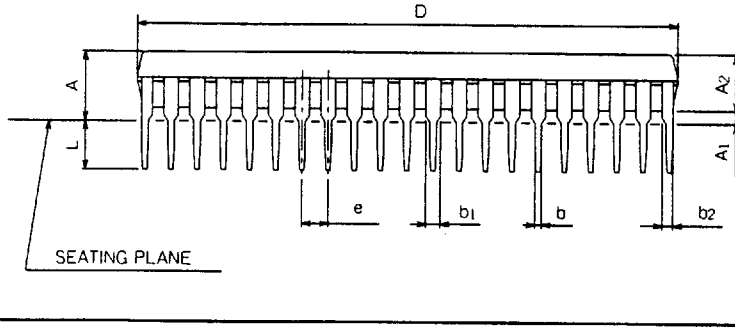
42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)
SDIP042-P-0600	-	4.1

Scale : 2/1





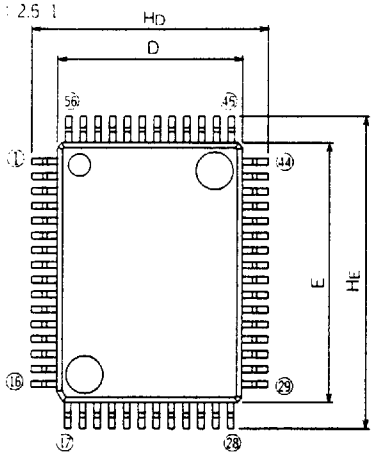
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A1	0.51	–	–
A2	–	3.8	–
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
|e1|	–	15.24	–
L	3.0	–	–
θ	0	–	15

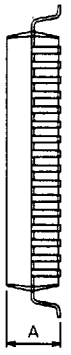
56P6N-A

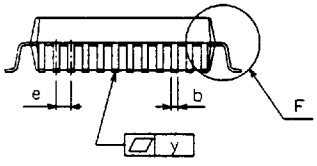
Plastic 56pin 10×14mm body QFP

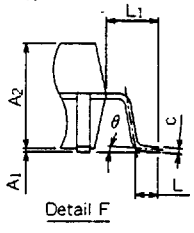
EIAJ Package Code	JEDEC Code	Weight(g)
*QFP056-P-1014	–	0.79

Scale : 2.5 : 1

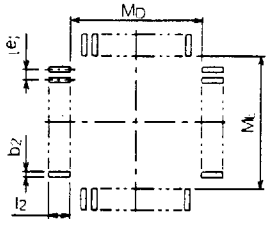








Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	9.8	10.0	10.2
E	13.8	14.0	14.2
e	–	0.8	–
H_D	12.5	12.8	13.1
H_E	16.5	16.8	17.1
L	0.4	0.6	0.8
L_1	–	1.4	–
y	–	–	0.1
θ	0	–	10
b_2	–	0.5	–
l_2	–	1.3	–
M_D	–	10.6	–
M_E	–	14.6	–