March 2015

FAN6100Q
Secondary-Side Constant Voltage and Constant Current Controller Compatible with Qualcomm® Quick Charge 2.0

Features

- Supports Qualcomm® Quick Charge 2.0 Specification
- Secondary-Side Constant Voltage (CV) and Constant Current (CC) Regulation
- Built-in Charge-Pump Circuit for Low Output Voltage Operation
- Internal, Accurate, Adaptive CV/CC Reference Voltage
- Low-Value Current Sensing Resistor for High Efficiency
- Programmable Cable Voltage Drop Compensation
- Two Operational Transconductance Amplifiers with Open-Drain Type for Dual-Loop CV/CC Control
- Compatible with Fairchild's FAN501A
- Adaptive Secondary-Side Output Over-Voltage Protection through Photo-Coupler
- Output Under-Voltage Protection
- Low Quiescent Current Consumption in Green Mode < 850 µA
- Wide V_{IN} Supply Voltage Range
- Available in 20-Pin 3 x 4 mm MLP Package

Applications

- Battery Chargers for quick charge application
- AC/DC Adapters for Portable Devices that Require CV/CC Control

Description

The FAN6100Q is a integrated secondary side power adaptor controller that is compatible with Qualcomm® Quick Charge™ 2.0 Class A technology. It is designed for use in application that requires Constant Voltage (CV) and Constant Current (CC) regulation.

The controller consists of two operational amplifiers for voltage and current loop regulation with adjustable reference voltage. The CC control loop also incorporates a current sense amplifier with gain of 10. Outputs of the CV and CC amplifiers are tied together in open drain configuration.

The FAN6100Q enables power adaptor's output voltage adjustment if it detects a protocol capable powered device. It can be capable of outputting 5.0 V at the beginning, and then 9 V or 12 V to meet requirement of High-Voltage Dedicated Charging Port (HVDCP) power supply. If a non compliant powered device is detected, the controller disables output voltage adjustment to ensure safe operation with smart phone and tablets that support only 5 V.

FAN6100Q also incorporates an internal charge pump circuit to maintain CC regulation down to power supply's output voltage, V_{BUS} of 2 V without an external voltage supply to the IC. Programmable cable voltage drop compensation allows precise CV regulation at the end of a USB cable via adjusting one external resistor.

The device is available in the 20-pin MLP 3 x 4 package.

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Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6100QMPX	-40°C to +125°C	20-Lead, MLP, QUAD, JEDEC MO-220, 3 mm x 4 mm, 0.5 mm Pitch, Single DAP	Tape & Reel

Application Diagram

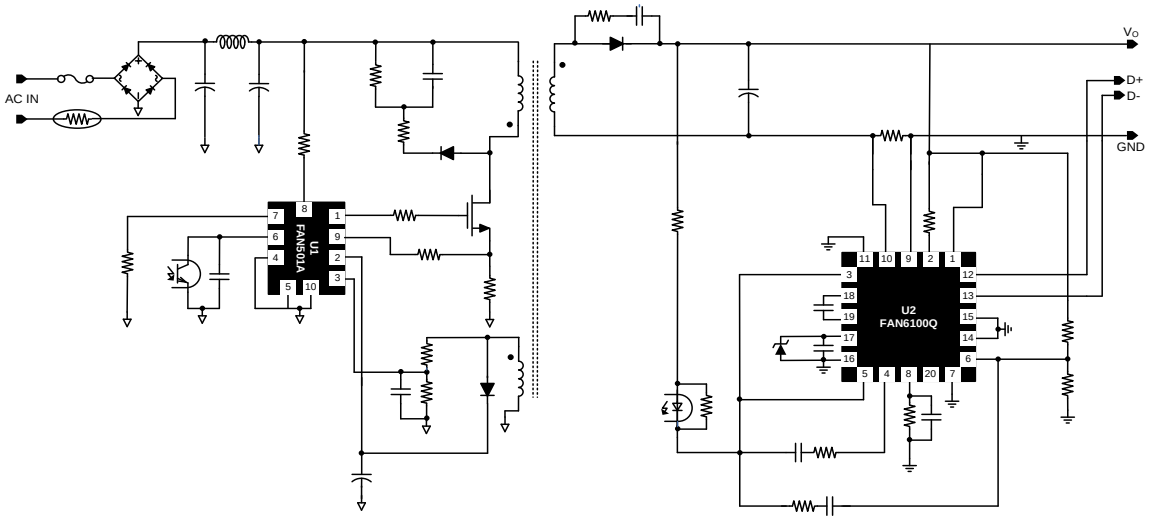


Figure 1. Typical Application

Internal Block Diagram

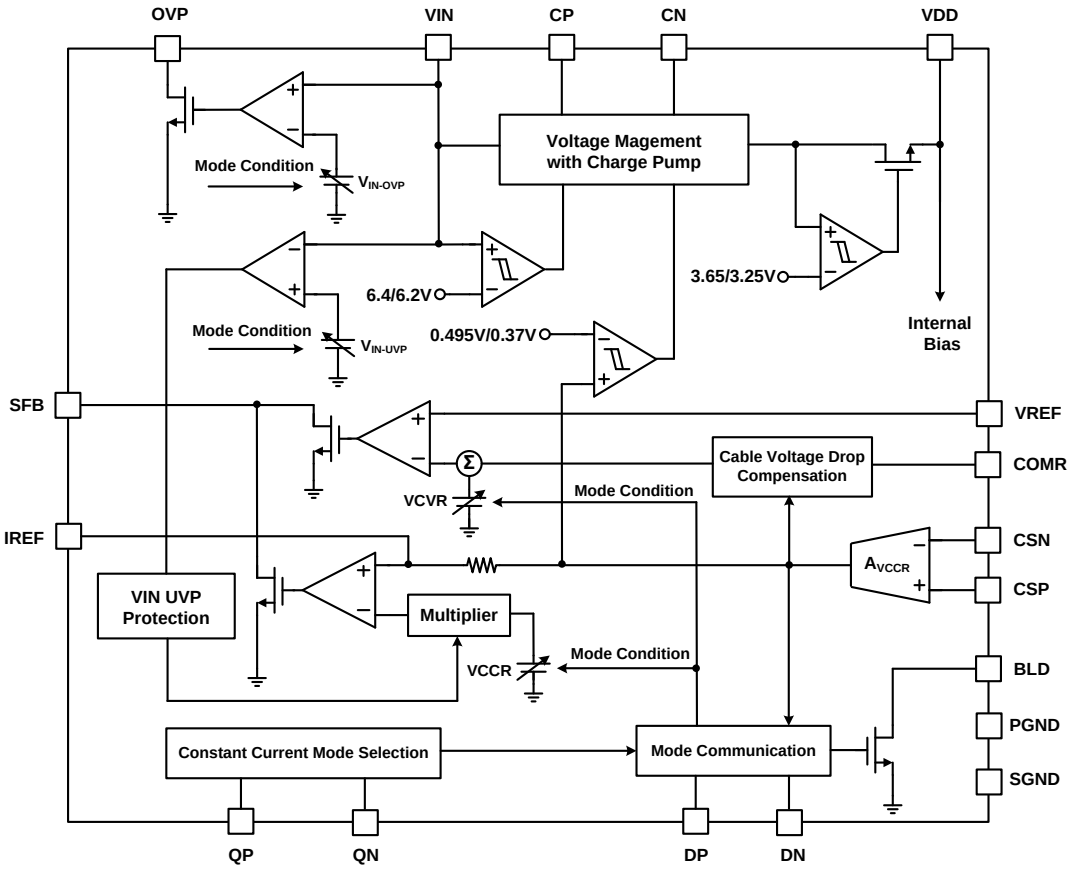
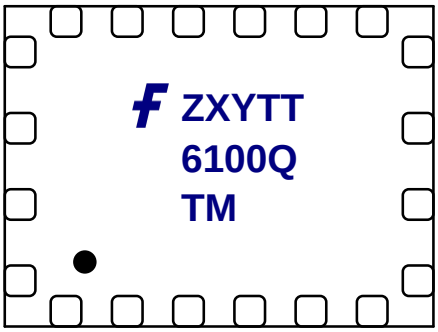


Figure 2. Function Block Diagram

Marking Information



F- Fairchild Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package Type (MP=MLP)
M: Manufacture Flow Code

Figure 3.Top Mark

Pin Configuration

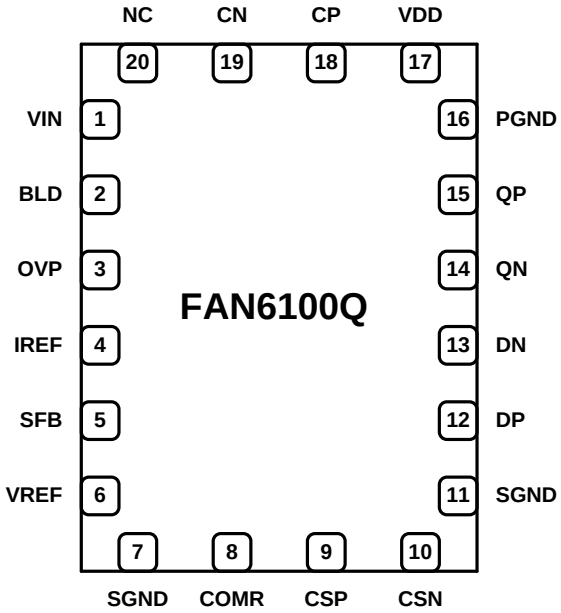


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	VIN	Input Voltage Detection. This pin is tied to output terminal of the power adaptor to monitor output voltage and supply internal charge pump circuit.
2	BLD	Output Bleeder Current Setting. This pin connects to output terminal of the power adaptor via an external resistor to form an output discharging path when mode changes from high-output voltage to low-output voltage.
3	OVP	Output Over-Voltage-Protection. This pin is used for adaptive output over-voltage-protection. Typically an opto-coupler is connected to this pin to generate pull-low protection signal.
4	IREF	Reference Output Current Sensing Voltage. The voltage is the amplifying output current sensing voltage. This pin is tied to the internal CC loop amplifier positive terminal.
5	SFB	Secondary-Side Feedback Signal. Common output terminal of the dual operational transconductance amplifiers with open drain operation. Typically an opto-coupler is connected to this pin to provide feedback signal to the primary-side PWM controller.
6	VREF	Reference Output Voltage Sensing Voltage. This pin is used to sense the output voltage for CV regulation via resistor divider. It is tied to the internal CV loop amplifier positive terminal.
7	SGND	Signal Ground.
8	COMR	Programmable Cable-Drop Voltage Compensation. An external resistor is connected to this pin to adjust output voltage compensation weighting.
9	CSP	Positive Terminal of Output Current Sensing Amplifier. This pin connects directly to the positive voltage terminal of the current sense resistor. CSP need to be tied to ground of power adaptor via short PCB trace.
10	CSN	Negative Terminal of Output Current Sensing Amplifier. This pin connects directly to the negative voltage terminal of the current sense resistor. CSN need to be tied to negative terminal of output capacitor via short PCB trace.
11	SGND	Signal Ground.
12	DP	Positive Terminal of Communication Interface. This pin is tied to the USB D+ data line input.
13	DN	Negative Terminal of Communication Interface. This pin is tied to the USB D- data line input.
14	QN	LSB Switch for Mode Selection of Output Current.
15	QP	MSB Switch for Mode Selection of Output Current.
16	PGND	Power Ground.
17	VDD	Power Supply. IC operating current is supplied through this pin. This pin is typically connected to an external VDD capacitor.
18	CP	Positive Voltage Terminal of Charge Pump.
19	CN	Negative Voltage Terminal of Charge Pump. An external capacitor is necessary to be connected between CP pin and CN pin.
20	NC	No Connect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{VIN}	VIN Pin Input Voltage			20	V
V_{BLD}	BLD Pin Input Voltage			20	V
V_{OVP}	OVP Pin Input Voltage			20	V
V_{SFB}	SFB Pin Input Voltage		-0.3	20	V
V_{IREF}	IREF Pin Input Voltage		-0.3	6.0	V
V_{VREF}	VREF Pin Input Voltage		-0.3	6.0	V
V_{COMR}	COMR Pin Input Voltage		-0.3	6.0	V
V_{CSP}	CSP Pin Input Voltage		-0.3	6.0	V
V_{CSN}	CSN Pin Input Voltage		-0.3	6.0	V
V_{DP}	DP Pin Input Voltage		-0.3	6.0	V
V_{DN}	DN Pin Input Voltage		-0.3	6.0	V
V_{QN}	QN Pin Input Voltage		-0.3	6.0	V
V_{QP}	QP Pin Input Voltage		-0.3	6.0	V
V_{DD}	VDD Pin Input Voltage		-0.3	6.0	V
V_{CP}	CP Pin Input Voltage		-0.3	6.0	V
V_{CN}	CN Pin Input Voltage		-0.3	6.0	V
P_D	Power Dissipation (T_A=25°C)			0.88	W
θ_{JA}	Thermal Resistance (Junction-to-Air)			110	°C/W
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-40	+150	°C
T_L	Lead Temperature, (Wave soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114		2.0	kV
		Charged Device Model, JEDEC:JESD22_C101		2.0	

Note:

1. All voltage values, except differential voltages, are given with respect to GND pin.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_J	Junction Temperature	-40	+125	°C
V_{DD-OP}	VDD Operating Voltage	3.12	6.00	V
V_{IN-OP}	VIN Operating Voltage		16	V

Electrical Characteristics

V_{IN}=5 V or 9 V or 12 V at T_J = -40°C to 125°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Section						
V_{IN-OP}	Continuous Operating Voltage				16	V
$I_{IN-OP-5V}$	Operating Supply Current at 5 V	V_{IN}=5 V, V_{CSP}=100 mV, V_{CSN}=0V		2.4	3.2	mA
$I_{IN-OP-9V,12V}$	Operating Supply Current Over 5 V (9 V, 12 V)	V_{IN}=12 V, V_{CSP}=100 mV, V_{CSN}=0 V		1.2	2.0	mA
$I_{IN-Green}$	Green Mode Operating Supply Current	V_{IN}=5 V, V_{CSP}=V_{CSN}=0 V		850	1050	µA
I_{IN-ST}	Startup Current	V_{IN}=1 V, V_{CSP}=100 mV, V_{CSN}=0 V			15	µA
$V_{IN-UVP-L-5V}$	V_{IN} Under-Voltage-Protection Enable Voltage at 5 V		2.35	2.50	2.65	V
$V_{IN-UVP-H-5V}$	V_{IN} Under-Voltage-Protection Disable Voltage at 5 V		2.85	3.00	3.15	V
$V_{IN-UVP-L-9V}$	V_{IN} Under-Voltage-Protection Enable Voltage at 9 V		6.50	6.75	7.00	V
$V_{IN-UVP-H-9V}$	V_{IN} Under-Voltage-Protection Disable Voltage at 9 V		7.40	7.65	7.90	V
$V_{IN-UVP-L-12V}$	V_{IN} Under-Voltage-Protection Enable Voltage at 12 V		8.70	9.00	9.30	V
$V_{IN-UVP-H-12V}$	V_{IN} Under-Voltage-Protection Disable Voltage at 12 V		9.85	10.20	10.55	V
$t_{D-VIN-UVP}$	V_{IN} Under-Voltage-Protection Debounce Time		10	15	20	ms
$V_{IN-EN-L}$	Charge-Pump Enable Threshold Voltage		1.5	2.0	2.5	V
V_{IN-CP}	Charge Pump Disable Threshold Voltage		6.20	6.40	6.60	V
$V_{IN-CP-Hys}$	Hysteresis Voltage for Charge Pump Disable Threshold Voltage			0.20		V
$V_{IN-OVP-5V}$	V_{IN} Over-Voltage-Protection Voltage at 5 V		5.80	6.00	6.20	V
$V_{IN-OVP-9V}$	V_{IN} Over-Voltage-Protection Voltage at 9 V		10.50	10.80	11.10	V
$V_{IN-OVP-12V}$	V_{IN} Over-Voltage-Protection Voltage at 12 V		14.00	14.40	14.80	V
$t_{D-VIN-OVP}$	V_{IN} Over-Voltage-Protection Debounce Time		16	28	40	µs
VDD Section						
V_{DD-ON}	Turn-on Threshold Voltage		3.50	3.65	3.80	V
V_{DD-OFF}	Turn-off Threshold Voltage		3.12	3.25	3.38	V
f_{S-CP}	Charge Pump Switching Frequency[2]		120	125	130	kHz
CC Mode Selection Section						
QP/QN-$_{VR}$	QP/QN State for Variable CC Mode		QP=0 and QN=0			
QP/QN-$_{FIX-1.5A}$	QP/QN State for Fixative 1.5 A CC Mode		QP=0 and QN=1			
QP/QN-$_{FIX-2.0A}$	QP/QN State for Fixative 2.0 A CC Mode		QP=1 and QN=0			
QP/QN-$_{CLPM}$	QP/QN State for Current Limit Protection Mode		QP=1 and QN=1			
t_{D_Mode}	CC Mode Selection De-bounce Time		3.5	4.0	4.5	ms

Continued on the following page…

Electrical Characteristics

V_{IN}=5 V or 9 V or 12 V at T_J = -40°C to 125°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Constant Current Sensing Section						
A_{V-CCR}	Output Current Sensing Amplifier Gain(3)		9.7	10.0	10.3	V/V
$V_{CCR-VR-5V}$	Reference Voltage for Constant Current Regulation at Variable CC 5 V Mode		1.155	1.200	1.245	V
$V_{CCR-VR-9V}$	Reference Voltage for Constant Current Regulation at Variable CC 9 V Mode		0.920	0.960	1.000	V
$V_{CCR-VR-12V}$	Reference Voltage for Constant Current Regulation at Variable CC 12 V Mode		0.685	0.715	0.745	V
$V_{CCR-FIX-1.5A}$	Reference Voltage for Constant Current Regulation at Fixative 1.5 A CC Mode		0.835	0.870	0.905	V
$V_{CCR-FIX-1.5A-12V}$	Reference Voltage for Constant Current Regulation at Fixative 1.5 A CC 12 V Mode		0.635	0.660	0.685	V
$V_{CCR-FIX-2.0A}$	Reference Voltage for Constant Current Regulation at Fixative 2.0 A CC Mode		1.155	1.200	1.245	V
$V_{CCR-FIX-2.0A-12V}$	Reference Voltage for Constant Current Regulation at Fixative 2.0 A CC 12 V Mode		0.865	0.900	0.935	V
$A_{V-CCR-Protection}$	Constant Current Attenuator for Protection Mode				0.125	V/V
$A_{V-CCR-UVP}$	Constant Current Attenuator for V_{IN} Under-Voltage Protection				0.125	V/V
$V_{Green-H}$	Green Mode Disable Threshold Voltage		0.400	0.495	0.590	V
$V_{Green-L}$	Green Mode Enable Threshold Voltage		0.34	0.37	0.40	V
$t_{Green-BLANK}$	Green Mode Blanking Time at Startup(3)			40		ms
Z_{CSP},Z_{CSN}	Current Sensing Input Impedance		4			MΩ
Constant Voltage Sensing Section						
V_{CVR-5V}	Reference Voltage for Constant Voltage Regulation at 5 V		0.980	1.000	1.020	V
V_{CVR-9V}	Reference Voltage for Constant Voltage Regulation at 9 V		1.765	1.800	1.835	V
$V_{CVR-12V}$	Reference Voltage for Constant Voltage Regulation at 12 V		2.355	2.400	2.445	V
Cable Drop Compensation Section						
$K_{COMR-CDC}$	Design Parameter for Cable-Drop Voltage Compensation		0.90	1.00	1.10	µA/V
Constant Current Amplifier Section						
G_{m-CC}	CC Amplifier Transconductance(3)			3.5		S
f_{P-CC}	CC Amplifier Dominate Pole(3)			10		kHz
$R_{CC-IN-CC}$	CC Amplifier Input Resistor(3)		8.50	13.75	19.00	kΩ
Constant Voltage Amplifier Section						
G_{m-CV}	CV Amplifier Transconductance(3)			3.5		S
f_{P-CV}	CV Amplifier Dominate Pole(3)			10		kHz
$I_{Bias-IN-CV}$	CV Amplifier Input Bias Current(3)				30	nA

Continued on the following page…

Electrical Characteristics

V_{IN}=5 V or 9 V or 12 V at T_J = -40°C to 125°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output Bleeder Section						
I_{BLD}	Output Bleeder Current(3)		100		700	mA
t_{BLD}	Output Bleeder Current Discharging Time		290	320	350	ms
Secondary-Side Feedback Section						
$I_{SFB\text{-}Sink\text{-}MAX}$	Maximum SFB Pin Sink Current(3)		2			mA
OVP Section						
$I_{OVP\text{-}Sink\text{-}MAX}$	Maximum OVP Pin Sink Current		2			mA
Qualcomm Protocol Section						
V_{DPL}	DP Low Level Threshold Voltage	BC1.2 Detection	0.23	0.25	0.27	V
V_{DPH}	DP High Level Threshold Voltage		1.94	2.00	2.06	V
V_{DNL}	DN Low Level Threshold Voltage	BC1.2 Detection	0.30	0.35	0.40	V
V_{DNH}	DN High Level Threshold Voltage		1.94	2.00	2.06	V
V_{SEL_REF}	Output Voltage Selection Reference		1.8	2.0	2.2	V
$t_{BC1.2}$	DP and DN High Debounce Time		1.0		1.5	S
t_{DP_UNPLUG}	Unplug DP Low Debounce Time		20	40	60	ms
t_{TOGGLE}	DN Low Debounce Time after BC1.2 Detection is Complete				1	ms
t_{V_CHANGE}	Mode Change Signal Detection Debounce Time		20	40	60	ms
$t_{V\_REQUEST}$	Blanking Time after Mode Change Signal Detection is Complete				200	ms
R_{DP}	DP Resistance		300	500	700	kΩ
R_{DN}	DN Pull-Low Resistance		14.25	19.53	24.80	kΩ

Notes:

2. Guaranteed for temperature range -5°C ~85°C.
3. Guaranteed by design.

Typical Performance Characteristics

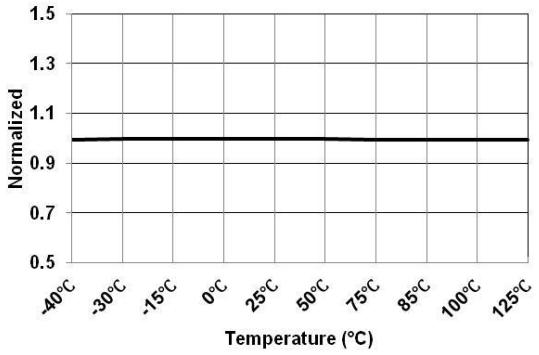


Figure 5. V_{DD} Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

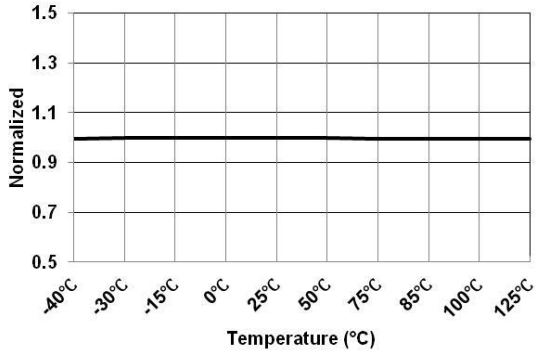


Figure 6. V_{DD} Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

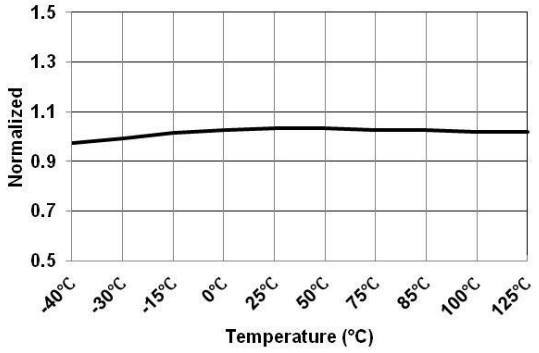


Figure 7. Operating Current Under 5 V ($I_{IN-OP-5V}$) vs. Temperature

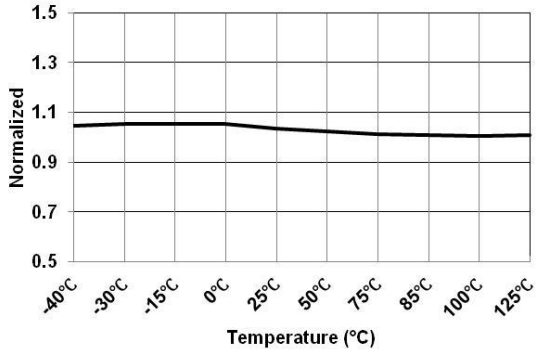


Figure 8. Operating Current Over 5 V ($I_{IN-OP-9V,12V}$) vs. Temperature

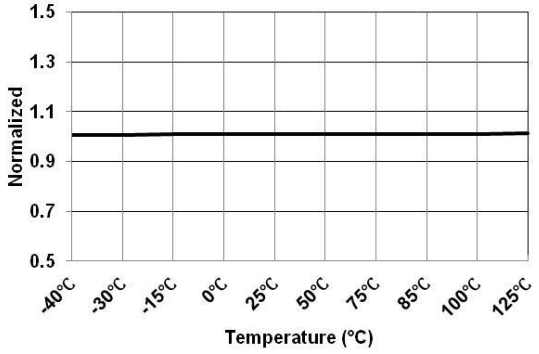


Figure 9. Reference Voltage for CC Regulation at Variable CC 5 V Mode ($V_{CCR-VR-5V}$) vs. Temperature

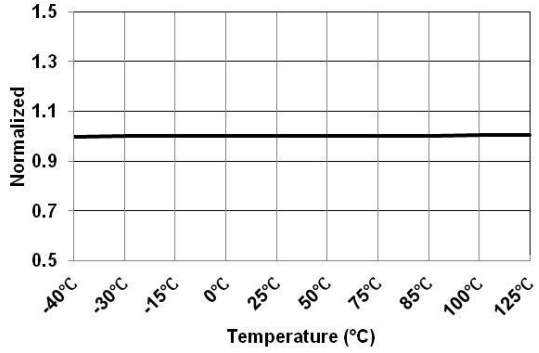


Figure 10. Reference Voltage for CC Regulation at Variable CC 9 V Mode ($V_{CCR-VR-9V}$) vs. Temperature

Typical Performance Characteristics

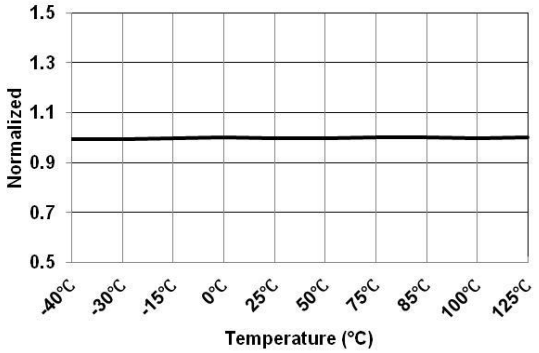


Figure 11. Reference Voltage for CC Regulation at Variable CC 12 V Mode ($V_{CCR-VR-12V}$) vs. Temperature

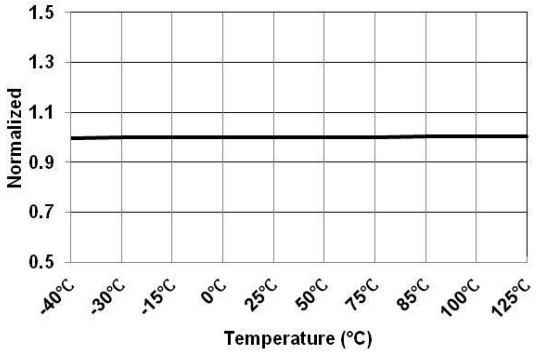


Figure 12. Reference Voltage for CC Regulation at Fixative 1.5 A CC Mode ($V_{CCR-FIX-1.5A}$) vs. Temperature

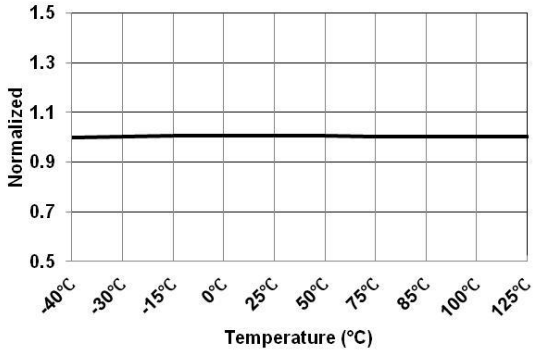


Figure 13. Reference Voltage for CC regulation at Fixative 1.5 A CC 12 V Mode ($V_{CCR-FIX-1.5A-12V}$) vs. Temperature

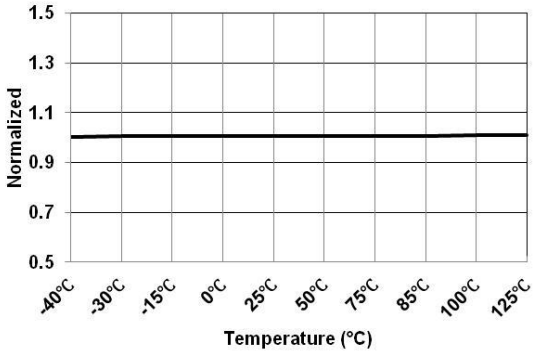


Figure 14. Reference Voltage for CC Regulation at Fixative 2.0 A CC Mode ($V_{CCR-FIX-2.0A}$) vs. Temperature

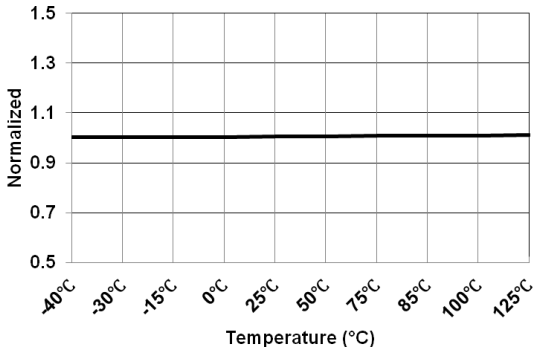


Figure 15. Reference Voltage for CC Regulation at Fixative 2.0 A CC 12 V Mode ($V_{CCR-FIX-2.0A-12V}$) vs. Temperature

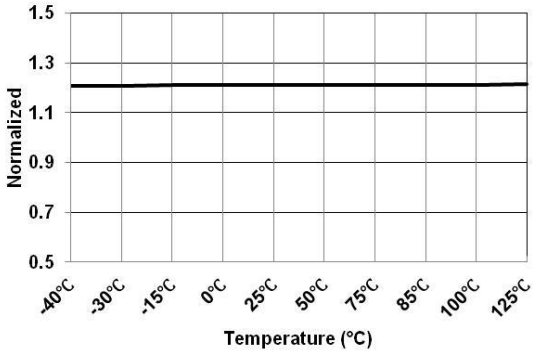


Figure 16. Reference Voltage for CV Regulation at 5.0 V (V_{CVR-5V}) vs. Temperature

Typical Performance Characteristics

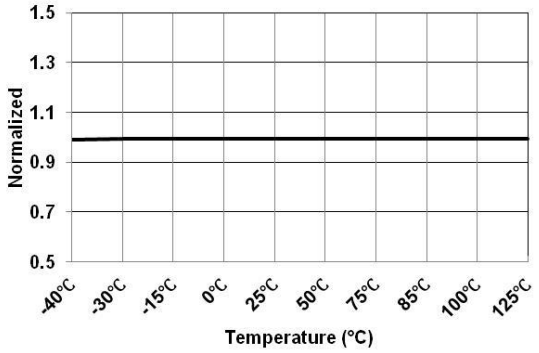


Figure 17.Reference Voltage for CV Regulation at 9 V (V_{CVR-9V}) vs. Temperature

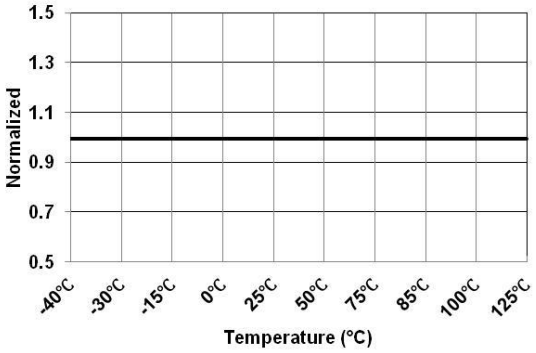


Figure 18. Reference Voltage for CV Regulation at 12 V ($V_{CVR-12V}$) vs. Temperature

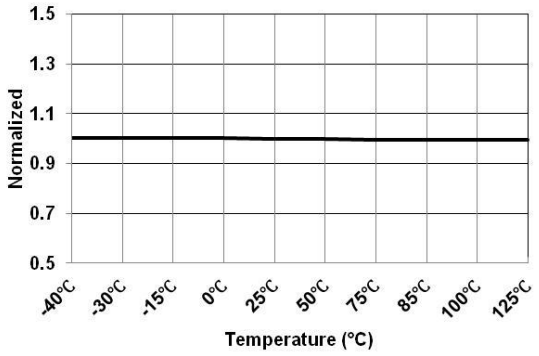


Figure 19. V_{IN} OVP Voltage Under 5 V ($V_{IN-OVP-5V}$) vs. Temperature

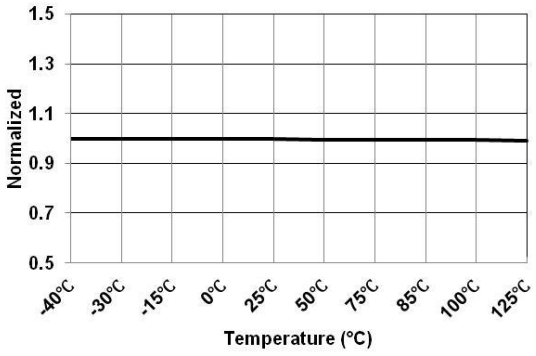


Figure 20. V_{IN} OVP Voltage at 9 V ($V_{IN-OVP-9V}$) vs. Temperature

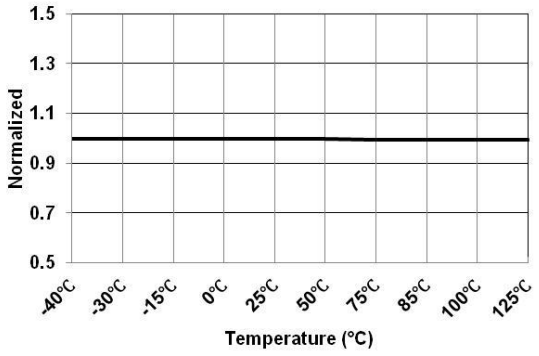


Figure 21. V_{IN} OVP Voltage at 12 V ($V_{IN-OVP-12V}$) vs. Temperature

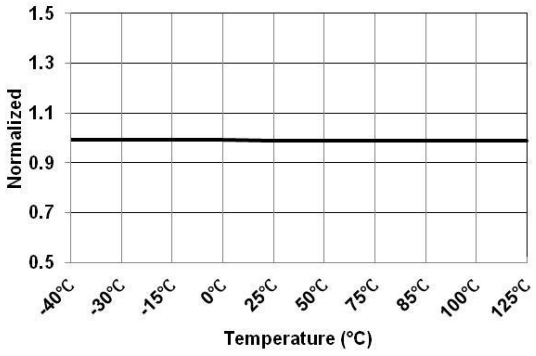


Figure 22. V_{IN} UVP Enable Voltage Under 5 V ($V_{IN-UVP-L-5V}$) vs. Temperature

Typical Performance Characteristics

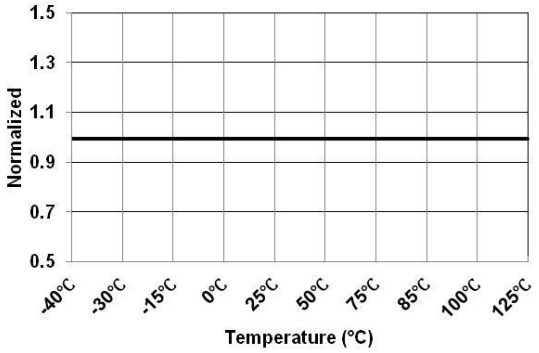


Figure 23. V_{IN} UVP Disable Voltage Under 5 V ($V_{IN-UVP-H-5V}$) vs. Temperature

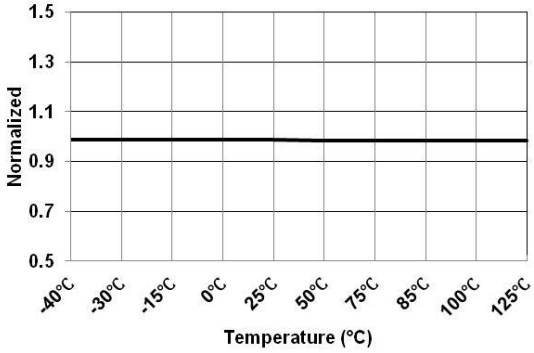


Figure 24. V_{IN} UVP Enable Voltage at 9 V ($V_{IN-UVP-L-9V}$) vs. Temperature

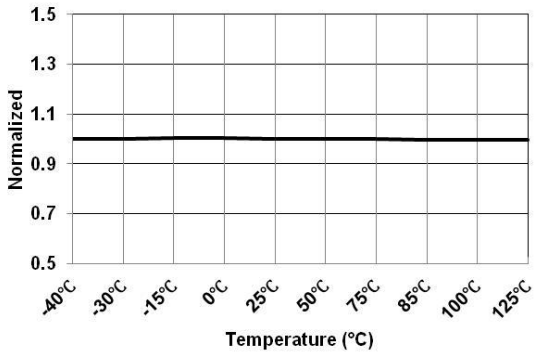


Figure 25. V_{IN} UVP Disable Voltage at 9 V ($V_{IN-UVP-H-9V}$) vs. Temperature

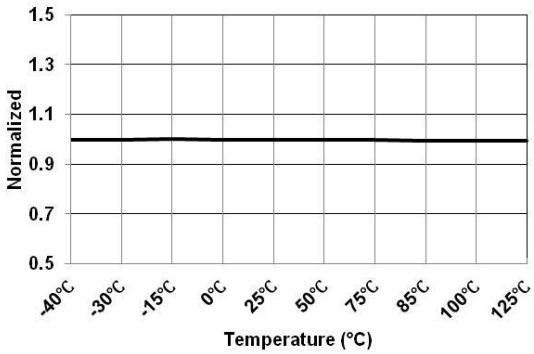


Figure 26. V_{IN} UVP Enable Voltage at 12 V ($V_{IN-UVP-L-12V}$) vs. Temperature

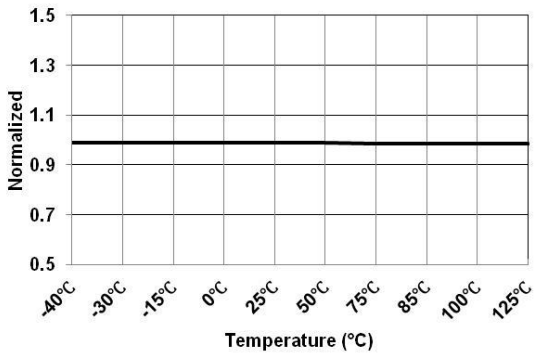


Figure 27. V_{IN} UVP Disable Voltage at 12 V ($V_{IN-UVP-H-12V}$) vs. Temperature

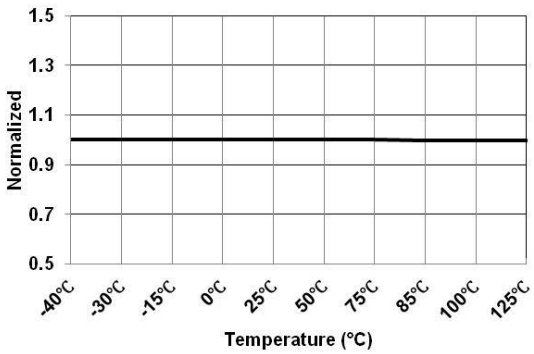


Figure 28. Charge Pump Disable Threshold Voltage (V_{IN-CP}) vs. Temperature

Typical Performance Characteristics

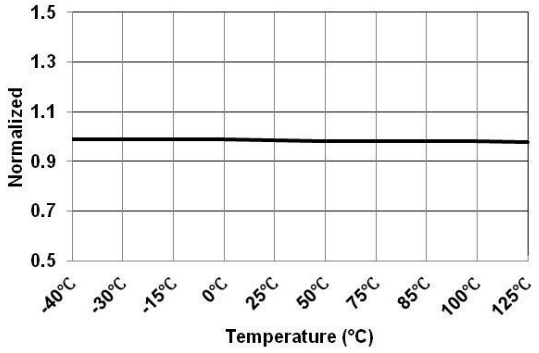


Figure 29.DP Low Level Threshold Voltage (V_{DPL}) vs. Temperature

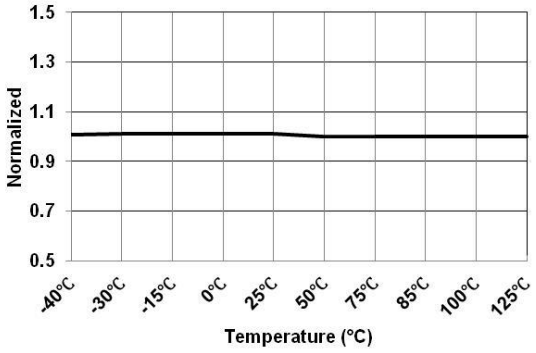


Figure 30.DN Low Level Threshold Voltage (V_{DNL}) vs. Temperature

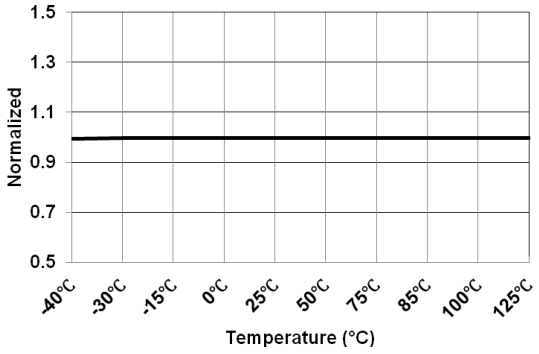


Figure 31.DP High Level Threshold Voltage (V_{DPH}) vs. Temperature

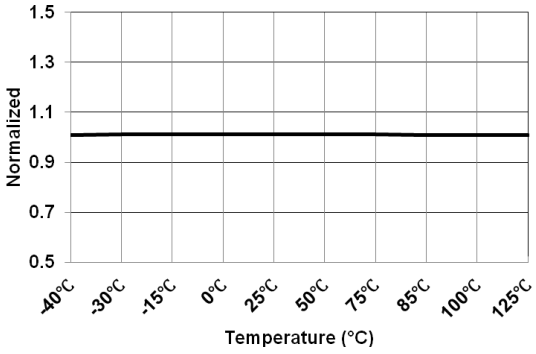


Figure 32. DN High Level Threshold Voltage (V_{DNH}) vs. Temperature

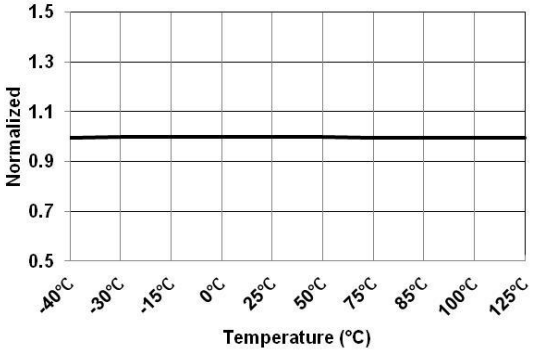


Figure 33.Output Voltage Selection Reference (V_{SEL_REF}) vs. Temperature

Functional Description

The integrated secondary-side power adaptor controller FAN6100Q which is compatible with Qualcomm® Quick Charge™ 2.0 Class A technology for quick charger application. The FAN6100Q enables power supply's output voltage adjustment if it detects a protocol capable mobile and tablet. When a compliant powered is detected, FAN6100Q will produce BC1.2 procedure then will permit receiving output voltage change signal from portable device by DP and DN pin signal. For Qualcomm® Quick Charge™ 2.0 Class A technology application, it can be capable of outputting 5.0 V at the beginning, and then 9 V or 12 V to meet class A requirement of HVDCP power supplies. These voltages are based on the capabilities of the downstream device. The downstream device requests an output voltage for the HVDCP power supply. If a non compliant powered device is detected, the controller disables adaptive output voltage to ensure safe operation with smart phone and tablets that support only 5 V.

The controller consists of two operational amplifiers for Constant Voltage (CV) and Constant Current (CC) regulation with adjustable references voltage. The CC control loop also incorporates a current sense amplifier with gain of 10. Outputs of the CV and CC amplifiers are tied together in open drain configuration. FAN6100Q also incorporates an internal charge pump circuit to maintain CC regulation down to the power supply's output voltage, V_{BUS} of 2 V without an external voltage supply to the IC. Programmable cable voltage drop compensation allows precise CV regulation at the end of USB cable via adjusting one external resistor.

Furthermore, protection functions of the FAN6100Q include adaptive VIN Over-Voltage Protection (VIN OVP) and adaptive VIN Under-Voltage Protection (VIN UVP).

Constant-Voltage Regulation Operation

Figure 34 shows the primary-side internal PWM control circuit of FAN501A and secondary side regulator circuit of FAN6100Q which consists of two operational amplifiers for constant voltage (CV) and constant current (CC) regulation with adjustable voltage references.

The constant voltage (CV) regulation is implemented in the same way as the conventional isolated power supply. The output voltage is sensed on the VREF pin via the resistor divider, R_{F1} and R_{F2} and compared with the internal reference voltage for constant voltage regulation (V_{CVR}) to generate a CV compensation signal (COMV) on the SFB pin. The compensation signal is transferred to the primary-side using an opto-coupler and applied to the PWM comparator through attenuator Av to determine the duty cycle.

The output voltage can be derived by setting R_{F1} and R_{F2}, calculated by:

$$V_O = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \quad (1)$$

Constant-Current Regulation Operation

The constant current (CC) regulation is implemented with sensing the output current. The output current is sensed via current-sense resistor (R_{CS}) connected between the CSP and CSN pins and placed on the output ground return path. The sensed signal is amplified by internal current sensing amplifier $A_{V\text{-}CCR}$ before the amplified current feedback signal is fed into the positive terminal of the internal operational amplifier and compared with the internal reference voltage for constant current regulation (V_{CCR}) to generate a CC compensation signal (COMI) on the SFB pin. The compensation signal is transferred to the primary-side using an opto-coupler to the primary-side PWM controller. The constant current point (I_{O_CC}) can be set by selecting the current sensing resistor as:

$$I_{O\_CC} = \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS}} \quad (2)$$

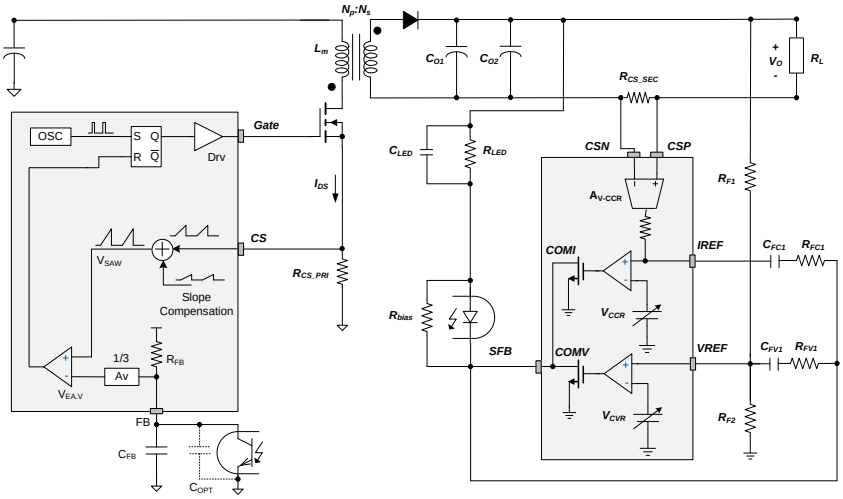


Figure 34. Internal PWM Control Circuit

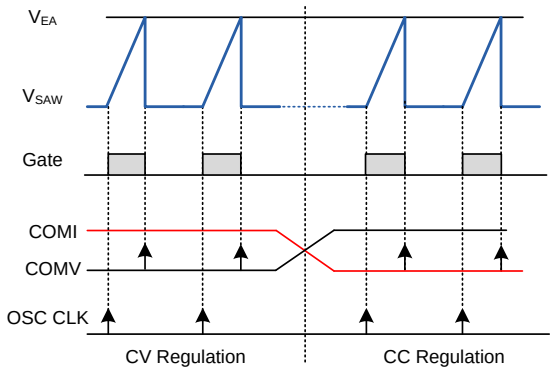


Figure 35. PWM Operation for CV and CC

V_{EA} is compared with an internal sawtooth waveform (V_{SAW}) by PWM comparators to determine the duty cycle. As seen in Figure 34, outputs of comparators is used as a reset signal of flip-flop to determine the MOSFET turn-off instant. The lower signal, either COMV or COMI, is transferred to the primary-side to determine the duty cycle, as shown in Figure 35. During CV regulation, COMV is transferred to the primary-side to determine the duty cycle while COMI is saturated to HIGH. During CC regulation, COMI is transferred to the primary-side to determine the duty cycle while COMV is saturated to HIGH.

Green Mode Operation

FAN6100Q has Green Mode operation with low quiescent current consumption (<850 µA). During the Green Mode, the charge pump function is disabled to reduce power consumption. The FAN6100Q enters green mode when the amplified output current sensed signal is smaller than 0.37 V. If the amplified output current sensed signal increases to larger than 0.495 V, FAN6100Q leaves green mode and the charge pump function is enabled.

Once FAN6100Q enters Green Mode, the operating current is also reduced from 2.4 mA to 850 µA to minimize power consumption. It provides low power consumption by the green mode operation at no load.

Constant Current Mode Selection

FAN6100Q provides flexible output CC choice for a variety of power rating designs. The control signal is a logic level signal for constant current mode determined by QP and QN pins setting. The output constant current mode selection specifications are as follows:

Table 1. Mode Descriptions and Settings

Mode Description	Mode Setting
Variable CC Mode	QP=0 and QN=0
Fixative 1.5 A CC Mode	QP=0 and QN=1
Fixative 2.0 A CC Mode	QP=1 and QN =0

For variable CC mode setting, it is variable output CC for each mode. The QP and QN should be connected to ground as low level signal. The variable output CC for each mode specifications are as follows:

Table 2. Variable CC Mode Specifications

Output Voltage	Rated Current
5 V	2.0 A
9 V	1.67 A
12 V	1.25 A

For fixative 1.5 A CC Mode setting, it is fixative CC output 1.5 A except for 12 V mode. The QP should be connected to ground as a low-level signal and QN can be open to generate a high-level signal. The specifications are as follows:

Table 3. Fixative 1.5A CC Mode Specifications

Output Voltage	Rated Current
5 V	1.5 A
9 V	
12 V	1.1 A

For fixative 2.0 A CC Mode setting, it is fixative CC output 2.0 A except for 12 V mode. The specifications are as follows:

Table 4. Fixative 2.0A CC Mode Specifications

Output Voltage	Rated Current
5 V	2.0 A
9 V	
12 V	1.56 A

Once protection mode has occurred, the output current is adjusted and modified by $A_{V\text{-}CCR\text{-}Protection}$. The output current can be calculated as:

$$I_{O\_CC\_protection} \le \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR-FIX-1.5A}}{R_{CS}} \cdot A_{V-CCR-protection} \quad (3)$$

Cable Voltage Drop Compensation

FAN6100Q incorporates programmable cable voltage drop compensation function via adjusting one external resistor to maintain constant voltage regulation at end of the USB cable.

Figure 36 shows the internal block of the cable voltage drop compensation function. Output current information is obtained from the amplified current sensing voltage. Depending on the weighting of the external resistor, the current signal is modulated to offset the CV loop reference voltage, V_{CVR}. Thus, output voltage is increased by this offset voltage on the CV loop reference to compensate for cable voltage drop.

The external compensation resistor, RCOMR, can be calculated by:

$$R_{COMR} = \frac{R_{F2}}{R_{F1} + R_{F2}} \cdot \frac{R_{Cable}}{R_{CS}} \cdot \frac{1}{A_{V-CCR}} \cdot \frac{1}{K_{COMR-CDC}} \quad (4)$$

where:

R_{F1} and R_{F2} = output feedback resistor divider derived from Eq. (1);

R_{Cable} = cable resistance;

R_{CS} = current sensing resistor derived from Eq. (2);

$K_{COMR-CDC}$ = cable compensation design parameter of the controller, which is 1.0 µA/V; and

A_{V-CCR} = derived from Eq. (2), 10 V/V.

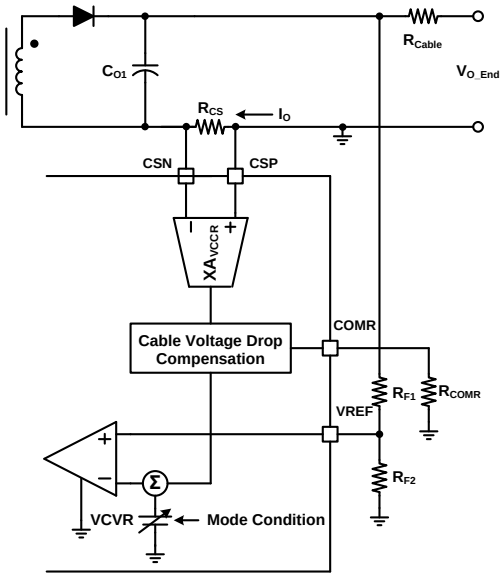


Figure 36. Cable Voltage Drop Compensation Block

Supply Voltage and Charge Pump Operation

Figure 37 shows the supply voltage circuit, including V_{DD} and the charge-pump circuit. FAN6100Q can withstand up to 20 V on the VIN pin and enable this pin to be connected directly to the output terminal of a power supply. It is typical to use about 100 Ω resistor between the VIN pin and the output terminal of a power supply and then connect 470 nF capacitor on the VIN pin if ESD immunity needs to be enhanced.

During startup, the charge-pump circuit is enabled when V_{IN} voltage is larger than 2 V and disabled after 40 ms from the V_{DD} voltage reaches V_{DD-ON} (3.65 V). The charge-pump circuit is used to boost the V_{DD} voltage to maintain normal operation for the controller when output voltage is low. The charge-pump stage includes a Low Dropout (LDO) pre-regulator and a charge-pump circuit. The LDO pre-regulator regulates the V_{CLAMP} voltage to 2.7 V and then boosts up the V_{DD} voltage when V_{IN} is lower than V_{IN-CP} (6.4 V) and out of Green Mode. When V_{IN} is greater than the value 6.2 V which subtract V_{IN-CP} from $V_{IN-CP-Hys}$ or lower than V_{IN-CP} (6.4 V) in Green Mode, the charge-pump circuit is disabled and the V_{IN} voltage is fed directly to V_{DD}.

The charge-pump circuit needs an external capacitor, CCP, typically 220 nF~1 µF, as the energy storage element. To stabilize the operation of the clamping LDO stage, it is typical to use 1 µF capacitor to keep the LDO loop stable.

When charge-pump circuit is disabled, the output capacitor supplies charging current to charge the hold-up capacitor C_{VDD}. The V_{DD} voltage is clamped at 5.4 V by internal Zener diode when the charge-pump circuit is disabled. The C_{VDD} typically 220 nF~1 µF, as the energy storage element.

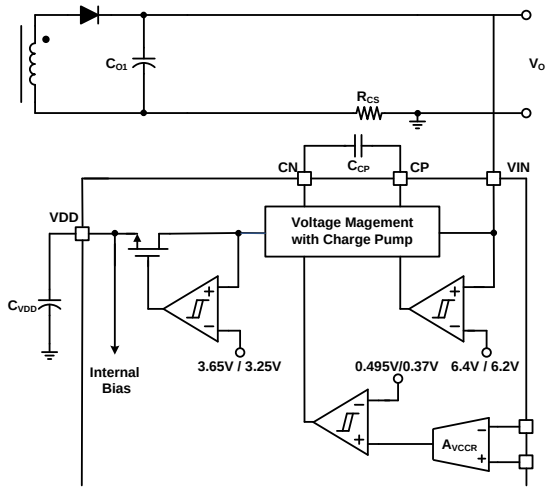


Figure 37. Supply Voltage Block

Output Bleeder Section

For HVDCP power supply application, a discharge path on the output of the HVDCP power supply is necessary to ensure that a high output voltage level can transfer to a low output voltage level quickly during mode changes. This is especially critical under no-load condition where the natural decay rate of the output voltage is low. To enable output bleeder function when the mode changes from high output voltage to low output voltage can ensure short voltage transition time.

Figure 38 shows the internal block of bleeder function. The FAN6100Q implements the output bleeder function to discharge the output voltage rapidly during mode changes. The BLD pin is connected to the output

voltage terminal as the discharging path. When the high-output voltage to low-output voltage mode change signal is initiated, an internal switch is turned on to discharge the output voltage. The switch stays on until $t_{BLD-MAX}$ is reached. The BLD pin can withstand up to 20 V and enable this pin to be connected directly to the output terminal of a HVDCP power supply, but the output voltage shall be not lower than 4.1 V at output voltage transition and short transition time consideration, it recommends adding 2-step bleeder circuit, which is one 5.1 V Zener diode and one resistance (RBLD), to avoid output voltage drop deeply.

The first step bleeder current is determined by internal constant current design, the type value is 240 mA. The second step Bleeder Discharging Current (IBLD) can be adjusted by external Bleeder Series Resistor (RBLD), it can be calculated as:

$$I_{BLD} = \frac{V_O}{R_{BLD}} \quad (5)$$

where RBLD is bleeder resistor connected between the output side and the BLD pin.

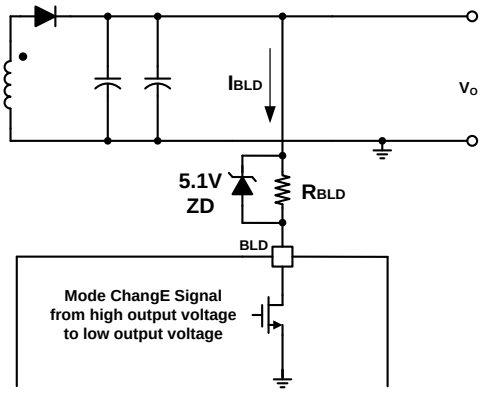


Figure 38. Output Bleeder Function

V_{IN} Over-Voltage-Protection (OVP)

Figure 39 shows the V_{IN} OVP block, which is adaptive operated according to mode condition. Output voltage is sensed through VIN pin for OVP detection. Once output voltage rises to V_{IN-OVP} by each mode and then V_{IN} OVP is triggered, where V_{IN} OVP occurs, the OVP pin is pulled down to ground through an internal switch until V_{DD-OFF} (3.25 V) is reached.

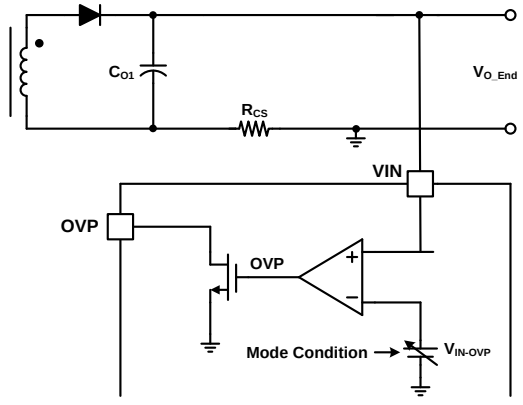


Figure 39. V_{IN} Over-Voltage-Protection Block

V_{IN} Under-Voltage-Protection

Figure 40 shows the V_{IN} under-voltage-protection ($V_{IN\ UVP}$) block. The output current is reduced to protect the system at 5 V, 9 V and 12 V conditions when V_{IN} UVP function is triggered. Once output voltage drops below $V_{IN-UVP-L}$, the CC reference voltage VCCR is adjusted and modified by $A_{V-CCR-UVP}$. The output current can be calculated as:

$$I_{O\_CC} \le \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS}} \cdot A_{V-CCR-UVP} \quad (6)$$

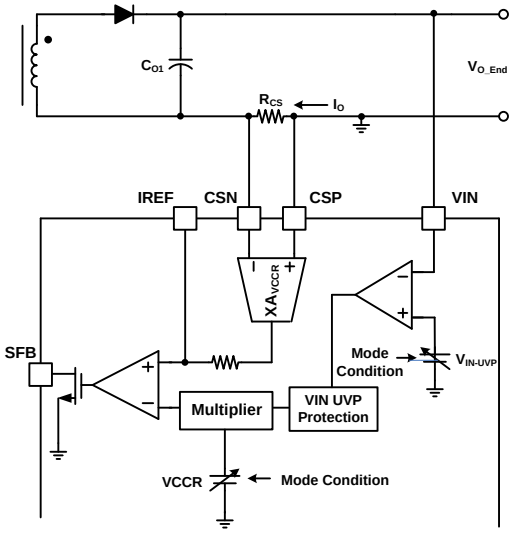


Figure 40. V_{IN} Under-Voltage Protection Block

Protocol Communication

FAN6100Q is compatible with Qualcom® Quick Charge™ 2.0 Class A technology which is capable of outputting 5 V at the beginning, and then 9 V or 12 V. FAN6100Q can compatible with USB BC1.2 specification and permit receiving output voltage change signal form portable device by DP and DN pin signal.

If portable device has detected as a HVDCP, FAN6100Q will allow to progress USB BC1.2 procedure. After complete BC1.2 procedure, the output voltage is determined by both DP & DN voltage. The voltage on DP & DN is show in Table 5. The detection voltage specifications are as follows:

Table 5. DP & DN Voltage

Detection Voltage		HVDCP Power Supply
DP	DN	Output Voltage
0.6 V	0.6 V	12 V
3.3 V	0.6 V	9 V
0.6 V	3.3 V	Reserved
3.3 V	3.3 V	Reserved
0.6 V	GND	5 V

FAN6100Q complies with Qualcomm QC2.0 UL compliance guidance and meets all specification.

Typical Application Circuit

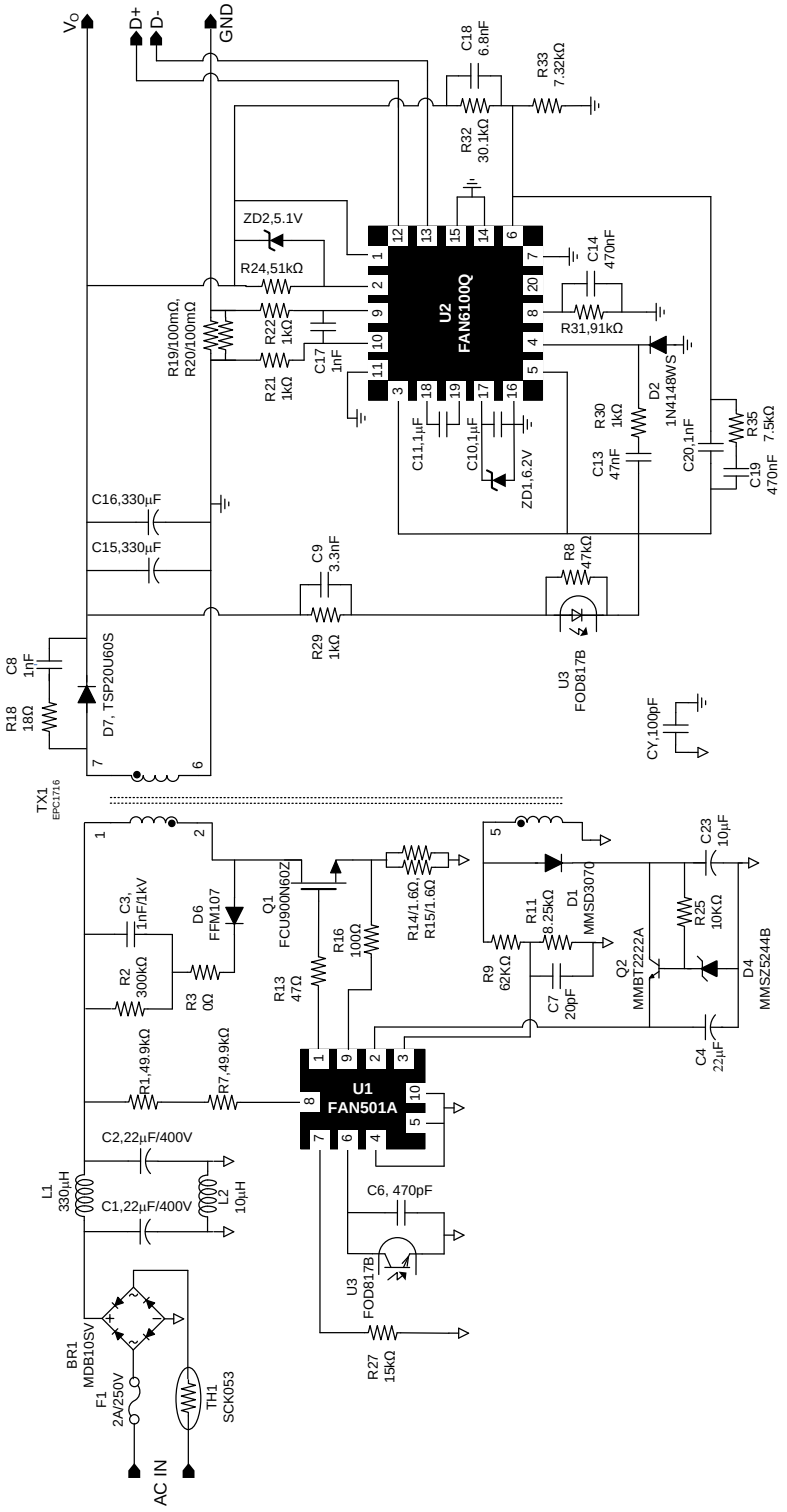


Figure 41. Schematic of Typical Application Circuit

Transformer Specification

Core: EPC-1716

Bobbin: EPC-1716

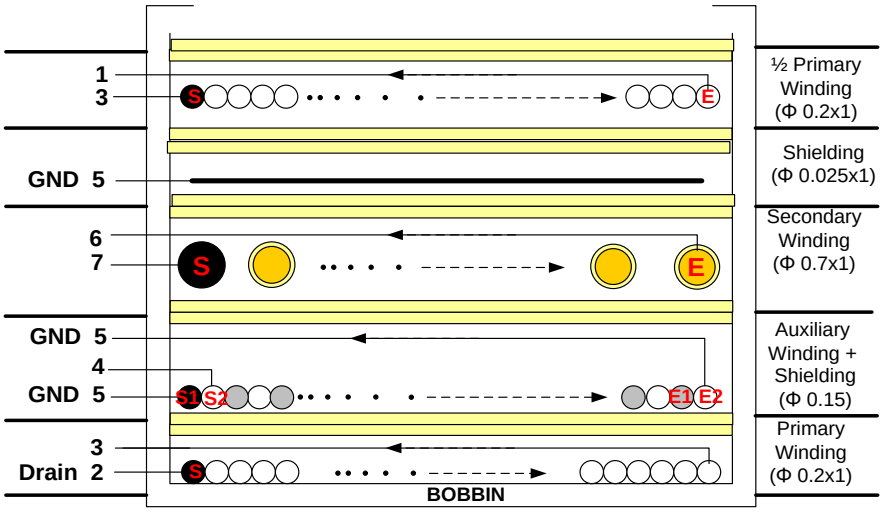
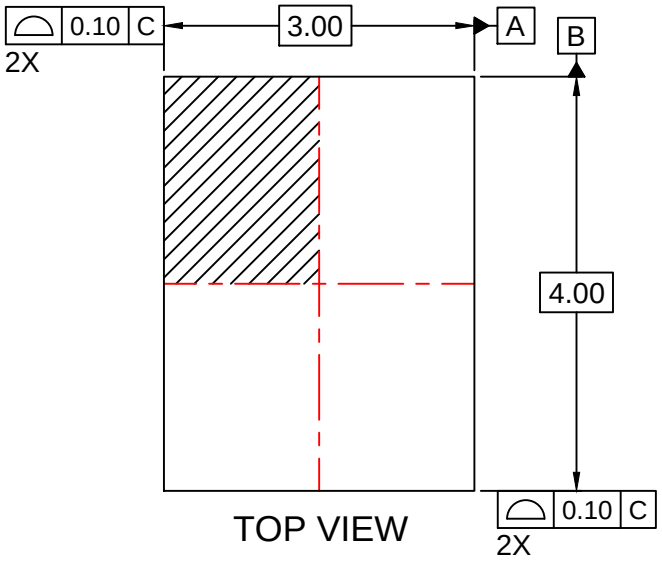


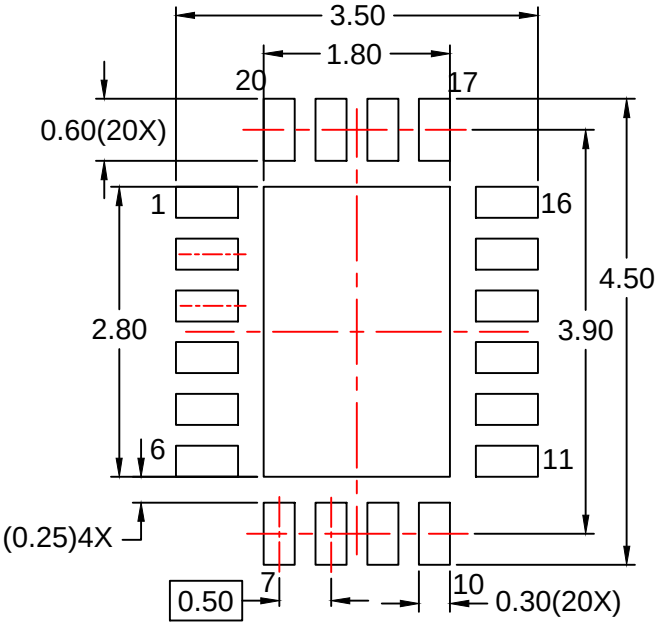
Figure 42. Transformer Diagram

Winding	Terminal		Wire	Turns	Isolation Layer
	Start Pin	End Pin			Turns
NP-2	3	1	0.2 mm×1	26	2
Copper Shielding	5	Open	Copper Foil 0.025 mm	1	2
Ns	7	6	0.7 mm×1	6	2
Na	4	5	0.15 mm×1	11	2
Na-Shield	5	Open	0.15 mm×1	11	2
NP-1	2	3	0.2 mm×1	34	2
Bobbin – EPC1716					

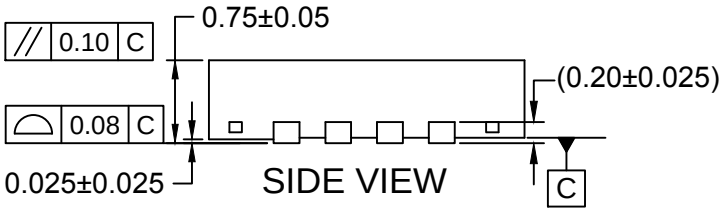
Inductance	1-2	600 µH± 5%	100 kHz
Effective Leakage	1-2	<30 µH Maximum	Short Other Pin



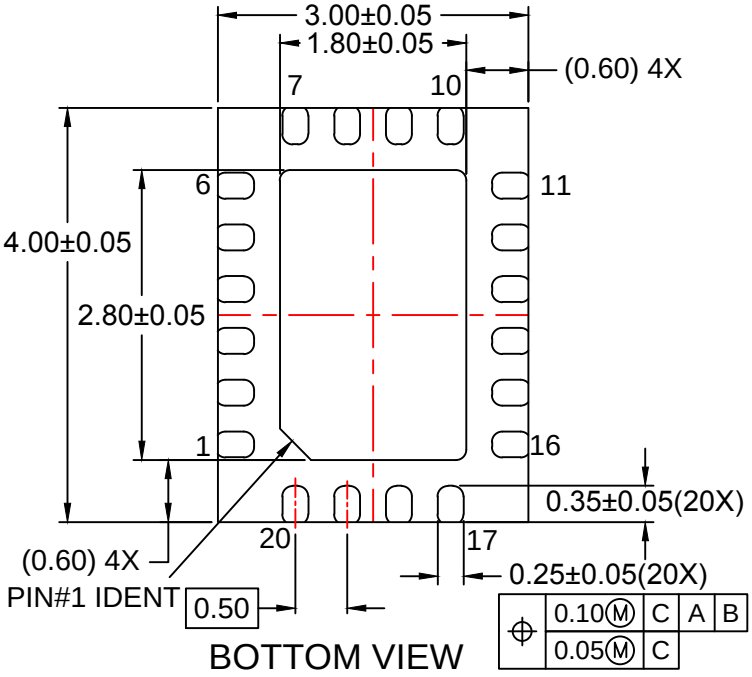
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. DOES NOT FULLY CONFORMS TO JEDEC REGISTRATION MO-220.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-MLP20Drev2.
F. FAIRCHILD SEMICONDUCTOR.

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FastvCore™
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FPS™
F-PFS™
FRFET®
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Definition of Terms

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Rev. I77