MC642

PWM Fan Speed Controller with Fault Detection

The MC642 is a pulse width modulation (PWM) fan speed controller for use with DC motors. It provides temperature proportional speed control. A thermistor connected to the V_{IN} input furnishes the required control voltage of 1.25 V to 2.65 V for 0% to 100% PWM duty cycle. Minimum fan speed is set by a simple resistor divider on the V_{MIN} input. An integrated Start–Up Timer ensures reliable motor start–up at turn–on, coming out of Shutdown Mode, or following a transient fault. A stalled, open, or unconnected fan causes the MC642 to trigger its start–up timer *once*. If the fault persists, the $\overline{\text{FAULT}}$ output goes low, and the device is latched in Shutdown Mode.

Features

- Shutdown Mode for Power Saving
- Supports Low Cost NTC/PTC Thermistors
- Temperature Proportional Speed for Acoustic Control/ Longer Fan Life
- Fan Voltage Independent of MC642 Supply Voltage
- Fault Detection Circuits Protect Against Fan Failure and Aid System Testing
- Operating Temperature Range: 0°C to +85°C

Typical Applications

- Power Supplies
- Personal Computers
- UPS's, Power Amplifiers, etc.

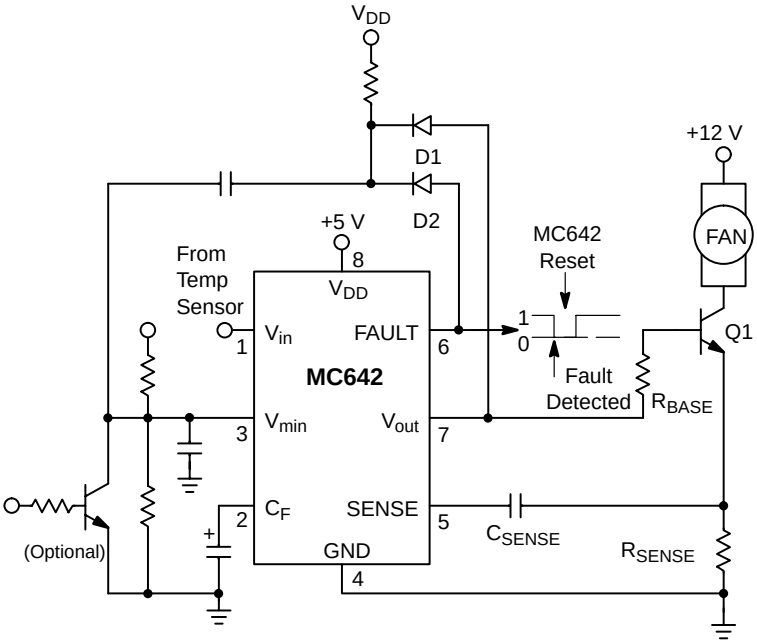

Figure 1. Typical Application Diagram

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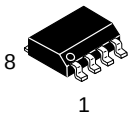
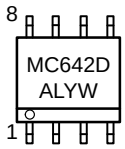
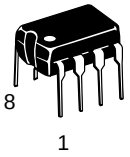
MARKING DIAGRAMS

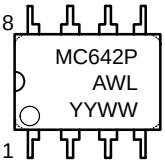


SO–8
D SUFFIX
CASE 751



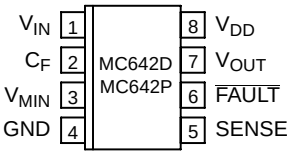


PDIP–8
P SUFFIX
CASE 626



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONFIGURATION



ORDERING INFORMATION

Device	Package	Shipping
MC642DR2	SO–8	2500 Tape/Reel
MC642P	PDIP–8	50 Units/Rail

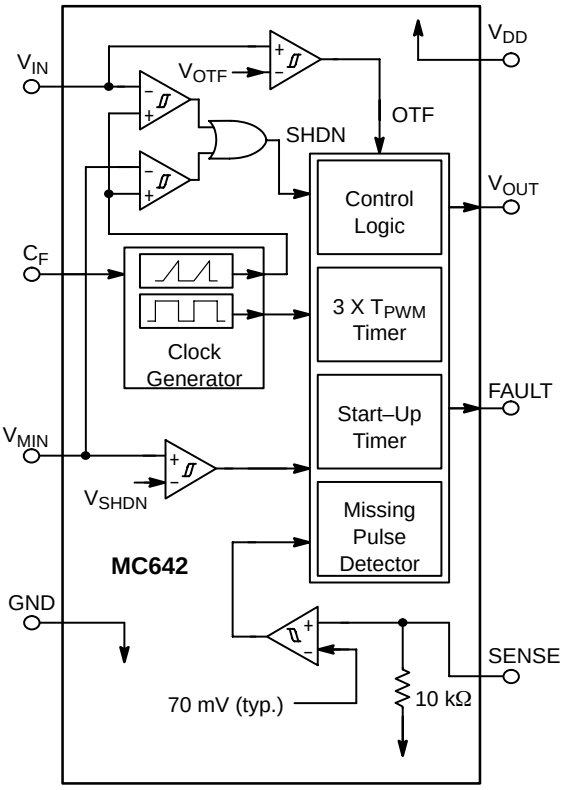


Figure 2. Functional Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{IN}	The thermistor network (or other temperature sensor) connects to this input. A voltage range of 1.25 V to 2.65 V (typical) on this pin drives an active duty cycle of 0% to 100% on the V_{OUT} pin.
2	C_F	Positive terminal for the PWM ramp generator timing capacitor. The recommended C_F is 1 μF for 30 Hz PWM operation.
3	V_{MIN}	An external resistor divider connected to this input sets the minimum fan speed by fixing the minimum PWM duty cycle (1.25 V to 2.65 V = 0% to 100%, typical). The MC642 enters Shutdown mode when $0 \le V_{MIN} \le V_{SHDN}$. During Shutdown, the FAULT output is inactive, and supply current falls to 25 μA (typical). The MC642 exits Shutdown mode when $V_{MIN} \ge V_{REL}$. See *Applications* section for more details.
4	GND	Ground Terminal
5	SENSE	Pulses are detected at this pin as fan rotation chops the current through a sense resistor. The absence of pulses indicates a fault.
6	$\overline{\text{FAULT}}$	Fault (open collector) output. This line goes low to indicate a fault condition. When $\overline{\text{FAULT}}$ goes low due to a fan fault, the device is latched in Shutdown Mode until deliberately cleared or until power is cycled. $\overline{\text{FAULT}}$ may be connected to V_{MIN} if a hard shutdown is desired. $\overline{\text{FAULT}}$ will also be asserted when the PWM reaches 100% duty cycle, however the device will not latch itself off unless $\overline{\text{FAULT}}$ is tied to V_{MIN} externally.
7	V_{OUT}	PWM signal output. This active high complimentary output connects to the base of an external NPN motor drive transistor. This output has asymmetrical drive. – See *Electrical Characteristics* section.
8	V_{DD}	Power Supply Input. May be independent of fan power supply. See *Electrical Characteristics* section.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Value	Unit
Package Power Dissipation ($T_A \le 70°C$) Plastic DIP Small Outline (SOIC)	 730 470	mW
Derating Factors	8.0	mW/°C
Supply Voltage	6.0	V
Input Voltage, Any Pin	(GND – 0.3) to (V_{CC} + 0.3)	V
Operating Temperature Range	0 to +85	°C
Maximum Chip Temperature	150	°C
Storage Temperature Range	–65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	+300	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

ELECTRICAL CHARACTERISTICS ($T_{MIN} < T_A < T_{MAX}$, V_{DD} = 3.0 V to 5.5 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	–	5.5	V
Supply Current, Operating Pins 3, 5, 7 Open, C_F = 1 μF, $V_{IN} = V_{(CMAX)}$	I_{DD}	–	0.5	1.0	mA
Supply Current, Shutdown Mode Pins 1, 5, 6, 7 Open, C_F = 1 μF, V_{IN} = 0.35 V (Note 1.)	$I_{DD(SHDN)}$	–	25	–	μA
V_{IN}, V_{MIN} Input Leakage (Note 1.)	I_{IN}	–1.0	–	1.0	μA
V_{OUT} Output					
V_{OUT} Rise Time (I_{OH} = 5.0 mA) (Note 1.)	t_R	–	–	50	μsec
V_{OUT} Fall Time (I_{OH} = 1.0 mA) (Note 1.)	t_F	–	–	50	μsec
Pulse Width (On V_{MIN}) to Clear Fault Mode V_{SHDN}, V_{HYST} Specifications	$t_{(SHDN)}$	30	–	–	μsec
Sink Current at V_{OUT} Output V_{OL} = 10% of V_{DD}	I_{OL}	1.0	–	–	mA
Source Current at V_{OUT} Output V_{OH} = 80% of V_{DD}	I_{OH}	5.0	–	–	mA
V_{IN}, V_{MIN}, Inputs					
Input Voltage at V_{IN} or V_{MIN} for 100% PWM Duty Cycle	$V_{C(MAX)}$, V_{OTF}	2.5	2.65	2.8	V
$V_{C(MAX)} - V_{C(MIN)}$	$V_{C(SPAN)}$	1.3	1.4	1.5	V
Voltage Applied to V_{MIN} to Guarantee Shutdown Mode	V_{SHDN}	–	–	V_{DD} x 0.13	V
Voltage Applied to V_{MIN} to Release Shutdown Mode V_{DD} = 5 V	V_{REL}	V_{DD} x 0.19	–	–	V
Pulse–Width Modulator					
PWM Frequency (C_F = 1.0 μF)	F	26	30	34	Hz
Sense Input					
SENSE Input Threshold Voltage with Respect to GND	$V_{TH(SENSE)}$	50	70	90	mV
Fault Output					
Output Low Voltage (I_{OH} = 2.5 mA)	VOL	–	–	0.3	V
Missing Pulse Detector Timeout	tMP	–	32/F	–	Sec
Startup Time	tSTARTUP	–	32/F	–	Sec
Diagnostic Timer Period	tDIAG	–	3/F	–	Sec

1. Guaranteed by design, not tested.

DETAILED OPERATING DESCRIPTION

PWM

The PWM (Pulse Width Modulation) circuit consists of a ramp generator and threshold detector. The frequency of the PWM is determined by the value of the capacitor connected to the C_F input. A frequency of 30 Hz is recommended (C_F = 1 μF). The PWM is also the timebase for the startup and fault timer (see below). The PWM voltage control range is 1.25 V to 2.65 V (typical) for 0% to 100% output duty cycle.

V_{OUT} Output

The V_{OUT} pin is designed to drive a low–cost transistor or MOSFET as the low side power switching element in the system. Various examples of driver circuits are shown in the following pages. This output has asymmetric complementary drive and is optimized for driving NPN transistors or N–channel MOSFET's. Since the system relies on PWM rather than linear power control, the dissipation in the power switch is kept to a minimum. Generally, very small devices (TO–92 or SOT package) will suffice. (See Output Drive Transistor Selection paragraph in Applications Information section.)

Start–Up Timer

To ensure reliable fan startup, the StartUp Timer turns the V_{OUT} output on for 32 cycles of the PWM whenever the fan is started from the off–state. This occurs at power–up and when coming out of shutdown mode. If the PWM frequency is 30Hz (C_F = 1 μF), the resulting start–up time will be about one second. If a Fault is detected (see below), the Diagnostic Timer is triggered once, followed by the Startup–Up Timer. If the fault persists, the device is shut down. See *FAULT Output* below.

Shutdown Control (Optional)

When V_{MIN} (pin 3) is pulled below V_{SHDN}, the MC642 will go into Shutdown mode. This can be accomplished by driving V_{MIN} with an open drain logic signal or using an external transistor as shown in Figure 3. All functions are suspended until the voltage on V_{MIN} becomes higher than V_{REL} (0.85 V @ V_{DD} = 5.0 V). Pulling V_{MIN} below V_{SHDN} will always result in complete device shutdown and reset. The $\overline{\text{FAULT}}$ output is unconditionally inactive in Shutdown mode.

A small amount of hysteresis, typically one percent of V_{DD} (50 mV at V_{DD} = 5.0 V), is designed into the V_{SHDN}/V_{REL} threshold. The levels specified for V_{SHDN} and V_{REL} in the *Electrical Characteristics* section include this hysteresis plus adequate margin to account for normal variations in the absolute value of the threshold and hysteresis.

CAUTION: Shutdown mode is unconditional. i.e., the fan will not activate regardless of the voltage on V_{IN}. (Note: The fan should not be shut down until all heat–producing activity in the system is at a negligible level.)

SENSE Input

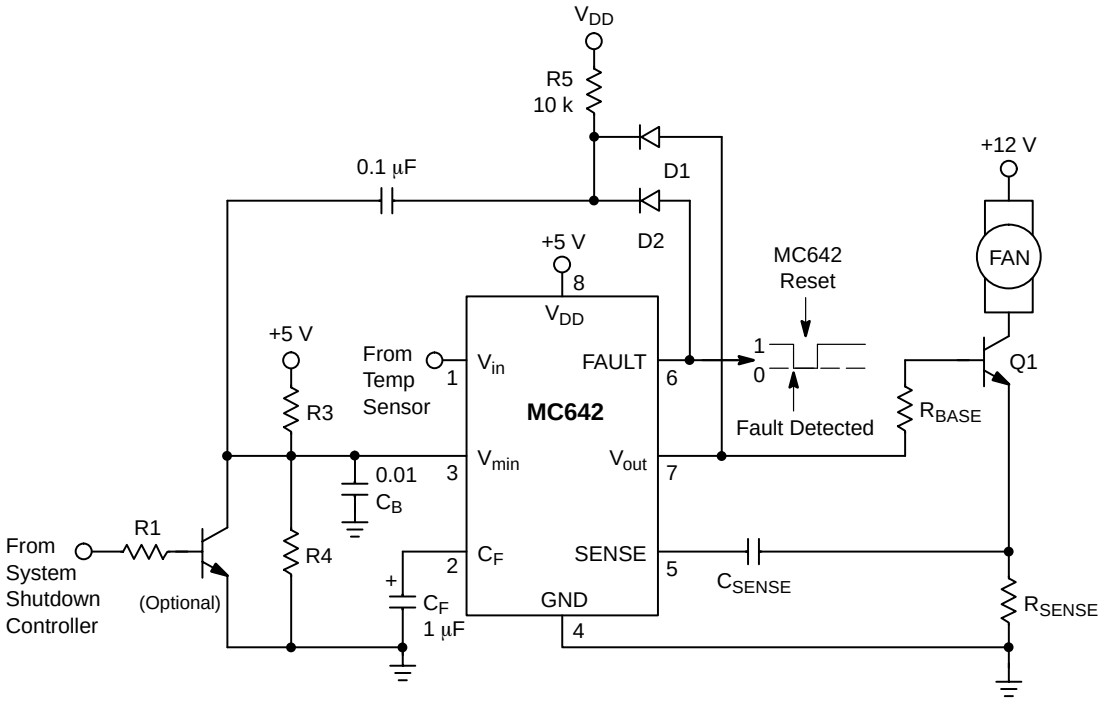
The SENSE input, pin 5, is connected to a low–value current sensing resistor in the ground return leg of the fan circuit. During normal fan operation commutation occurs as each pole of the fan is energized. This commutation causes brief interruptions in the fan current, which is seen as pulses across the sense resistor. When the device is not in Shutdown Mode and pulses are not appearing at the SENSE input, a fault condition exists.

The short, rapid changes in fan current (high dI/dt) cause corresponding dV/dt pulses across the sense resistor, R_{SENSE}. The waveform on R_{SENSE} is differentiated and converted to a logic–level pulse–train by C_{SENSE} and the internal signal processing circuitry (See Figure 3). The presence and frequency of this pulse–train is a direct indication of fan operation. See the *Applications Information* section for more details.

$\overline{\text{FAULT}}$ Output

The MC642 detects faults in two ways:
(1) Pulses appearing at SENSE due to the PWM turning on are blanked and the remaining pulses are filtered by a missing pulse detector. If consecutive pulses are not detected for 32 PWM cycles (1 Sec if C_F = 1 μF), the Diagnostic Timer is activated and V_{OUT} is driven continuously for three PWM cycles (100 msec if C_F = 1 μF). If a pulse is not detected within this window, the Startup–Timer is triggered. This should clear a transient fault condition. If the Missing Pulse Detector times out again, the PWM is stopped and $\overline{\text{FAULT}}$ goes low. When $\overline{\text{FAULT}}$ is activated due to this condition, the device is latched in Shutdown mode and will remain off indefinitely. (Diodes D_1, D_2 and resistor R5 (See Figure 3) are provided to ensure that fan restarting is the result of a fan fault, and not an over–temperature fault. A CMOS logic OR gate may be substituted for these components if available).

When $\overline{\text{FAULT}}$ is activated due to this condition, the device is latched in Shutdown mode and will remain off indefinitely. **Important: At this point, action *must* be taken to restart the fan by momentarily pulling V_{MIN} below V_{SHDN}, or by cycling system power. In either case the fan *cannot* be permitted to remain disabled due to a fault condition, as severe system damage could result. If the fan cannot be restarted, the system should be shut down.** The MC642 may be configured to continuously attempt fan restarts if so desired.



* The parallel combination of R3 and R4 must be > 10 k.

Figure 3. Typical Fan Control Application

Continuous restart mode is enabled by connecting the $\overline{\text{FAULT}}$ output to V_{MIN} through a 0.1 μF capacitor as shown in Figure 3. When so connected, the MC642 automatically attempts to restart the fan whenever a fault condition occurs. When the fault output is driven low, the V_{MIN} input is momentarily pulled below V_{SHDN}, initiating a reset and clearing the fault condition. Normal fan startup is then attempted as previously described. The $\overline{\text{FAULT}}$ output may be connected to external logic (or the interrupt input of a microcontroller) to shut down the MC642 if multiple fault pulses are detected at approximately one second intervals.

(2) $\overline{\text{FAULT}}$ is also asserted when the PWM control voltage applied to V_{IN} becomes greater than that needed to drive 100% duty cycle (see *Electrical Characteristics*). This indicates that the fan is at maximum drive and the potential exists for system overheating. Either heat dissipation in the system has gone beyond the cooling system's design limits or some other fault exists such as fan bearing failure or an airflow obstruction. This output may be treated as a System Overheat warning and used to trigger system shutdown. However in this case, the fan will continue to run even when $\overline{\text{FAULT}}$ is asserted. If a shutdown is desired, $\overline{\text{FAULT}}$ may be connected to V_{MIN} outside the device. This will latch the MC642 in Shutdown Mode when any fault occurs.

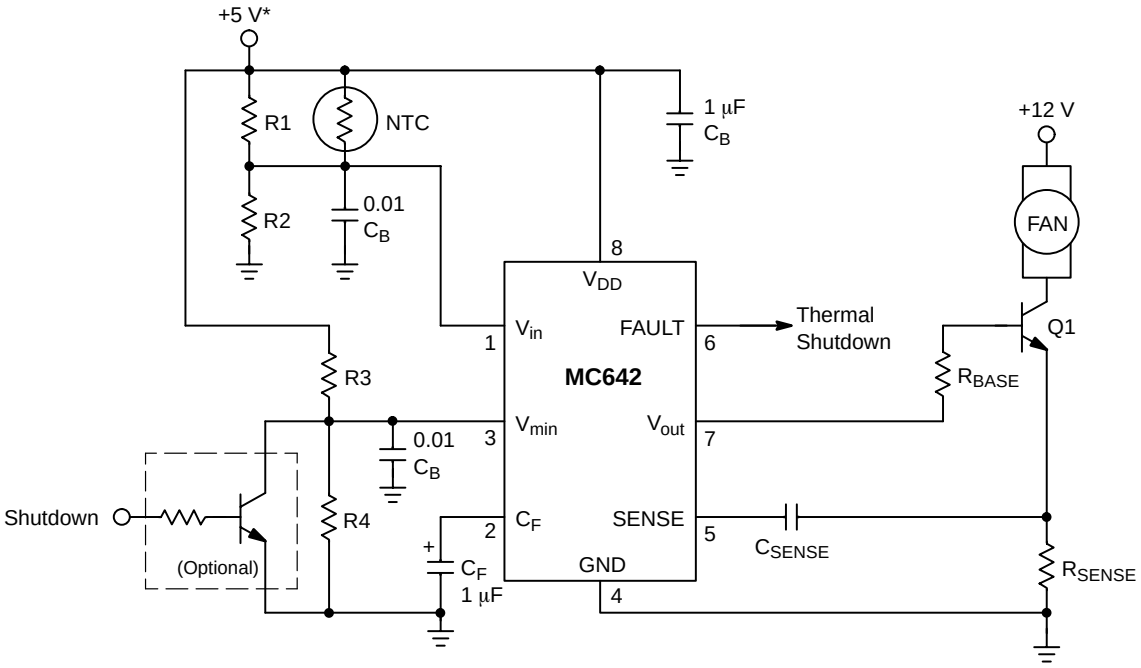
SYSTEM BEHAVIOR

The flowcharts describing the MC642's behavioral algorithm are shown in Figure 5. They can be summarized as follows:

Power–Up

1. Assuming the device is not being held in Shutdown mode ($V_{MIN} > V_{REL}$):
2. Turn V_{OUT} output on for 32 cycles of the PWM clock. This ensures that the fan will start from a dead stop.
3. During this Start–up time, if a fan pulse is detected then branch to Normal Operation; if none are received.
4. Activate the 32–cycle Start–up Timer one more time and look for fan pulses; if a fan pulse is detected, proceed to Normal Operation; if none are received....
5. Proceed to Fan Fault
6. End

After this period elapses, the MC642 begins normal operation.



NOTE: *See Cautions Regarding Latch–Up Considerations in the Applications Section.

Figure 4. Typical Fan Control Application Using NTC Thermistor

Normal Operation

Normal Operation is an endless loop which may only be exited by entering Shutdown mode or Fan Fault. The loop can be thought of as executing at the frequency of the oscillator and PWM.

1. Reset the Missing Pulse Detector
2. Is MC642 in Shutdown? If so...
   a. V_{OUT} duty–cycle goes to zero.
   b. FAULT is disabled.
   c. Exit the loop and wait for $V_{MIN} > V_{REL}$ to resume operation (indistinguishable from Power–Up).
3. If an over–temperature fault occurs ($V_{IN} > V_{OTF}$) then activate $\overline{\text{FAULT}}$; release $\overline{\text{FAULT}}$ when $V_{IN} < V_{OTF}$.
4. Drive V_{OUT} to a duty–cycle proportional to greater of V_{IN} and V_{MIN} on a cycle by cycle basis.
5. If a fan pulse is detected, branch back to the start of the loop.
6. If the missing pulse detector times out ...
7. Activate the 3–cycle Diagnostic Timer and look for pulses; if a fan pulse is detected, branch back to the start of the loop; if none are received...
8. Activate the 32–cycle Startup Timer and look for pulses; if a fan pulse is detected, branch back to the start of the loop; if none are received...
9. Quit Normal Operation and go to Fan Fault.
10. End

Fan Fault

Fan Fault is essentially an infinite loop wherein the MC642 is latched in Shutdown Mode. This mode can only be released by a Reset, i.e., V_{MIN} being brought below V_{SDHN}, then above V_{REL}, or by power–cycling.

1. While in this state, $\overline{\text{FAULT}}$ is latched on (low), and the V_{OUT} output is disabled.
2. A Reset sequence applied to the V_{MIN} pin will exit the loop to Power Up.
3. End

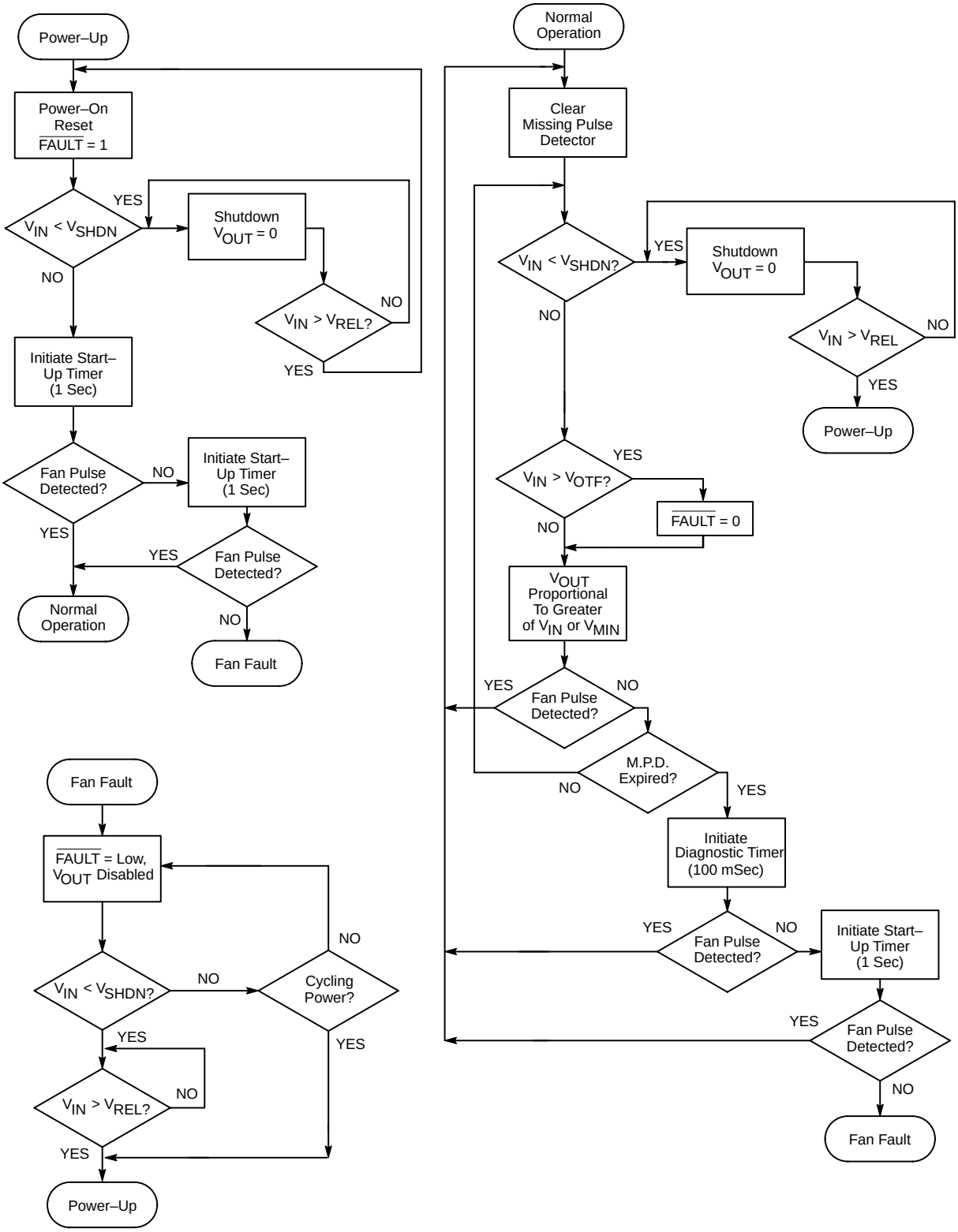


Figure 5. MC642 Behavioral Algorithm Flowchart

APPLICATIONS INFORMATION

Designing with the MC642 involves the following:

1. The temp sensor network must be configured to deliver 1.25 V to 2.65 V on V_{IN} for 0% to 100% of the temperature range to be regulated.
2. The minimum fan speed (V_{MIN}) must be set.
3. The output drive transistor and associated circuitry must be selected.
4. The Sense Network, R_{SENSE} and C_{SENSE}, must be designed for maximum efficiency while delivering adequate signal amplitude.
5. If Shutdown capability is desired, the drive requirements of the external signal or circuit must be considered.

Temperature Sensor Design

The temperature signal connected to V_{IN} must output a voltage in the range of 1.25 V to 2.65 V (typical) for 0% to 100% of the temperature range of interest. The circuit of Figure 6 is a convenient way to provide this signal.

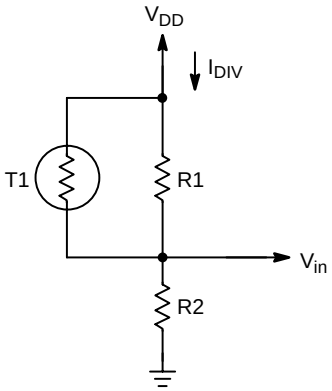


Figure 6. Temperature Sensing Circuit

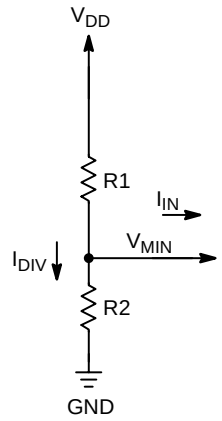


Figure 7. V_{MIN} Circuit

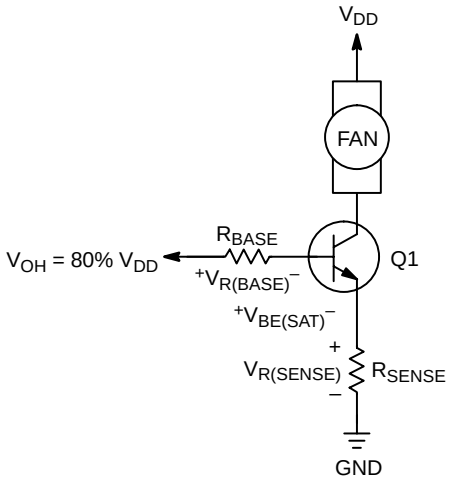


Figure 8. Circuit for Determining R_{BASE}

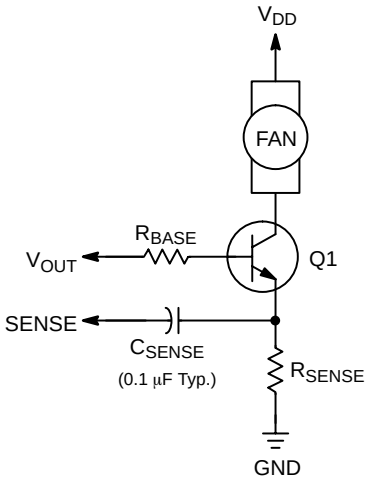


Figure 9. SENSE Network

Figure 6 illustrates a simple temperature dependent voltage divider circuit. T1 is a conventional NTC thermistor, and R1 and R2 are standard resistors. The supply voltage, V_{DD}, is divided between R2 and the parallel combination of T1 and R1. (For convenience, the parallel combination of T1 and R1 will be referred to as R_{TEMP}.) The resistance of the thermistor at various temperatures is obtained from the manufacturer's specifications. Thermistors are often referred to in terms of their resistance at 25°C. A thermistor with a 25°C resistance on the order of 100 kΩ will result in reasonable values for R1, R2, and I_{DIV}. In order to determine R1 and R2, we must specify the fan duty–cycle, i.e. V_{IN}, at any two temperatures. Equipped with these two points on the system's operating curve and the thermistor data, we can write the defining equations:

$$\frac{V_{DD} \times R2}{R_{TEMP}(t1) + R2} = V(t1) \qquad \text{(eq. 1)}$$

$$\frac{V_{DD} \times R2}{R_{TEMP}(t2) + R2} = V(t2)$$

Where *t1* and *t2* are the chosen temperatures and R_{TEMP} is the parallel combination of the thermistor and R1. These two equations permit solving for the two unknown variables, R1 and R2. Note that resistor R1 is not absolutely necessary, but it helps to linearize the response of the network.

Minimum Fan Speed

A voltage divider on V_{MIN} sets the minimum PWM duty cycle and, thus, the minimum fan speed. As with the V_{IN} input, 1.25 V to 2.65 V corresponds to 0% to 100% duty cycle. Assuming that fan speed is linearly related to duty–cycle, the minimum speed voltage is given by the equation:

$$V_{MIN} = \frac{\text{Minimum Speed}}{\text{Full Speed}} \times (1.4V) + 1.25\ V = 1.81\ V \qquad \text{(eq. 2)}$$

For example, if 2500 RPM equates to 100% fan speed, and a minimum speed of 1000 RPM is desired, then the V_{MIN} voltage is:

$$V_{MIN} = \frac{1000}{2500} \times (1.4V) + 1.25\ V = 1.81\ V \qquad \text{(eq. 3)}$$

The V_{MIN} voltage may be set using a simple resistor divider as shown in Figure 7. Per the *Electrical Characteristics*, the leakage current at the V_{MIN} pin is no more than 1 μA. It would be very conservative to design for a divider current, I_{DIV}, of 100 μA. If V_{DD} = 5.0 V then...

$$I_{DIV} = 1e^{-4}A = \frac{5.0V}{R1 + R2}\text{, therefore} \qquad \text{(eq. 4)}$$

$$R1 + R2 = \frac{5.0V}{1e^{-4}A} = 50{,}000\Omega = 50k\Omega$$

We can further specify R1 and R2 by the condition that the divider voltage is equal to our desired V_{MIN}. This yields the following equation:

$$V_{MIN} = V_{DD} \times \frac{R2}{R1 + R2} \qquad \text{(eq. 5)}$$

Solving for the relationship between R1 and R2 results in the following equation:

$$R1 = R2 \times \frac{V_{DD} - V_{MIN}}{V_{MIN}} \qquad \text{(eq. 6)}$$

In the case of this example, R1 = (1.762) R2. Substituting this relationship back into Equation 4 yields the resistor values:

R2 = 18.1 kΩ, and
R1 = 31.9 kΩ

In this case, the standard values of 32 kΩ and 18 kΩ are very close to the calculated values and would be more than adequate.

One boundary condition which may impact the selection of the minimum fan speed is the irregular activation of the Diagnostic Timer due to the MC642 "missing" fan commutation pulses at low speeds. Typically, this only occurs at very low duty–cycles (25% or less). It is a natural consequence of low PWM duty–cycles. Recall that the SENSE function detects commutation of the fan as disturbances in the current through R_{SENSE}. These can only occur when the fan is energized, i.e., V_{OUT} is "on". At very low duty–cycles, the V_{OUT} output is "off" most of the time. The fan may be rotating normally, but the commutation events are occurring during the PWM's off–time.

The phase relationship between the fan's commutation and the PWM edges tends to "walk around" as the system operates. At certain points, the MC642 may fail to capture a pulse within the 32–cycle Missing Pulse Detector window. When this happens, the 3–cycle Diagnostic Timer will be activated, the V_{OUT} output will be active continuously for three cycles and, if the fan is operating normally, a pulse will be detected. If all is well, the system will return to normal operation. There is no harm in this behavior, but it may be audible to the user as the fan will accelerate briefly when the Diagnostic Timer fires. For this reason, it is recommended that V_{MIN} be set no lower than 1.8 V.

SENSE Network (R_{SENSE} and C_{SENSE})

The network comprised of R_{SENSE} and C_{SENSE} allow the MC642 to detect commutation of the fan motor. This network can be thought of as a differentiator and threshold detector. The function of R_{SENSE} is to convert the fan current into a voltage. C_{SENSE} serves to AC–couple this voltage signal and provide a ground–referenced input to the SENSE pin. Designing a proper SENSE Network is simply a matter of scaling R_{SENSE} to provide the necessary amount of gain, i.e., the current–to–voltage conversion ratio. A 0.1 μF ceramic capacitor is recommended for C_{SENSE}. Smaller values require larger sense resistors, and higher value capacitors are bulkier and more expensive. Using a 0.1 μF results in reasonable values for R_{SENSE}. Figure 9 illustrates a typical SENSE Network. Figure 10 shows the waveforms observed using a typical SENSE Network.

Table 1 lists the recommended values of R_{SENSE} according to the nominal operating current of the fan. Note that the current draw specified by the fan manufacturer may not be the fan's nominal operating current, but may be a worst–case rating for near–stall conditions. The values in the table refer to actual average operating current. If the fan current falls between two of the values listed, use the higher resistor value. The end result of employing Table 1 is that the signal developed across the sense resistor is approximately 450 mV in amplitude.

Table 1. R_{SENSE} vs. Fan Current

Nominal Fan Current (mA)	R_{SENSE} (Ω)
50	9.1
100	4.7
150	3.0
200	2.4
250	2.0
300	1.8
350	1.5
400	1.3
450	1.2
500	1.0

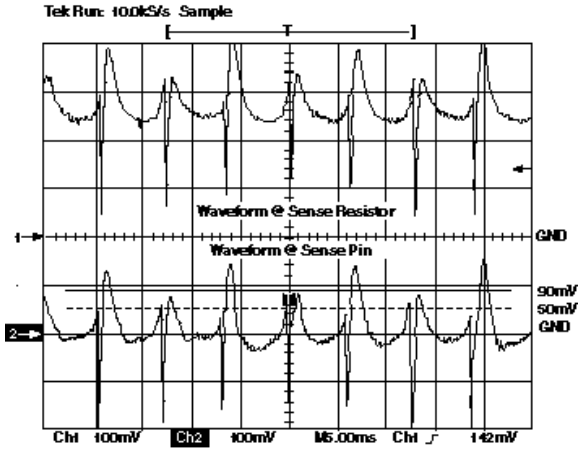
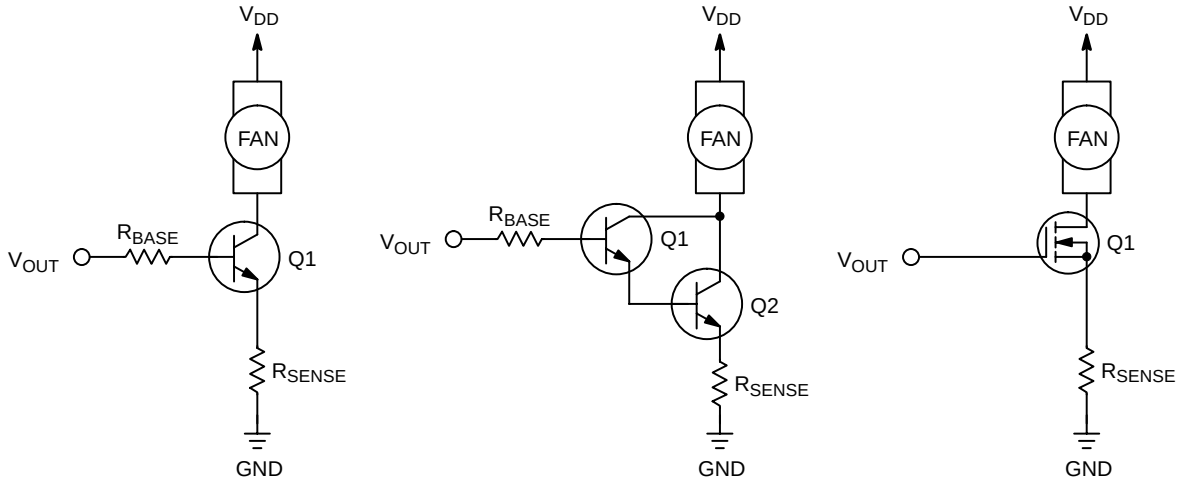


Figure 10. SENSE Waveforms



a) Single Bipolar Transistor b) Darlington Transistor Pair c) N–Channel MOSFET

Figure 11. Output Drive Transistor Circuit Topologies

Output Drive Transistor Selection

The MC642 is designed to drive an external transistor for modulating power to the fan. This is shown as “Q1” in Figures 4, 8, 9, 11, 12, and 13. The V_{OUT} pin has a minimum source current of 5 mA and a minimum sink current of 1mA at V_{DD} = 5.0 V. Bipolar transistors or MOSFET’s may be used as the power switching element as shown below. When high current gain is needed to drive larger fans, two transistors may be used in a Darlington configuration. These circuit topologies are shown in Figure 11: (a) shows a single NPN transistor used as the switching element; (b) Illustrates the Darlington pair; and (c) shows an N–channel MOSFET.

One major advantage of the MC642’s PWM control scheme versus linear speed control is that the dissipation in the pass element is kept very low. Generally, low–cost devices in very small packages such as TO–92 or SOT, can be used effectively. For fans with nominal operating currents of no more than 200 mA, a single transistor usually suffices. Above 200 mA, the Darlington or MOSFET solution is recommended. For the fan sensing function to work correctly it is imperative that the pass transistor be fully saturated when “on”. The minimum gain (h_{FE}) of the transistor in question must be adequate to fully saturate the transistor when passing the full fan current while being driven within the 5 mA I_{OH} of the V_{OUT} output.

Table 2 gives examples of some commonly available transistors. This table is a guide only. There are many transistor types which might work as well as those listed. The only critical issues when choosing a device to use as Q1 are: (1) the breakdown voltage, $V_{CE(BR)}$, must be large enough to stand off the highest voltage applied to the fan (NOTE: this may be when the fan is off!); (2) the gain (h_{FE}) must be high enough for the device to remain fully saturated while conducting the maximum expected fan current and being driven with no more than 5 mA of base/gate drive at maximum temperature; (3) rated fan current draw must be within the transistor’s current handling capability; and (4) power dissipation must be kept within the limits of the chosen device.

Table 2. Transistors for Q1

Device	$V_{BE(SAT)}$	MIN h_{FE}	$V_{BR(CEO)}$	I_C	R_{BASE} (Ω)
MPS2222	1.3	100	30	150	800
MPS2222A	1.2	100	40	150	800
2N4400	0.95	50	40	150	820
2N4401	0.95	100	40	150	820
MPS6601	1.2	50	25	500	780
MPS6602	1.2	50	40	500	780

A base–current limiting resistor is required with bipolar transistors. This is shown in Figure 8. The correct value for this resistor can be determined as follows: (see Figure 8).

$$\begin{aligned} V_{OH} &= V_{SENSE} + V_{BE(SAT)} + V_{RBASE} \\ V_{RSENSE} &= I_{FAN} \times R_{SENSE} \\ V_{RBASE} &= V_{BASE} \times I_{BASE} \\ I_{BASE} &= I_{FAN}/h_{FE} \end{aligned} \quad \text{(eq. 7)}$$

V_{OH} is specified as 80% of V_{DD} in the *Electrical Characteristics* table; $V_{BE(SAT)}$ is given in the transistor datasheet. It is now possible to solve for R_{BASE}.

$$R_{BASE} = \frac{V_{OH} - V_{BE(SAT)} - V_{RSENSE}}{I_{RBASE}} \quad \text{(eq. 8)}$$

Some applications require the fan to be powered from the negative 12 V supply to keep motor noise out of the positive voltage power supplies. As shown in Figure 12, Zener diode D2 offsets the –12 V power supply voltage holding transistor Q1 OFF when V_{OUT} is LOW. When V_{OUT} is HIGH, the voltage at the anode of D2 increases by V_{OH}, causing Q1 to turn ON. Operation is otherwise the same as the case of fan operation +12 V.

Latch–up Considerations

As with any CMOS IC, the potential exists for latch–up if signals are applied to the device which are outside the power supply range. This is of particular concern during power–up if the external circuitry, such as the sensor network, V_{MIN} divider, shutdown circuit, or fan, are powered by a supply different from that of the MC642. Care should be taken to ensure that the MC642’s V_{DD} supply powers–up *first*. If possible, the networks attached to V_{IN} and V_{MIN} should connect to the V_{DD} supply at the same physical location as the IC itself. Even if the IC and any external networks are powered by the same supply, physical separation of the connecting points can result in enough parasitic capacitance and/or inductance in the power supply connections to delay one power supply “routing” versus another.

Power Supply Routing and Bypassing

Noise present on the V_{IN} and V_{MIN} inputs may cause erroneous operation of the $\overline{\text{FAULT}}$ output. As a result, these inputs should be bypassed with a 0.01 μF capacitor mounted as close to the package as possible. This is particularly true of V_{IN}, which usually is driven from a high impedance source (such as a thermistor). In addition, the V_{DD} input should be bypassed with a 1 μF capacitor. Grounds should be kept as short as possible. To keep fan noise off the MC642 ground pin, individual ground returns for the MC642 and the low side of the fan current sense resistor should be used.

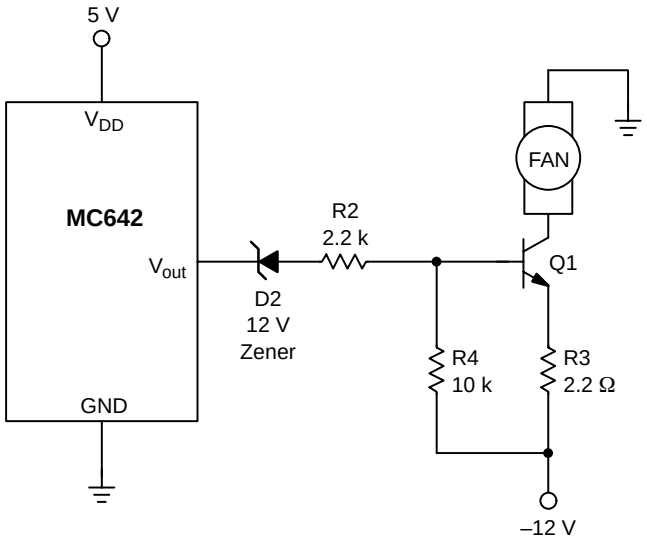


Figure 12. Powering Fan From –12V Supply

Design Example (Figure 13)

Step 1. Circulate R1 and R2 based on using an NTC having a resistance of 4.6 kΩ at T_{MIN} and 1.1 kΩ at T_{MAX}.

R1 = 75 kΩ

R2 = 1 kΩ

Step 2. Set minimum fan speed

V_{MIN} = 1.8 V

Limit the divider current to 100 μA from which R5 = 33 k and R6 = 18 kΩ

Step 3. Design the output circuit

Maximum fan motor current = 250 mA. Q1 beta is chosen at 100 from which R7 = 1.5 kΩ

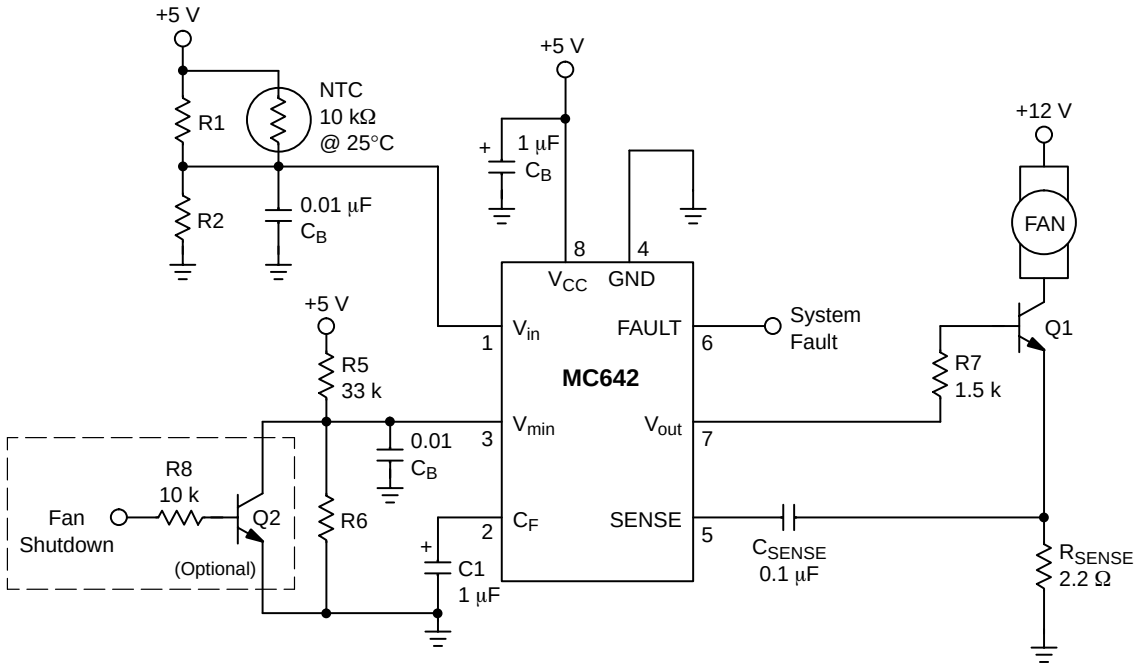


Figure 13. Design Example

MC642 as a Microcontroller Peripheral (Figure 14)

In a system containing a microcontroller or other host intelligence, the MC642 can be effectively managed as a CPU peripheral. Routine fan control functions can be performed by the MC642 without processor intervention. The micro–controller receives temperature data from one or more points throughout the system. It calculates a fan operating speed based on an algorithm specifically designed for the application at hand. The processor controls fan speed using complementary port bits I/01 through I/03. Resistors R1 through R6 (5% tolerance) form a crude 3–bit DAC that translates the 3–bit code from the processor's outputs into a 1.6 V DC control signal. (A monolithic DAC or digital pot may be used instead of the circuit shown.)

With V_{MIN} set to 1.8 V, the MC642 has a minimum operating speed of approximately 40% of full rated speed when the processor's output code is 000. Output codes 001 to 111 operate the fan from roughly 40% to 100% of full speed. An open drain output from the processor can be used to reset the MC642 following detection of a fault condition. The $\overline{\text{FAULT}}$ output can be connected to the processor's interrupt input, or to an I/O pin for polled operation.

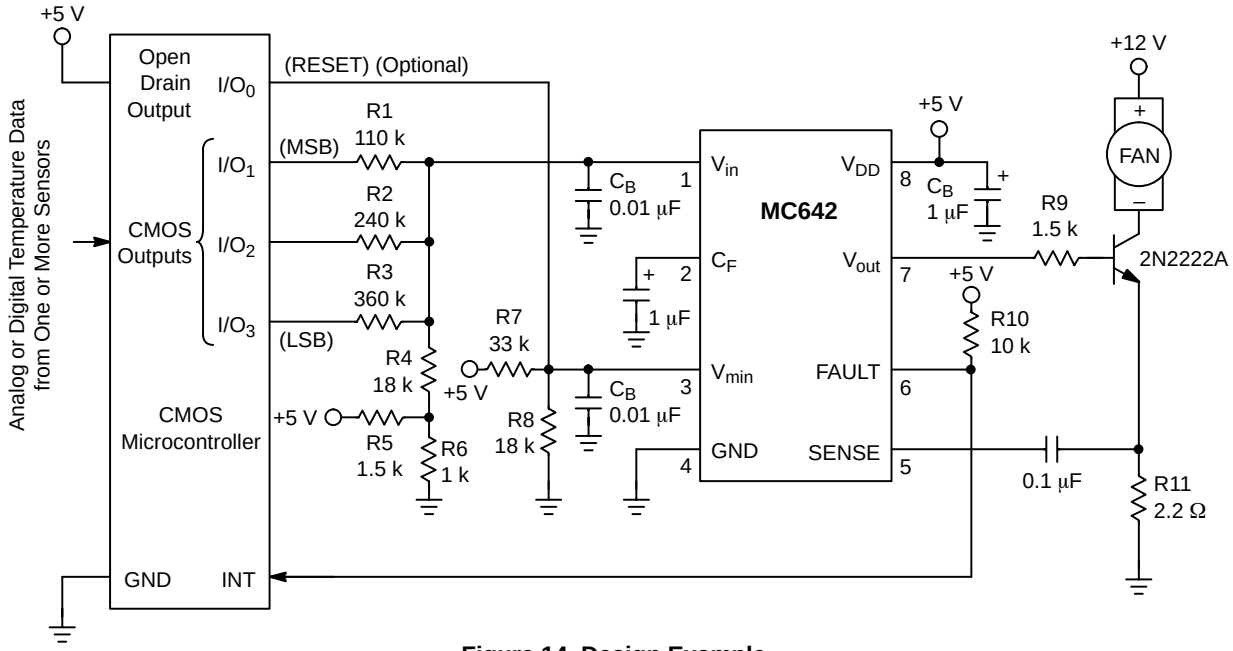
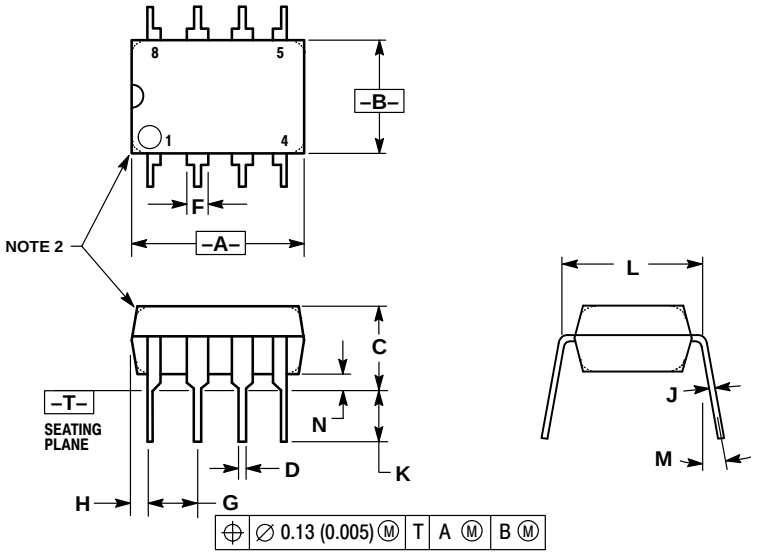


Figure 14. Design Example

PACKAGE DIMENSIONS

PDIP–8
P SUFFIX
CASE 626–05
ISSUE L

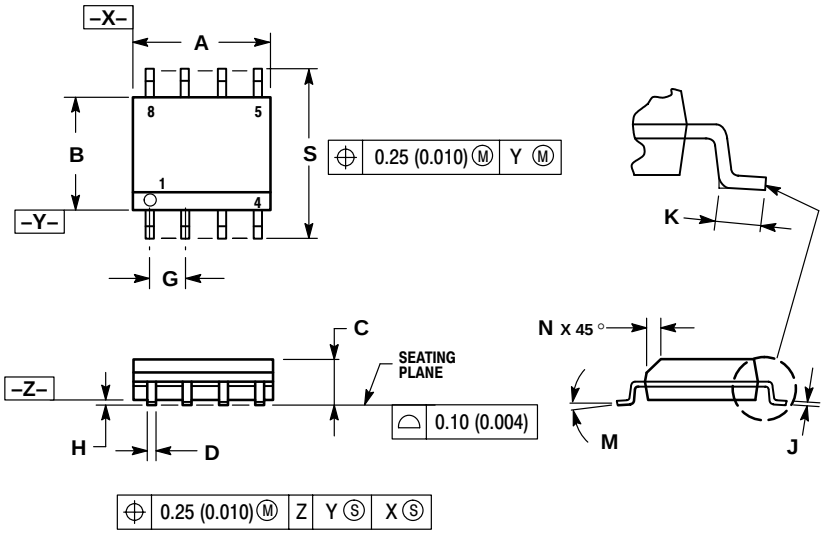


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE DIMENSIONS

SO–8
D SUFFIX
CASE 751–07
ISSUE W



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1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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