

MC74LCX373

Low-Voltage CMOS Octal Transparent Latch

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX373 is a high performance, non-inverting octal transparent latch operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX373 inputs to be safely driven from 5 V devices.

The MC74LCX373 contains 8 D-type latches with 3-state outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are enabled. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

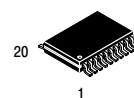
- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in all Three Logic States (10 μ A)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V;
Machine Model >200 V



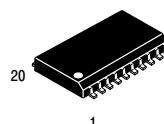
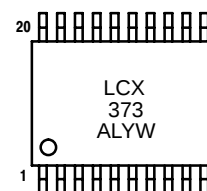
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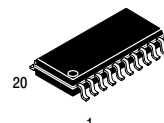
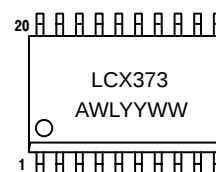
MARKING DIAGRAMS



TSSOP-20
DT SUFFIX
CASE 948E



SO-20
DW SUFFIX
CASE 751D



SO EIAJ-20
M SUFFIX
CASE 967



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74LCX373DW	SO-20	38 Units/Rail
MC74LCX373DWR2	SO-20	1000 Units/Reel
MC74LCX373DT	TSSOP-20	75 Units/Rail
MC74LCX373DTEL	TSSOP-20	2000 Units/Reel
MC74LCX373DTR2	TSSOP-20	2500 Units/Reel
MC74LCX373M	SO EIAJ-20	40 Units/Rail
MC74LCX373MEL	SO EIAJ-20	2000 Units/Reel

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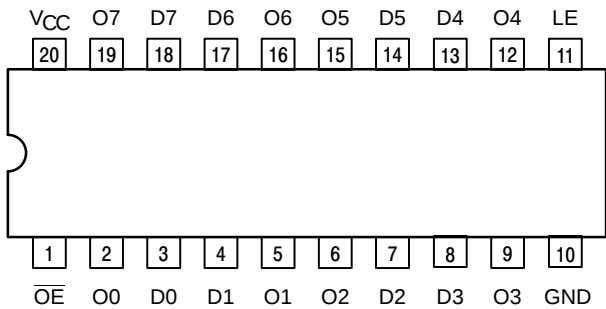


Figure 1. Pinout (Top View)

PIN NAMES

PINS	FUNCTION
$\overline{OE}$	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

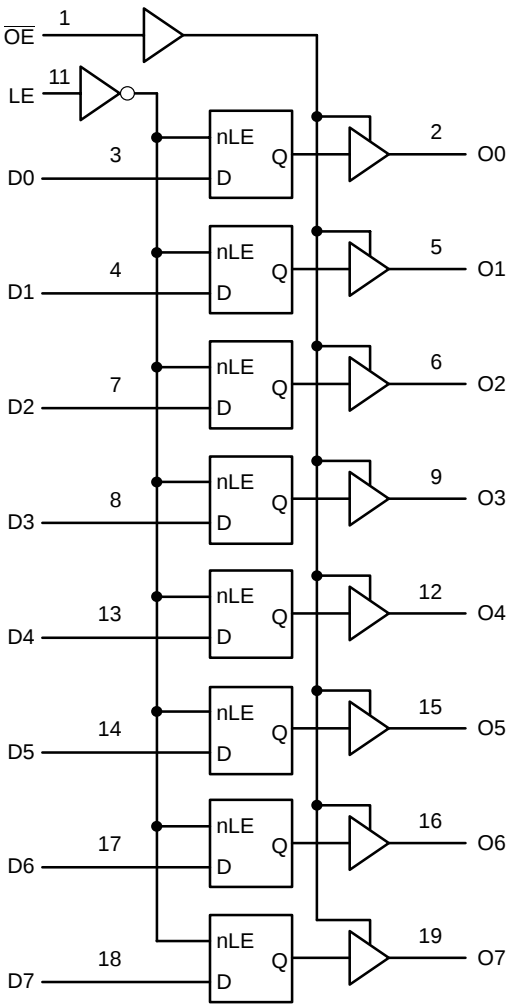


Figure 2. Logic Diagram

TRUTH TABLE

INPUTS			OUTPUTS	OPERATING MODE
OE	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition
NC = No Change, State Prior to the Latch Enable High-to-Low Transition
X = High or Low Voltage Level or Transitions are Acceptable
Z = High Impedance State
For I_{CC} Reasons DO NOT FLOAT Inputs

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MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V _{CC}	DC Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 ≤ V _I ≤ +7.0		V
V _O	DC Output Voltage	−0.5 ≤ V _O ≤ +7.0	Output in 3-State	V
		−0.5 ≤ V _O ≤ V _{CC} + 0.5	Output in HIGH or LOW State (Note 1.)	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	−65 to +150		°C

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V _I	Input Voltage	0		5.5	V
V _O	Output Voltage (HIGH or LOW State) (3-State)	0 0		V _{CC} 5.5	V
I _{OH}	HIGH Level Output Current V _{CC} = 3.0 V – 3.6 V V _{CC} = 2.7 V – 3.0 V V _{CC} = 2.3 V – 2.7 V			− 24 − 12 − 8	mA
I _{OL}	LOW Level Output Current V _{CC} = 3.0 V – 3.6 V V _{CC} = 2.7 V – 3.0 V V _{CC} = 2.3 V – 2.7 V			+ 24 + 12 + 8	mA
T _A	Operating Free-Air Temperature	−40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Unit
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2.)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2.)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA	V _{CC} - 0.2		V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
		V _{CC} = 3.0 V; I _{OH} = -24 mA	2.2		
V _{OL}	LOW Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _I	Input Leakage Current	2.3 V ≤ V _{CC} ≤ 3.6 V; 0 V ≤ V _I ≤ 5.5 V		±5	μA
I _{OZ}	3-State Output Current	2.3 ≤ V _{CC} ≤ 3.6 V; 0V ≤ V _O ≤ 5.5 V; V _I = V _{IH} or V _{IL}		±5	μA
I _{OFF}	Power-Off Leakage Current	V _{CC} = 0 V; V _I or V _O = 5.5 V		10	μA
I _{CC}	Quiescent Supply Current	2.3 ≤ V _{CC} ≤ 3.6 V; V _I = GND or V _{CC}		10	μA
		2.3 ≤ V _{CC} ≤ 3.6 V; 3.6 ≤ V _I or V _O ≤ 5.5 V		±10	
ΔI _{CC}	Increase in I _{CC} per Input	2.3 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS t_R = t_F = 2.5 ns; R_L = 500 Ω

Symbol	Parameter	Waveform	Limits						Unit
			T _A = −40°C to +85°C						
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 2.5 V ± 0.2 V		
			C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _N to O _N	1	1.5 1.5	8.0 8.0	1.5 1.5	9.0 9.0	1.5 1.5	9.6 9.6	ns
t _{PLH} t _{PHL}	Propagation Delay LE to O _N	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	1.5 1.5	10.5 10.5	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH and LOW Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	1.5 1.5	10.5 10.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	1.5 1.5	9.0 9.0	ns
t _S	Setup Time, HIGH or LOW D _N to LE	3	2.5		2.5		4.0		
t _H	Hold Time, HIGH or LOW D _N to LE	3	1.5		1.5		2.0		
t _W	LE Pulse Width, HIGH	3	3.3		3.3		4.0		
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3.)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

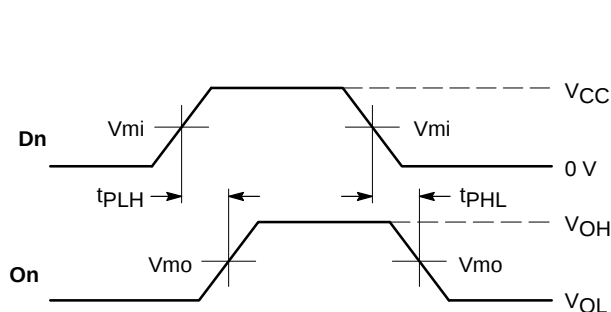
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
VOLP	Dynamic LOW Peak Voltage (Note 4.)	$V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$		0.8		V
		$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$		0.6		V
VOLV	Dynamic LOW Valley Voltage (Note 4.)	$V_{CC} = 3.3\text{ V}, C_L = 50\text{ pF}, V_{IH} = 3.3\text{ V}, V_{IL} = 0\text{ V}$		-0.8		V
		$V_{CC} = 2.5\text{ V}, C_L = 30\text{ pF}, V_{IH} = 2.5\text{ V}, V_{IL} = 0\text{ V}$		-0.6		V

4. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

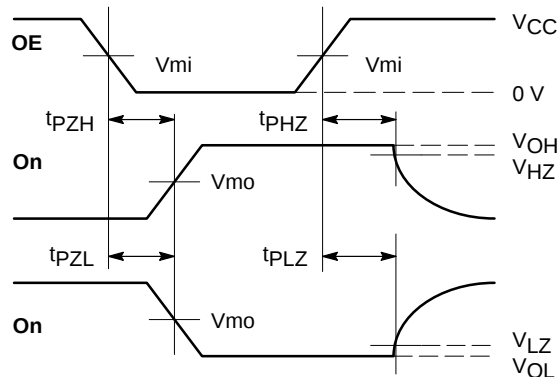
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or } V_{CC}$	25	pF



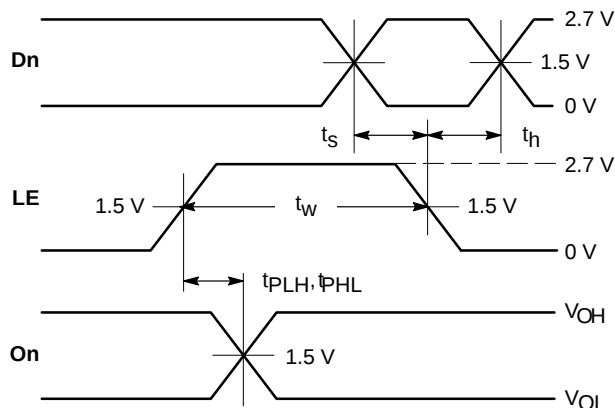
WAVEFORM 1 – PROPAGATION DELAYS

$t_R = t_F = 2.5\text{ ns}$, 10% to 90%; $f = 1\text{ MHz}$; $t_W = 500\text{ ns}$



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.5\text{ ns}$, 10% to 90%; $f = 1\text{ MHz}$; $t_W = 500\text{ ns}$



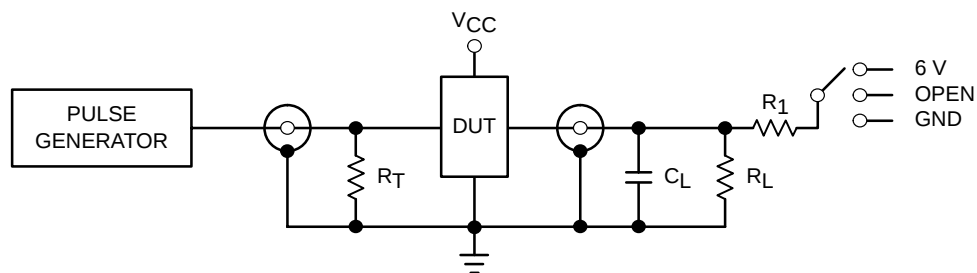
WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES

$t_R = t_F = 2.5\text{ ns}$, 10% to 90%; $f = 1\text{ MHz}$; $t_W = 500\text{ ns}$ except when noted

Symbol	V_{CC}		
	$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$2.5\text{ V} \pm 0.2\text{ V}$
Vmi	1.5 V	1.5 V	$V_{CC}/2$
Vmo	1.5 V	1.5 V	$V_{CC}/2$
VHZ	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.15\text{ V}$
VLZ	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.15\text{ V}$

Figure 3. AC Waveforms

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TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6 V at $V_{CC} = 3.3 \pm 0.3$ V 6 V at $V_{CC} = 2.5 \pm 0.2$ V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH} , t_{PHZ}	GND

$C_L = 50$ pF at $V_{CC} = 3.3 \pm 0.3$ V or equivalent (includes jig and probe capacitance)

$C_L = 30$ pF at $V_{CC} = 2.5 \pm 0.2$ V or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4. Test Circuit