

# MC100E336

## 5V ECL 3-Bit Registered Bus Transceiver

The MC100E336 contains three bus transceivers with both transmit and receive registers. The bus outputs (BUS0–BUS2) are specified for driving a 25  $\Omega$  bus; the receive outputs (Q0 – Q2) are specified for 50  $\Omega$ . The bus outputs feature a normal HIGH level ( $V_{OH}$ ) and a cutoff LOW level – when LOW, the outputs go to –2.0 V and the output emitter-follower is “off”, presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

The Transmit Enable pins (TEN) control whether current data is held in the transmit register, or new data is loaded from the A/B inputs. A LOW on both of the Bus Enable inputs (BUSEN), when clocked through the register, disables the bus outputs to –2.0 V.

The receiver section clocks bus data into the receive registers, after gating with the Receive Enable (RXEN) input.

All registers are clocked by a positive transition of CLK1 or CLK2 (or both).

Additional leadframe grounding is provided through the Ground pins (GND) which should be connected to 0 V. The GND pins are not electrically connected to the chip.

The 100 Series contains temperature compensation.

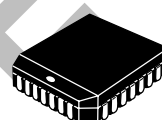
- 25  $\Omega$  Cutoff Bus Outputs
- 50  $\Omega$  Receiver Outputs
- Transmit and Receive Registers
- 1500 ps Max. Clock to Bus
- 1000 ps Max. Clock to Q
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- PECL Mode Operating Range:  $V_{CC} = 4.2$  V to 5.7 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -4.2$  V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 code V–0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 430 devices



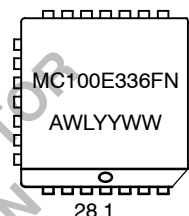
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### MARKING DIAGRAM



PLCC-28  
FN SUFFIX  
CASE 776

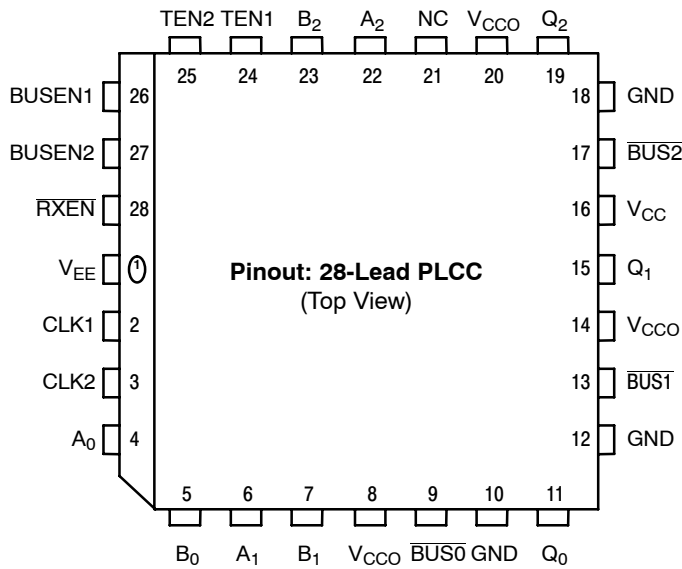


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

| Device        | Package | Shipping       |
|---------------|---------|----------------|
| MC100E336FN   | PLCC-28 | 37 Units/Rail  |
| MC100E336FNR2 | PLCC-28 | 500 Units/Reel |

# MC100E336



\* All  $V_{CC}$  and  $V_{CCO}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CCO}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

## PIN DESCRIPTION

| PIN                  | FUNCTION           |
|----------------------|--------------------|
| TEN1, TEN2           | ECL Transit Enable |
| A0-A2                | ECL Data Inputs A  |
| B0-B2                | ECL Data Inputs B  |
| Q0-Q1                | ECL Output         |
| BUSEN1, BUSEN2       | ECL Bus Enables    |
| BUS0-BUS2            | ECL Bus Outputs    |
| RXEN                 | ECL Receive Enable |
| CLK1, CLK2           | ECL Clock Input    |
| $V_{CC}$ , $V_{CCO}$ | Positive Supply    |
| $V_{EE}$             | Negative Supply    |
| GND                  | Ground             |
| NC                   | No Connect         |

Figure 1. Pinout Diagram

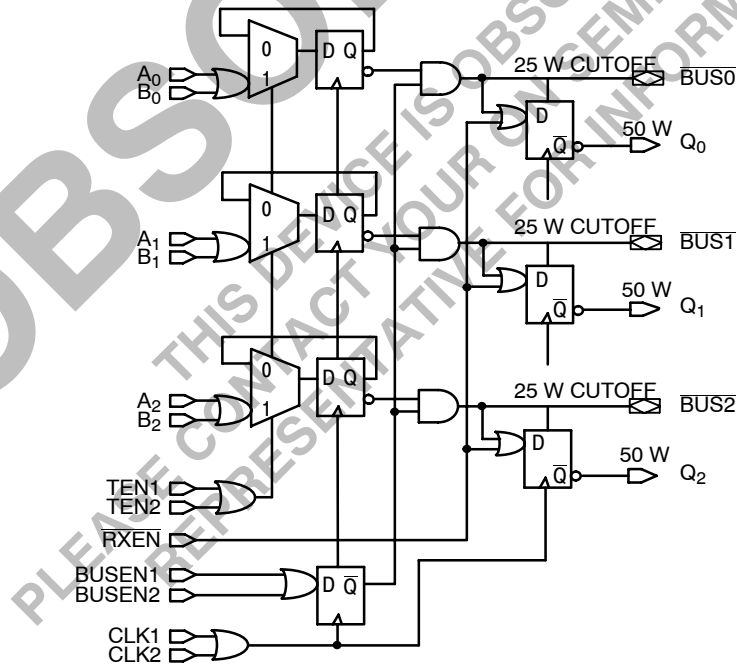


Figure 2. Logic Diagram

**MAXIMUM RATINGS** (Note 1)

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating                     | Units        |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|----------------------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 8                          | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | -8                         | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6                    | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100                  | mA<br>mA     |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | 0 to +85                   | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | -65 to +150                | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 LFPM<br>500 LFPM                             | 28 PLCC<br>28 PLCC                                                   | 63.5<br>43.5               | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | std bd                                         | 28 PLCC                                                              | 22 to 26                   | °C/W         |
| V <sub>EE</sub>  | PECL Operating Range<br>NECL Operating Range       |                                                |                                                                      | 4.2 to 5.7<br>-5.7 to -4.2 | V<br>V       |
| T <sub>sol</sub> | Wave Solder                                        | < 2 to 3 sec @ 248°C                           |                                                                      | 265                        | °C           |

1. Maximum Ratings are those values beyond which device damage may occur.

**100E SERIES PECL DC CHARACTERISTICS** V<sub>CCx</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 2)

| Symbol           | Characteristic                                 | 0°C  |      |            | 25°C |      |            | 85°C |      |            | Unit |
|------------------|------------------------------------------------|------|------|------------|------|------|------------|------|------|------------|------|
|                  |                                                | Min  | Typ  | Max        | Min  | Typ  | Max        | Min  | Typ  | Max        |      |
| I <sub>EE</sub>  | Power Supply Current                           |      | 125  | 150        |      | 125  | 150        |      | 144  | 173        | mA   |
| V <sub>OH</sub>  | Output HIGH Voltage (Note 3)                   | 3975 | 4050 | 4120       | 3975 | 4050 | 4120       | 3975 | 4050 | 4120       | mV   |
| V <sub>OL</sub>  | Output LOW Voltage (Note 3)                    | 3190 | 3295 | 3380       | 3190 | 3255 | 3380       | 3190 | 3260 | 3380       | mV   |
| V <sub>IH</sub>  | Input HIGH Voltage                             | 3835 | 4050 | 4120       | 3835 | 4120 | 4120       | 3835 | 4120 | 4120       | mV   |
| V <sub>IL</sub>  | Input LOW Voltage                              | 3190 | 3300 | 3525       | 3190 | 3525 | 3525       | 3190 | 3525 | 3525       | mV   |
| V <sub>CUT</sub> | Cut-off Output Voltage (Note 3)                | 2.9  |      | 2.97       | 2.9  |      | 2.97       | 2.9  |      | 2.97       | V    |
| I <sub>IH</sub>  | Input HIGH Current<br>RXEN<br>All Other Inputs |      |      | 225<br>150 |      |      | 225<br>150 |      |      | 225<br>150 | μA   |
| I <sub>IL</sub>  | Input LOW Current                              | 0.5  | 0.3  |            | 0.5  | 0.25 |            | 0.5  | 0.2  |            | μA   |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / -0.8 V.

3. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> - 2.10 V.

**100E SERIES NECL DC CHARACTERISTICS** V<sub>CCx</sub> = 0.0 V; V<sub>EE</sub> = -5.0 V (Note 4)

| Symbol           | Characteristic                                 | 0°C   |       |            | 25°C  |       |             | 85°C  |       |            | Unit |
|------------------|------------------------------------------------|-------|-------|------------|-------|-------|-------------|-------|-------|------------|------|
|                  |                                                | Min   | Typ   | Max        | Min   | Typ   | Max         | Min   | Typ   | Max        |      |
| I <sub>EE</sub>  | Power Supply Current                           |       | 125   | 150        |       | 125   | 150         |       | 144   | 173        | mA   |
| V <sub>OH</sub>  | Output HIGH Voltage (Note 5)                   | -1025 | -950  | -880       | -1025 | -950  | -880        | -1025 | -950  | -880       | mV   |
| V <sub>OL</sub>  | Output LOW Voltage (Note 5)                    | -1810 | -1705 | -1620      | -1810 | -1745 | -1620       | -1810 | -1740 | -1620      | mV   |
| V <sub>IH</sub>  | Input HIGH Voltage                             | -1165 | -950  | -880       | -1165 | -880  | -880        | -1165 | -880  | -880       | mV   |
| V <sub>IL</sub>  | Input LOW Voltage                              | -1810 | -1700 | -1475      | -1810 | -1475 | -1475       | -1810 | -1475 | -1475      | mV   |
| V <sub>CUT</sub> | Cut-off Output Voltage (Note 3)                | 2.9   |       | 2.97       | 2.9   |       | 2.97        | 2.9   |       | 2.97       | V    |
| I <sub>IH</sub>  | Input HIGH Current<br>RXEN<br>All Other Inputs |       |       | 225<br>150 |       |       | 225<br>1502 |       |       | 225<br>150 | μA   |
| I <sub>IL</sub>  | Input LOW Current                              | 0.5   | 0.3   |            | 0.5   | 0.25  |             | 0.5   | 0.2   |            | μA   |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.46 V / -0.8 V.

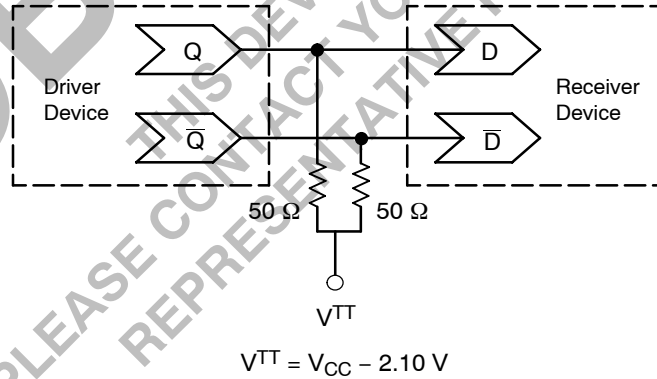
5. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> - 2.10 V.

# MC100E336

**AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 6)

| Symbol                 | Characteristic                                                                                | 0°C                      |                            |                    | 25°C                     |                            |                    | 85°C                     |                            |                    | Unit |
|------------------------|-----------------------------------------------------------------------------------------------|--------------------------|----------------------------|--------------------|--------------------------|----------------------------|--------------------|--------------------------|----------------------------|--------------------|------|
|                        |                                                                                               | Min                      | Typ                        | Max                | Min                      | Typ                        | Max                | Min                      | Typ                        | Max                |      |
| $f_{MAX}$              | Maximum Toggle Frequency                                                                      |                          | TBD                        |                    |                          | TBD                        |                    |                          | TBD                        |                    | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>Clk to Q<br>Clk to $\overline{BUS}$                            | 500<br>825               | 700<br>1250                | 100<br>1800        | 500<br>825               | 700<br>1250                | 1000<br>1800       | 500<br>825               | 700<br>1250                | 1000<br>1800       | ps   |
| $t_s$                  | Setup Time<br>$\overline{BUS}$ , $\overline{RXEN}$<br>$BUSEN$<br>A, B Data<br>TEN             | 150<br>100<br>300<br>450 | -150<br>-200<br>-50<br>150 |                    | 150<br>100<br>300<br>450 | -150<br>-200<br>-50<br>150 |                    | 150<br>100<br>300<br>450 | -150<br>-200<br>-50<br>150 |                    | ps   |
| $t_h$                  | Hold Time<br>$\overline{BUS}$ , $\overline{RXEN}$<br>$BUSEN$<br>A, B Data<br>TEN              | 450<br>500<br>350<br>200 | 150<br>200<br>50<br>-150   |                    | 450<br>500<br>350<br>200 | 150<br>200<br>50<br>-150   |                    | 450<br>500<br>350<br>200 | 150<br>200<br>50<br>-150   |                    | ps   |
| $t_{PW}$               | Minimum Pulse Width<br>Clk                                                                    | 400                      |                            |                    | 400                      |                            |                    | 400                      |                            |                    | ps   |
| $t_{JITTER}$           | Cycle-to-Cycle Jitter                                                                         |                          | TBD                        |                    |                          | TBD                        |                    |                          | TBD                        |                    | ps   |
| $t_r$<br>$t_f$         | Rise/Fall Times<br>20 - 80% ( $Q_n$ )<br>20 - 80% ( $BUS_n$ Rise)<br>20 - 80% ( $BUS_n$ Fall) | 300<br>500<br>300        | 450<br>800<br>500          | 700<br>1000<br>800 | 300<br>500<br>300        | 450<br>800<br>500          | 700<br>1000<br>800 | 300<br>500<br>300        | 450<br>800<br>500          | 700<br>1000<br>800 | ps   |

6. 100 Series:  $V_{EE}$  can vary +0.46 V / -0.8 V.



**Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

**Resource Reference of Application Notes**

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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