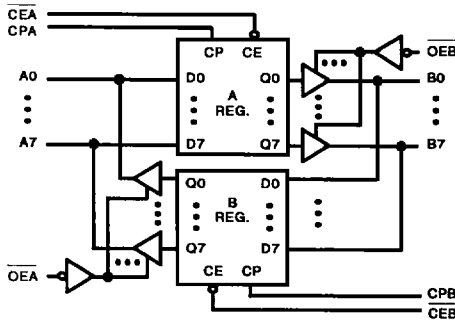


CD54/74FCT2952A, CD54/74FCT2952BT CD54/74FCT2953A, CD54/74FCT2953BT

July 1990

Octal Register-Transceivers, 3-State

CD54/74FCT2952A, CD54/74FCT2952BT - Non-Inverting
CD54/74FCT2953A, CD54/74FCT2953BT - Inverting



FCT2952A FUNCTIONAL DIAGRAM

Type Features:

- Buffered inputs
- Typical propagation delay:
5.6ns @ VCC = 5V, TA = 25°C, CL = 50pF (FCT2952A, FCT2953A)

The CD54/74FCT2952A, 2952BT, 2953A and 2953BT octal register-transceivers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

These devices contain two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Each register has separate clock, clock enable, and 3-state output enable signals associated with it.

The CD54/74FCT2952A, 2952BT, 2953A and 2953BT are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

Family Features:

- SCR-latchup-resistant BiCMOS process and circuit design
- FCTXXXXA - Speed of bipolar FAST*/AS/S;
FCTXXXXBT - 30% faster than FAST*/AS/S with significantly reduced power consumption
- 64/48-mA output sink current (commercial/extended industrial)
- Output voltage swing limited to 3.7V @ VCC = 5V
- Controlled output-edge rates
- Input/output isolation to VCC
- BiCMOS technology with low quiescent power

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54FCT2952A and 2953A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

REGISTER FUNCTION TABLE
(APPLIES TO A OR B REGISTER)

INPUTS			INTERNAL Q	FUNCTION
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L H	 	L L	L H	Load Data

OUTPUT CONTROL

$\overline{OE}$	INTERNAL Q	OUTPUTS		FUNCTION
		FCT2952A,BT	FCT2953A,BT	
H	X	Z	Z	Disable Outputs
L L	L H	L H	H L	Enable Outputs

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (VCC)	−0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$)	−20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$)	−50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O	+70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O	−30mA
DC VCC CURRENT (I_{CC})	140mA
DC GROUND CURRENT (I_{GND})	528mA
POWER DISSIPATION PER PACKAGE (PD):	
For $T_A = -55^{\circ}C$ to $+100^{\circ}C$ (PACKAGE TYPE E)	500mW
For $T_A = +100^{\circ}C$ to $+125^{\circ}C$ (PACKAGE TYPE E)	Derate Linearly at 8mW/°C to 300mW
For $T_A = -55^{\circ}C$ to $+70^{\circ}C$ (PACKAGE TYPE M)	400mW
For $T_A = +70^{\circ}C$ to $+125^{\circ}C$ (PACKAGE TYPE M)	Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE E, M	−55°C to +125°C
STORAGE TEMPERATURE (T_{stg})	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 in. $\pm$ 1/32 in. (1.59mm $\pm$ 0.79mm) from case for 10s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only	+300°C

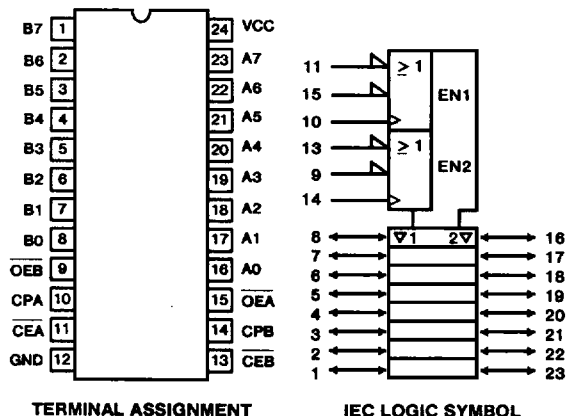
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

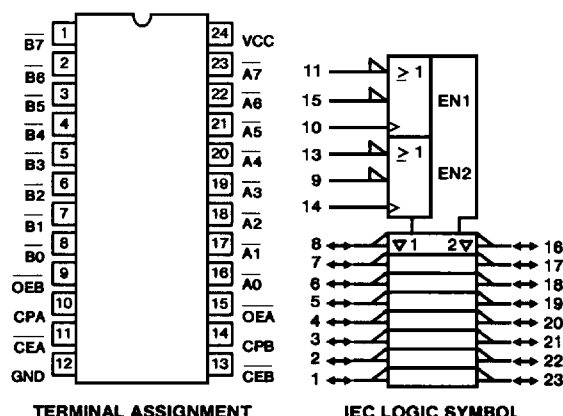
CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range, VCC*: CD74 Series, $T_A = 0^{\circ}C$ to $70^{\circ}C$ CD54 Series, $T_A = -55^{\circ}C$ to $+125^{\circ}C$	4.75	5.25	V
	4.5	5.5	V
DC Input Voltage, V_I	0	VCC	V
DC Output Voltage, V_O	0	$\leq VCC$	V
Operating Temperature, T_A	−55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT2952A, CD54/74FCT2952BT TYPES



CD54/74FCT2953A, CD54/74FCT2953BT TYPES



STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V

54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		VCC (V)	AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		VI (V)	IO (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or VIL	-15	MIN	2.4	-	2.4	-	-	-	V
			-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or VIL	64	MIN	-	0.55	-	0.55	-	-	V
			48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	μA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	μA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	μA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	μA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.

† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS		SYMBOL	V _{CC} (V)	CD54/74FCT2952A, 2953A						CD54/74FCT2952BT, 2953BT						UNITS
				AMBIENT TEMPERATURE (T _A)												
				+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C				
					TYP	MIN	MAX	MIN		MAX	TYP	MIN	MAX	MIN	MAX	
Clock Pulse Width	CPA, CPB	tW	5†		3	-	3	-					-		ns	
Setup Time	An, Bn to CPA, CPB	tSU	5		2	-	2.5	-					-		ns	
	CEA, CEB to CPA, CPB	tSU	5		3	-	3	-					-		ns	
Hold Time	An, Bn to CPA, CPB	tH	5		2	-	2	-					-		ns	
	CEA, CEB to CPA, CPB	tH	5		2	-	2	-					-		ns	

†5V: min. is @ 4.5V

5V: min. is @ 4.75V for 0°C to +70°C

typ. is @ 5V

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS		SYMBOL	V _{CC} (V)	CD54/74FCT2952A, 2953A						CD54/74FCT2952BT, 2953BT						UNITS
				AMBIENT TEMPERATURE (T _A)												
				+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C				
					TYP	MIN	MAX	MIN		MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays:	CPA, CPB to Bn, An	tPLH, tPHL	5†	5.5	2	10	2	11	CONTACT LOCAL SALES OFFICE FOR AVAILABILITY						ns	
Output Enable Time	$\overline{OE}A$ or $\overline{OE}B$ to An or Bn	tPZL, tPZH	5	5.5	1.5	10.5	1.5	13							ns	
Output Disable Time	$\overline{OE}A$ or $\overline{OE}B$ to An or Bn	tPLZ, tPHZ	5	5.5	1.5	10	1.5	10							ns	
Power Dissipation Capacitance	CPD §	-	56 Typical						56 Typical						pF	
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 1	5	0.5 Typical @ +25°C												V	
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 1	5	1 Typical @ +25°C												V	
Input Capacitance	CI	-	-	-	10	-	10	-	-	10	-	10	-	10	pF	
Input/Output Capacitance	CI/O	-	-	-	15	-	15	-	-	15	-	15	-	15	pF	

†5V: min. is @ 5.5V

max. is @ 4.5V

5V: min. is @ 5.25V for 0°C to +70°C

max. is @ 4.75V for 0°C to +70°C

typ. is @ 5V

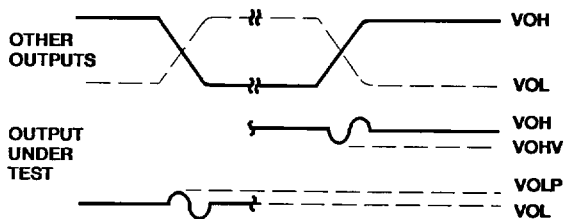
§CPD, measured per function, is used to determine the dynamic power consumption.

PD (per package) = $V_{CC} I_{CC} + \sum (V_{CC}^2 f_i C_{PD} + V_{O}^2 f_i C_L + V_{CC} \Delta I_{CC} D)$ where: V_{CC} = supply voltage ΔI_{CC} = flow through current x unit load C_L = output load capacitance

D = duty cycle of Input high

 f_i = output frequency f_i = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics:
 $PRR \leq 1\text{MHz}$, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with $0.1\mu\text{F}$ capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

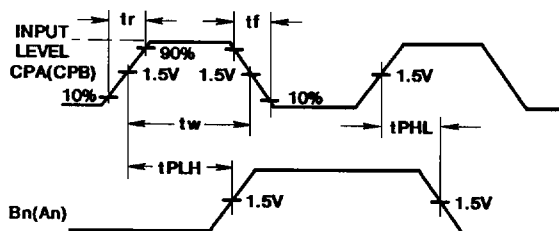


Figure 2 - CD54/74FCT2952A, 2952BT propagation delay times.

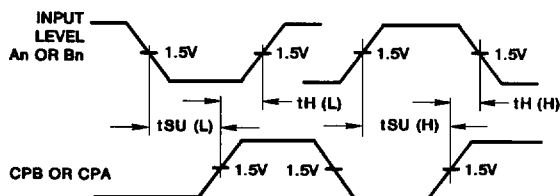
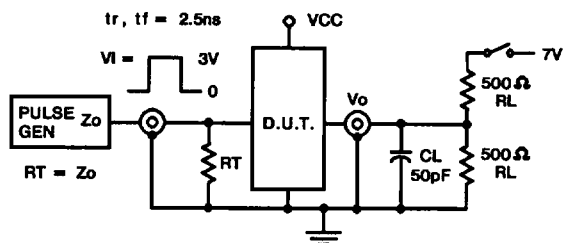
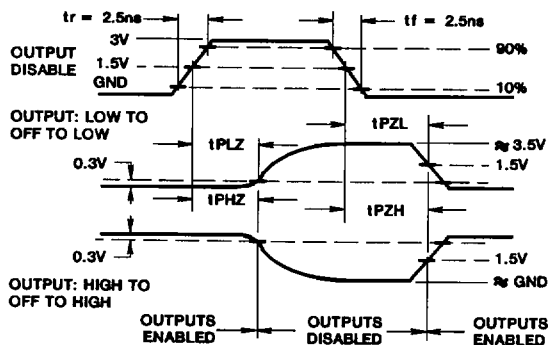


Figure 3 - Setup and hold times.



TEST	SWITCH POSITION
t_{PLZ} , t_{PZL} , OPEN DRAIN	CLOSED
t_{PHZ} , t_{PZH} , t_{PLH} , t_{PHL}	OPEN

Figure 4 - Three-state propagation delay times and test circuit.