



4127

LOGARITHMIC AMPLIFIER

FEATURES

- ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY
- WIDE INPUT DYNAMIC RANGE
6 Decades of Current
4 Decades of Voltage
- VERSATILE
Log, Antilog, and Log Ratio Capability

DESCRIPTION

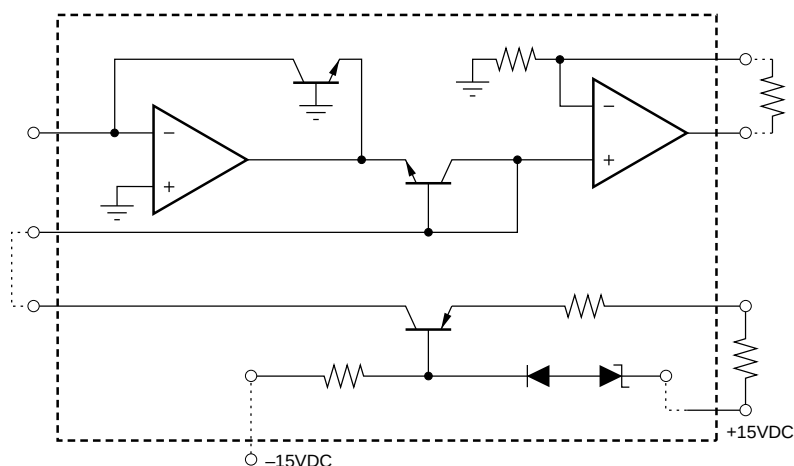
Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input

current and four decades of input voltage. In addition, a current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to $+70^{\circ}\text{C}$.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

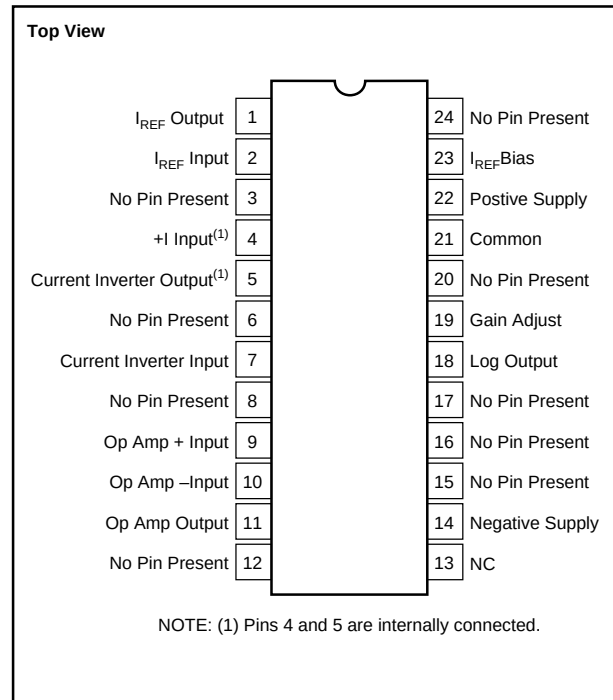
ELECTRICAL

Typical Specifications at +25°C with rated supplies, unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY⁽¹⁾ , % of FSR Current Source Input: 1nA to 1mA Voltage Input: 1mV to 10V	0.5% max 0.5% max	1% max 1% max
INPUT Current Source Input, Pin 4 Current Source Input, Pin 7 Reference Current Input, Pin 2 Absolute Maximum Inputs	+1nA to +1mA -1nA to -1mA +1μA to +1mA ±10mA or ±Supply Volts	
OUTPUT Voltage Current Impedance	±10V ±5mA 10Ω	
FREQUENCY RESPONSE -3dB Small Signal at Current Input of 100μA of 10μA of 1μA of 100nA of 10nA Step Response to within ±1% of Final Value ($I_R = 1\mu A$, $A = 5$)	90kHz 50kHz 5kHz 250Hz 80Hz 10ms	
STABILITY Scale Factor Drift ($\Delta A/^\circ C$) Reference Current Drift ($\Delta I_R/^\circ C$) Input Offset Current Drift ($\Delta I_S/^\circ C$) Input Offset Voltage Drift Accuracy vs Supply Variation Reference Current Input Offset Voltage Input Noise - Current Input Input Noise - Voltage Input	±0.0005A/°C ±0.001 $I_R/^\circ C$ for $I_R \geq 1\mu A$ ±0.003 $I_R/^\circ C$ for $400nA < I_R < 1\mu A$ 10pA at +25°C, Doubles Every 10°C ±10μV/°C ±0.001 I_R/V ±300μV/V 1pA, rms, 10Hz to 10kHz 10μA, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS Input Offset Voltage Input Bias Current Input Impedance Large Signal Voltage Gain Output Current	5mV 40nA 1MΩ 85dB 5mA	
TEMPERATURE RANGE Specification Operating Storage	0°C to +60°C -10°C to +70°C -55°C to +125°C	
POWER SUPPLY REQUIREMENTS Rated Supply Voltages Supply Voltage Range Supply Current Drain at Quiescent, max at Full Load, max	±15VDC ±14VDC to ±16VDC ±20mA ±26mA	

NOTE: (1) Log conformity at 25°C.

PIN CONFIGURATION



PACKAGE INFORMATION

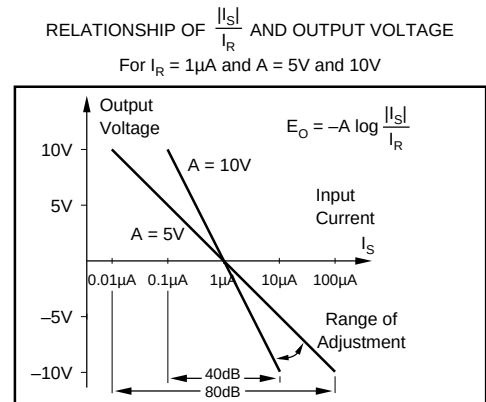
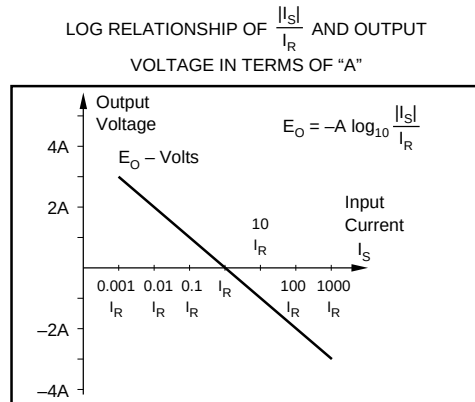
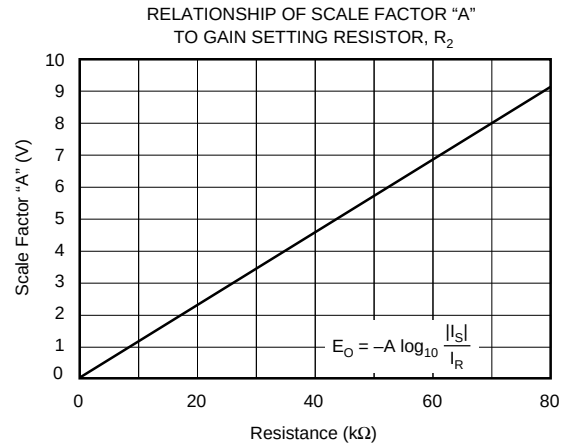
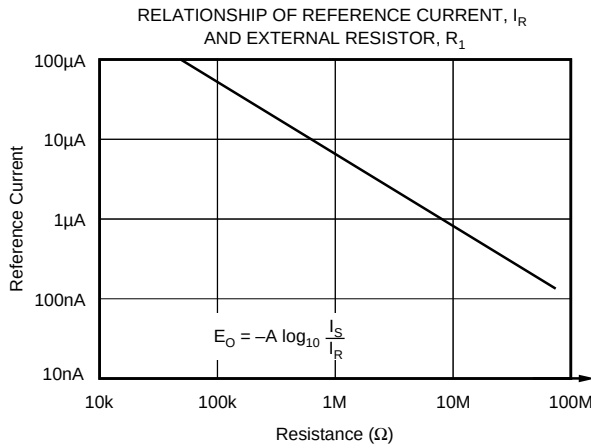
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
4127KG	24-Pin	075
4127JG	24-Pin	075

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

TYPICAL PERFORMANCE CURVES

At +25°C with rated supplies, unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are

subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic

mic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range, but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickup.

The input op amps, A_1 and A_3 , have FET input stages for low noise and very-low input bias current. The op amp, A_1 , will make the collector current of Q_1 equal to the signal input current I_S , and the collector current of Q_2 will be the reference input current I_R .

From the semiconductor junction characteristics, the base-to-emitter voltage will be:

$$V_{BE} \approx \frac{mKT}{q} \ln \frac{I_C}{I_L},$$

where: I_C = Collector current
 I_L = Reverse saturation current
 q , m , K = Constants
 T = Absolute temperature

$$\text{So } E_1 = -\frac{mKT_1}{q} \ln \frac{I_S}{I_{L1}} \text{ and } E_2 - E_1 = \frac{mKT_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics, then:

$$E_2 = \frac{mKT}{q} \left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L} \right]$$

$$E_2 = \frac{-mKT}{q} \ln \frac{I_S}{I_R}$$

The output op amp, A_2 , provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of $(mKT)/q$ is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage, E_O , expressed as a log will be:

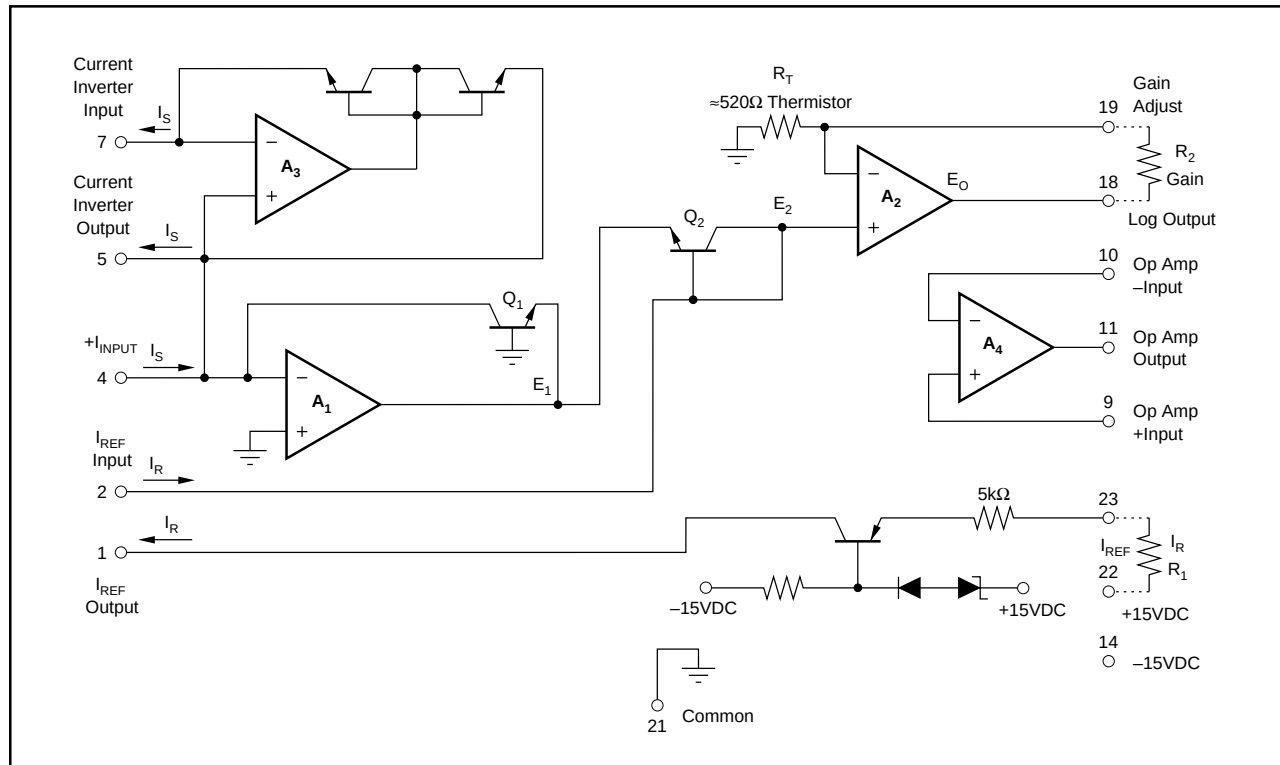


FIGURE 1. Functional Diagram.

$$E_O = -A \log_{10} \frac{I_S}{I_R},$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T} (26\text{mV}) \frac{1}{0.434}, R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor “A”. R_1 and R_2 must be trimmed to the desired values, but the approximate relationships are shown in Typical Performance Curves.

The relationship between the input current, I_S , and the output voltage, E_O , in terms of the externally adjusted parameters, I_R and “A”, is illustrated in Typical Performance Curves. This relationship is, of course, restricted to values of I_S between 1nA and 1mA and output voltages of less than $\pm 10\text{V}$.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full $\pm 10\text{V}$ output range. Once an output range of $\pm 10\text{V}$ has been chosen, then “A” and I_R can be determined from the Min/Max of the input current, I_S .

$$E_O = -A \log \frac{I_S}{I_R}, \text{ where } I_{\text{MIN}} < I_S < I_{\text{MAX}}$$

The output range of $\pm 10\text{V}$ for an input range of I_{MIN} to I_{MAX} means that:

$$+10 = -A \log \frac{I_{\text{MIN}}}{I_R} \text{ and } -10 = -A \log \frac{I_{\text{MAX}}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{\text{MAX}} + I_{\text{MIN}}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{\text{MAX}} I_{\text{MIN}}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{\text{MAX}}}{\sqrt{I_{\text{MAX}} I_{\text{MIN}}}}$$

In terms of the input current range for I_S , the values for I_R and A that will provide a full $\pm 10\text{V}$ output swing are:

$$I_R = \sqrt{I_{\text{MAX}} I_{\text{MIN}}} \text{ and } A = \frac{10}{\log \frac{I_{\text{MAX}}}{I_R}}$$

EXAMPLE

Assume that I_{MIN} is +10nA and I_{MAX} is +100 μA .

This is an 80dB range.

$$I_R = \sqrt{I_{\text{MAX}} I_{\text{MIN}}} = \sqrt{(10^{-4})(10^{-8})} = 10^{-6}, \text{ or } 1\mu\text{A}.$$

$$\frac{I_{\text{MAX}}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{\text{MAX}}}{I_R} = 2; \text{ So, } A = 5$$

For an I_R of 1 μA and A of 5,

$$E_O = -5 \log \frac{I_S}{1\mu\text{A}}$$

CONNECTION DIAGRAMS

Transfer function is $E_O = -A \log \frac{I_1}{I_R}$ where I_1 is a positive

input current and I_R is the resistor-programmed internal reference current (see Figure 2).

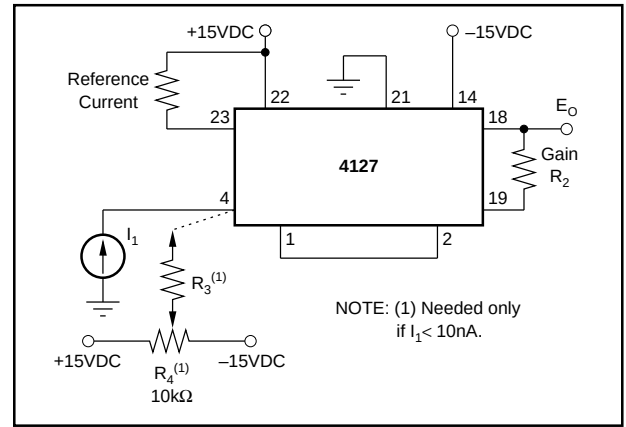


FIGURE 2. Transfer Function When I_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$, adjust R_1 such that $E_O = 0$.
3. Apply $|I_1| = I_{\text{MAX}}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{\text{MIN}}| \geq 10\text{nA}$. Otherwise, apply $|I_1| = 1\text{nA}$, make $R_3 = 1\text{k}\Omega$ and adjust R_4 for the proper output voltage. For R_3 , a single resistor is recommended. A voltage divider network is difficult to use due to amplifier offset voltage.

Transfer function is $E_O = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative

input current and I_R is the resistor-programmed internal reference current (see Figure 3).

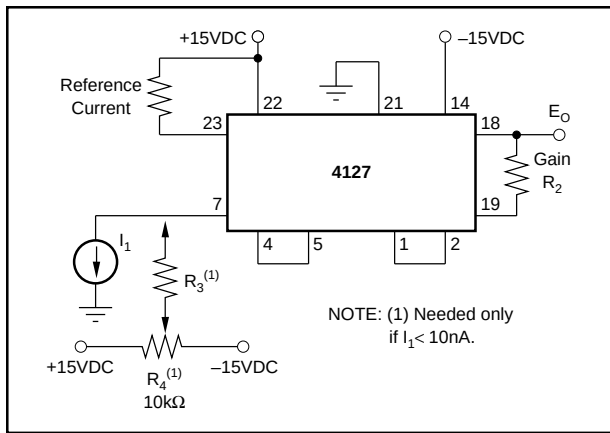


FIGURE 3. Transfer Function When I_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_O = 0$.
3. Apply $|I_1| = I_{MAX}$, adjust R_2 for the proper output voltage
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1MIN}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1kM\Omega$ and adjust R_4 for the proper output voltage. For R_3 , a single resistor is recommended. A voltage divider network is difficult to use due to amplifier offset voltage.

Transfer function is $E_O = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current (see Figure 4).

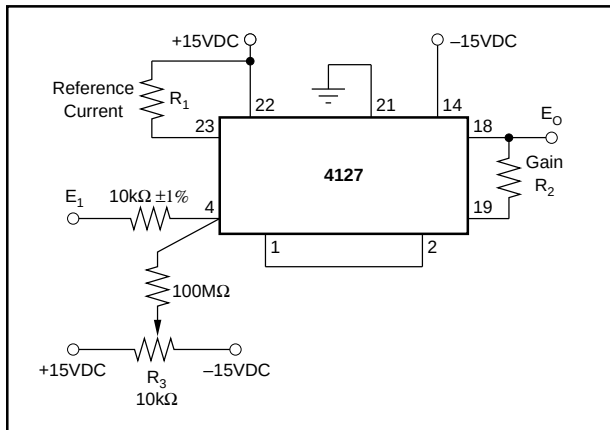


FIGURE 4. Transfer Function When E_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_O = 0$.
3. Apply $E_1 = E_{MAX}$, adjust R_2 for the proper output voltage.

4. Apply $E_1 = E_{MIN}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_O = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current (see Figure 5).

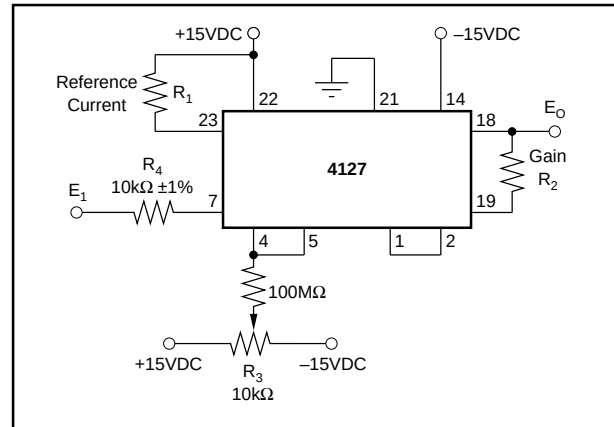


FIGURE 5. Transfer Function When E_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_O = 0$.
3. Apply $|E_1| = E_{MAX}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{MIN}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_O = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA$, $|I_2| \geq 1\mu A$ (see Figure 6).

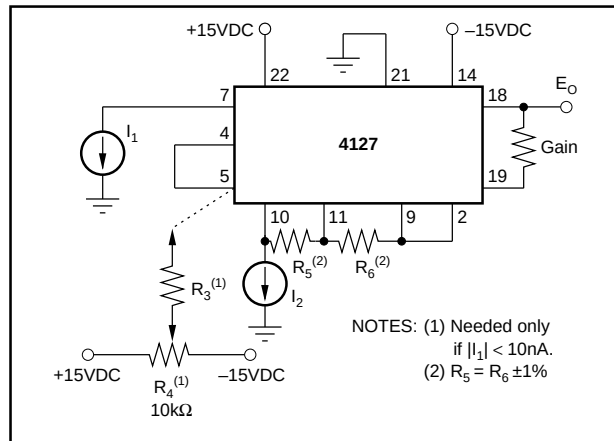


FIGURE 6. Transfer Function When I_1 and I_2 are Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $I_{1\text{ MIN}} \geq 10\text{nA}$, otherwise connect the R_3 and R_4 network, with $R_4 = 10\text{k}\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm 5\text{mV}$, it is not practical to use a T-network to replace R_3 .

Transfer function is $E_o = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1\text{nA}$, $I_2 \geq 1\mu\text{A}$ (see Figure 7).

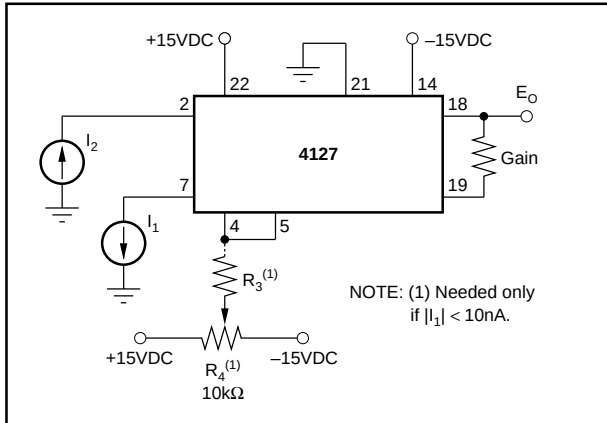


FIGURE 7. Transfer Function When I_1 is Negative, I_2 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $|I_1|_{\text{MIN}} \geq 10\text{nA}$, otherwise connect the R_3 and R_4 network, with $R_4 = 10\text{k}\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm 5\text{mV}$, it is not practical to use a T-network to replace R_3 .

Transfer function is $E_o = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1\text{nA}$, $I_2 \geq 1\mu\text{A}$ (see Figure 8).

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $I_{1\text{ MIN}} \geq 10\text{nA}$, otherwise connect the R_3 and R_4 network, with $R_4 = 10\text{k}\Omega$ and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the

range of $\pm 5\text{mV}$, it is not practical to use a T-network to replace R_3 .

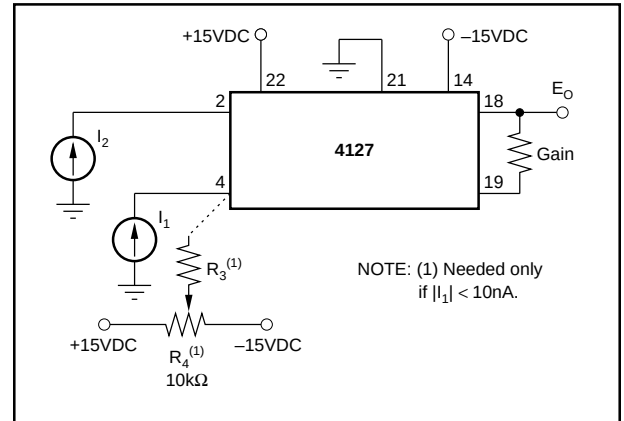


FIGURE 8. Transfer Function When I_1 and I_2 is Positive.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor, R_o , into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 9.

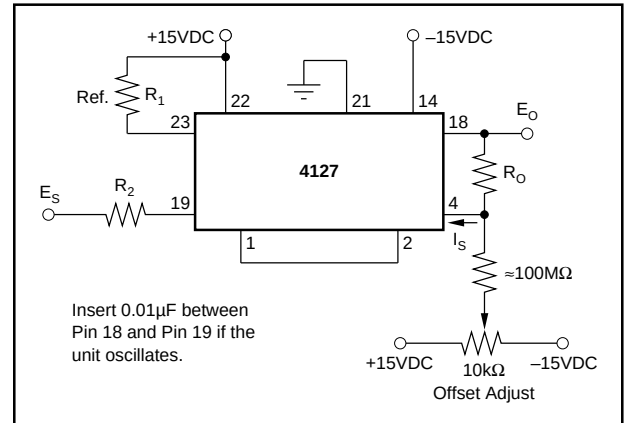


FIGURE 9. Antilog Operation.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A_2 must equal E_2 , so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, R_T \approx 520\Omega$$

Since the output is connected through R_o to pin 4, the current I_s will equal E_o/R_o and E_2 will be

$$E_2 = -\frac{mKT}{q} \ln \frac{E_o}{R_o I_R}$$

Combining expressions for E_2 gives the relationship:

$$\frac{R_T}{R_T + R_2} E_S = - \frac{mKT}{q} \ln \frac{E_O}{R_O I_R}$$

$$- \frac{E_S}{A} = \log \frac{E_O}{R_O I_R}$$

where:

$$A \approx \frac{R_T + R_2}{R_T} (26\text{mV}) \frac{1}{0.434}$$

$$E_O = R_O I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_O and I_R will set the scale factor. For example, an R_O of $1\text{M}\Omega$ and I_R of $1\mu\text{A}$ will give a scale factor of unity

and $E_O = \text{Antilog} - \frac{E_S}{A}$

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
4127JG	NRND	CDIP	JNA	24		TBD	Call TI	Call TI
4127KG	NRND	CDIP	JNA	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated