



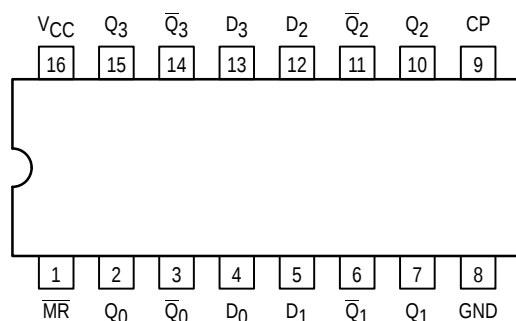
MC54/74F175

QUAD D FLIP-FLOP

The MC54/74F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where both true and complementary outputs are required and clock and clear inputs are common to all flip-flops. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- Four Edge-triggered D-type Inputs
- Buffered Positive Edge-triggered Common Clock
- Buffered Asynchronous Common Reset
- True and Complementary Outputs
- ESD > 4000 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



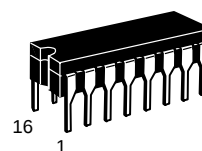
FUNCTION TABLE

Inputs	Outputs	
@ t_{H} , $\overline{\text{MR}} = \text{H}$	@ $t_{\text{H}} + 1$	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

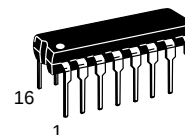
t_{H} = Bit time before clock positive-going transition
 $t_{\text{H}} + 1$ = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

QUAD D FLIP-FLOP

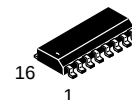
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

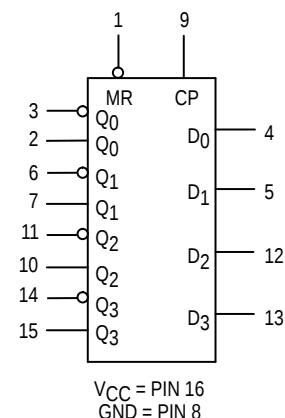


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

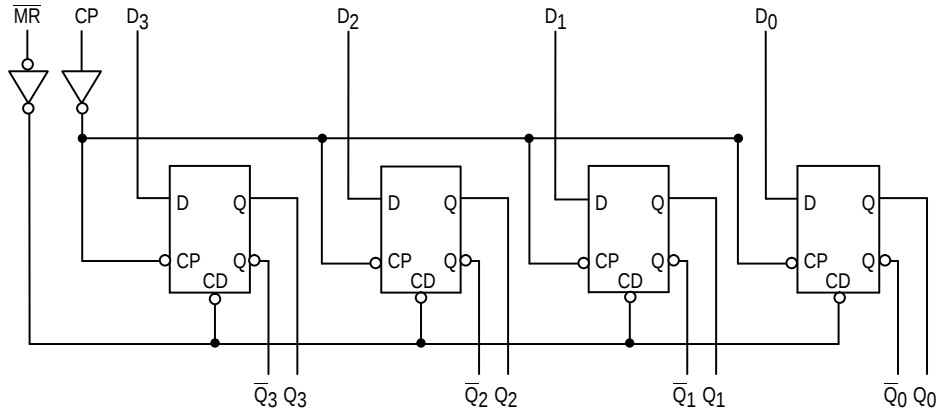
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F175

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\bar{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs, one setup time before, on the LOW-to-HIGH clock (CP) transition, causing individual Q and

$\bar{Q}$ outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and $\bar{Q}$ outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18 \text{ mA}$	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 4.50 \text{ V}$
		74	2.7	3.4	V	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 4.75 \text{ V}$
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 20 \text{ mA}$	$V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7 \text{ V}$	$V_{CC} = \text{MAX}$
				100	μA	$V_{IN} = 7.0 \text{ V}$	$V_{CC} = \text{MAX}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5 \text{ V}$	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0 \text{ V}$	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current		22.5	34	mA	$D_n = \bar{MR} = 4.5 \text{ V}$ $CP = \text{ } \int$	$V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F175

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = −55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		100		100		MHz
t _{PLH}	Propagation Delay	3.5	5.0	6.5	3.5	8.5	3.5	7.5	ns
t _{PHL}	CP to Q _n or $\overline{Q}_n$	4.0	6.5	8.5	4.0	10.5	4.0	9.5	
t _{PHL}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.5	9.0	11.5	4.5	15	4.5	13	ns
t _{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	4.0	6.5	8.5	4.0	10	4.0	9.0	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = −55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns
t _S (L)	D _Ń to CP	3.0			3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0			1.0		1.0		
t _H (L)	D _Ń to CP	1.0			1.0		1.0		ns
t _W (H)	CP Pulse Width, HIGH	4.0			4.0		4.0		
t _W (L)	or LOW	5.0			5.0		5.0		
t _W (L)	$\overline{\text{MR}}$ Pulse Width, LOW	5.0			5.0		5.0		ns
t _{rec}	Recovery Time, $\overline{\text{MR}}$ to CP	5.0			5.0		5.0		ns