# UCS3205

## 5A, 22V Bidirectional Load Switch with Fast Role Swap

### Features

- Integrated N-Channel Load Switch
- Fast Role Swap Capability that meets the USB Power Delivery Specification Requirements
- 2.85 to 22V Bidirectional Load Switch Input Voltage Range (supply voltage can be $V_{IN}$ or $V_{OUT}$)
- 5A Continuous Current
- 30 mΩ Typical On Resistance
- Configurable Current Limit Threshold with External Resistor
- Scaled Analog Voltage Output of Current Flowing through Switch for External Measurement
- Auto-Recovery Fault Handling or Latch Mode
- Configurable Overvoltage Lockout
- Back-Voltage Protection
- Output Voltage Slew Rate Control
- Configurable Quick Output Discharge
- Overtemperature Protection (thermal shutdown)
- Packages: 19-Lead 3 x 3 x 0.9 mm VQFN

### Applications

- USB Power Delivery
- Consumer, Industrial and Automotive Power Protection

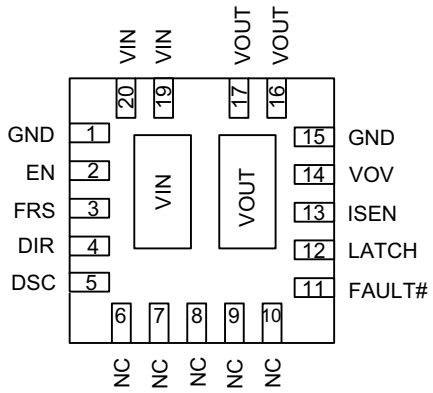
### Description

The UCS3205 is 5A, 22V load switch with Fast Role Swap (FRS) capability, bidirectional current capability, configurable overcurrent limiting, auto-recovery Fault handling, overvoltage lockout, back-voltage protection, slew rate control, quick output discharge and a scaled analog output of the forward current passing through the switch.

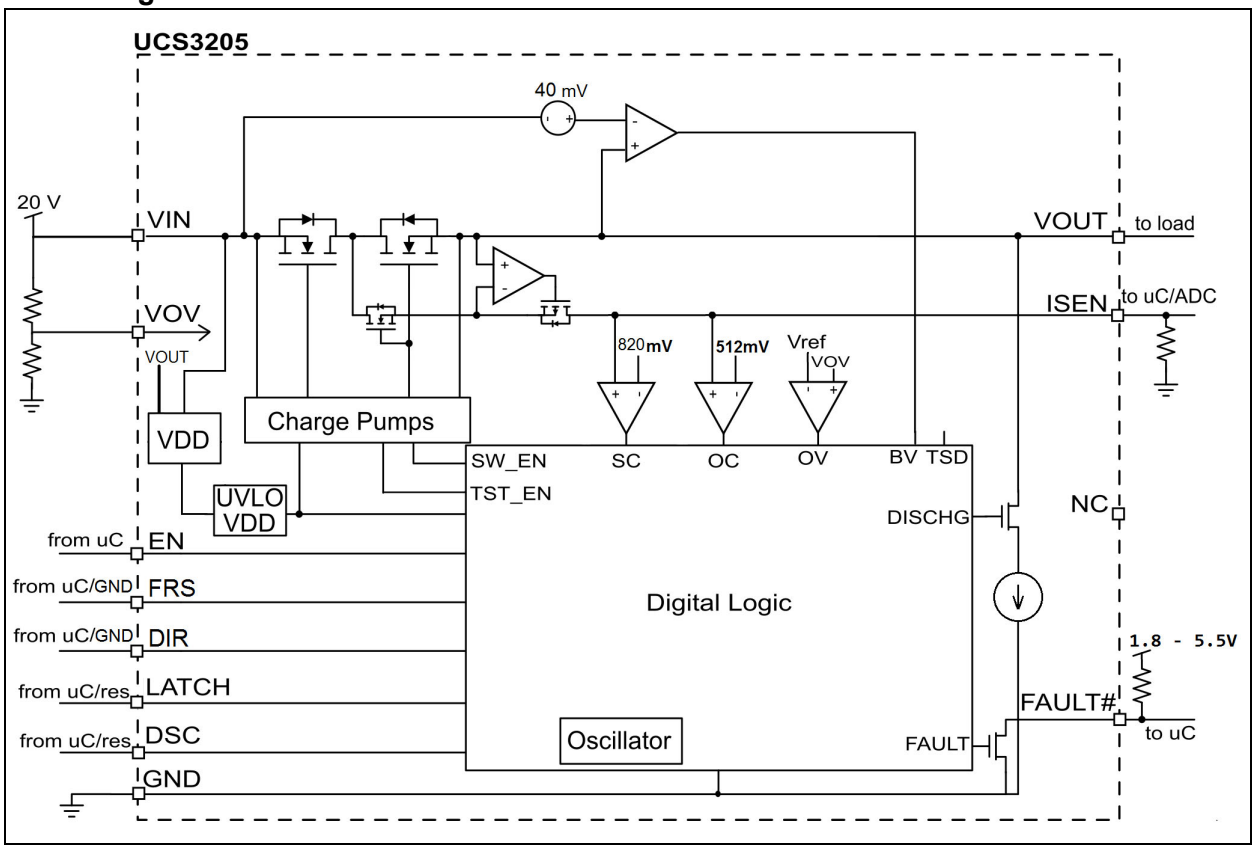
### Package Type

**UCS3205**

19-Lead 3 x 3 x 0.9 mm VQFN



## Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings†

Voltage on VIN and VOUT Pins ..... -0.3V to 25V
FAULT# Pin Pull-up Voltage ($V_{PULLUP}$) ..... -0.3V to 6V
Port Power Switch Current ..... Internally Limited
Voltage on Any Other Pin to Ground ..... -0.3V to 6V
Current on the FAULT# Pin ..... 10 mA
Operating Junction Temperature ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Package Power Dissipation ..... 67°C/W
ESD Protection on VIN, VOUT, GND Pins (IEC 61000-4-2) ..... ±15 kV
ESD Protection on VIN, VOUT, GND Pins (JEDEC JESD22-A114; Human Body Model) ..... ±6 kV
ESD Protection on All Other Pins (JEDEC JESD22-A114; Human Body Model) ..... ±2 kV
ESD Protection on All Pins (JEDEC JESD22-C101; Charge Device Model) ..... ±500V

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Specifications**: Unless otherwise indicated, $T_A$ = +25°C, $V_{IN}$ or $V_{OUT}$ = 2.85V to 22V.

| Characteristic | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Power and Interrupts – DC | | | | | | |
| Minimum Start-up Supply Voltage | $V_{IN\_STRT}$ | 3.1 | — | — | V | |
| Minimum Supply Voltage After Start-up | $V_{IN}$ | 2.85 | — | — | V | |
| Minimum Start-up Supply Voltage | $V_{OUT\_STRT}$ | 3.1 | — | — | V | |
| Minimum Supply Voltage After Start-up | $V_{OUT}$ | 2.85 | — | — | V | |
| Quiescent Current | $I_Q$ | — | 200 | 260 | µA | Current measured into VIN or VOUT when current out of VOUT or VIN, respectively, is 0A, EN = ‘high’ |
| Shutdown Current | $I_{SD}$ | — | 20 | 30 | µA | Current measured in the VIN pin when EN and DSC pins are ‘low’ |

**Note 1:** This parameter is characterized, not 100% tested.
**2:** This parameter is ensured by design.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications**: Unless otherwise indicated, $T_A$ = +25°C, $V_{IN}$ or $V_{OUT}$ = 2.85V to 22V.

| Characteristic | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Power-on Reset | | | | | | |
| VIN, VOUT Undervoltage Lockout Threshold | $V_{UV\_HIGH}$ | 2.25 | — | 2.45 | V | |
| VIN, VOUT Undervoltage Lockout Threshold | $V_{UV\_LOW}$ | 2.05 | — | 2.24 | V | |
| VIN, VOUT Undervoltage Lockout Hysteresis | $V_{UVLO\_HYS}$ | — | 150 | — | mV | |
| I/O Pins – FRS, DIR, EN, LATCH, DSC, FAULT#, VOV | | | | | | |
| Output Low Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{SINK\_IO}$ = 8 mA, FAULT# |
| Input High Voltage | $V_{IH}$ | 1.26 | — | — | V | EN, LATCH, DSC, FRS, DIR |
| Input Low Voltage | $V_{IL}$ | — | — | 0.54 | V | EN, LATCH, DSC, FRS, DIR |
| Leakage Current | $I_{LEAK}$ | — | — | ±10 | µA | Powered or unpowered, $V_{PULLUP}$ ≤ (1.8V-5.5V) (**Note 1**) |
| Overvoltage Sense Threshold | $V_{OV}$ | 1.225 | 1.25 | 1.275 | V | |
| Switch Turn-On Delay for FRS | $t_{FRS\_SWAP}$ | — | — | 60 | µs | $V_{IN}$ = 5V, $C_{IN}$ = 100 µF, $C_{OUT}$ = 10 µF, $V_{OUT}$ ≥ 90% of $V_{IN}$ (**Note 1**) |
| FRS Pre-Arm Ready Time | $t_{FRS\_PREARM}$ | — | 200 | 270 | µs | Minimum FRS hold time before EN = 1, $V_{IN}$ > $V_{UV\_HIGH}$ |
| Digital Input Deglitch Time | $t_{DIG\_HOLD}$ | — | 20 | — | µs | Digital input hold time to be asserted |
| Interrupt Pins – AC Parameters | | | | | | |
| Start-up FAULT# Blanking Time | $t_{FAULT}$ | 2.5 | 2.6 | 2.7 | ms | Blanking time, coming out of Reset (**Note 2**) |
| FAULT# Pin Overcurrent Masking Time | $t_{MASK}$ | 8 | 10 | 12 | ms | USB PD required masking time |
| FAULT# Pulse Width | $t_{FAULT\_ACK}$ | 40 | 51 | 65 | ms | Minimum time for FAULT# pin to remain set to 'low' |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is ensured by design.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications**: Unless otherwise indicated, $T_A$ = +25°C, $V_{IN}$ or $V_{OUT}$ = 2.85V to 22V.

| Characteristic | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| ISEN Pin | | | | | | |
| Configurable Current Limit | $I_{LIM}$ | 1.59 | 1.71 | 1.83 | A | $R_{ILIM}$ = 1.5 kΩ, see calculation in **Section 4.2 "Overcurrent Detection"** for other $I_{LIM}$ values |
| Current Limit Accuracy | $I_{ACCY}$ | — | — | ±7 | % | See calculation in **Section 4.2 "Overcurrent Detection"** for $I_{LIM}$ values **(Note 2)** |
| Current Limit Resistor | $R_{ILIM}$ | 450 | — | 5000 | Ω | |
| **Port Power Switch** | | | | | | |
| Port Power Switch – DC Parameter | | | | | | |
| On Resistance | $R_{DS\_ON}$ | — | 30 | 40 | mΩ | $V_{IN}$ = 5V, $I_{OUT}$ = 2A |
| VOUT Leakage Current | $I_{LEAK\_VOUT}$ | — | — | 5 | µA | $V_{IN}$ = 22V, current flowing out the VOUT pin when EN is pulled down, $V_{OUT}$ = 0V |
| Back-Voltage Fault Protection Threshold | $V_{BV\_FAULT\_ON}$ | 20 | 30 | 50 | mV | $V_{OUT} > V_{IN}$, $V_{IN} > V_{UVLO}$ |
| Back-Voltage FRS Active Threshold | $V_{BV\_FAULT\_OFF}$ | 1 | 20 | 35 | mV | $V_{IN} > V_{UVLO}$, switch turned on when $(V_{OUT} - V_{IN}) < V_{BV\_FAULT\_OFF}$ |
| Back-Drive Current | $I_{BD\_1}$ | — | 0 | 5 | µA | $V_{IN} < V_{UVLO}$, EN = 0V, current flowing between VIN and GND when the VOUT pin is connected to a 20V supply **(Note 2)** |
| Forward Leakage | $I_{BD\_2}$ | — | 0 | 10 | µA | DIR = 1, $V_{IN} > V_{UVLO}$, EN = 0V, current flowing between VIN and GND when the VOUT pin is connected to a 20V supply **(Note 2)** |
| Thermal Shutdown Threshold | $T_{TSD}$ | — | 145 | — | °C | Die temperature at which the power switch will turn off |
| Thermal Shutdown Hysteresis | $T_{TSD\_HYST}$ | — | 20 | — | °C | After shutdown, due to $T_{TSD}$ being reached, die temperature drop required before the power switch can be turned on again |
| Discharge Thermal Shutdown Threshold | $T_{DSC\_TSD}$ | — | 165 | — | °C | Die temperature at which the discharge switch will turn off |
| Discharge Current | $I_{DISCHG}$ | — | 150 | — | mA | |
| Slew Rate | SR | — | 20 | — | V/ms | |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is ensured by design.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications**: Unless otherwise indicated, $T_A$ = +25°C, $V_{IN}$ or $V_{OUT}$ = 2.85V to 22V.

| Characteristic | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Port Power Switch – AC Parameters | | | | | | |
| Minimum Start-up Time | $t_{STRT\_EN}$ | 60 | — | — | ms | Minimum time from $V_{IN\_STRT} \geq 3.1V$ to an EN low-to-high transition |
| Start-up Current Limit Duration | $t_{STRT\_CLD}$ | — | 2.5 | — | ms | Time from $V_{IN} > V_{UVLO}$ until short circuit and overcurrent comparator are enabled (slew rate control enabled), EN = 1 **(Note 1)** |
| Turn-On Delay | $t_{ON\_SW}$ | — | 0.5 | — | ms | Time from the transition of EN from low-to-high until switch is on ($V_{OUT}$ > 500 mV), $C_{OUT}$ = 10 µF, DIR = 1, time from the transition of EN from low-to-high until switch is on ($V_{IN}$ > 500 mV), $C_{IN}$ = 10 µF |
| Turn-Off Delay | $t_{OFF\_SW}$ | — | 150 | 230 | µs | Time from the transition of EN from high-to-low until switch is off ($V_{OUT} < V_{IN}$ – 500 mV), $V_{IN}$ = 5V, DIR = 0, DSC = 1, no $C_{OUT}$, time from the transition of EN from high-to-low until switch is off, ($V_{IN} < V_{OUT}$ – 500 mV), $V_{OUT}$ = 5V, $R_{IN}$ = 50Ω, DIR = 1, 50 kΩ to GND on VIN, no $C_{IN}$ |
| Charge Time | $t_{CHARGE}$ | — | 1 | — | ms | Time from the transition of EN from low-to-high until $V_{OUT}$ = 19V (95% of $V_{IN}$ = 20V) with $R_{ILIM}$ = 1.5kΩ, $C_{OUT}$ = 10 µF **(Note 1)** |
| Discharge Time | $t_{OUT\_DISCHARGE}$ | — | 2 | — | ms | Time from the transition of EN from high-to-low until $V_{OUT}$ = 0.8V ($V_{IN}$ = 20V), $C_{OUT}$ = 10 µF, DSC = 1 **(Note 1)** |
| OC Turn-Off Time | $t_{OFF\_SW\_OC}$ | — | 10 | — | µs | Time from overcurrent event (current less than short-circuit limit) to switch off after $t_{MASK}$ elapses (10 ms), $C_{OUT}$ = 10 µF |
| Turn-Off Time | $t_{OFF\_SW\_ERR}$ | — | 7 | — | µs | Time from TSD, OV, BV, SC event to switch off, no $C_{OUT}$ **(Note 1)** |
| VIN or VOUT Output Rise Time | $t_{R\_IN\_OUT}$ | — | 0.8 | — | ms | Measured from 10% to 90% of $V_{OUT}$ ($V_{IN}$ = 20V), $C_{OUT}$ = 10 µF with $R_{ILIM}$= 1.5 kΩ, 20 V/ms slew rate, measured from 10% to 90% of $V_{IN}$ ($V_{OUT}$ = 20V), $C_{IN}$ = 10 µF |
| Short Circuit FAULT# Assertion Time | $t_{SHORT\_FAULT}$ | — | 20 | — | µs | Time from detection of short to port power switch disconnect and FAULT# pin assertion |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is ensured by design.

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications**: Unless otherwise indicated, $T_A$ = +25°C, $V_{IN}$ or $V_{OUT}$ = 2.85V to 22V.

| Characteristic | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Auto-Retry Time | $t_{RETRY}$ | — | 51 | — | ms | Time delay before Fault condition check |
| Maximum Discharge Time | $t_{DISCHARGE}$ | — | 50 | 60 | ms | Amount of time discharge internal current source applied ($I_{DISCHG}$), DSC = 1, internal 50 kΩ equivalent current source applied when DSC = 1 **(Note 1)** |

**Note 1:** This parameter is characterized, not 100% tested.

**2:** This parameter is ensured by design.

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated: $T_A$ = +25°C, $V_{IN}$ = 20V, $V_{EN}$ = 5V, $V_{OUT}$ = 20V, $I_{OUT}$ = 2A, $C_{IN}$ = 100 µF, $C_{OUT}$ = 10 µF.

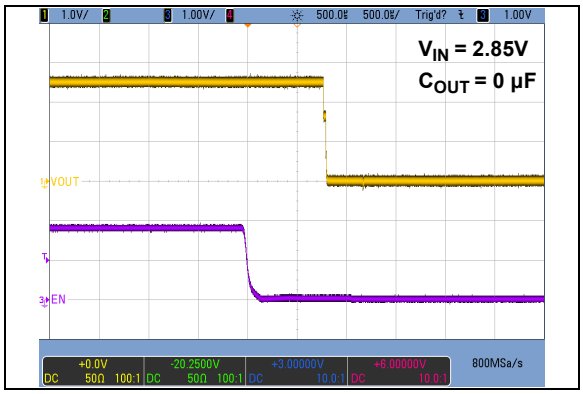



***FIGURE 2-1:*** *$V_{OUT}$ Fall Time.*

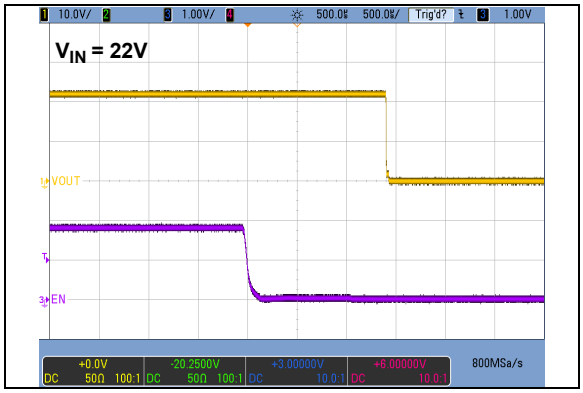



***FIGURE 2-2:*** *$V_{OUT}$ Fall Time.*


***FIGURE 2-3:*** *Overcurrent Fault Response Delay Time.*

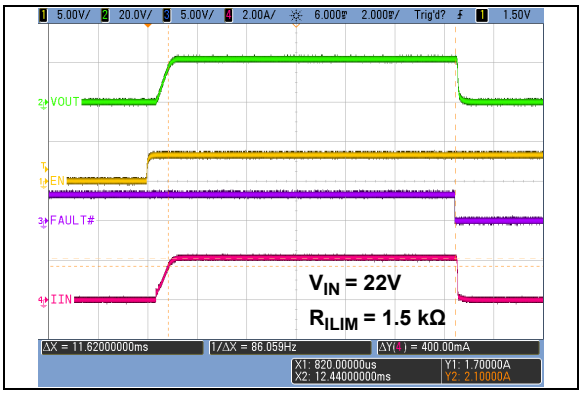



***FIGURE 2-4:*** *Overcurrent Fault Response Delay Time.*

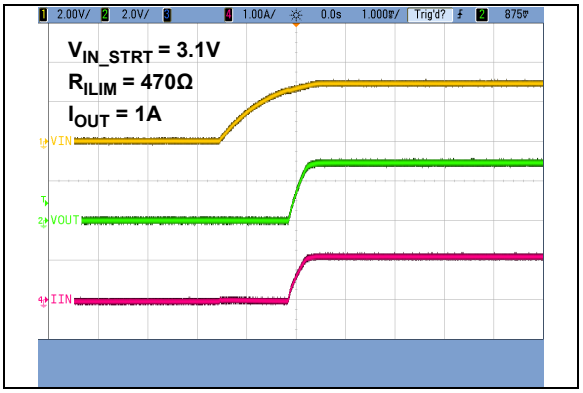



***FIGURE 2-5:*** *Soft Start Turn-On.*

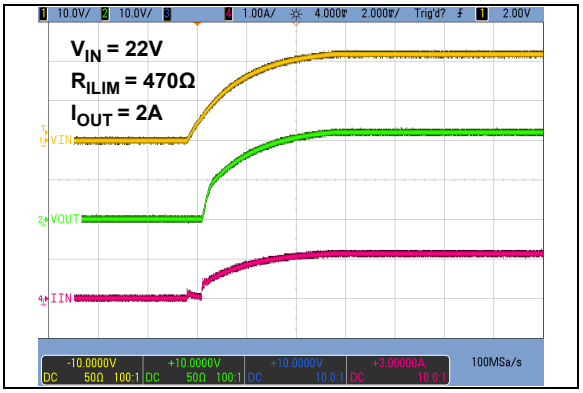



***FIGURE 2-6:*** *Soft Start Turn-On.*

**Note:** Unless otherwise indicated: $T_A$ = +25°C, $V_{IN}$ = 20V, $V_{EN}$ = 5V, $V_{OUT}$ = 20V, $I_{OUT}$ = 2A, $C_{IN}$ = 100 µF, $C_{OUT}$ = 10 µF

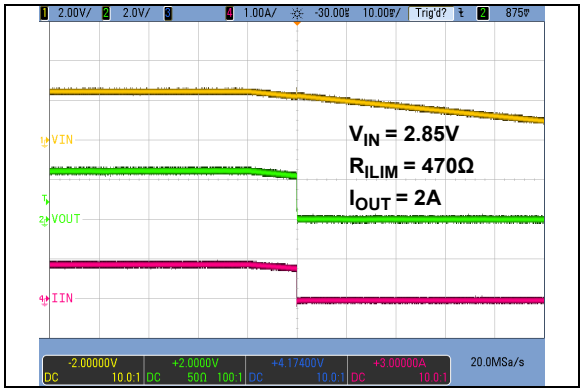



***FIGURE 2-7:*** *Soft Start Turn-Off.*

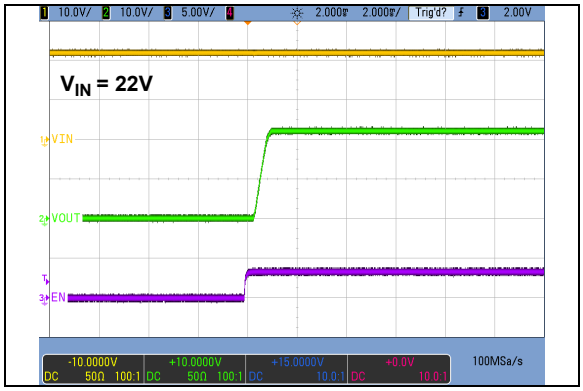



***FIGURE 2-10:*** *Turn-On with Enable.*

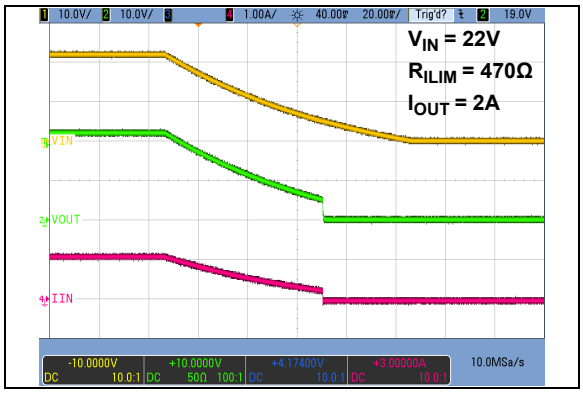



***FIGURE 2-8:*** *Soft Start Turn-Off.*


***FIGURE 2-11:*** *Turn-Off with Enable.*

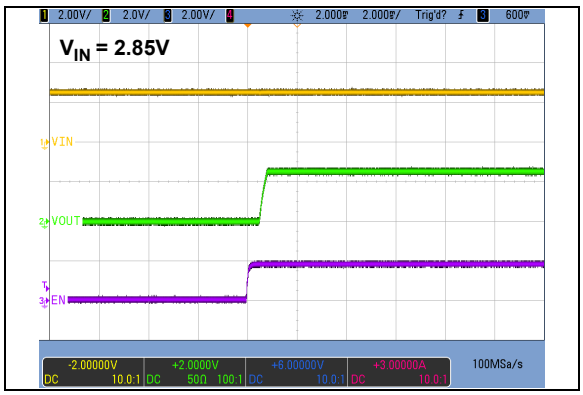



***FIGURE 2-9:*** *Turn-On with Enable.*


***FIGURE 2-12:*** *Turn-Off with Enable.*

**Note:** Unless otherwise indicated: $T_A$ = +25°C, $V_{IN}$ = 20V, $V_{EN}$ = 5V, $V_{OUT}$ = 20V, $I_{OUT}$ = 2A, $C_{IN}$ = 100 µF, $C_{OUT}$ = 10 µF.

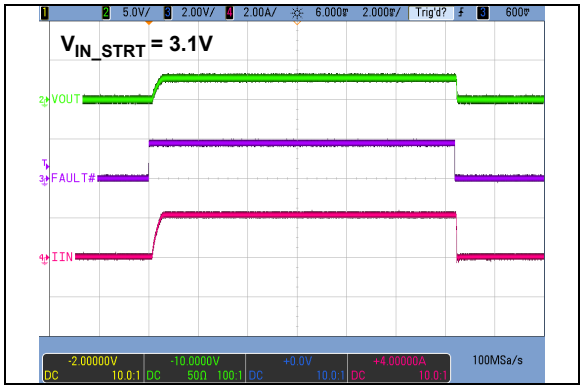



***FIGURE 2-13:*** *Turn-On Into 20% Overload.*

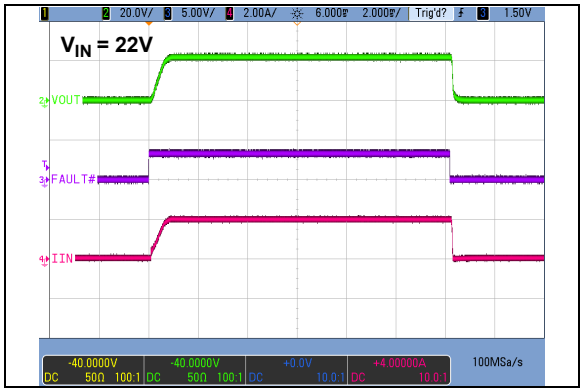



***FIGURE 2-14:*** *Turn-On Into 20% Overload.*

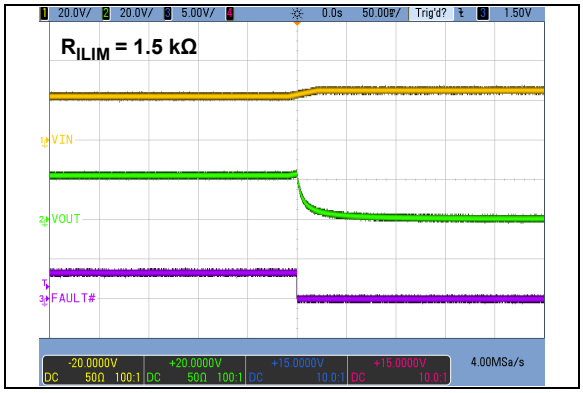



***FIGURE 2-15:*** *$V_{IN}$ Overvoltage.*


***FIGURE 2-16:*** *Output Recovery from Short Circuit.*

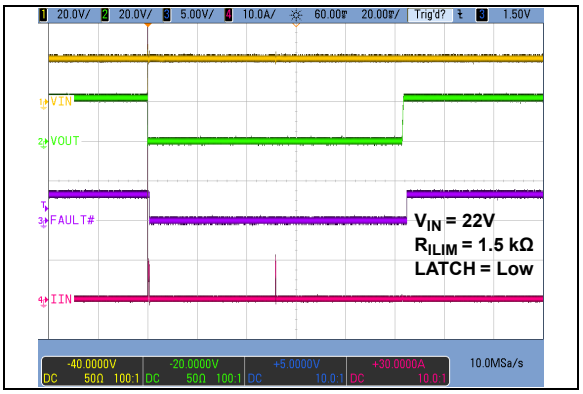



***FIGURE 2-17:*** *Output Recovery from Short Circuit.*

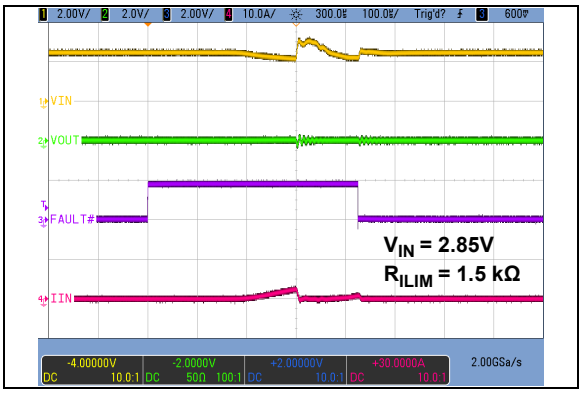



***FIGURE 2-18:*** *Turn-On into Short to GND.*

**Note:** Unless otherwise indicated: $T_A$ = +25°C, $V_{IN}$ = 20V, $V_{EN}$ = 5V, $V_{OUT}$ = 20V, $I_{OUT}$ = 2A, $C_{IN}$ = 100 µF, $C_{OUT}$ = 10 µF.

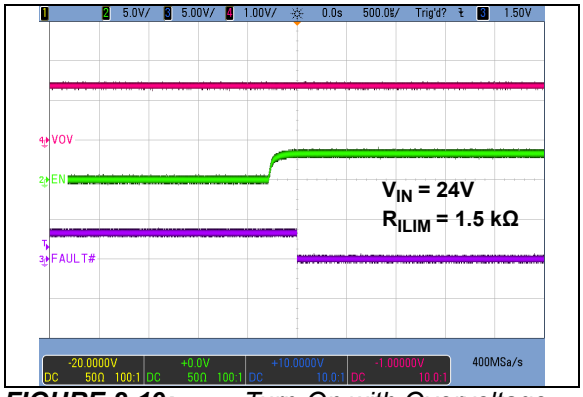



***FIGURE 2-19:*** *Turn-On with Overvoltage on $V_{IN}$.*

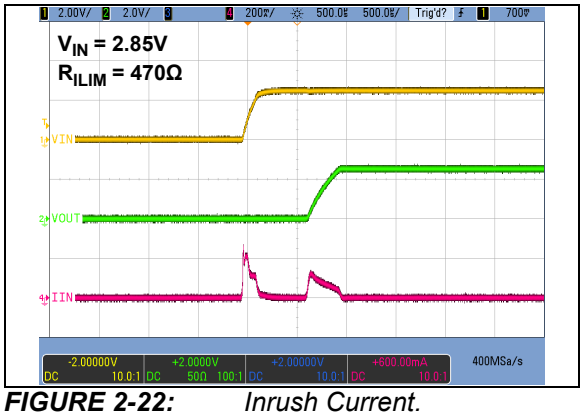



***FIGURE 2-22:*** *Inrush Current.*

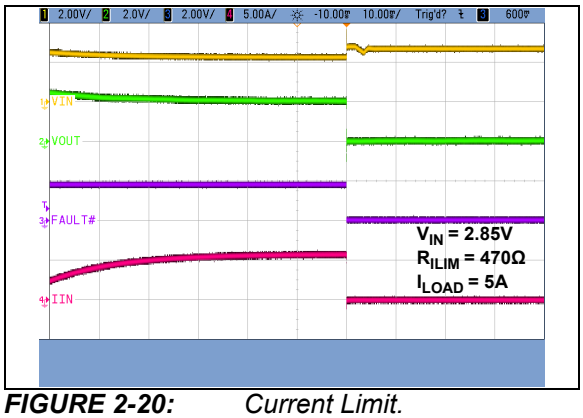



***FIGURE 2-20:*** *Current Limit.*

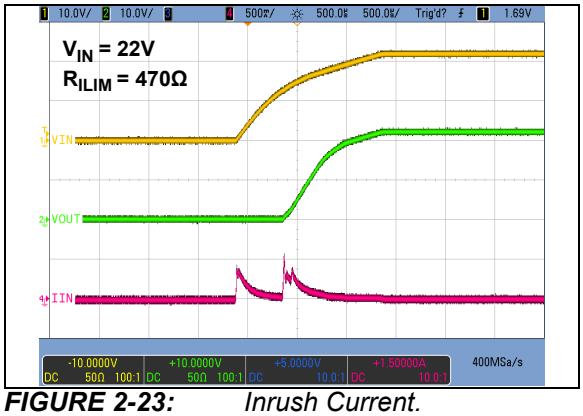



***FIGURE 2-23:*** *Inrush Current.*

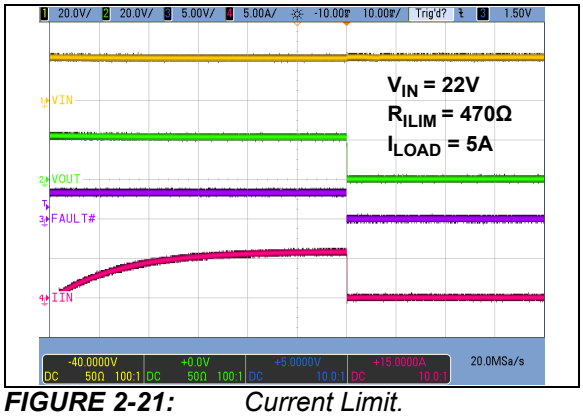



***FIGURE 2-21:*** *Current Limit.*

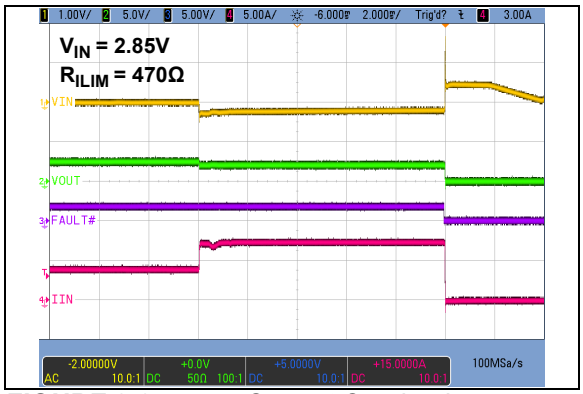



***FIGURE 2-24:*** *Current Overload Response.*

**Note:** Unless otherwise indicated: $T_A$ = +25°C, $V_{IN}$ = 20V, $V_{EN}$ = 5V, $V_{OUT}$ = 20V, $I_{OUT}$ = 2A, $C_{IN}$ = 100 µF, $C_{OUT}$ = 10 µF.

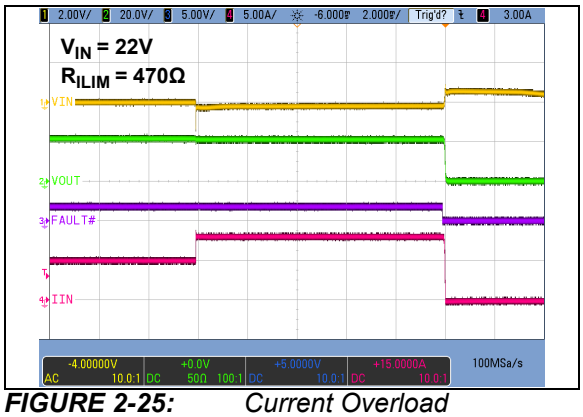



***FIGURE 2-25:*** *Current Overload Response.*

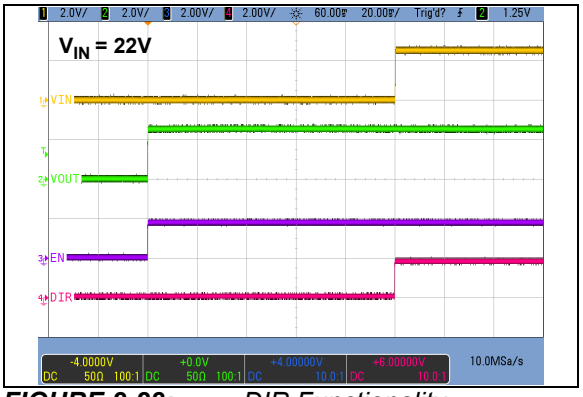



***FIGURE 2-28:*** *DIR Functionality.*

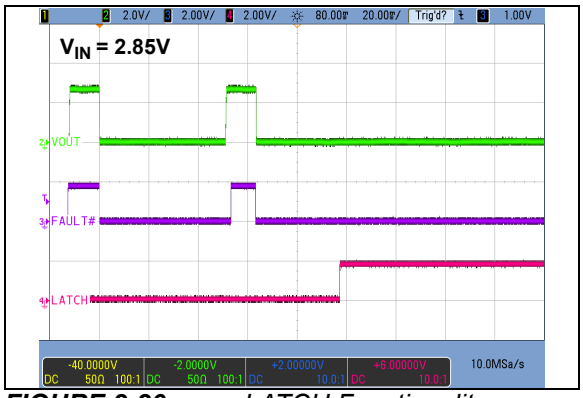



***FIGURE 2-26:*** *LATCH Functionality.*

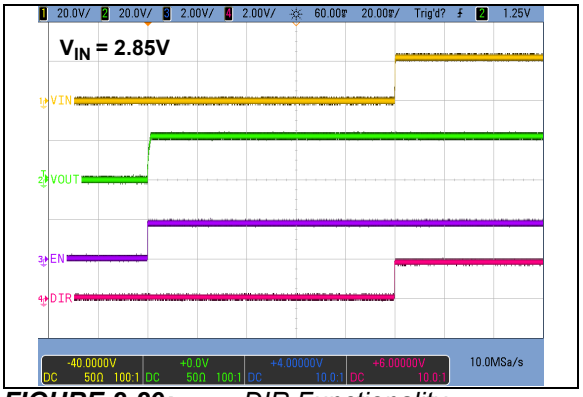



***FIGURE 2-29:*** *DIR Functionality.*

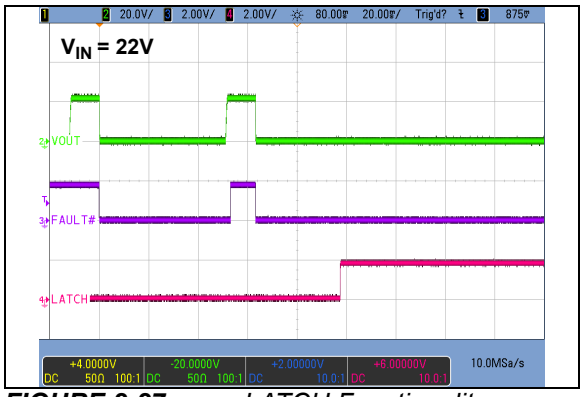



***FIGURE 2-27:*** *LATCH Functionality.*

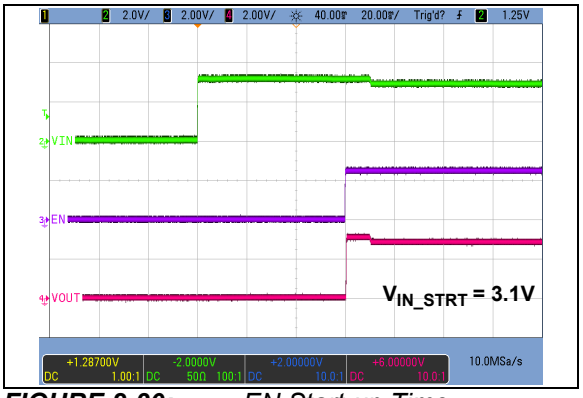



***FIGURE 2-30:*** *EN Start-up Time.*

## 3.0 PIN DESCRIPTION

Table 3-1 describes the function of each pin as related to the proposed pinout.

**TABLE 3-1: PIN DESCRIPTION TABLE**

| Pin | Sym | Pin Type | Description |
|---|---|---|---|
| 1,15 | GND | Ground | Ground for the power supply and the load switch. |
| 2 | EN | Digital Input | The power switch is enabled when this pin is pulled high. |
| 3 | FRS | Digital Input | Fast Role Swap control input. This pin enables the circuitry for supporting the Fast Role Swap behavior defined in the USB Power Delivery Specification. |
| 4 | DIR | Digital Input | Current direction control input. When this pin is high, the reverse current blocking protection is disabled, allowing the current to flow through the switch in the opposite direction. |
| 5 | DSC | Digital Input | The triggered output discharge is enabled when this pin is high. |
| 6,7,8,9,10 | NC | **No Connect** | No Connect. **These pins MUST be left floating.** |
| 11 | FAULT# | Open-Drain Output | A Logic Low state indicates a Fault condition. This pin requires an external pull-up resistor. |
| 12 | LATCH | Digital Input | If low, the UCS3205 will attempt to restart after a Fault condition (Auto-Retry mode). If high, the device will latch off when a Fault condition is detected, and will not attempt to restart until EN is cycled off and on. |
| 13 | ISEN | Analog Output | This pin is a scaled analog output of the current passing through the switch. It requires an external resistor, which sets the current limit threshold. This pin can be connected to external measurement or detection circuitry, such as ADC, comparator or an MCU. |
| 14 | VOV | Analog Input | Overvoltage threshold setting pin. Connect to a resistor divider from VIN. |
| VOUT Exposed Pad, 16,17 | VOUT | High Power | Load switch output. |
| VIN Exposed Pad, 19,20 | VIN | High Power | Load switch input. |

## 4.0 FUNCTIONAL DESCRIPTION

The UCS3205 is a single-channel load switch with highly integrated load protection for applications up to 22V.

The device protects the power supply with its configurable current limit feature. The current limit threshold is set with an external resistor. The same pin can be connected to external measurement or detection circuitry, such as an ADC, comparator or MCU, eliminating the need for a shunt in the power path.

The UCS3205 protects the load from being supplied by voltages higher than intended (overvoltage lockout). It also has a thermal shutdown circuit, which will shut the switch off when junction temperature exceeds the limit.

The device implements Fast Role Swap (FRS) capability and reverse current blocking that can be disabled via the DIR pin, allowing it to work as a bidirectional switch depending on the application requirements. **The device's DIR pin is normally grounded for Fast Role Swap applications. The FRS pin is normally grounded for bidirectional current flow applications.**

This device can be programmed to either latch off or retry in the event of a Fault.

### 4.1 Mode Control

Figure 4-1 shows the UCS3205 state diagram.

#### 4.1.1 RESET MODE

When the UCS3205 is in the Reset state, the device is in its lowest current consumption state. The port power switch is off. The FAULT# pin is not asserted. If the FAULT# pin is asserted prior to entering Reset state, it will be released. When in Reset mode, a low-to-high transition on the EN pin will start the transition of the UCS3205 to its next state. If there are no Faults detected and $t > t_{STRT\_CLD}$ has elapsed, the UCS3205 will transition into the Operating state. If there is an Overvoltage, Back-Voltage, Short-Circuit, Overcurrent, or Thermal Shutdown Fault, the device will transition into the Fault state.

#### 4.1.2 OPERATING MODE

In order for the UCS3205 to enter Operating mode, $V_{IN}/V_{OUT}$ must be above $V_{IN\_STRT}/V_{OUT\_STRT}$ for $t_{STRT\_EN}$, before the low-to-high transition on EN, before turning on the switch can take place. Once the switch is on, the $V_{IN}$ voltage can be decreased to 2.85V. Whenever the UCS3205 is in Operating mode, the port power switch will be on. In this case, the FAULT# pin is not asserted. If the FAULT# pin is asserted prior to entering Reset state, it will be released. The UCS3205 cannot be in the Operating state if any of the following conditions exist:

- Overvoltage, Short-Circuit, Overcurrent, Thermal Shutdown or Back-Voltage Fault
- $V_{IN} < V_{UV\_HIGH}$
- $EN < V_{IH}$

When in Operating mode, a high-to-low transition on the EN pin will make the UCS3205 transition into the Reset state. If any Fault conditions occur while in the Operating state, the UCS3205 will automatically transition into the Fault state.

#### 4.1.3 FAULT MODE

The UCS3205 automatically enters the Fault state from the Operating and Retry states when any of the following events are detected:

- An Overvoltage (OV) condition on the VIN pin (see **Section 4.4 "$V_{IN}$ Overvoltage Detection"**).
- A Short-Circuit (SC) condition (see **Section 4.3 "Short-Circuit Detection"**).
- An Overcurrent (OC) condition (see **Section 4.2 "Overcurrent Detection"**).
- Maximum allowable internal die temperature is exceeded – Thermal Shutdown (TSD) (see **Section 4.8 "Thermal Shutdown"**).
- A Back-Voltage (BV) condition (see **Section 4.7 "Back-Voltage Detection"**).

The UCS3205 enters the Fault state from the Reset state when there is a low-to-high transition on the EN pin and any of the following events are detected:

- Maximum allowable internal die temperature is exceeded
- Back-Voltage condition,
- Short-Circuit condition on the VOUT pin
- Overcurrent condition on the VOUT pin
- Overvoltage condition on the VIN pin

When the UCS3205 is in Fault mode, the port power switch will be off and the FAULT# pin is asserted.

#### 4.1.4 RETRY MODE

The only way for the UCS3205 to enter the Retry state is from the Fault state and the LATCH pin must be low. When the UCS3205 is in Retry mode, the port power switch will be on and the FAULT# pin is asserted (see Figure 4-5).

## 4.2 Overcurrent Detection

An OC (Overcurrent) signal is sent to the digital logic when the voltage on the ISEN pin exceeds $V_{SEN}$ = 0.512V. The value of the resistor that must be connected to the ISEN pin to set the current limit threshold can be calculated with the following equation:

**EQUATION 4-1: OVERCURRENT THRESHOLD**

$$R_{ILIM} = \frac{V_{SEN}}{\frac{I_{LIM}}{5000}} = \frac{0.512 \times 5000}{I_{LIM}}$$

For $I_{LIM\_MAX}$ = 5.5A (to allow 5A continuous current), the result is $R_{ILIM\_MAX}$ = 470Ω.

For $I_{LIM\_MIN}$ = 0.55A (to allow 0.5A continuous current), the result is $R_{ILIM\_MIN}$ = 4.7 kΩ.

## 4.3 Short-Circuit Detection

A SC (Short Circuit) signal is sent to the digital logic when the voltage on the ISEN pin exceeds $V_{SEN}$ = 0.820V. This corresponds to a current level that is 160% of $I_{LIM\_MAX}$.

The short-circuit current limit threshold can be calculated with the following equation:

**EQUATION 4-2: SHORT-CIRCUIT THRESHOLD**

$$I_{SC} = \frac{V_{SEN} \times 5000}{R_{ILIM}} = \frac{0.820 \times 5000}{R_{ILIM}}$$

Thus, for $I_{LIM\_MAX}$ = 5.5A ($R_{ILIM\_MAX}$ = 470Ω), the SC signal will be sent if the current exceeds 8.8A. For $I_{LIM\_MIN}$ = 0.55A ($R_{ILIM\_MIN}$ = 4.7 kΩ), the SC signal will be sent if the current exceeds 0.88A.

## 4.4 $V_{IN}$ Overvoltage Detection

An OV (Overvoltage) signal is sent to the digital logic when the voltage on the VOV pin is higher than $V_{REF}$ = 1.25V. The overvoltage threshold can be configured by selecting the resistor values of the voltage divider connected to VIN.

## 4.5 LATCH and DSC Functionality

The LATCH pin controls the retry function. If the LATCH pin is high at the time when a Fault is detected, the digital logic remains in a Fault state until the EN pin is toggled low-to-high and the Fault recovery procedure begins. If the LATCH pin is low, the device enters into Auto-Retry mode by running the Fault recovery procedure every $t_{RETRY}$, until no Fault condition is detected or until the EN pin is pulled low.

If the DSC pin is high and the switch is off, the UCS3205 discharges the output for the duration of $t_{DISCHARGE}$ unless the DSC pin is pulled low (the DSC pin overrides the discharge timer).

## 4.6 Fault and Enable Functionality for Combined Mode

Combined mode is implemented on HUBs that have a limited amount of pins in multiple port applications. To alleviate this, both the FAULT and EN pins of the UCS3205 are connected to PRTCTL of the HUB, which is internally pulled up.

The HUB must have enough time to Acknowledge a Fault. The UCS3205 will keep Fault asserted low for the duration of $t_{FAULT\_ACK}$ while EN is low (switched off).

## 4.7 Back-Voltage Detection

Back-voltage detection is only valid when the power switch is on (EN = 1). When the power switch is on (EN = 1) and the DIR pin is a logic '0', a BV (Back-Voltage) signal is sent to the digital logic when the output voltage (on the VOUT pin) is higher than the input voltage (on the VIN pin) by more than $V_{BV\_FAULT\_ON}$.

When the DIR pin is a logic '1', back-voltage detection is disabled, so the current through the switch is allowed to flow in either direction; from VIN to VOUT (forward direction) or from VOUT to VIN (reverse direction). The FRS pin of the UCS3205 must be grounded for applications where this functionality is needed. Please note, the UCS3205 does not monitor or limit the current in the reverse direction.

## 4.8 Thermal Shutdown

The thermal shutdown circuitry sends the Thermal Shutdown (TSD) signal to the digital logic when the die temperature exceeds $T_{TSD}$. It has a hysteresis of $T_{TSD\_HYST}$.

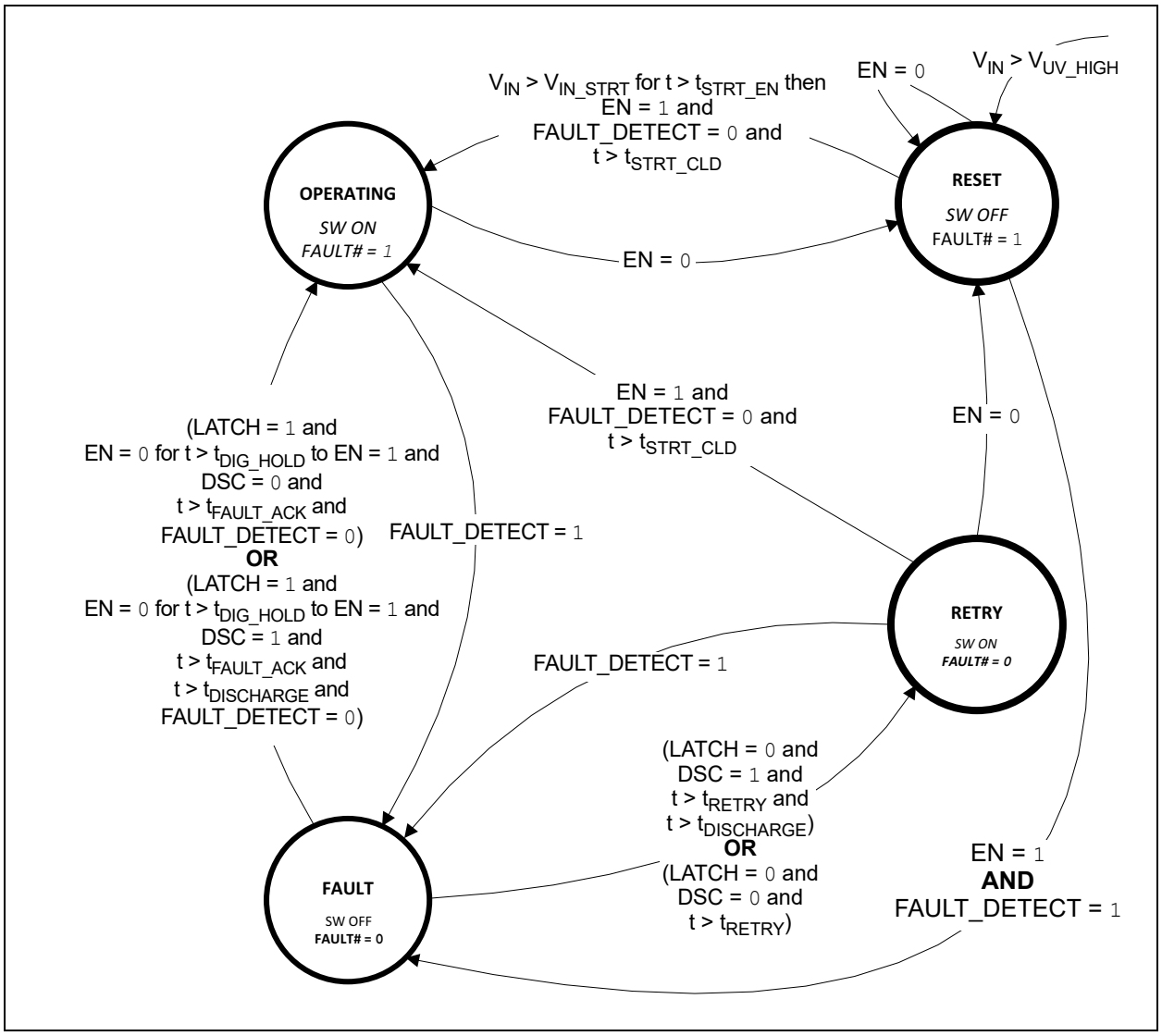



***FIGURE 4-1:*** *UC3205 State Diagram.*

## 4.9 Fast Role Swap (FRS)

The Fast Role Swap circuit enables the application to change the role of sinking current to sourcing current within the allowed time defined by the USB Power Delivery Specification. The FRS circuit is pre-enabled when the FRS pin is pulled high for the duration of $t_{FRS\_PREARM}$ and remains in this Ready state as long as the FRS pin remains high. All Fault protections remain active, but the FAULT# pin and associated Fault Handling states are not asserted unless EN = 1. Pre-enabling the FRS is valid only in a Reset state (EN = 0). A low-to-high FRS transition received while EN = 1 will not affect operation. If FRS = 1 and in a Reset state (EN = 0), the UCS3205 will then monitor the EN pin for a low-to-high transition. A low-to-high transition on EN will fully enable the FRS circuit and the switch will be turned on in $t_{FRS\_SWAP}$ after $V_{OUT}$ drops below $V_{IN}$. When $t_{FRS\_SWAP}$ elapses, the application's $V_{OUT}$ voltage will be above 90% of the $V_{IN}$ voltage. Any high-to-low transitions on the FRS pin are ignored during FRS conditions. A high-to-low transition on EN will turn off the switch and exit FRS. See Figure 4-2, Figure 4-3, and Figure 4-4.

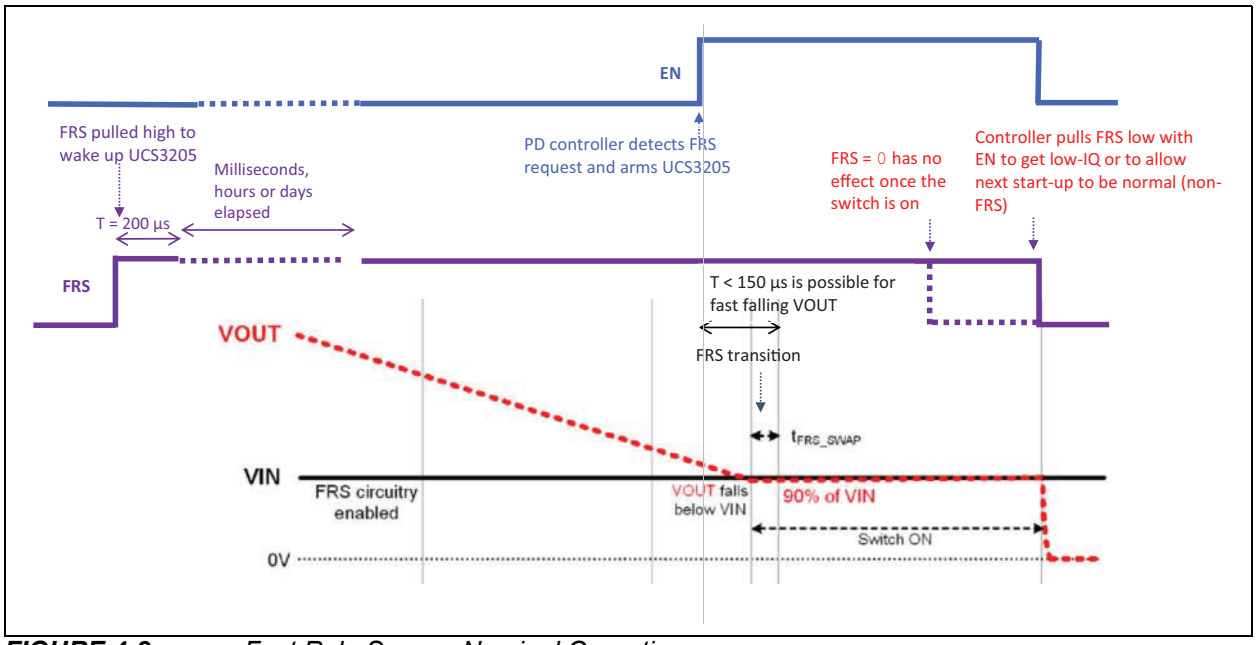



***FIGURE 4-2:*** *Fast Role Swap – Nominal Operation.*

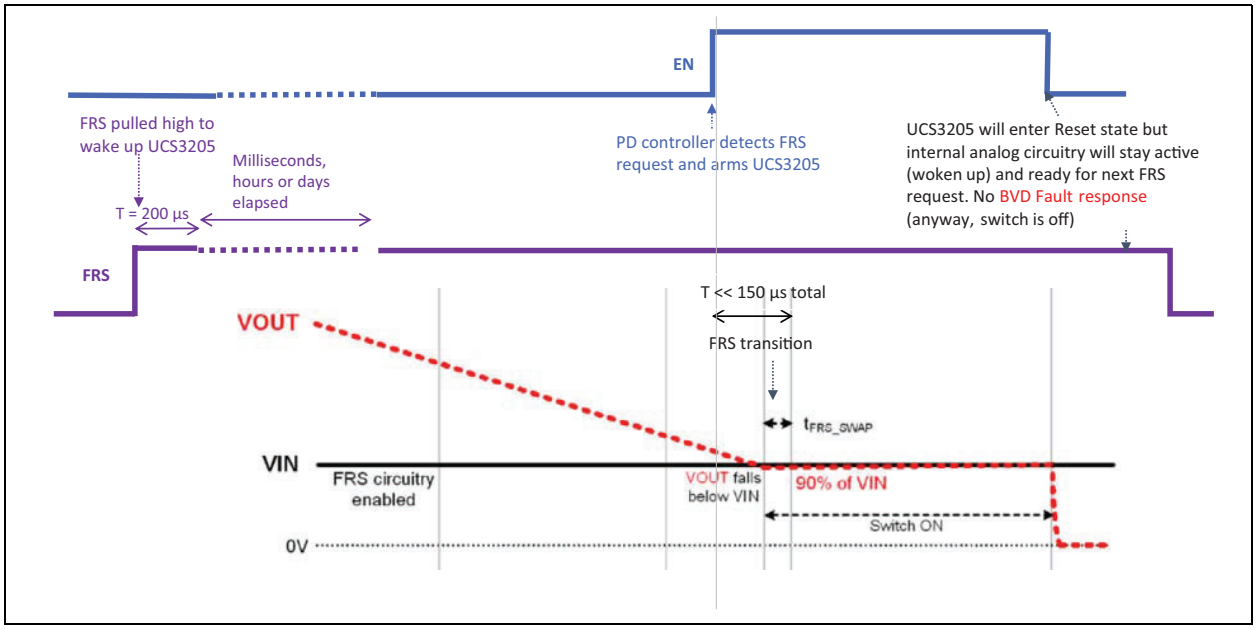



***FIGURE 4-3:*** *Fast Role Swap – FRS Circuitry Remains Awake.*

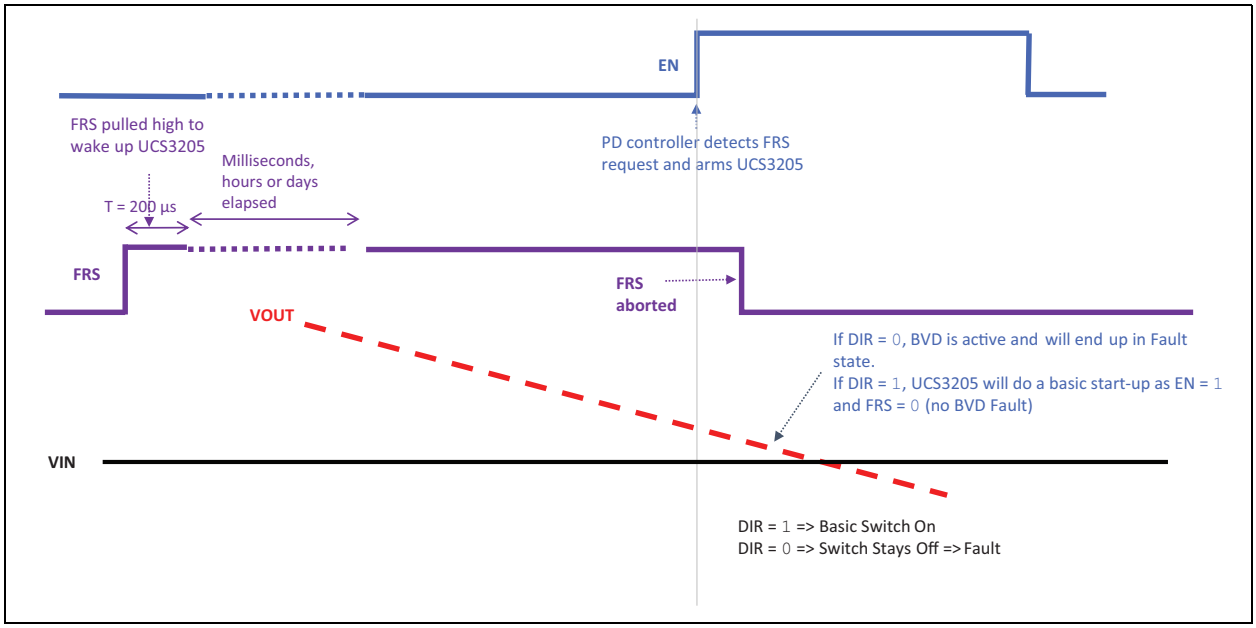



***FIGURE 4-4:*** *Fast Role Swap – Aborted.*

## 4.10 Output Discharge

To perform output discharge, the digital logic sends a signal to connect the internal current source between the VOUT pins and ground.

The output discharge can be done only when the switch is off, so only when the EN pin is low or after a Fault condition has been detected.

The DSC pin controls the output discharge behavior according to the Table 4-1.

**TABLE 4-1: OUTPUT DISCHARGE CONFIGURATION**

| DSC Pin State | Output Discharge Behavior |
|---|---|
| Always low | The output is never discharged. |
| Always high | Automatic output discharge. |
| Temporarily high when EN is low, under external circuit control | External triggered output discharge. |

## 4.11 Automatic Output Discharge

The VOUT pin is automatically discharged if the DSC pin is $V_{IH}$ while:

- The EN pin transitions from high-to-low, or
- A Fault condition has been detected.

The automatic output discharge ends when:

- The EN pin transitions from low-to-high, or
- The auto-recovery Fault handling starts, or
- The discharge timer reaches $t_{DISCHARGE}$, or
- The DSC pin transitions from high-to-low, or
- Overtemperature is detected. Overtemperature threshold during discharge is +170°C.

## 4.12 Triggered Output Discharge

To enable the external triggered output discharge, the DSC pin must be normally connected to ground, but pulled high temporarily when the output needs to be discharged.

The output is discharged when the EN pin is pulled low and the DSC pin is pulled high.

The output discharge ends when:

- The DSC pin transitions from high-to-low, or
- The EN pin transitions from low-to-high, or
- The discharge timer reaches $t_{DISCHARGE}$, or
- Overtemperature is detected. Overtemperature threshold during discharge is +170°C.

## 4.13 Fault Handling

A Fault state means that at least one of the following conditions has occurred:

- Short Circuit (SC signal),
- Overcurrent (OC signal),
- Overvoltage (OV signal),
- Thermal Shutdown (TSD signal), or
- Back-Voltage (BV signal) – **Fault DOES NOT apply when the Power Switch is off (EN = 0)**.

When the Fault state is detected, the digital logic turns off the switch and asserts the FAULT# pin.

At the time when the Fault is detected, the UCS3205 discharges the output for the duration of $t_{DISCHARGE}$. If the LATCH pin is $V_{IH}$ at the time when the Fault is detected, the digital logic remains in the Fault state until the EN pin is toggled low-to-high, the Fault conditions are no longer present (OV, TSD, BV) and the Fault recovery procedure begins.

If the LATCH pin is $V_{IL}$ at the time when the Fault is detected, the UCS3205 subsequently enters Auto-Retry mode, where it runs the Fault recovery procedure every $t_{RETRY}$, until no Fault condition (Overvoltage [OV signal], Thermal Shutdown [TSD signal], Back-Voltage [BV signal if DIR = 0]) is detected or until the EN pin is pulled low.

Figure 4-5 shows the Auto-Retry mode (LATCH pulled low) Fault recovery timing in the case of a short circuit.

At the end of the Fault recovery procedure, if none of the Fault conditions are met, the FAULT# pin is deasserted and the power switch is turned on.

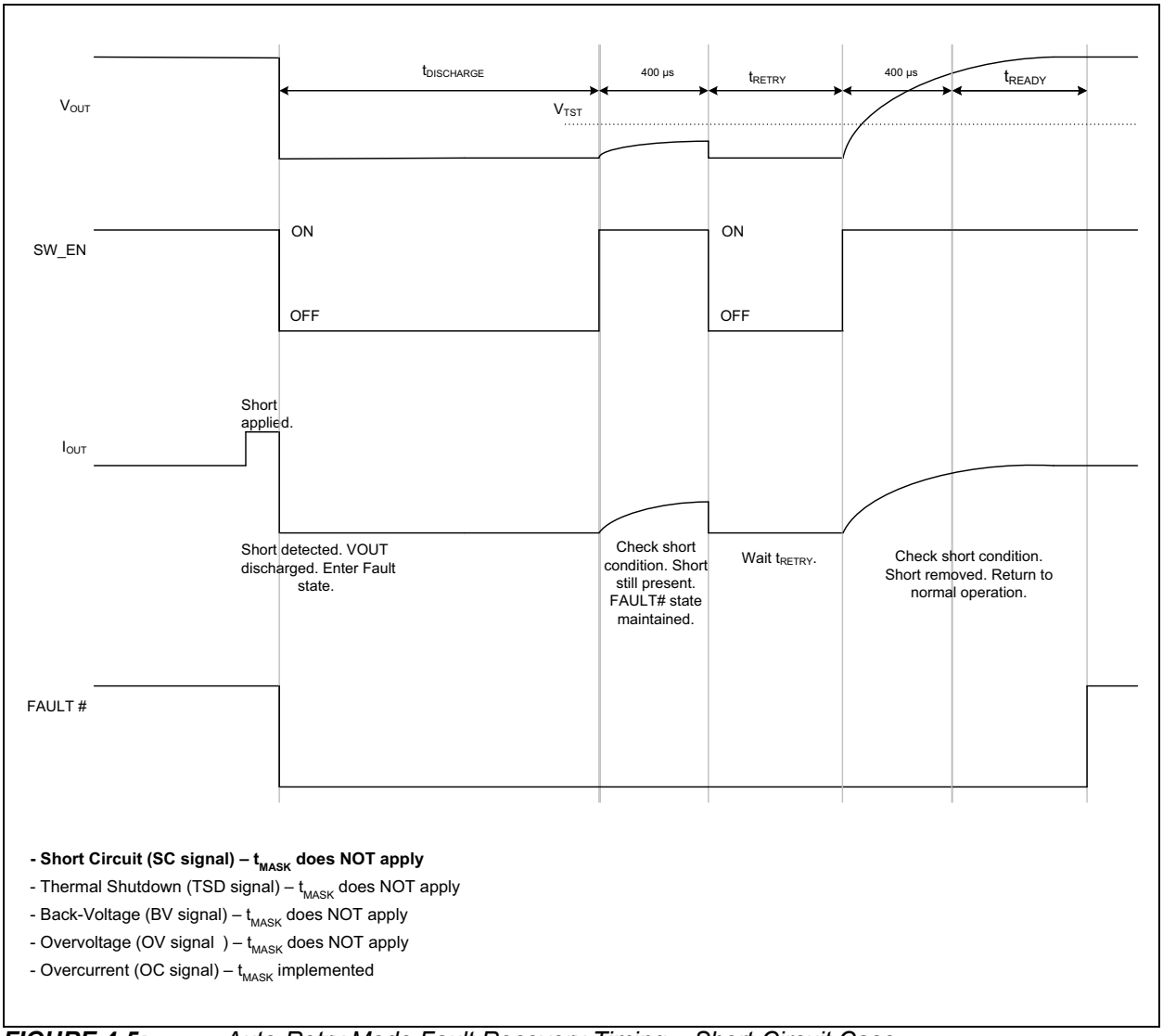



***FIGURE 4-5:*** *Auto-Retry Mode Fault Recovery Timing – Short-Circuit Case.*

## 4.14 Typical Application

Figure 4-6 illustrates an example of a typical application of the UCS3205.

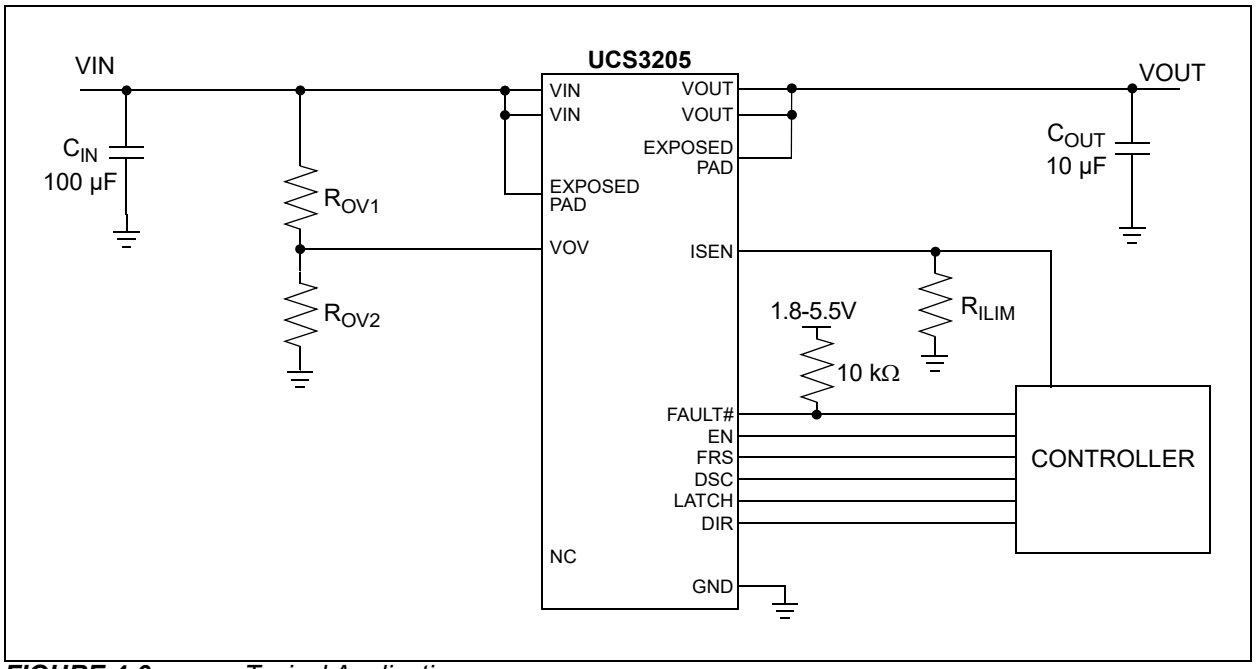
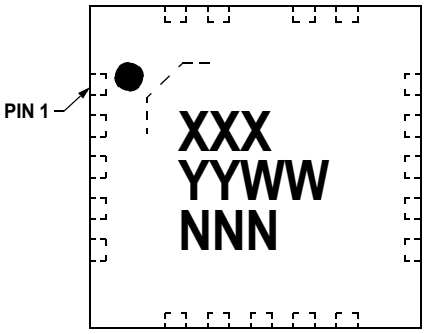



***FIGURE 4-6:*** *Typical Application.*

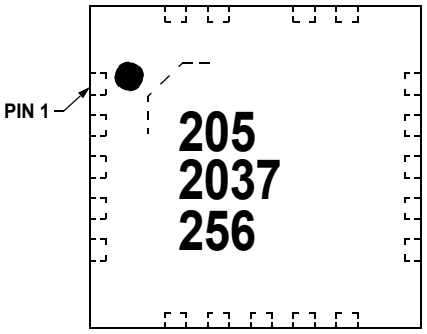
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

19-Lead VQFN (3x3x0.9 mm)




Example

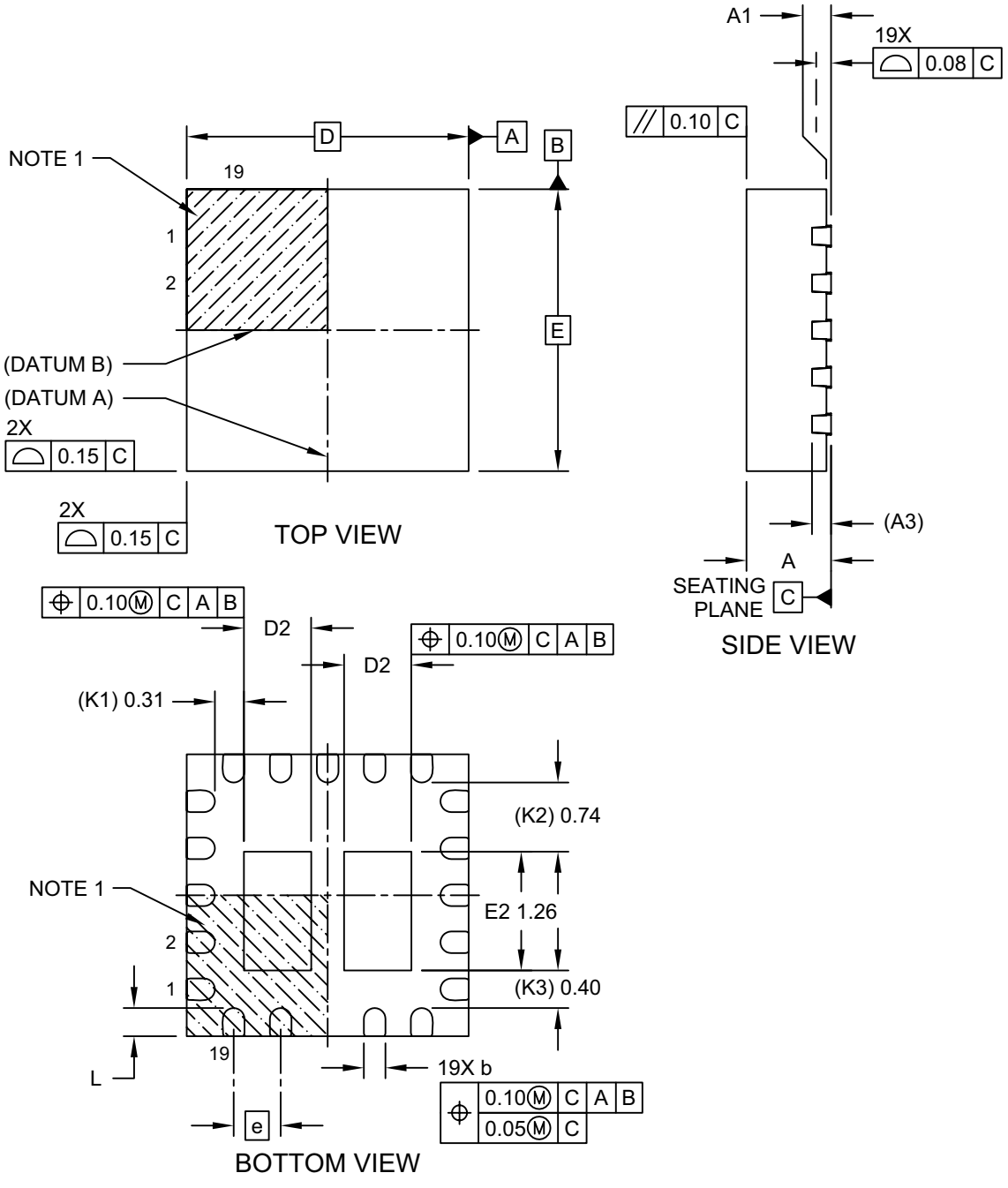



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3)* | Pb-free JEDEC designator for Matte Tin (Sn) |
| | | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

**19-Lead Very Thin Plastic Quad Flat, No Lead Package (Q8A) - 3x3x0.9 mm Body [VQFN] With Dual Exposed Pads**

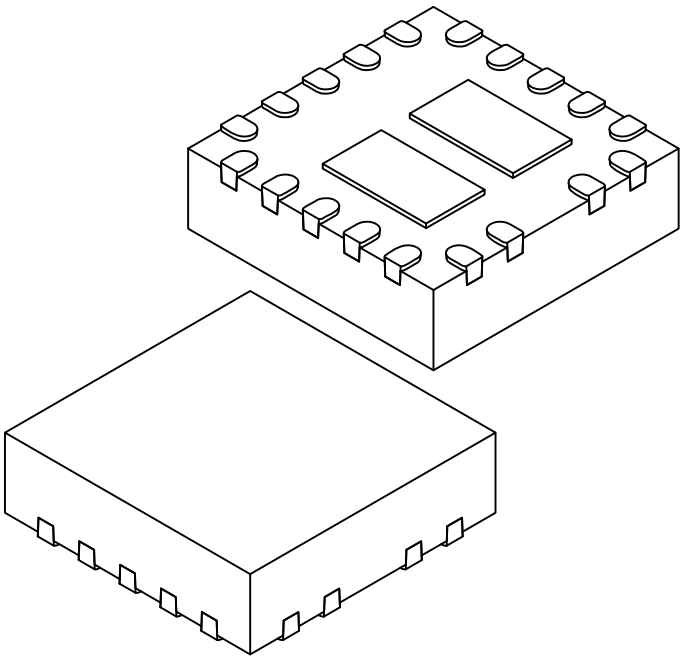
| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |




Microchip Technology Drawing C04-1273 Rev A Sheet 1 of 2

## 19-Lead Very Thin Plastic Quad Flat, No Lead Package (Q8A) - 3x3x0.9 mm Body [VQFN] With Dual Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 19 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.203 REF | |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 0.615 | 0.715 | 0.815 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.165 | 1.265 | 1.365 |
| Terminal Width | b | 0.18 | 0.23 | 0.35 |
| Terminal Length | L | 0.30 | 0.30 | 0.40 |
| Terminal-to-Exposed-Pad | K1 | | 0.31 REF | |
| Terminal-to-Exposed-Pad | K2 | | 0.74 REF | |
| Terminal-to-Exposed-Pad | K3 | | 0.40 REF | |

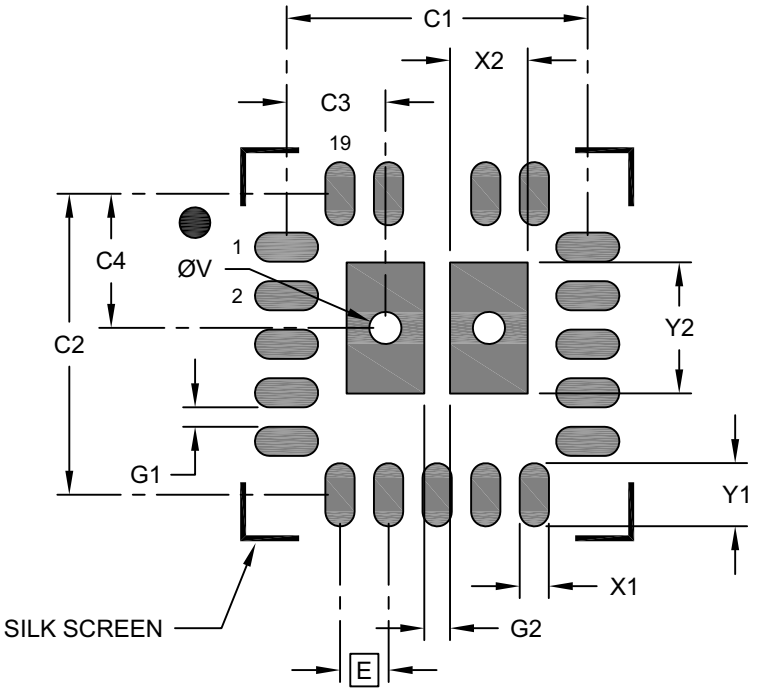
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1273 Rev A Sheet 2 of 2

### 19-Lead Very Thin Plastic Quad Flat, No Lead Package (Q8A) - 3x3x0.9 mm Body [VQFN] With Dual Exposed Pads

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 0.80 |
| Optional Center Pad Length | Y2 | | | 1.35 |
| Contact Pad Spacing | C1 | | 3.10 | |
| Contact Pad Spacing | C2 | | 3.10 | |
| Contact Pad to Thermal Via (X2) | C3 | | 1.03 | |
| Contact Pad to Thermal Via (X2) | C4 | | 1.38 | |
| Contact Pad Width (X19) | X1 | | | 0.30 |
| Contact Pad Length (X19) | Y1 | | | 0.65 |
| Contact Pad to Contact Pad (X14) | G1 | 0.20 | | |
| Center Pad to Center Pad | G2 | 0.27 | | |
| Thermal Via Diameter | V | | 0.33 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3273 Rev A

# APPENDIX A: REVISION HISTORY

## Revision A (September 2020)

- Initial release of this document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | [X](1) | X | /XXX | /XXX |
|---|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package | Qualification |

| | | |
|---|---|---|
| **Device:** | UCS3205: | 5A, 22V Bidirectional Load Switch with Fast Role Swap |
| **Tape and Reel Option:** | Blank = | Standard Packaging (tube or tray) |
| | T = | Tape and Reel(1) |
| **Temperature Range:** | E = | -40°C to +125°C (Extended) |
| **Package:** | Q8A = | Plastic Quad Flat, No Lead Package, 3 x 3 x 0.9 mm Body with Dual Exposed Pads, 19-Lead VQFN |
| **Qualification:** | Blank = | Standard Qualification |
| | VAO = | AEC-Q100 Automotive Qualification |

**Examples:**

a) UCS3205T-E/Q8A: Tape and Reel, Extended Temperature, 19-Lead VQFN Package

b) UCS3205-E/Q8A: Extended Temperature, 19-Lead VQFN Package

c) UCS3205T-E/Q8AVAO: Tape and Reel, Extended Temperature, 19-Lead VQFN Package, Automotive Qualified

d) UCS3205-E/Q8AVAO: Extended Temperature, 19-Lead VQFN Package, Automotive Qualified

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



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